Requirements for ALICE ITS3... and a bit beyond

Jerome Baudot

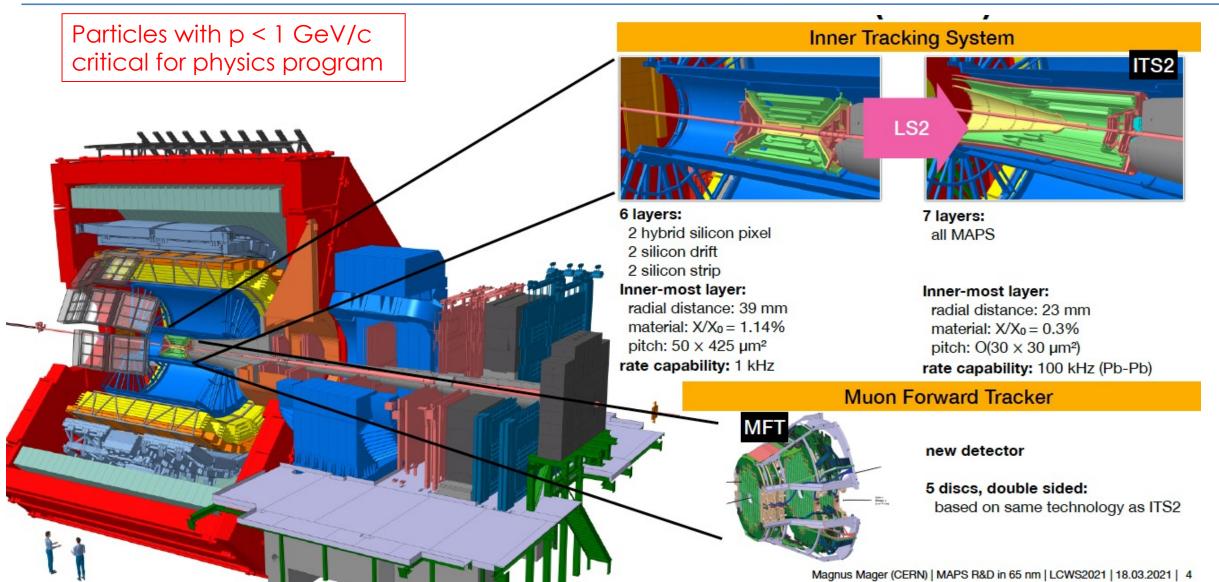


Disclaimer:

no time to contact proper ALICE physicist for this talk Material mostly stolen from Magnus Mager's talk @ LCWS https://indico.cern.ch/event/995633/contributions/4259506

ALICE today



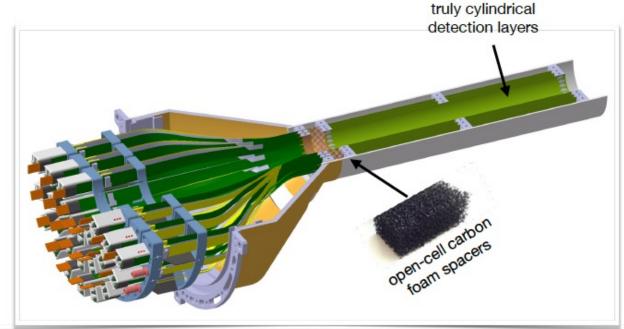


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ITS3 concept

ALICE-PUBLIC-2018-013





Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm²)	610	816	1016
Pixel sensor dimensions (mm²)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm²)	O (10 x 10)		

Key ingredients:

- 300 mm wafer-scale chips, fabricated using stitching
- thinned down to 20-40 µm (0.02-0.04%
 X0), making them flexible
- bent to the target radii
- mechanically held in place by carbon foam ribs

Key benefits:

- extremely low material budget:
 0.02-0.04% X0
 (beampipe: 500 µm Be: 0.14% X0)
- homogeneous material distribution: negligible systematic error from material distribution

The whole detector will comprise six (!) chips – and barely anything else

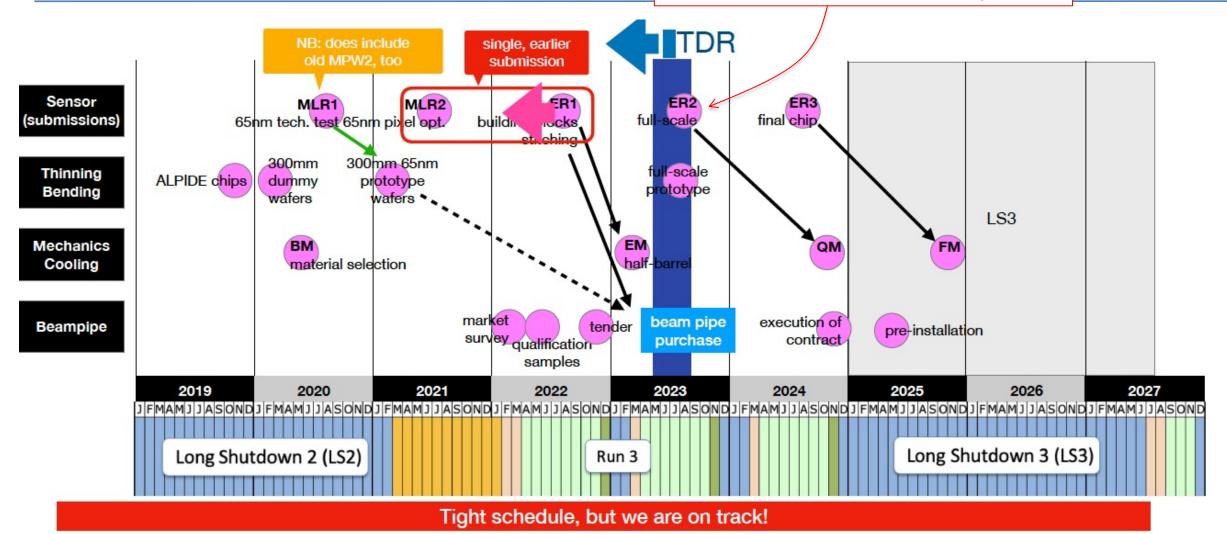
Probably 15x15 µm

Magnus Mager (CERN) | MAPS R&D in 65 nm | LCWS2021 | 18.03.2021 | 9

ITS3 timeline

Could be technological demonstrator shared by various scientific project





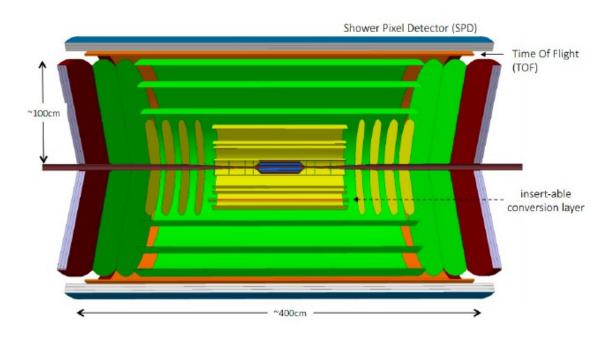
MLR: multiple layer per reticle, ER: engineering run,

BM: breadboard module, EM: engineering module, QM: qualification module, FM: final module

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Beyond ITS3: ALICE-3





"100% CMOS" experiment

Characteristics:

- . Hyper-granularity
- $|\eta| < 4$
- $B_7 = 0.2, 0.5 \text{ and/or } 1 \text{ T } ?$
- $0.05\% 0.8\% \text{ x/X}_{0} \text{ per layer}$
- $p_{\rm T} > 50 {\rm MeV/c}$
- . "triggerless"
- . O(1 MHz) MB readout

Target PID species:

- . h^{\pm} , π , K, p + light nuclei
- . soft e±, γ

1st design sub-detectors:

- . CMOS tracker, pixel $\mathcal{O}(20x20 \, \mu \text{m}^2) \approx 10 \, \text{layers}, |\eta| < 4$
- . pixellated TOF CMOS SPAD $\sigma_{TOF} \approx \mathcal{O}(20 \text{ ps})$, $|\eta| < 1.4$
- . electron pre-shower (CMOS sampled), $|\eta| < 4$



LS4 project budget ~100 MCHF

ALICE ≈ Eol, arXiv:1902.01211

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Some personal comments



- The ITS3 concept is a breakthrough in our domain
 - The breakthrough is the **stitching** part (not the 65 nm technology)
 - Some initial requirements are a compromise
 - Naturally it is risky
 - Yield of stitched sensor
 - Compatibility of power dissipation required over large sensor with air-cooling
 - Budget for sensor fab+thinning/bending
 - R&D phase ~1MCHF
 - Construction ~ 1.3 MCHF

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 μm	20-40 μm
Pixel size	27 x 29 μm	O(10 x 10 μm) 5 um resol OK
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 μs	~ 200 ns
Time resolution	$\sim 1 \ \mu s$	< 100 ns (option: <10ns) ?
Max particle fluence	100 MHz/cm ²	100 MHz/cm ²
Max particle readout rate	10 MHz/cm ²	100 MHz/cm ²
Power Consumption	40 mW/cm ²	< 20 mW/cm ² (pixel matrix) Critical
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10 ⁻⁷ event/pixel	< 10 ⁻⁷ event/pixel
NIEL radiation tolerance	$\sim 3 \times 10^{13} \text{ 1 MeV } n_{eq}/\text{cm}^2$	$10^{14} 1 \text{ MeV } n_{eq}/\text{cm}^2$
TID radiation tolerance	3 MRad	10 MRad

ITS-3 Kick-off Dec.2019, M.Mager

- The 65nm process offers other benefits (that we cannot ignore)
 - Spatial resolution is first (getting down to 3 um)
 - Due to thin sensitive layer => time resolution might come almost for free