# TPS65lSC digital flow: Trial at IPHC

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C4Pi digital team

# Context (1/2)

- Starting point:
  - The need of a digital bloc for the decoder of the DAC
  - Can we try to implement the digital flow ?
- Final point:
  - Development of small blocks with a final integration in Virtuoso
  - Scripts following best practices in digital design
- Purpose of this presentation:
  - It is mainly a translation of the documentations provided by Tower
  - To ease and to speed up, digital flow setup
  - There are “bugs” in digital PDK to be compatible with Virtuoso
  - Sorry, there are a lot of technical details

# Context (2/2)

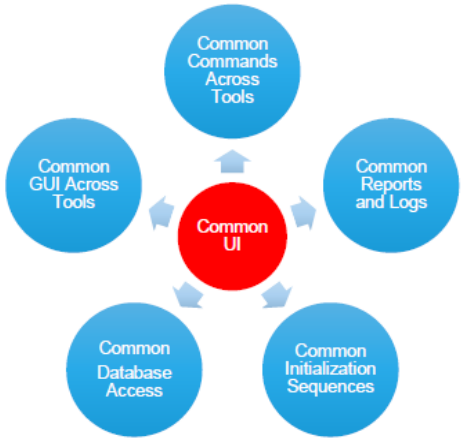
- Implementation of a small block for DAC
  - No IO have been used
  - No memories have been used
- Two kinds of methodology tested:
  - Stylus Common-UI with home made scripts based on OA libraries
  - Stylus Flowkit 2.0 methodology based on LEF libraries
    - Write flow template command:
      - write_flow_template -type stylus
      - -tools {
        - genus innovus quantus tempus voltus}
      - -enable_feature {
        - opt_postcts_split opt_postroute_split opt_signoff
        - report_static_ir report_dynamic_ir
        - sta_glitch sta_eco }
      - -optional_feature
        - report_inline
    - Intermediate step saved in innovus database format (default in flowkit)
    - Final layout view saved in OA from innovus

# Stylus Flowkit (1/2)

## Motivations - Why Stylus?

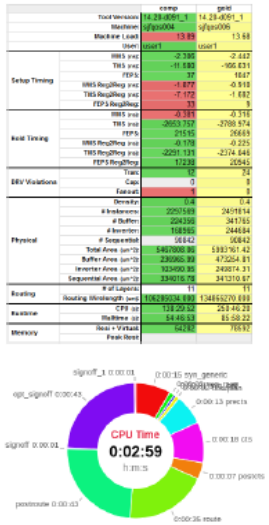
**3 different components**

### 1 Common User Interface



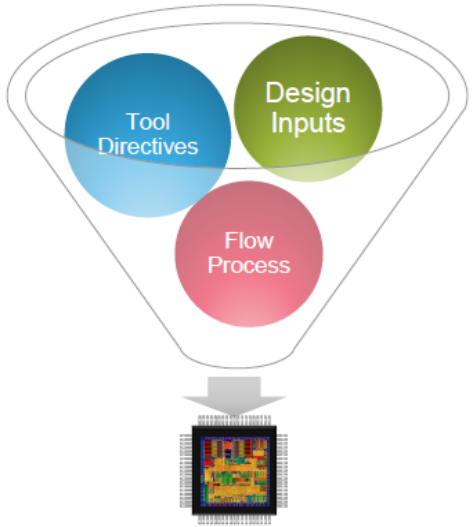

**Improved ease-of-use and designer productivity**

### 2 Unified Metrics




**Consistent reporting across the whole digital flow**

### 3 Flowkit




**Quickly capture and deploy digital flows**



cadence

# Stylus Flowkit (1/2)

## Overview of both flows - Stylus Flowkit (FK)

**Key concepts**

- Code generation is performed once
  - Allows the user to make arbitrary modifications in a straightforward way
  - Simplify the means for adding user content
- No external tools are used
  - In particular, makefiles are no longer generated.
- All flow configuration and state is stored in the database
  - Includes the history of steps run
  - Easy to figure out the flow that has produced a particular result.
  - Can restart the flow from a saved DB
- Flow control and “shopping-list” using friendly YAML markup language
- Only available in Stylus Common-UI



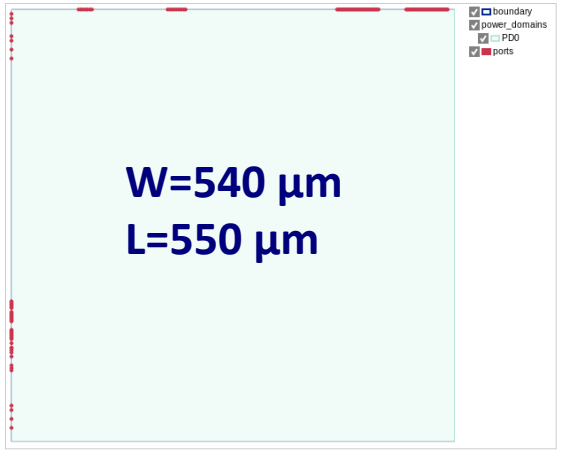

cadence

# MIMOSIS1 sequencer trial in 180 nm

**Stylus Metrics** | run

Summary | Timing | Clock | Design | Power | Route | Flow

| | |
|---|---|
| Design | sequencerTMR |
| Tools | genus-19.15-s090_1 innovus-19.16-s053_1 tempus-19.16-s053_1 voltus-19.16-s053_1 |
| Flow | stylus |
| Enabled features | |
| Tag | |
| Run host | sbgue29.in2p3.fr |
| Run directory | /home1/uelec/himmi/cadence/TOWER_TPS65ISC/flowkit/sequencer_180n |
| Last step | signoff |




**Stylus QOR summary**

| Snapshot | Type | Setup (all) | | | Setup (reg2reg) | | | Hold (all) | | | Hold (reg2reg) | | | DRV | | | Clock | | Design | | | Power | Route | | Tool | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | WNS (ns) | TNS (ns) | FEPS | WNS (ns) | TNS (ns) | FEPS | WNS (ns) | TNS (ns) | FEPS | WNS (ns) | TNS (ns) | FEPS | Tran (ns) | Load (pF) | Fanout | Insts | Area (um^2) | Density (%) | Insts | Area (um^2) | Leakage (mW) | DRC | WL (um) | Errors | Wall (s) | Memory (MB) |
| syn_generic | | 5.363 | 0 | 0 | 8.250 | 0 | 0 | | | | | | | 0 | 0 | 0 | | | 0.00 | 17,098 | 402,582 | 0.00 | | | e:0 w:235 | 0:01:09 | 501 |
| syn_map | | 2.672 | 0 | 0 | 6.570 | 0 | 0 | | | | | | | 0 | 0 | 0 | | | 0.00 | 7,207 | 203,793 | 0.00 | | | e:0 w:163 | 0:01:07 | 482 |
| syn_opt | | 2.672 | 0 | 0 | 6.570 | 0 | 0 | | | | | | | 0 | 0 | 0 | | | 0.00 | 6,997 | 201,297 | 0.00 | | | e:0 w:164 | 0:00:17 | 484 |
| floorplan | | | | | | | | | | | | | | | | | | | 68.67 | 6,997 | 201,297 | | 0 | | e:24 w:2321 | 0:00:11 | 1,531 |
| prects | | 2.985 | 0 | 0 | 7.115 | 0 | 0 | | | | | | | -0 | -1 | -19 | | | 69.17 | 7,055 | 202,771 | 0.00 | | 451,865 | e:24 w:2311 | 0:01:08 | 2,025 |
| cts | | 2.910 | 0 | 0 | 6.677 | 0 | 0 | -0.691 | -304 | 1,119 | -0.340 | -110 | 713 | 0 | 0 | -7 | 69 | 2,969.792 | 70.22 | 7,056 | 205,863 | 0.00 | 0 | 463,269 | e:24 w:2319 | 0:01:43 | 2,477 |
| postcts | | 3.410 | 0 | 0 | 7.177 | 0 | 0 | 0.007 | 0 | 0 | 0.060 | 0 | 0 | 0 | 0 | -7 | 69 | 2,969.792 | 70.30 | 7,066 | 206,073 | 0.00 | | 465,308 | e:24 w:2311 | 0:00:30 | 2,223 |
| route | | 2.438 | 0 | 0 | 6.321 | 0 | 0 | -0.023 | -0 | 26 | 0.061 | 0 | 0 | 0 | 0 | -7 | 69 | 2,969.792 | 70.30 | 7,066 | 206,073 | 0.00 | 0 | 504,072 | e:24 w:2376 | 0:01:08 | 2,334 |
| postroute | | 2.449 | 0 | 0 | 6.322 | 0 | 0 | 0.001 | 0 | 0 | 0.061 | 0 | 0 | 0 | 0 | -7 | 69 | 2,969.792 | 70.32 | 7,072 | 206,151 | 0.00 | 0 | 504,989 | e:24 w:2379 | 0:01:39 | 2,433 |
| postroute : signoff | | 1.964 | 0 | 0 | 6.464 | 0 | 0 | 0.200 | 0 | 0 | 0.062 | 0 | 0 | 0 | 0 | 4 | | | 72.59 | 7,397 | 212,790 | 0.00 | | 504,989 | e:12 w:1155 | 0:00:00 | 4,111 |
| opt_signoff | | 2.592 | 0 | 0 | 6.463 | 0 | 0 | 0.000 | 0 | 0 | 0.062 | 0 | 0 | 0 | 0 | -7 | 69 | 2,969.792 | 70.34 | 7,075 | 206,192 | 0.00 | 0 | 505,046 | e:24 w:2382 | 0:03:15 | 2,297 |
| opt_signoff : signoff | | 1.964 | 0 | 0 | 6.463 | 0 | 0 | 0.200 | 0 | 0 | 0.062 | 0 | 0 | 0 | 0 | 4 | | | 72.62 | 7,404 | 212,894 | 0.00 | | 505,046 | e:12 w:1155 | 0:00:00 | 4,124 |
| min | | 1.964 | 0 | 0 | 6.321 | 0 | 0 | -0.691 | -304 | 0 | -0.340 | -110 | 0 | -0 | -1 | -19 | 69 | 2,969.792 | 0.00 | 6,997 | 201,297 | 0.00 | 0 | 451,865 | | 0:00:00 | 482 |
| avg | | 2.856 | 0 | 0 | 6.763 | 0 | 0 | -0.044 | -44 | 164 | 0.004 | -16 | 102 | -0 | -0 | -4 | 69 | 2,969.792 | 52.88 | 7,958 | 222,315 | 0.00 | 0 | 488,073 | | 0:01:01 | 2,085 |
| max | | 5.363 | 0 | 0 | 8.250 | 0 | 0 | 0.200 | 0 | 1,119 | 0.062 | 0 | 713 | 0 | 0 | 4 | 69 | 2,969.792 | 72.62 | 17,098 | 402,582 | 0.00 | 0 | 505,046 | | 0:03:15 | 4,124 |
| graph | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Stylus runtime summary**







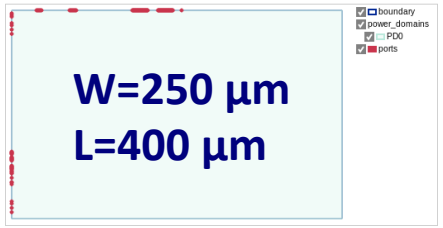
- MIMOSIS1 is a reticule size MAPS based on ALPIDE for CBM experiment
- Fully reworked digital part to sustain higher peak hit rate without trigger
- A robust and versatile sequencer used in several sensors developed at IPHC

# MIMOSIS1 sequencer trial in 65nm

**Stylus Metrics** | run

Summary | Timing | Clock | Design | Power | Route | Flow

| | |
|---|---|
| Design | sequencerTMR |
| Tools | genus-19.15-s090_1 innovus-19.16-s053_1 tempus-19.16-s053_1 voltus-19.16-s053_1 |
| Flow | stylus |
| Enabled features | |
| Tag | |
| Run host | sbgue29.in2p3.fr |
| Run directory | /home1/uelec/himmi/cadence/TOWER_TPS65ISC/flowkit/sequencer_65n |
| Last step | signoff |




**Stylus QOR summary**

| Snapshot | Type | Setup (all) WNS (ns) | Setup (all) TNS (ns) | Setup (all) FEPS | Setup (reg2reg) WNS (ns) | Setup (reg2reg) TNS (ns) | Setup (reg2reg) FEPS | Hold (all) WNS (ns) | Hold (all) TNS (ns) | Hold (all) FEPS | Hold (reg2reg) WNS (ns) | Hold (reg2reg) TNS (ns) | Hold (reg2reg) FEPS | DRV Tran (ns) | DRV Load (pF) | DRV Fanout | Clock Insts | Clock Area (um^2) | Design Density (%) | Design Insts | Design Area (um^2) | Power Leakage (mW) | Route DRC | Route WL (um) | Tool Errors | Tool Wall (s) | Tool Memory (MB) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| syn_generic | | 7.864 | 0 | 0 | 10.279 | 0 | 0 | | | | | | | 0 | 0 | 0 | | | 0.00 | 17,494 | 202,696 | 2.46 | | | e:0 w:1494 | 0:01:21 | 508 |
| syn_map | | 4.935 | 0 | 0 | 8.232 | 0 | 0 | | | | | | | 20,990 | 0 | 0 | | | 0.00 | 8,663 | 62,787 | 1.90 | | | e:0 w:1424 | 0:01:54 | 492 |
| syn_opt | | 4.963 | 0 | 0 | 8.232 | 0 | 0 | | | | | | | 18,290 | 0 | 0 | | | 0.00 | 8,682 | 62,523 | 1.95 | | | e:0 w:1427 | 0:00:59 | 494 |
| floorplan | | | | | | | | | | | | | | | | | | | 63.47 | 8,682 | 62,523 | | 0 | | e:0 w:645 | 0:00:15 | 2,068 |
| prects | | 4.001 | 0 | 0 | 8.597 | 0 | 0 | | | | | | | -497 | -0 | 0 | | | 64.50 | 9,074 | 63,534 | 2.00 | | 245,053 | e:0 w:617 | 0:01:26 | 3,037 |
| cts | | 4.210 | 0 | 0 | 8.374 | 0 | 0 | -0.561 | -405 | 1,343 | -0.410 | -207 | 820 | -20 | 0 | 0 | 108 | 1,343,680 | 66.19 | 9,279 | 65,202 | 2.09 | 0 | 275,953 | e:0 w:627 | 0:02:01 | 3,173 |
| postcts | | 4.710 | 0 | 0 | 8.874 | 0 | 0 | 0.000 | 0 | 0 | 0.002 | 0 | 0 | -20 | 0 | 0 | 108 | 1,343,680 | 66.35 | 9,314 | 65,356 | 2.10 | | 280,888 | e:0 w:617 | 0:01:07 | 2,435 |
| route | | 4.260 | 0 | 0 | 8.577 | 0 | 0 | -0.255 | -53 | 391 | 0.002 | 0 | 0 | -21 | 0 | 0 | 108 | 1,343,680 | 66.35 | 9,314 | 65,356 | 2.10 | 0 | 291,688 | e:0 w:670 | 0:01:31 | 2,800 |
| postroute | | 4.260 | 0 | 0 | 8.576 | 0 | 0 | -0.131 | -4 | 63 | 0.002 | 0 | 0 | -21 | 0 | 0 | 108 | 1,343,680 | 66.55 | 9,371 | 65,553 | 2.11 | 0 | 292,483 | e:0 w:671 | 0:03:02 | 2,858 |
| postroute : signoff | | 4.898 | 0 | 0 | 9.182 | 0 | 0 | 0.200 | 0 | 0 | 0.029 | 0 | 0 | 42 | 0 | | | | 75.57 | 10,480 | 74,440 | 2.11 | | 292,483 | e:0 w:308 | 0:00:00 | 4,331 |
| opt_signoff | | 4.508 | 0 | 0 | 8.672 | 0 | 0 | 0.002 | 0 | 0 | 0.017 | 0 | 0 | -20 | 0 | 0 | 108 | 1,343,680 | 66.60 | 9,384 | 65,605 | 2.11 | 0 | 292,598 | e:0 w:692 | 0:06:43 | 2,808 |
| opt_signoff : signoff | | 5.005 | 0 | 0 | 9.182 | 0 | 0 | 0.200 | 0 | 0 | 0.029 | 0 | 0 | 42 | 0 | | | | 75.51 | 10,488 | 74,380 | 2.11 | | 292,598 | e:0 w:308 | 0:00:00 | 4,308 |
| min | | 4.001 | 0 | 0 | 8.232 | 0 | 0 | -0.561 | -405 | 0 | -0.410 | -207 | 0 | -497 | -0 | 0 | 108 | 1,343,680 | 0.00 | 8,663 | 62,523 | 1.90 | 0 | 245,053 | | 0:00:00 | 492 |
| avg | | 4.874 | 0 | 0 | 8.798 | 0 | 0 | -0.078 | -66 | 257 | -0.047 | -30 | 117 | 3,524 | -0 | 0 | 108 | 1,343,680 | 50.92 | 10,019 | 77,496 | 2.09 | 0 | 282,968 | | 0:01:42 | 2,443 |
| max | | 7.864 | 0 | 0 | 10.279 | 0 | 0 | 0.200 | 0 | 1,343 | 0.029 | 0 | 820 | 20,990 | 0 | 0 | 108 | 1,343,680 | 75.57 | 17,494 | 202,696 | 2.46 | 0 | 292,598 | | 0:06:43 | 4,331 |
| graph | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Stylus runtime summary**







| | Design Density (%) | Design Insts | Design Area (um^2) | Power Leakage (mW) | Route DRC | Route WL (um) |
|---|---|---|---|---|---|---|
| 180 nm | 72.62 | 7,404 | 212,894 | 0.00 | | 505,046 |
| 65 nm | 75.51 | 10,488 | 74,380 | 2.11 | | 292,598 |

**Nothing new:**

- **Smaller (~3 times)**
- **Faster (~2 times)**
- **Less power (60 % less, except leakage)**
- **Both in 4 metals, no clear impact of M1&M2 for 65 nm standard cells**

# Conclusion

- We have gone through all the steps of the digital flow except:
  - Scan chain
  - Macros (IO, memories, home made analog)
  - LEC with conformal (Logical Equivalence Checking)
  - No Digital on Top flow / No hierarchical flow
- We can distribute flowkit scripts as is
  - Need to be adapted to your needs
  - Could be a starting point for a common digital flow
- We digest the digital design documentation (not presented here due to NDA)
  - Ease the ramp-up
- Need to fix few variables for a common definition
  - Delay margins
  - PGV generations (area capacitance, voltage, RC corner)
  - …