Possible contributions to future development in 65nm technology

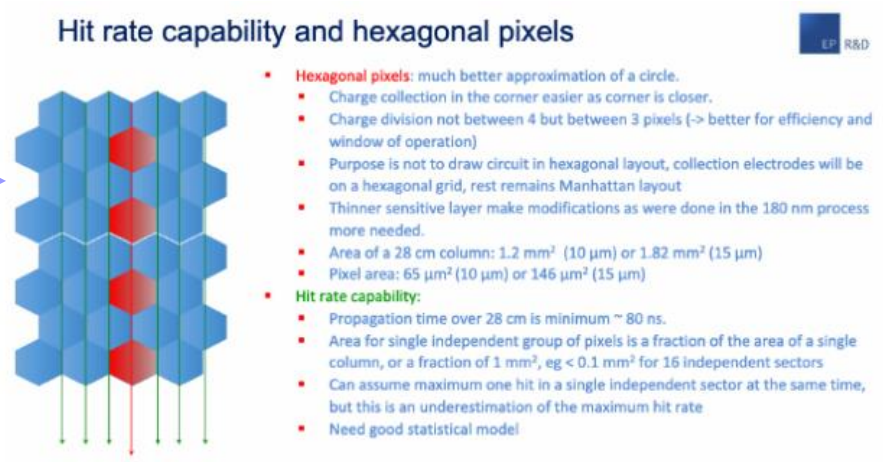
Andrei Dorokhov

10/03/2021

possible contribution (1)

- **Evolution of CE65 chip – charge collection R&D and optimization :**
  - **Larger area (now is < 2 mm x 2mm)**
  - **Different pixel pitch - also to be defined after first tests of CE65**
  - **Hexagonal pixels* (similar to staggered layout in mimosa22AHR, AMS0.35 run in 2010 and in FASTPIX ATTRACT project in 2020) in order to decrease chare sharing in between pixels (3 pixels instead of 4)**
  - **Technology options…**

(*) Talk by Gianluca Aglieri Rinella and Walter Snoeys, « Sketches for next submission, Chip Proposals, Floorplan » https://indico.cern.ch/event/1012366/contributions/4249722/attachments/2197004/3714850/20210225_Chip_Proposals_GAR_WS.pdf



possible contribution (1)

- **Evolution of CE65 chip – circuit R&D and optimization:**
  - **Front End circuit:**
    - **Analogue amplifier/SF for analogue information (charge sharing)**
    - **Digital Pixel : amplifier + discriminator for final pixel matrix**
  - **Stitching considerations(*) impact for pixel circuit for larger detector:**
    - **Top level rules (additional rules)**
    - **Yield (because of pixel circuit complexity, pixel transistor count ~100, usually only few transistors in imaging applications)**
    - **Layout issues – boundaries of repeated blocks (hexagonal pixels for example)**
    - **Speed / power – there is a challenge for ex. If total matrix line is 28cm X 10 cm…**

(*) Experience from RAL, talk by Iain Sedgwick, « Practical Design Considerations for Stitching » https://indico.cern.ch/event/1014420/contributions/4257813/attachments/2201756/3724170/Stitching_Talk.pdf

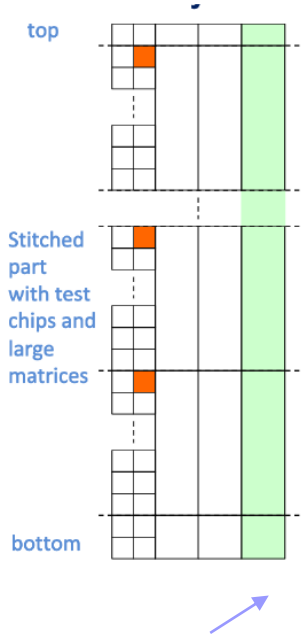
Conclusions for possible contribution (1)

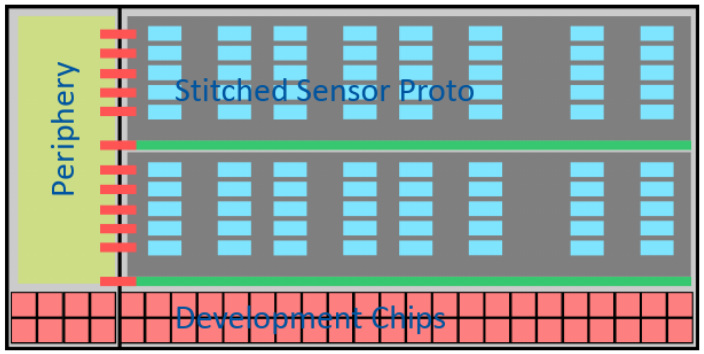
- For contributions (1) we already agreed, that we will have manpower to fulfill them
- In addition to that, we may contribute to another analogue block(s), which we already designed in MLR1 run (DACs for ex.)

possible contribution (2)

- **We have expressed our interest in development of stitched sensor prototype for ALICE ITS upgrade (*)**

Sketch of floorplan





20220225 | TPSCo65 design meeting | Sketches towards next submission

(*) From talk by Gianluca Aglieri Rinella and Walter Snoeys, « Sketches for next submission, Chip Proposals, Floorplan »

possible contribution (2)

- **Our possible contribution to the development of stitched sensor prototype includes:**
  - **Sub-blocks concepts and design**
  - **Study of readout architectures for the stitched sensor (*):**
    - **Global strobe with in-pixel storage and zero suppressed readout of binary information steered from the periphery (evolution of ALPIDE)**
    - **Hit-driven asynchronous hit information (position and time) transmission with pulse width modulation or other types of encoding**
  - **Backend design of sensor prototypes**

(*) More details in talk by Gianluca Aglieri Rinella and Walter Snoeys, « Sketches for next submission, Chip Proposals, Floorplan »

Conclusions for possible contribution (2)

- **We have strong motivation to do contribution (2) which are inline with ours future R&D**
  - **Need still to define our resources and availability…**