2nde sobmission TJ 65 nm at CERN
General context

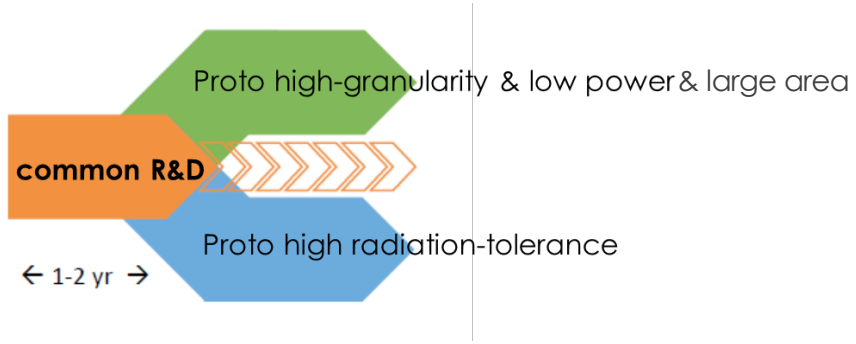
Christine, Claude, Jerome

- Contexte général des capteurs à pixels CMOS
- Applications en cours
- Perspectives des développements
- Collaborations
- Synthèse

Reminder on the initial strategy

We are in December 2019…

- EP roadmap WP1.2
  - Goals = prototyping 2 sensors



  - 2 phases
    1. Technology selection (with limited nb of designers) then advanced test structures (ADCs, bandgaps, …)
    2. Pre-prototyping the two sensors

- ALICE ITS3 roadmap
  - Calendar (for the circuit)

	Milestone	Description	Production[a]	Date
MS CD-1	1	**Technology test structures** single pixels, transistors, small memory cell array for studying the radiation hardness of the technology	MPW	Q4 2019
MS CD-2	2	**Pixel test vehicle** optimization of pixel and diode geometries	MPW	Q3 2020
MS CD-3	3	**Large area prototype** basic blocks: pixel matrix, periphery, output serial links exercising of stitching different parts	ER	Q4 2021
MS CD-4	4	**Full-scale prototype** prototype of final chip with all functionality	ER	Q4 2022
MS CD-5	5	**Final Chip** possible minor adjustments wrt milestone 4	ER	Q4 2023

[a] MPW: multi-project wafer run, ER: engineering run

  - Budget
    - R&D ~700 kCHF
    - Construction ~900 kCHF

Current situation

- MLR1 considered a success / **design**
  - A lot learned on the design: benefits & shortcomings (ex: ''leakage in digital cells'')
  - Phase 1 ''completed'' => move to Phase 2 for 2nd submission
    - Wafer-scale sensor 28x10 cm
    - Small sensors for improvement

Organization of designer group totally different!
=> Stronggly driven by CERN

- WARNINGs
  - **Tests:**
    - We still have nothing in our hands!!
    - Not assessed: radiation-hardness & detection efficiency
  - Proposed design only for the large-low-power-high-granularity proto
    - Where is the other option for rad-hardness?
  - 2nd submission still with Imaging techno (ICS advised by TJ for stitching)
    - Will we move to something else (benefits / nb of metal layers)?

Still a lot of basic R&D needed (power, hit-rate limit, …)

- Missing info
  - CERn is still the only one with access to technological info
    - No TCAD simulation possible outside CERN

Proposal by CERN for 2nd submission

A large sensor already!

Initiated by CE65-IPHC

CPPM experts identified

	Chip / Test Chip	Purpose	Comments
	Stitched Sensor Prototype	Develop stitching know-how	Focus on technology options, power distribution, yield Matrix as simple as possible
	CE65 ++	Pixel optimization vehicle	Evolution(s) of CE65 (e.g. larger area, hexagonal pitch, optimized pixels and front-end)
	Digital Logic Test chip	Prototype SPRAM, DPRAM, arrays of flops. Measure SEE cross sections (SEL, SEUs).	
	High Speed Data Transmission	Development of ~2 Gb/s links	Must be reliable and efficient. Early integration.
	Supply Regulation	Missing desired function	Needs band-gap as reference
	ADC prototypes	Missing desired function	Can combine with Bandgap, DAC to be selected/optimized from MLR1

Still room for small chips but in limited number

About specifications

- Initial ALICE-ITS3 proposal

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

→ also considered: 15x15 m

Not clearly useful for ALICE-ITS3
maybe degraded or two different protos

Again: no idea if this is doable in TJ-65nm

=> Seems an excellent vehicule for our current R&D goals