

Dalian-Strasbourg Collaboration on Smart Sensors R&D

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(on behalf of the DUT-IPHC coll.)

OUTLINE

- Context of collaboration between IPHC and DUT
- Questions addressed by the collaboration
- Status of work and plans

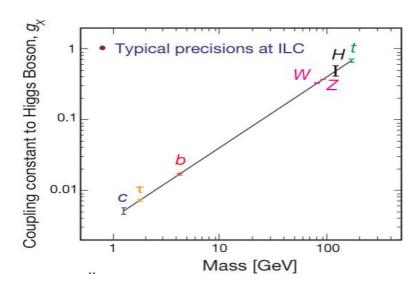
ILD-WORKSHOP

Development of pixel sensors for future vertex detectors: ILC, STAR, FIRST, CBM, ALICE, ...

$$\hookrightarrow$$
 Figure of merit : $\sigma_{\mathbf{ip}} = \mathbf{a} \oplus \mathbf{b}/\mathbf{p} \cdot \sin^{3/2} \theta$

- * a governs high momentum
- **b** governs low momentum (\sim 30 % particles < 1 GeV/c)

Accelerator	a (μm)	b ($\mu m \cdot GeV$)
LEP	25	70
SLD	8	33
LHC	12	70
RHIC-II	13	19
ILC	< 5	< 10



- R&D priority: achieve high resolution, highly integrated and thin pixel sensors
 - detector R&D on CMOS pixel sensors with application dependent optimisations

ILD-WORKSHOP

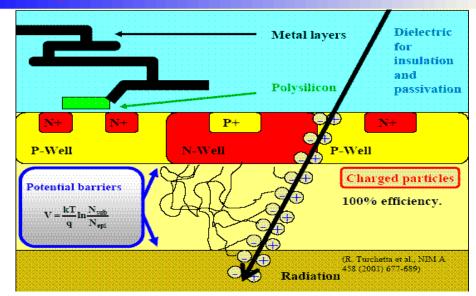


Main Features and Advantages of CMOS Sensors

- P-type low-resistivity Si hosting n-type "charge collectors"
 - signal created in epitaxial layer (low doping):

Q
$$\sim$$
 80 e-h / $\mu m \mapsto$ signal \lesssim 1000 e $^-$

- charge sensing through n-well/p-epi junction
- excess carriers propagate (thermally) to diode with help of reflection on boundaries
 with p-well and substrate (high doping)

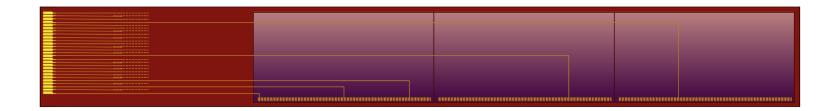


- Prominent advantages of CMOS sensors:
 - \diamond granularity: pixels of \lesssim 10×10 μm^2 \Longrightarrow high spatial resolution
 - \diamond low mat. budget: sensitive volume \sim 10 15 μm \Longrightarrow total thickness \lesssim 50 μm
 - \diamond signal processing μ circuits integrated in the sensors \Rightarrow compacity, high data throughput, flexibility, etc.
- Difficulties:
 - * Technical:
 - \diamond thinning to epitaxial layer + \sim 5 μm (\lesssim 30 μm in total)
 - dicing with negligible insensitive frame
 - \diamond integration of μ circuits in small pixels (nb of ML)
 - * Structural: technology potential not exploited in industry
 - o industrial manufacturing param. not optimised for HEP: epitaxial layer properties, nb of ML,

2 categories of research lines:

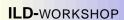
- * sensor manufacturing \Rightarrow optimised process parametres:
 - epitaxial layer (sensitive volume) characteristics: thickness, resistivity, etc.
 - number of Metal Layers: > 5-6
 - others: T design, etch stopper implantation, ...
- * sensor conditionning:

 - thinning \lesssim 50 μm edgeless dicing (< 5 μm dead zone)



Added value of collaboration:

- * control of fabrication timeline and costs
- * independence from industry policy
- * contacts and synergy with numerous young Chinese designers
 - ⇒ design tutoring at IPHC (several PhDs)





CMOS Sensor Design Activities by Chinese Students

MAPS performance Improvement



→ R&D on high readout speed, low noise, low power dissipation, highly integrated signal processing architecture with radiation tolerance

O Pixel optimisation :

- MIMOSA8 (2004), MIMOSA15 (2005), MIMOSA22 (2007/2008) ...
- 1 Architecture of pixel array organised in // columns read out:
- Pre-amp and CDS in each pixel
- A/D: 1 discriminator / column (offset compensation)
- Power vs Speed → trade off
- MIMOSA8 (2004), MIMOSA16 (2006), MIMOSA22 (2007/08)

2 Zero suppression logic:

- Reduce the raw data flow of MAPS
- Data compression factor ranging from 10 to 1000, depending on the hit density per frame
- SUZE-01 (2007) Anti-latch-up memory (2010)



Anti-laten-up memory (2010)

- 3 Serial link transmission with clock recovery
- Prototype (2008-2009)

Pixel Array

Analogue processing / pixel

A/D: 1 ADC ending each column

Zero suppression

Bias DC-DC Data transmission

4-5 bits ADCs (~103 ADC per sensor)

- LPCC, LPSC, IRFU, IPHC collaboration
- Potentially replacing column-level discri.
- 5 bits: $\sigma_{sp} \sim 1.7-1.6 \ \mu m$ 4 bits: $\sigma_{sp} < 2 \ \mu m$ for 20 μm pitch
- Next step: integrate ADCs with pixel array

5 Voltage regulator & DC-DC converter

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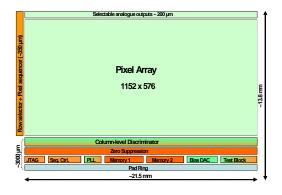


MIMOSA-26: Full Size CMOS Sensor with Integrated O



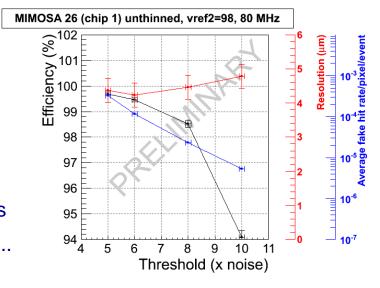
Full size sensor with integrated zero-suppression fab. in 2009:

- \star Active area: 1152 columns of 576 pixels (21.2 \times 10.6 mm²)
- Pitch: 18.4 $\mu m \rightarrowtail \sim$ 0.7 million pixels $\Rightarrow \sigma_{sp} \gtrsim$ 3.5 μm
- * $T_{r.o.} \lesssim 110 \ \mu s \Rightarrow \text{ suited to } > 10^6 \ \text{particles/cm}^2/\text{s}$
- \divideontimes P \sim 300 mW/cm 2 (static) + 100 mW/cm 2 (dynamic with 1% occ.)
- Data transmission: 1 output at \geq 160 Mbits/s (or 2 X 80 Mbits/s)
- 6 sensors equip the final set-up of the EUDET beam telescope
- 8 sensors will equip the FIRST vertex detector (hadrontherapy)



> 50 sensors tested in lab and \sim 10 sensors at CERN-SPS:

- * > 99.5 % detection efficiency routinely observed over the whole sensitive area, with a fake rate $\lesssim O(10^{-4})$
- * $\sigma_{sp}^{M26} \sim$ 4–4.5 μm (preliminary) \mapsto expect $\sigma_{sp} \lesssim$ 4 μm
- >>> MIMOSA-26 architecture validated for numerous applications ⇒ currently being extended for STAR-PIXEL and CBM-MVD, ... also investigated as an option for ALICE-ITS upgrade



MIMOSA Sensors' Roadmap

Monolithic Active Pixel Sensors (MAPS): A Long Term R&D

- Main objective: ILC, with staggered performances
 - MAPS applied to other experiments with intermediate requirements

EUDET 2007/2009

Beam Telescope



ILC >2012

Internatinal Linear Collider

■ FP6 EUDET Project (DESY-Hamburg, Germany)

Surface 6 x 2 cm²

Read-out speed A. 20 MHz -> D. at 100 MHz

Temp. & Power: No constraints

STAR Experiment (RHIC – Brookhaven, USA)

♦ Surface ~1600 cm²

Read-out speed A. 50 MHz → D. up to 250 MHz

√ Temp. & Power 30°C, ~100mW/cm²

■ CBM Experiment (GSI – Darmstadt, Germany)

Surface ~500 cm²

Read-out speed D. 15 x 10⁹ pixels/sensor/s
Rad Tol 1 MRad, > 10¹³ N_{eq}/cm²

ILC Experiment

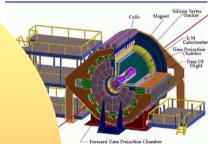
5-6 layers of detection ~3000 cm²

Read-out speed D. 15 x 10^9 pixels/sensor/s Temp. & Power 30° C, ~100 mW/cm²

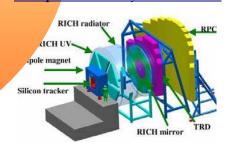
Rad Tol ~300 kRad, ~10¹² N_{eq}/cm²

STAR 2010

Solenoidal Tracker at RHIC







- → Spinoff: Interdisciplinary Applications, biomedical, ...
 - Partnerships: GIS IN2P3/Photonis & GIS IN2P3/SAGEM & Ohio University & Michigan University...

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Dalian VDSM CMOS Fabrication Chain

ullet 0.25 μm fabrication chain elements from INTEL:

- * provided by INTEL (agreement with Chinese government)
- * INTEL is installing a 0.065 μm fab. chain in Dalian
- \divideontimes DUT supposed to use the 0.25 μm chain to educate engineers for INTEL-0.065 fab.



Difficulties encountered:

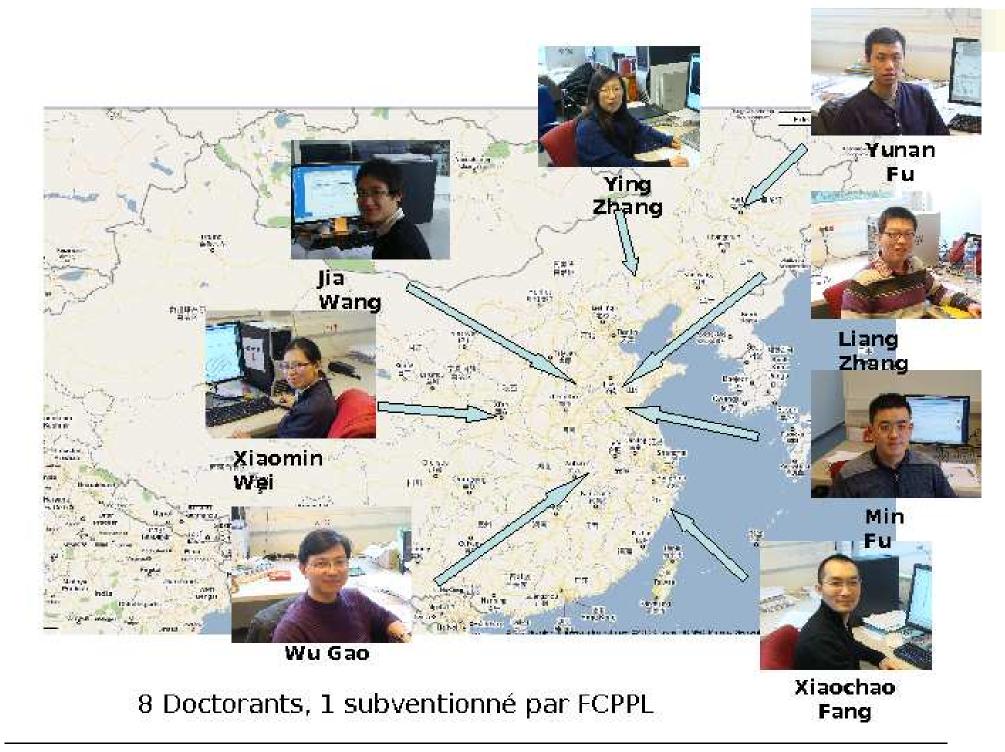
- * find, buy, refresh a large building to host fab. chain \Rightarrow 3000 m² (2000 m² clean room)
- * missing elements (10 Meuros):
 - elements of fab. chain
 - elements for fab. monitoring & quality control
- * no subvention for running costs (2 Meuros/yr)
 - ⇒ mask lithography: 300 kUSD
 - ⇒ search for industrial partners



>>> Fabrication chain commissioning delayed to end of 2010

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- Collaboration addressing several crucial issues for future high precision vertex detectors based on CMOS sensors \longrightarrow ILC, STAR, CBM, FIRST, ALICE, ...
 - * sensor manufacturing: customised VDSM CMOS fab. chain
 - chip designs for various applications
- Very constructive and fruitful collaboration \Rightarrow several talks at conferences and publications
 - * contribution to development of MIMOSA-26 (CMOS sensor state of the art)
 - contribution to generic data stream optimisation
 - * contribution to 3D sensor design
- Difficulties encountered \Rightarrow delays introduced in the customised fab. chain availability
 - * expected to be solved by 2011
 - * hope to start testing the chain next year



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