Participation in the Pixel Detector R&D Studies for ATLAS Upgrade

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Structure of this presentation

-- Brief description of the upgrade of the ATLAS pixel Detector

-- Introduction of the SEU test system of 40 MHz based on DE2 board

-- Introduction of the analog buffer design and simulation, which is used for signal monitoring in the FE - C4 design

The Pixel Detector in ATLAS

◇ Pixel Detector

-- 1.4 meter long cylinder with a diameter of 0.5 meter

-- 1744 modules

-- 80 millions pixels

◇ Module

-- Assembled with 16 FE (Front End) chips and MCC (Control Chip)

-- The chips are bump bonded on the substrate of the detector using the technique of Flip Chip

-- Size: 16.4 x 60.8 mm

◇ FE Chip :

-- contains 160 lines * 80 columns of pixel cells

-- Pixel Size : 50 x 400 um

-- 2889 pixels per FE chip

-- 46080 pixels per module

◇ Power Consumption :

-- 0.8W/cm^2 Each Circuit

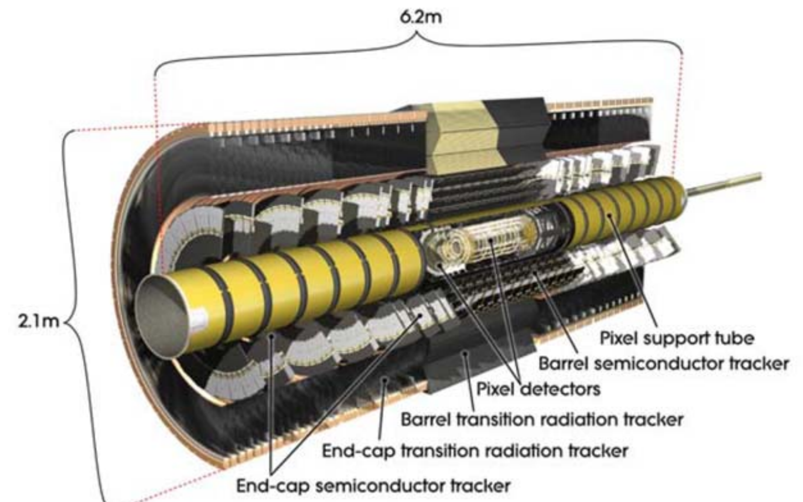


Fig 1. The ATLAS Inner Detector.

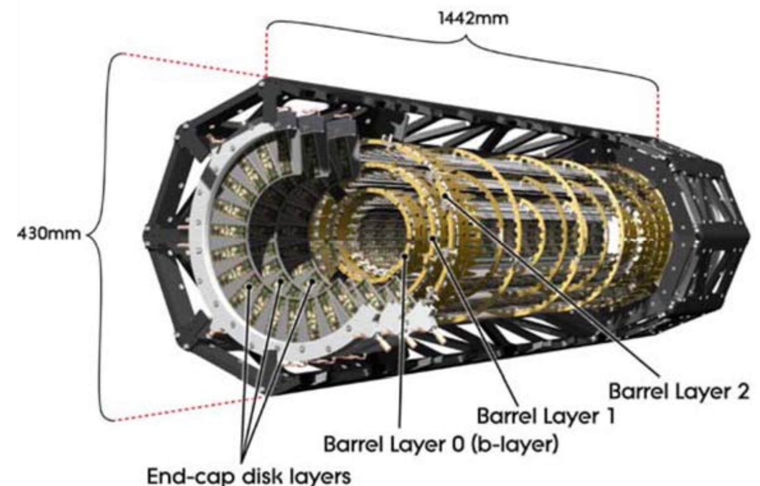


Fig 2. pixel detector consisting of barrel and endcap layers

Upgrade of the B-Layer

◇ Upgrade of the B-Layer

-- Its perfromance degrades after 2~3 years of LHC working with the luminosity of ~300 fb-1 (Dose ~50 Mrad)

-- Prepare the installation of B-Layer upgrade during year 2012-2013

-- Plan of the installation of Super LHC around year 2016-2017

◇ Different aspects of the R&D

-- Detector:

Increase the tolerance to radiation dose by the factor of 3

Introduce the 3D technique to the Sensor to improve the space resolution

-- Design of ASIC

Design new chips for the front end electronics

Increase the tolerance dose upto 200 Mrad

Better resistance to Single Event Upset (SEU)

Function under the luminosity of 10^{34}

◇ Enhancement of the performance

-- Reduction of the overall material

-- Increase the effective area

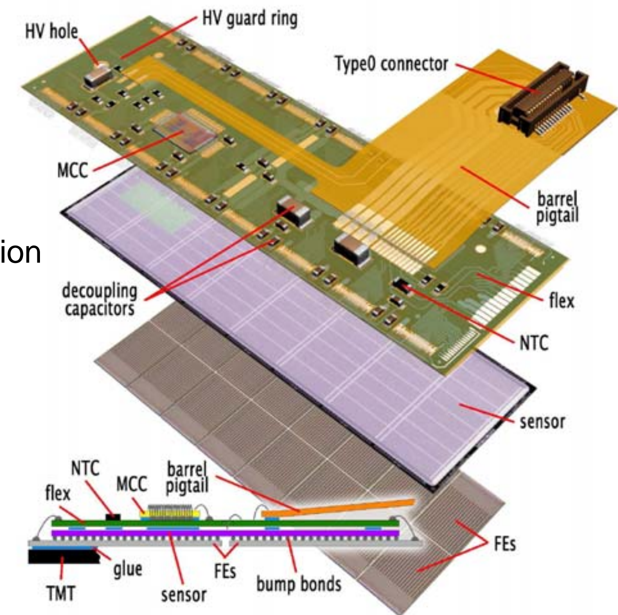
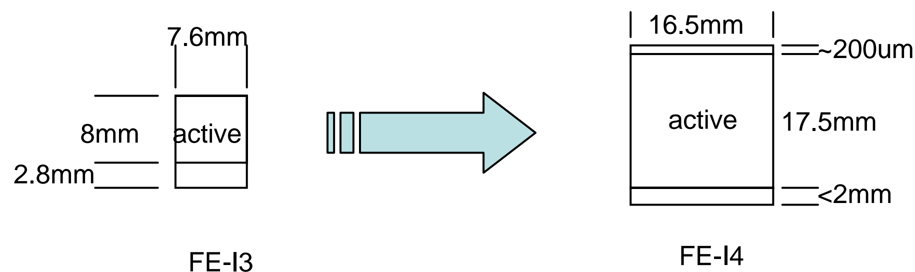


Fig 3. The Silicon Sensor Module

◇ Because the new system is a new layer which is inserted inside the original one, it requires a higher level of radiation resistance.

Upgrade of the Front End Chip

	FE-I3	FE-I4
Radiation Dose	> 50 MRad	> 200 MRad
Pixel Number Per Chip	18×160	80×336
Pixel Size (um²)	50×400	50×250
Chip Size (mm²)	7.6×10. 8	20.2×19. 0
Chip Number Per Module	16	4
Active Zone	74%	89%
Power Consumption of Analog Part (uA/pixel)	26	10
Power Consumption of Digital Part (uA/pixel)	17	10
Vdd-Aanlog (V)	1.6	1.5
Vdd-Digital (V)	2	1.2
Data Rate of the Pseudo-LVDS Output	40	160



Structure of the Front End Chip

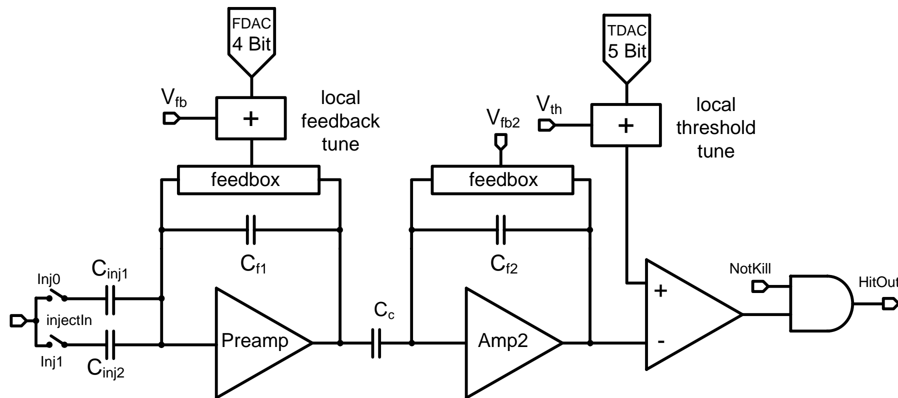


Fig. 4 Structure of the analog part in each pixel

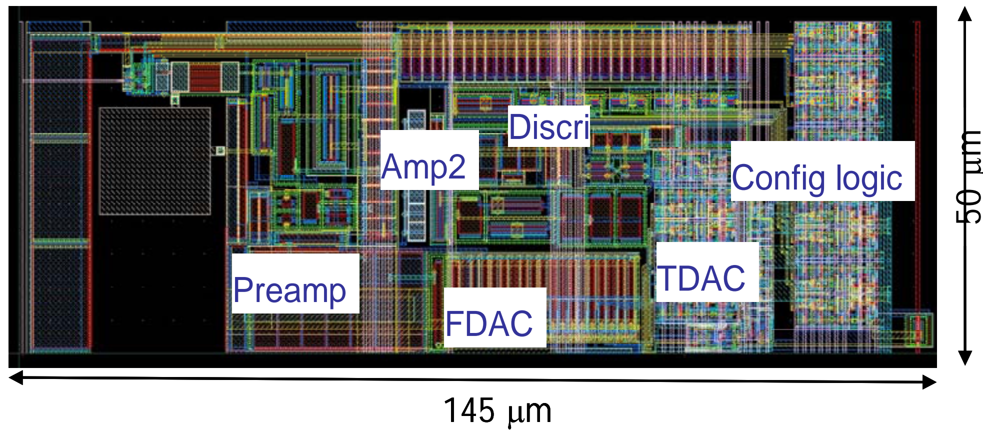


Fig. 5 Actual Layout of the analog part in each pixel

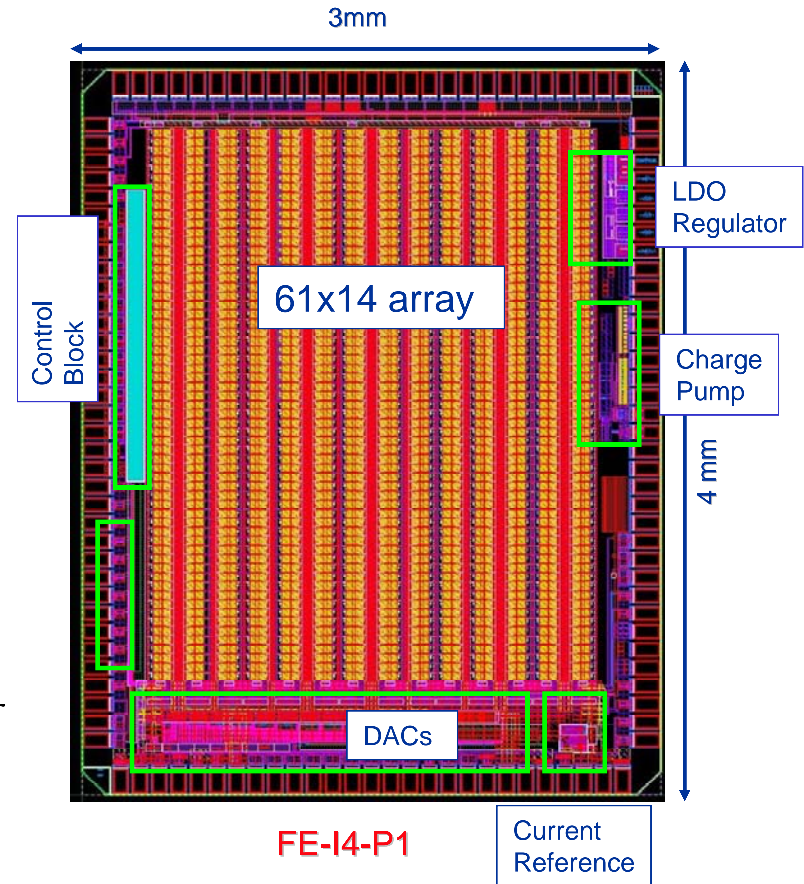


Fig. 6 Layout of FE-I4-P1

R&D of the front end electronics of the Super LHC – 3D Technology

◇ The upgrade of ATLAS Pixel Chips include two different kinds according to the different foundries.

-- **IBM**: FEI4-A → … for the Upgrade of B-Layer
-- **CHART**: FEC4- P1→ FEC4-P2 → FEC4-P3 (2D chip) → … → FETC xx (3D chip) for Super LHC

◇ Current State:

-- FEC4_P1 and FEC4_P2 made in 2009, to validate the technology's translation for 3D chip.
-- FEC4_P3 could validate more functionalities closed in the FEI4_A final design.

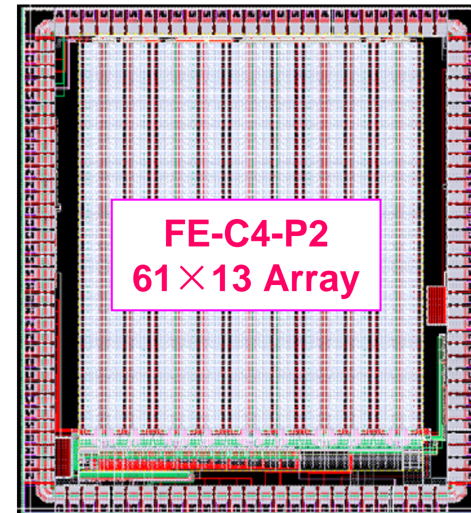
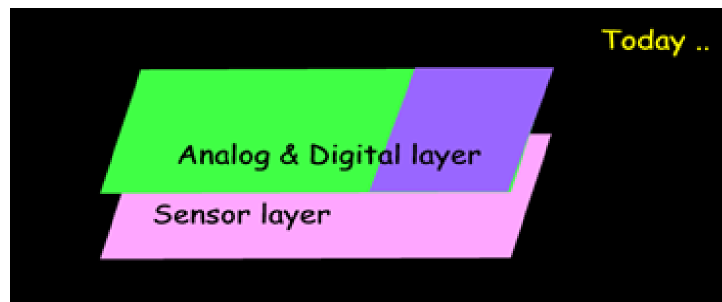


Fig. 7 Layout of FE-C4-P2



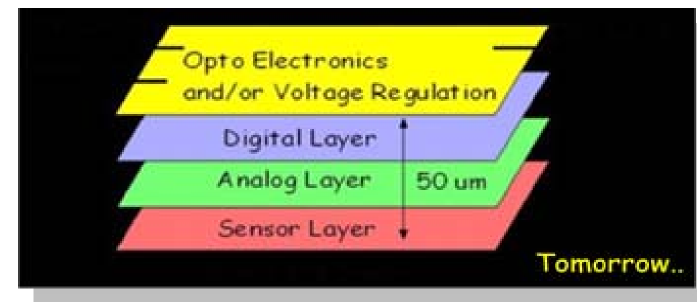


Fig. 8 The upgrade from 2 Dimension Chip to 3 Dimension Chip

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-- Introduction of the analog buffer design and simulation, which is used for signal monitoring in the FE - C4 design

The Design of the 40 MHz SEU Test System Based on DE2 Board

◇ Hardened By Design (HBD) approaches are used to reduce the effect of Single Event Upsets

-- Latches based on the Dual Interlocked Cell (DICE) have redundant storage nodes

-- restores the original state when an SEE error is introduced in one node

-- However, As the device size shrinks, the space between sensitive nodes becomes more critical for SEE because of the charge sharing between nodes.

◇ To test the performance of the architectures, SEU chips are designed

-- 7 blocs of cells are implemented in this chip

-- Each tested cell is composed of 3 latches connected in triple redundancy structure.

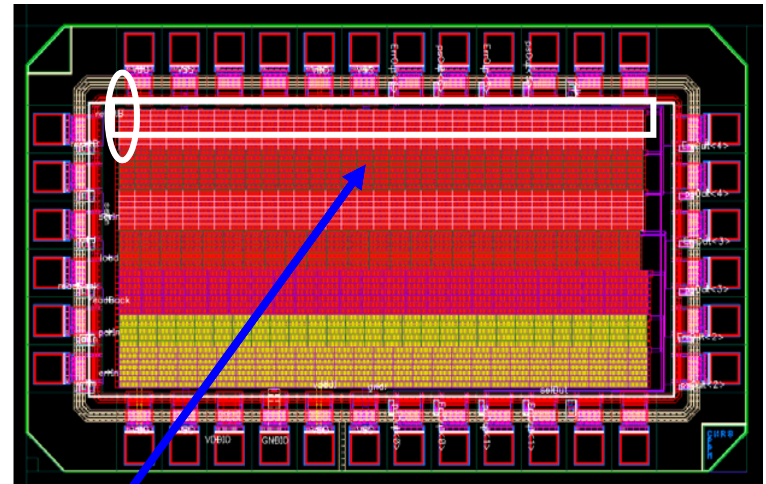


Fig. 9 Layout of the SEU Chip

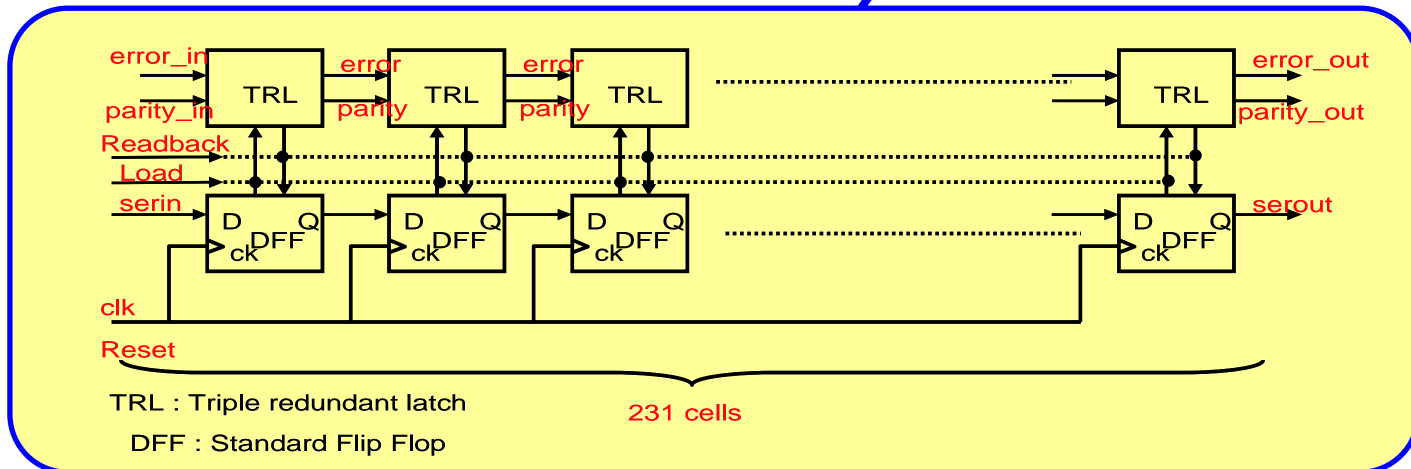


Fig. 10 The structure of one of the channels

The Experiment Setup of the SEU Test System for the irradiation

-- Irradiation tests were carried out using IRRAD3 beam line of the Proton Synchrotron (PS) facility at CERN.
-- The test beam provides a beam of 24 GeV protons It contains several spills of particles The duration of each spill is 400 ms.

-- The intensity can be tuned typically from 5×10^{10} to 1.5×10^{11} protons/spill.
-- The chip is controlled and read out by the FPGA on the DE2 Board (instead of the PCMCIA card in old setup), which is controlled by a PC laptop.
-- An interface board located in the computing area converts 5V TTL signals to LVDS signals.
-- Differential buffers drive a 20 meter twisted pair cable to transmit and receive pattern data and control signals in differential mode.
-- An intermediate board located in the irradiated zone is connected with a 5 meter flat cable to the board under test.
-- In order to have enough statistics for SEU estimation, the total proton fluencies provided to the chip is around $1.7 \times 10^{15}/cm^2$.

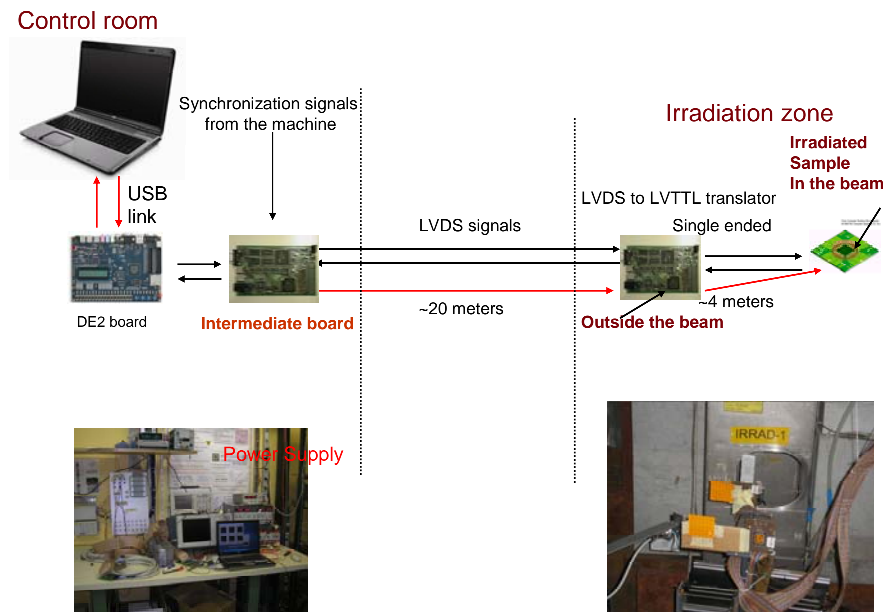


Fig. 11 Experiment Setup of the SEU system for irradiation test

Features of the SEU Test System based on DE2 Board for 40 MHz

◇ **Features for this SEU Test System:**

-- Operation frequency is greatly enhanced.

-- Flexible operation frequency. Operation frequency could vary from 1.2 kHz to 40 MHz.

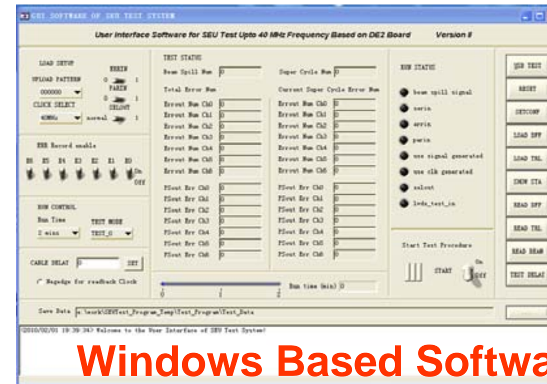
-- Better synchronization of the test sequence with the super cycle and beam signals from the PS Facility.

-- Full fledged system setup. A FPGA with Nios II embedded core and USB interface is implemented, and a windows based software is developed.

-- Signal integrity is carefully considered, since signals transmit through long cables.

◇ **Current Progress:**

-- The whole system has been established, and now in the process of long time test in the laboratory.



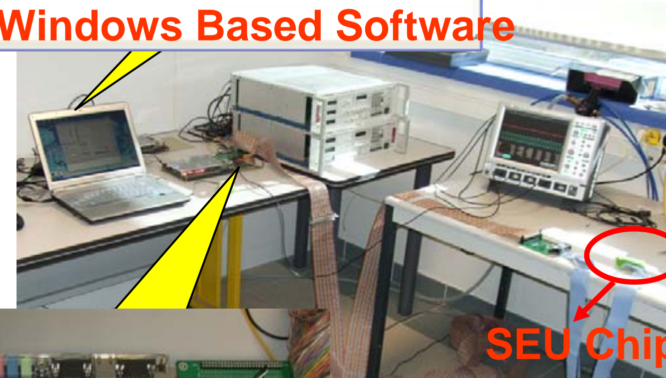


Fig. 12 The Setup of the SEU system in the laboratory test

Graphic User Interface of the software and functions of the FPGA

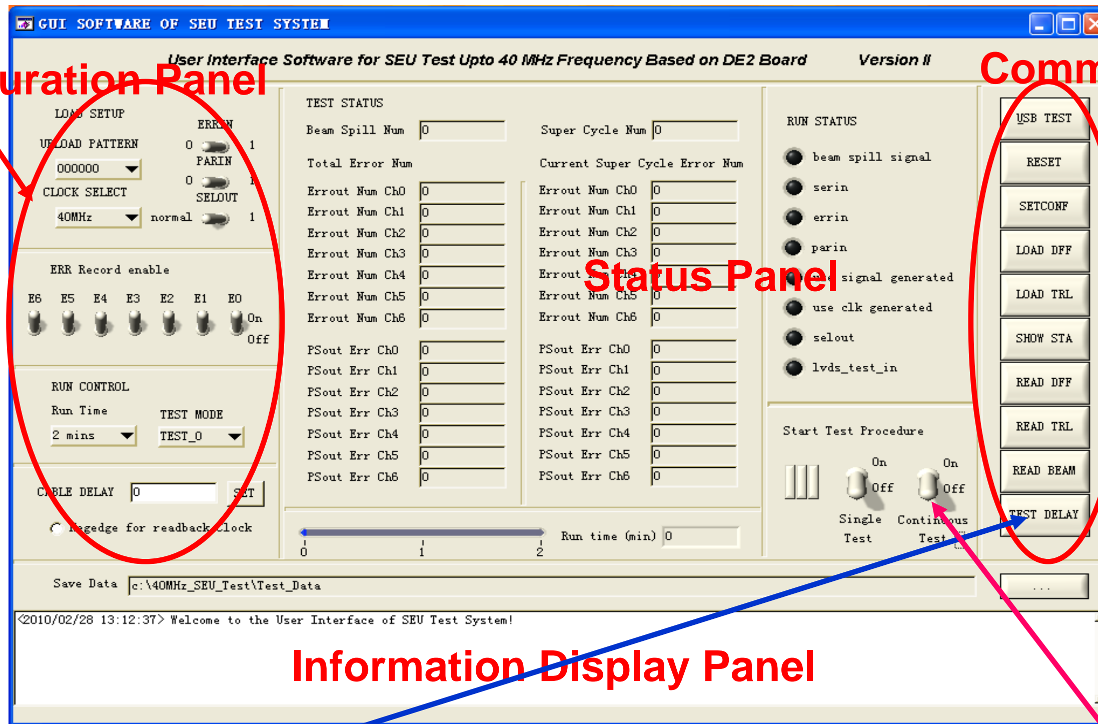


Fig. 13 The Graphic User Interface of the software

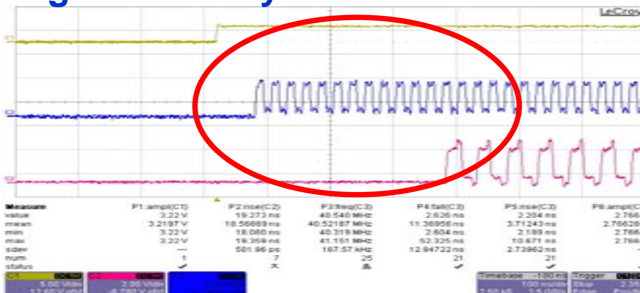
```
Test Mode:
1
Upload Pattern: // 0--
2
Clock Selection: // 0--
0
ERR Record Channel Enable: //Ch6 .. Ch0
1 1 1 1 1 1 0
Run Time: //
15
Edge Select: //1 -- Negative Edge
1
Cable Delay Value:
11
---------------------------------
Test Mode:
3
Upload Pattern: // 0--
2
Clock Selection: // 0--
0
ERR Record Channel Enable: //Ch6 .. Ch0
1 1 1 1 1 1 0
Run Time: //
15
Edge Select: //1 -- Negative Edge
1
Cable Delay Value:
11
---------------------------------
```

Automatic test function using scripts

Synchronization of the read back data

--Function of testing cable delay

40 MHz



The value of the cable delay (period) -- 12

Serout	s1	s2	s3	s4	s5	s6	s7
No.000	0	0	0	0	1	1	1
No.001	0	0	0	0	0	0	0
No.002	0	0	0	0	0	0	0
No.003	0	0	0	0	0	0	0
No.004	0	0	0	0	0	0	0
No.005	0	0	0	0	0	0	0
No.006	0	0	0	0	0	0	0
No.007	0	0	0	0	0	0	0
No.008	0	0	0	0	0	0	0
No.009	0	0	0	0	0	0	0
No.010	0	0	0	0	0	0	0
No.011	0	0	0	0	0	0	0
No.012	0	0	0	0	0	0	0

Basic Structure of the Logic in FPGA and the Software on the Laptop

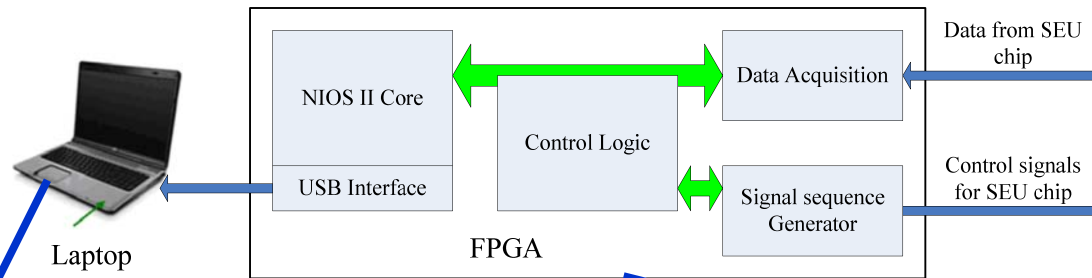


Fig. 14 The Architecture of the 40 MHz SEU Test System

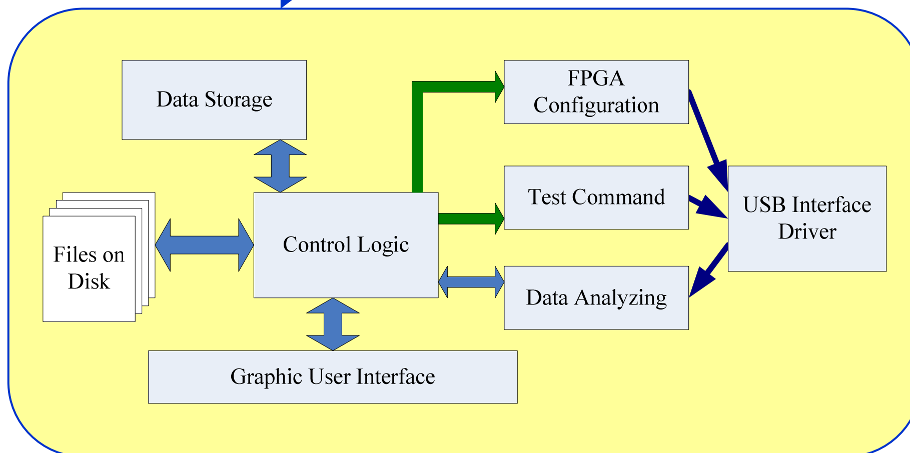


Fig. 15 The Architecture of GUI software on the Laptop

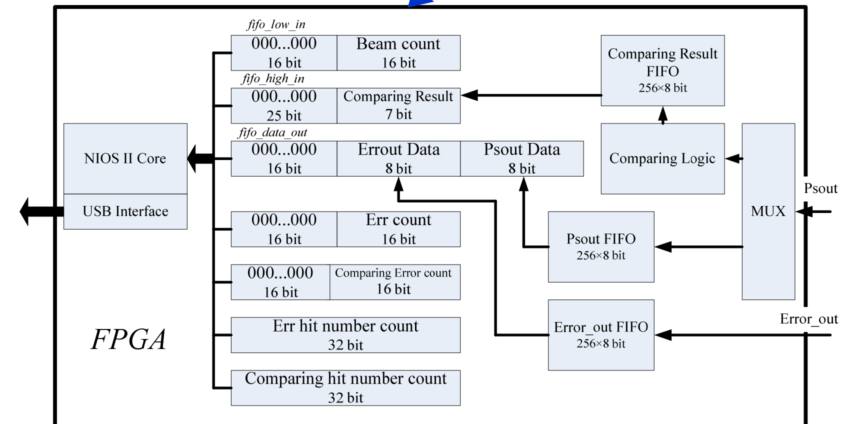


Fig. 16 The Architecture of the Logic of the FPGA on the DE2 Board

Simulation for the signal integrity of the transmission through long cables

-- Because the signals are transmitted through 20 meter long twisted cable and 5 meter long flat cable, while the operation frequency is up to 40 MHz, signal integrity is requires great care.

-- Simulations and tests have been conducted to find the optimum solution for impedance match and signal shielding.

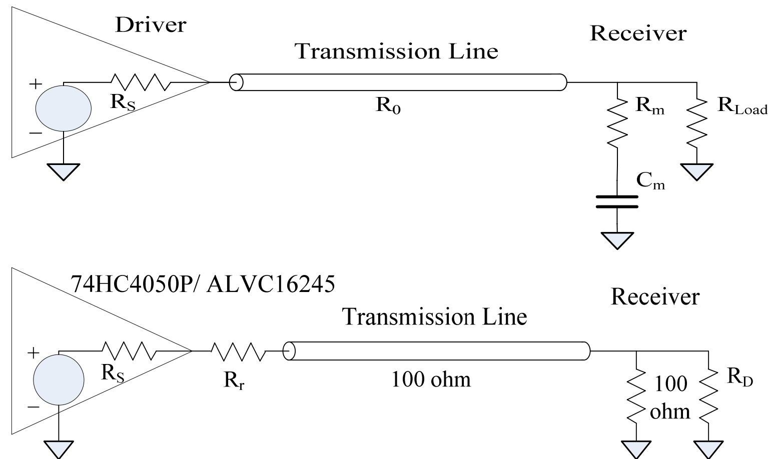


Fig. 17 The simulation setup for the signal transmission through long cables

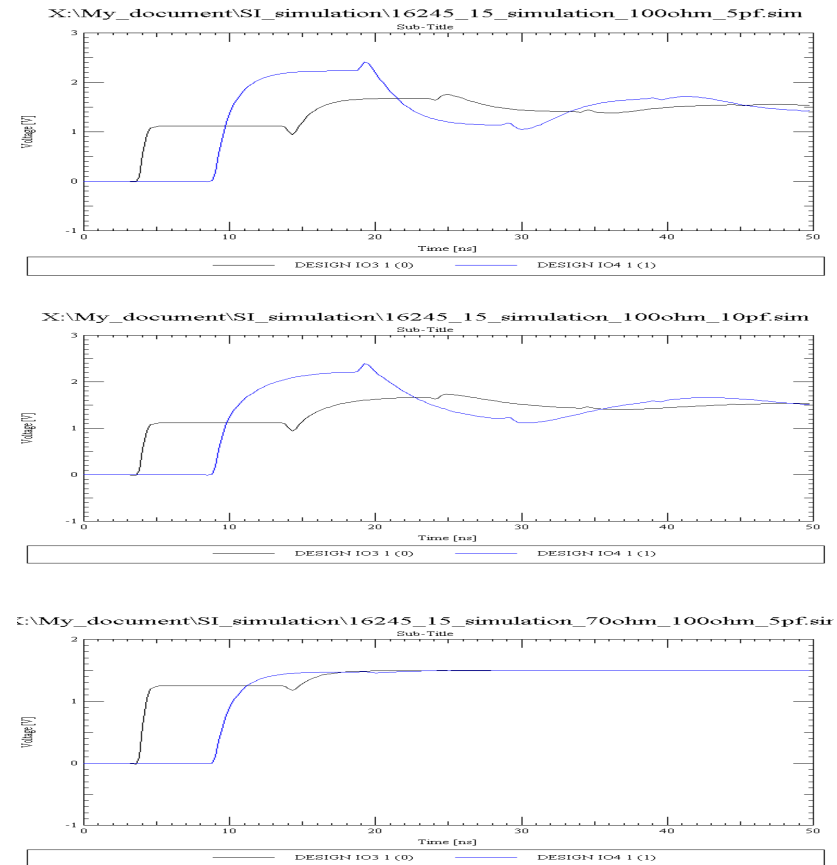


Fig. 18 The waveforms in the simulation result

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Analog buffer Design for FEC4_P3

◇ To test the performance of different parts in the FE-C4 Chip, the multiplexer and analog buffer is required to monitor different nodes.

-- The multiplexer is used to select different nodes as the input to the analog buffer for signal output.

-- The Analog Buffer block is a multi-purpose operational amplifier which could be used in different blocks.

◇ The characteristics of that buffer:

-- Cload max=50pF Rload max=1Kohm
-- Bandwith @unity gain: 60MHz ($@C_{load\ max}$, $R_{load\ max}$)
-- Positive slew rate : 29V/μs ($@C_{load\ max}$, $R_{load\ max}$)
-- Negative slew rate : 23V/μs ($@C_{load\ max}$, $R_{load\ max}$)
-- Power on quiescent current :
1.6mA(Vinputdc=100mV)~3.5 mA ($V_{inputdc}$=1.4V)
-- DC gain : 49dB(@Vi_{nputdc}=100mV or1.4V)
~80dB(@Vi_{nputdc}=750mV)
-- Bandwidth : 10kHz ($@C_{load\ max}$, $R_{load\ max}$)
-- Phase margin : 61° ($@C_{load\ max}$, $R_{load\ max}$)
-- Port: inn inp Ibias vdda gnda suba Bufferout PWR

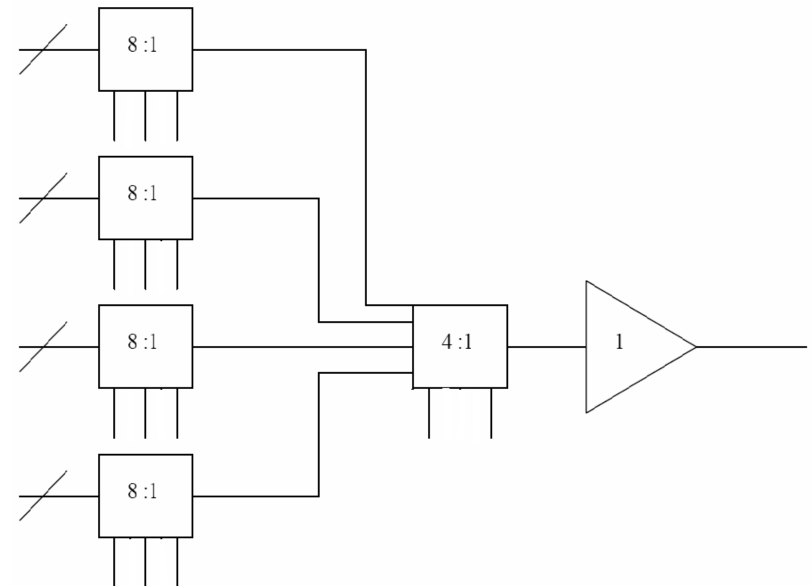

Fig. 19 The Multiplexer and Analog Buffer which is used to monitor the different nodes

Basic Structure of the analog buffer

◇ **Include 4 parts**

-- Bias part : provide bias for the circuits

-- Complementary input :

The input stage is a classical complementary NMOS and PMOS differential pair, ensuring a beyond rail to rail input.

-- Differential to single:

The second stage is a high-swing cascaded differential to single－ended circuitry with very high input impedance to maximize the first stage gain

-- Class AB output:

The third stage is a rail-to-rail class AB amplifier biased by a diode cascade circuitry

◇ **Rail-to-rail configuration**

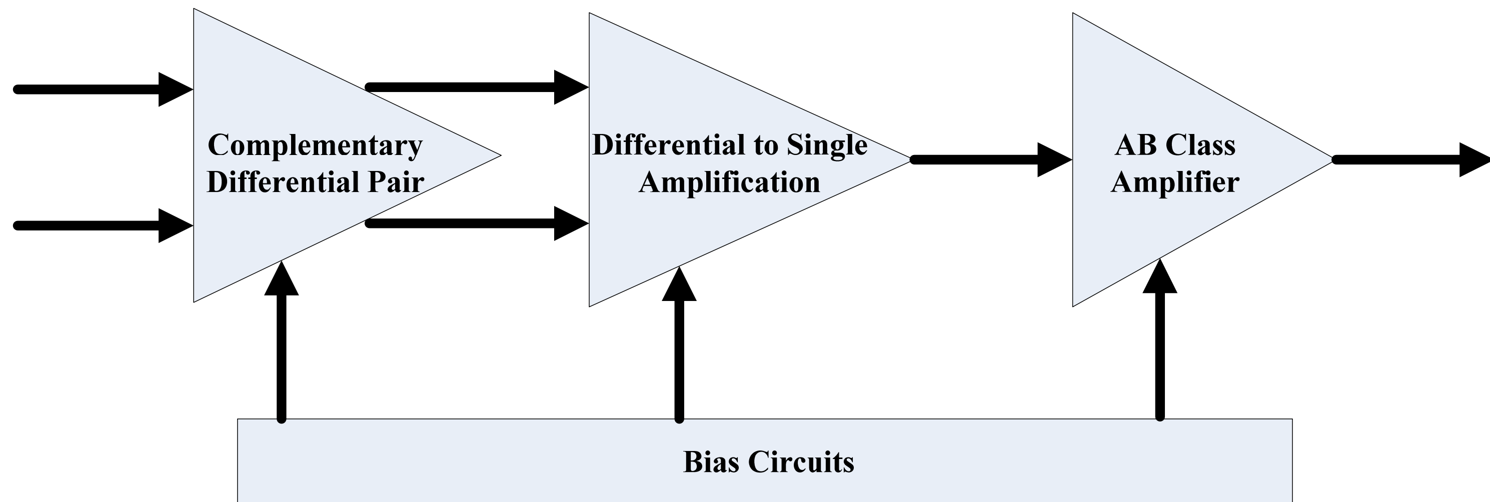

Fig. 20 The basic structure of the analog buffer

Simulation of the Analog Buffer

◇ Slew rate Simulation

The slew rate simulated in the mid dynamic is 29V/μs for positive signal and -23V/μs for negative signal.

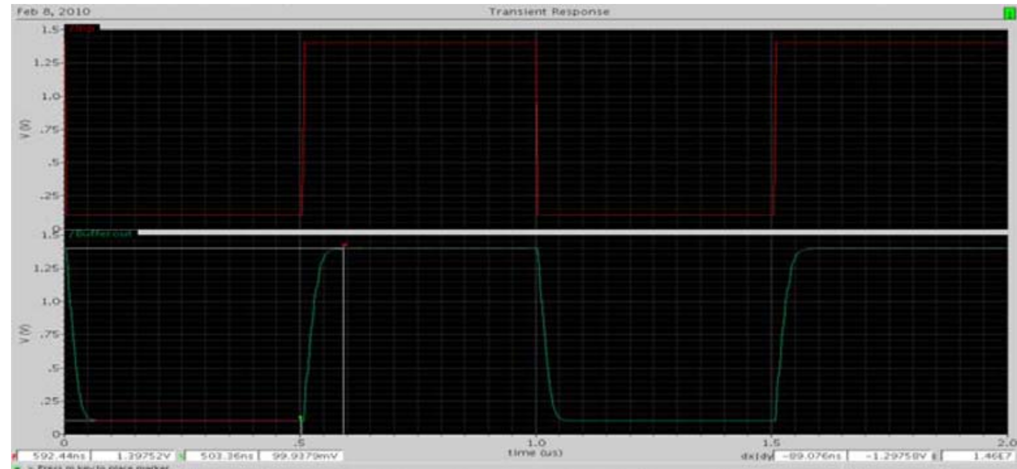

Fig. 21 The waveforms of the slew rate simulation result

◇ Unity gain transient simulation

One of the most requested application for the opamp is the unity gain buffer. The Simulation here shows the transient waveform of the opamp.(input Vs output)

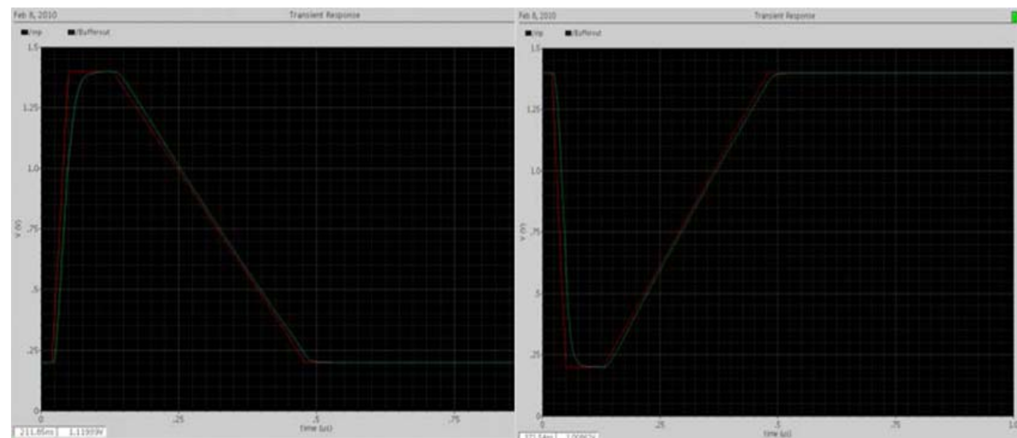

Fig. 22 The waveforms of the unity gain transient simulation result

Simulation of the Analog Buffer

◇ Power supply ripple rejection ratio

PSRR+:39dB PSRR－:57dB@$V_{inputdc}$=0.75V

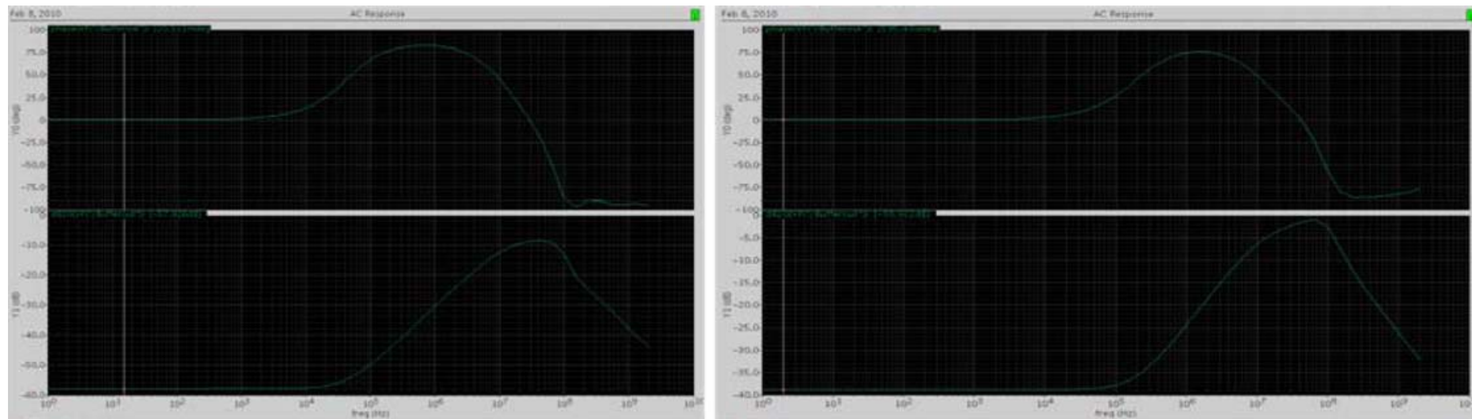

Fig. 23 The waveforms of the power supply ripple rejection ratio simulation result

◇ Open loop characteristics

-- DC gain :74dB
-- Bandwidth : 10 kHz (@ $C_{Loadmax}$, $R_{Loadmax}$)
-- Unity - Gain Bandwidth : 56 MHz
(@ $C_{Loadmax}$, $R_{Loadmax}$)
-- Phase Margin : 57 °
(@ $C_{Loadmax}$, $R_{Loadmax}$)

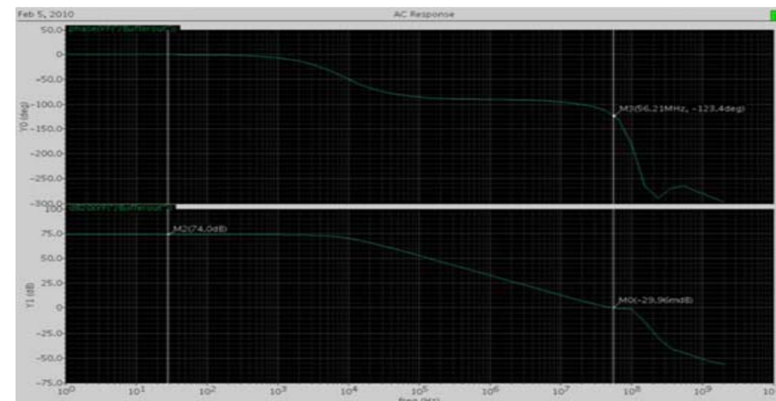

Fig. 24 The waveforms of the open loop characteristics simulation result

Simulation of the Analog Buffer and its Layout

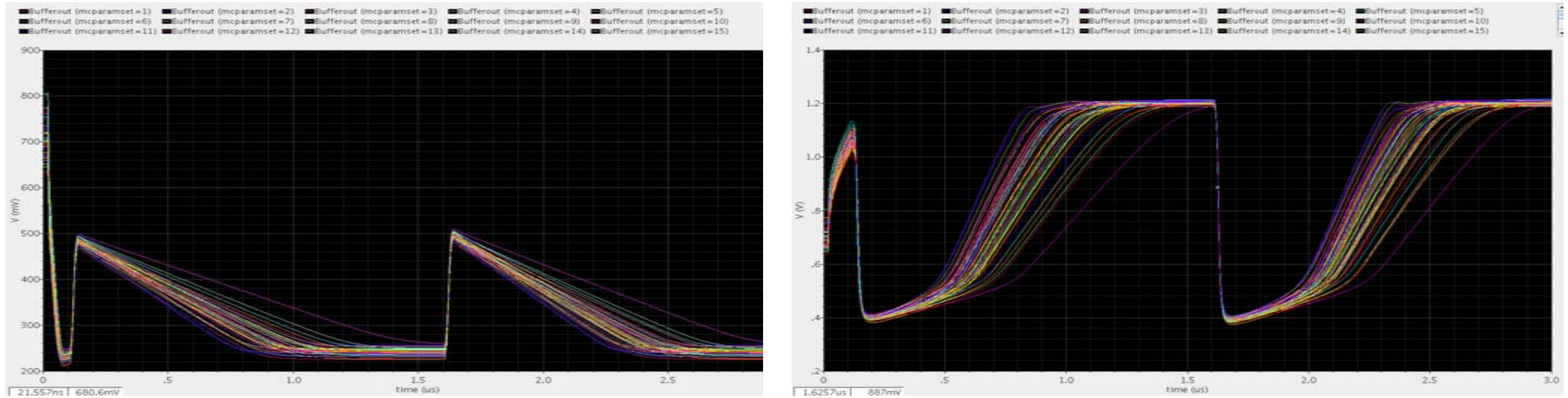

Fig. 25 Monte Carlo simulation (Frontend output through Mux and buffer)

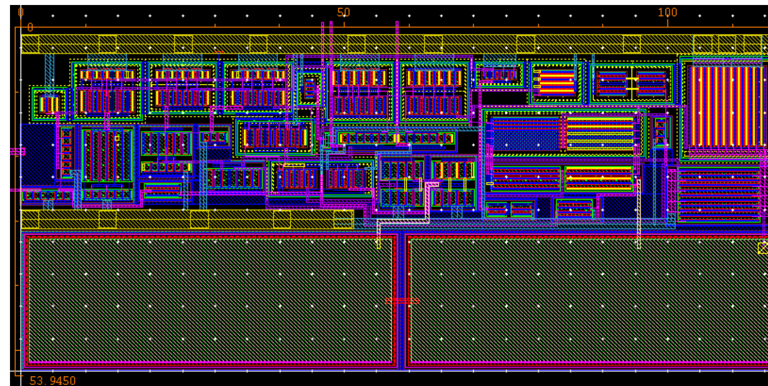

Fig. 26 Layout of the Analog Buffer

Summary

-- Cooperation has started on the Research and Design for the upgrade of the ATLAS Pixel Detector.

-- Work has been conducted for the front end electronics design.

-- The SEU test system of 40 MHz has been designed and now in long time test, then will be installed at CERN for irradiation test.

-- The Analog Buffer which is used in the design of FE-TC4 has been designed, simulated and the layout has been conducted.

-- More cooperation both in the establishment of the electronics test system and ASIC design for the front end chips is expected.

Thanks