

Trigger Processor STATUS

21th AGATA Week

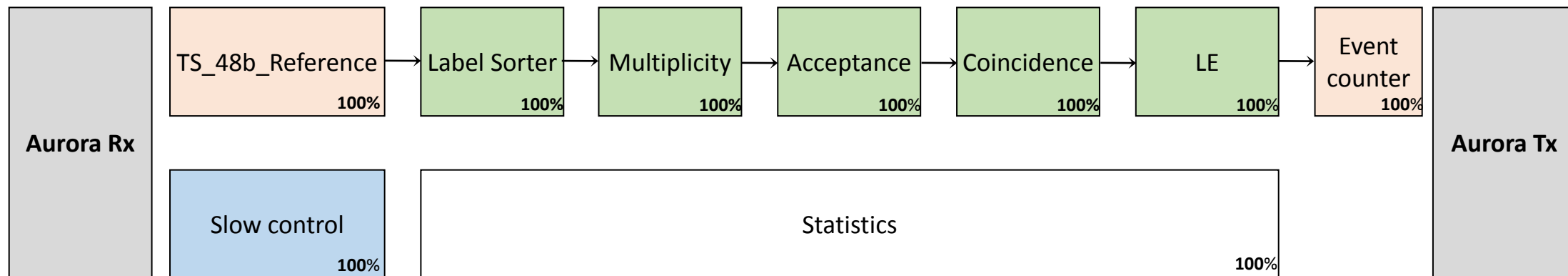
Electronics and Data Flow session

on Friday March 26, 2021



Xilinx Evaluation Kit : VC707 (Virtex-7 XC7VX485T-2FFG1761C)

TRIGGER PROCESSOR



STP-PHYSIQUE		Réf.
		N°x: 1 Pages: 8

GTS TRIGGER PROCESSOR SPECIFICATIONS TECHNIQUES

Version 1.0
24.10.2018

TRIGGER PROCESSOR GUIDE UTILISATEUR

Auteur : A BOUJRAD
Date : 2/04/2019

La documentation technique du « Trigger Processor » TP se trouve sur le site wiki du GANIL :

<http://wiki.ganil.fr/gap/GAMMA/attachement/wiki/EXOGAM2/Projet/TP/STP-439A%20-%20SP%20EXOGAM2%20Trigger%20Processor.pdf>

I-Présentation de la carte TP

Le TP est basé sur le kit d'évaluation Xilinx VC707 (Figure 1). Le manuel d'utilisateur de la VC707 se trouve à l'adresse :

https://www.xilinx.com/support/documentation/boards_and_kits/vc707ug085_vc707_eval_bd.pdf



Figure 1 Photo et Block Diagramme du Kit d'évaluation VC707

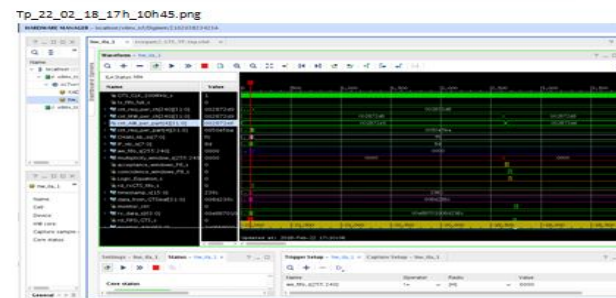
- Technical Specifications
- User Guide
- Tests Report
- Git Repository

TP tests Report

A. BOUJRAD
23/10/2020

22-27/02/2018

Nom	Date	Type	Taille
tp_22_02_18_17h_10_45.png	22/02/2018 17:09	Image PNG	93 Ko
tp_test_23_12_16_16.png	23/02/2018 12:36	Image PNG	79 Ko
12.png	23/02/2018 12:32	Image PNG	80 Ko
12.png	23/02/2018 12:32	Image PNG	79 Ko
tp_femt_cycle0.png	26/02/2018 09:29	Image PNG	67 Ko
tp_femt_cycle2.png	26/02/2018 09:21	Image PNG	69 Ko
tp_femt_cycle3.png	26/02/2018 09:21	Image PNG	67 Ko
tp_femt_cycle4.png	26/02/2018 09:22	Image PNG	69 Ko
tp_femt_cycle5.png	26/02/2018 09:26	Image PNG	63 Ko
tp_anomalie_1.png	26/02/2018 11:35	Image PNG	74 Ko
tp_start_cycle00.png	26/02/2018 11:44	Image PNG	71 Ko
tp_start_cycle01.png	26/02/2018 11:47	Image PNG	71 Ko
tp_message_in_fifo_full.png	26/02/2018 13:13	Image PNG	67 Ko
tp_message_in_fifo.png	26/02/2018 13:17	Image PNG	67 Ko
tp_message_in_fifo_full_05.png	26/02/2018 13:22	Image PNG	71 Ko
tp_start_T548_00.png	26/02/2018 14:50	Image PNG	66 Ko
tp_start_T548_05.png	26/02/2018 14:50	Image PNG	66 Ko
tp_start_valid.png	27/02/2018 09:38	Image PNG	71 Ko
tp_start_valid05.png	27/02/2018 09:51	Image PNG	72 Ko
tp_start_30.png	27/02/2018 14:45	Image PNG	63 Ko



Tests TP du 1/12/2020 A. BOUJRAD

Tests effectués dans le laboratoire Electronique (Abderrahman et Chibeb).
Puis tests sur AGATA (Emmanuel, Abderrahman et Chibeb).

A/ Test en Labo

avec le module Numexo2-106_IP=206) et PC ganp879.

Les canaux sont les suivants :

Channel	IP (Décimal)	IP (Hexa)
0	221	DD
1	220	DC
2	219	DB
3	218	DA
4	217	D9
5	216	D8
6	215	D7
7	214	D6
8	213	D5
9	212	D4

Commit to: master new branch

Message:

Amend Last Commit

Set author gate

Set author

Add Signed-off-by

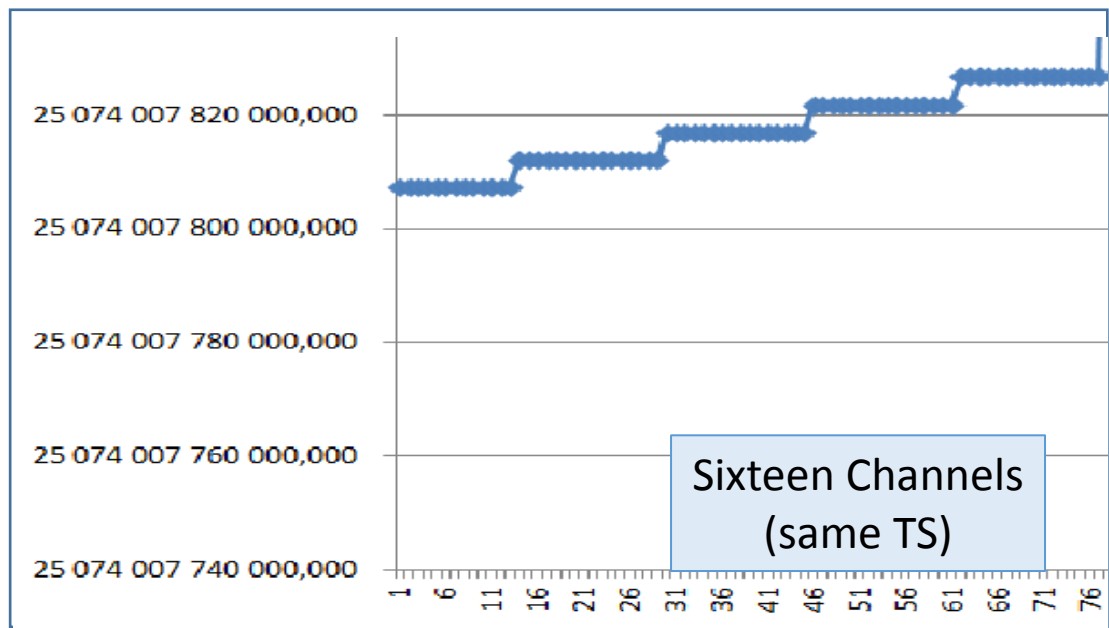
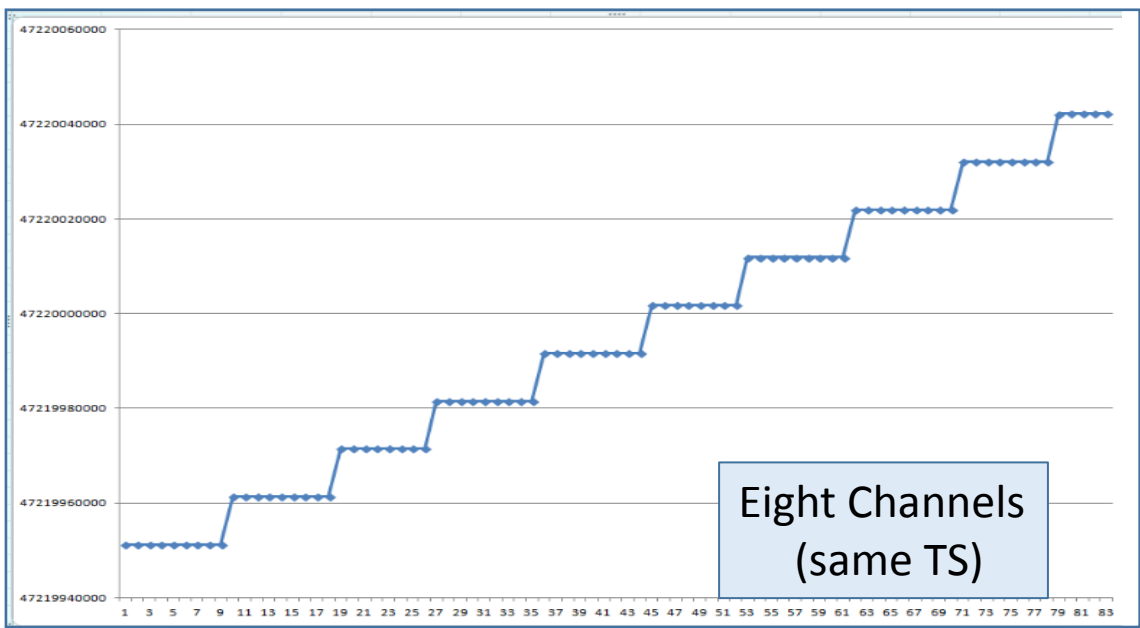
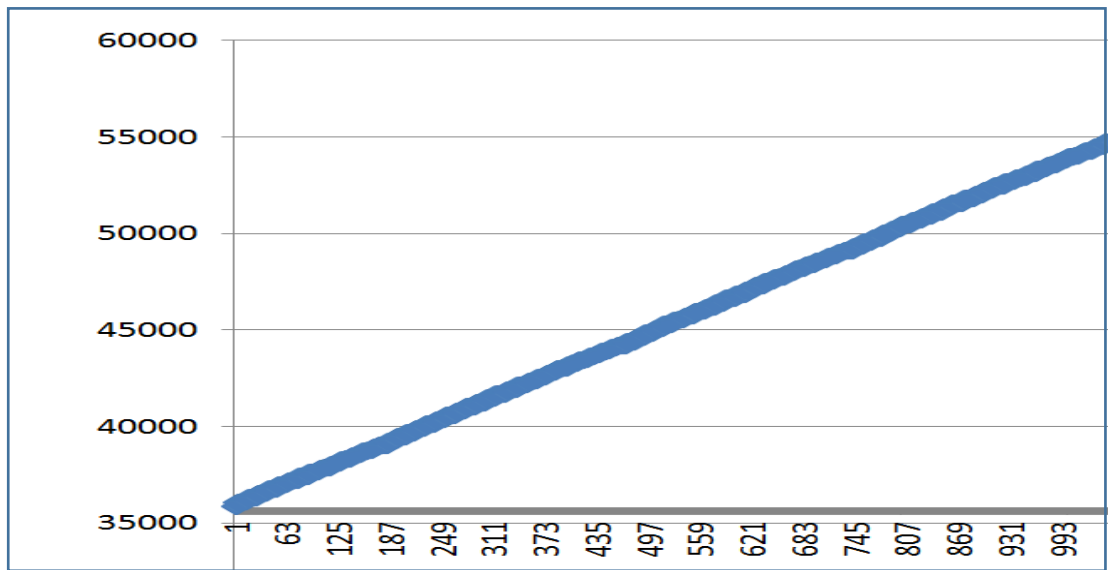
Changes made (double-click on file for diff):

Path	Extension	Status	Lines added	Lines removed
pcres/gts_leaf_v1_00_a/SC_Embedded/trunk		Added	1	0
pcres/gts_leaf_v1_00_a/data/gts_leaf_v2_1_0.mpd	mpd	Modified	98	12
pcres/gts_leaf_v1_00_a/data/gts_leaf_v2_1_0.pao	pao	Modified	26	1
pcres/gts_leaf_v1_00_a/dev/create_cip	cip	Modified	1	1
pcres/gts_leaf_v1_00_a/dev/gpwiz.log	log	Modified	264	103
pcres/gts_leaf_v1_00_a/dev/gpwiz.opt	opt	Modified	1	1
pcres/gts_leaf_v1_00_a/hdl/vhdl/gts_leaf.vhd	vhd	Modified	4	17
pcres/gts_leaf_v1_00_a/hdl/vhdl/gts_leaf_fd.vhd	vhd	Modified	39	11
pcres/gts_leaf_v1_00_a/hdl/vhdl/leaf_top.vhd	vhd	Modified	110	65
pcres/gts_leaf_v1_00_a/hdl/vhdl/trigger_leaf_exogam.vhd	vhd	Modified	39	12
pcres/gts_leaf_v1_00_a/hdl/vhdl/trigger_match.vhd	vhd	Modified	0	18
pcres/gts_leaf_v1_00_a/hdl/vhdl/user_logic.vhd	vhd	Modified	224	206
pcres/gts_leaf_v1_00_a/netlist/rifo_128b.ngc	ngc	Modified	1	1
pcres/gts_leaf_v1_00_a/netlist/rifo_128b.vhd	vhd	Modified	23	29

14 files selected, 14 files total

View Patch >>

Commit Cancel Help



	ATCA	GGP	Accept	Reject	Equation
1	1 channel in P1		100%		
2	2 channels in P1		100%		
3	19 channels in P1		100%		
4		1 channel in P1	100%		
5		2 channels in P1	100%		
6		20 channels in P1	100%		
7	19 channels in P1	20 channels in P2		0.2 % (GGP)	P1 OR P2

8 **2 adjacent ATCA** Cristals (Compton event) associated to **P1** (multiplicity > **2**) :
 Result : **10 to 20%** of coincidence as expected

9 **2 GGP** with Synchro Pulser associated to **P1** (multiplicity > **2**) :
 Result : **2%** of rejection (to be explained)

For tests **8 & 9** if multiplicity threshold is set to 3 a 0% validation is obtained as expected

- **Trigger Processor IP developments**
 - *Chiheb Belkhiria*
 - *Abderrahman Boujrad*

- **Python** (*Slow control, Statistics...*)
 - *Laurent Charles*
 - *Sébastien Coudert*
 - *Chiheb Belkhiria*

- **IPBUS**
 - *Laurent Charles*
 - *Chiheb Belkhiria*

- **GUI**
 - *Blandine Duclos*

- **TP tests**
 - *Abderrahman Boujrad*
 - *Emmanuel Clement*
 - *Chiheb Belkhiria*

(courtesy to B. Duclos)

The screenshot shows the Trigger Processor GUI with the following elements:

- File Menu:** File, Tools, Help
- File List:**
 - File 1: /home/duclos/Tempo/TP_GUI/TPAddrTable_8_256.dat
 - File 2: /home/duclos/Tempo/TP_GUI/TP_CfgTable_8_256.dat
- Status:** Last save: 17/03/2021 16:59, Nb partitions: 8, Nb voies: 256
- Partition Selection:** A vertical list on the left shows partitions P0 through P7. P1 is selected.
- Partition 0 View:** A grid of 256 channels (0-255) with columns labeled 'Voies', 'Parametres', and 'LE'. Channels 11 and 12 are highlighted in green.
- General Parameters:** A panel on the right titled 'Paramètres généraux TP' with tabs for 'Standards settings' and 'Advanced'.
- Buttons:** 'See synthesis' and 'TP Setup' at the bottom.

Annotations:

- Setup Files:** Points to the file list area.
- Channels association to a selected Partition:** Points to the highlighted channels in the Partition 0 grid.
- Partition selection:** Points to the P1 selection in the left sidebar.

Partition 0 Enabled

Voies Parametres LE

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

- By shape selection (in green) :

	73	74	75	76
	89	90	91	92
4	105	106	107	108
0	121	122	123	124
6	137	138	139	140

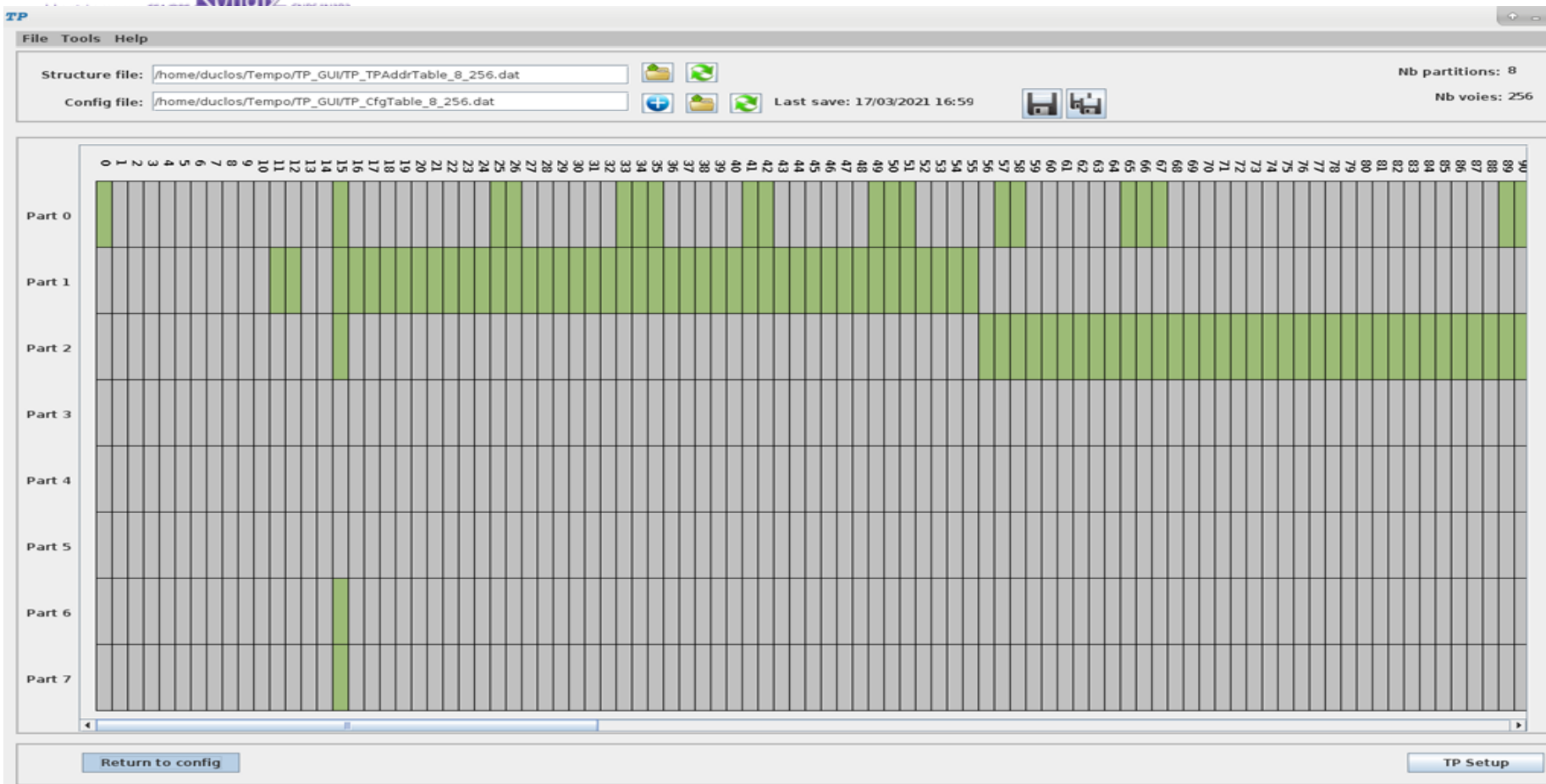
- By using the context Menu :

	69	70	71	72
	85			
0	101			
6	117			
2	133	134	135	136

- Assign all
- Unassign all
- Assign all the column
- Unassign all the column
- Assign all the line
- Unassign all the line

15
31
47
63
79

Part:
0
1
2
6
7



Nb partitions: 8
Nb voies: 256

tion.dataserver.Subprocess.Backend.Caler
.dataserver.Subprocess.Backend.Calendar
tion.dataserver.Subprocess.Backend.Addr

orkspace -XC+UseG1GC -XC+UseStringDe

Run Setup

Clear logs

Save logs

Exit Setup

```

root 22657 2 0 09:58 ? 00:00:00 [kworker/2:2]
duclos 24305 2179 0 11:35 ? 00:01:12 /usr/lib64/firefox/firefox
duclos 24365 24305 1 11:35 ? 00:02:09 /usr/lib64/firefox/plugin-container -gremomi /usr/lib64/firefox/omni-ja -appomni /usr/lib64/firefox/browser/omni-ja -appdir /usr/lib64/firefox/brow
root 24641 2 0 11:43 ? 00:00:03 [kworker/0:1]
root 26085 2 0 12:55 ? 00:00:00 [kworker/2:0]
duclos 26253 1 0 12:58 ? 00:00:00 /usr/bin/xfce4-terminal
duclos 26258 26253 0 12:58 ? 00:00:00 gnome-pty-helper
duclos 26259 26253 0 12:58 pts/0 00:00:00 -csh
duclos 26576 1 0 13:04 ? 00:00:01 /usr/bin/knotify4
duclos 27457 1 0 13:29 ? 00:00:00 /usr/lib64/libreoffice/program/oosplash --impress smb://wincluusers/utilisateurs$/duclos/Mes%20Documents/TP_GUI/Documentation-Presentation-Pre
duclos 27471 27457 5 13:29 ? 00:03:25 /usr/lib64/libreoffice/program/soffice.bin --impress smb://wincluusers/utilisateurs$/duclos/Mes%20Documents/TP_GUI/Documentation-Presentation-Pre
root 28605 2 0 14:07 ? 00:00:00 [kworker/3:2]
root 28870 2 0 14:18 ? 00:00:00 [kworker/3:1]
root 28998 2 0 14:23 ? 00:00:00 [kworker/0:0]
root 29018 2 0 14:23 ? 00:00:00 [kworker/3:0]
root 29093 2 0 14:25 ? 00:00:00 [kworker/1:2]
root 29216 2 0 14:28 ? 00:00:00 [kworker/0:2]
root 29389 814 0 14:32 ? 00:00:00 sleep 60
duclos 29406 2309 31 14:32 ? 00:00:01 /usr/lib/jvm/jdk1.8.0_161/bin/java -Dfile.encoding=UTF-8 -classpath /home/duclos/TP_GUI/TP_GUI/bin/Vues.Lanceur DEBUG DEV
duclos 29434 29406 0 14:32 ? 00:00:00 ps -ef
  
```

Partition 0 Enabled

Voies Parametres LE

Multiplicity window width

10 655 10 ns us

Multiplicity window Threshold

1 255 2

Acceptance window width

10 655350 300 ns us

Coincidence window width

10 655350 400 ns us

Coincidence window delay

10 655350 500 ns us

TP Windows

- Multiplicity window width
- Multiplicity window threshold
- Acceptance window
- Coincidence window width
- Coincidence window delay

Partition 0 Enabled

Voies Parametres LE

Partition Logical Equation

P7 P6 P5 P4 P3 P2 P1 P0 LE0 = 3

P1 OR P0

General Logical Equation

(P3 OR P2) AND (P1 OR P0)

Logic equation

- Partition selection
- LE Formula
- Logic equation expression

- **Continuation of the TP tests With AGATA system's**
 - High counting rate on April 2021
 - AGATA/NUMEXO2 coupling
- **Tests and validation of The GUI**
 - In the next weeks
- **Document finalization**