Trigger Processor STATUS

21th AGATA Week

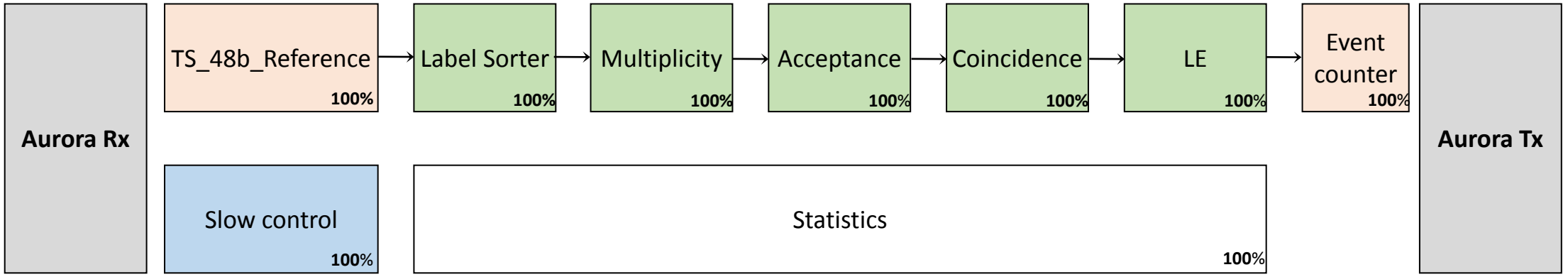
Electronics and Data Flow session

on Friday March 26, 2021

Trigger Processor development

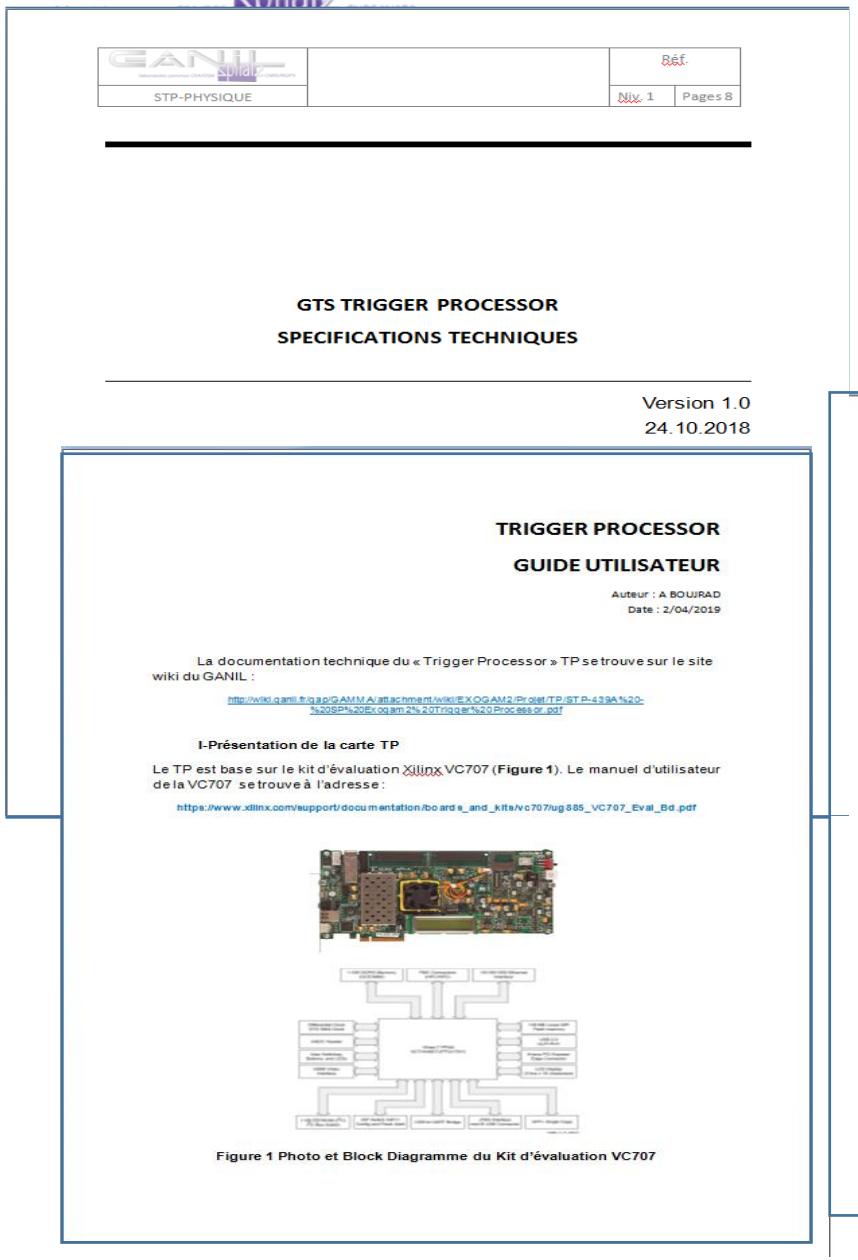
Xilinx Evaluation Kit : VC707 (Virtex-7 XC7VX485T-2FFG1761C)

TRIGGER PROCESSOR



TP Documentation

- Technical Specifications
- User Guide
- Tests Report
- Git Repository



		Réf.
STP-PHYSIQUE		Niv. 1 Pages 8

GTS TRIGGER PROCESSOR

SPECIFICATIONS TECHNIQUES

Version 1.0
24.10.2018

TRIGGER PROCESSOR

GUIDE UTILISATEUR

Auteur : A BOUJRAD
Date : 2/04/2019

La documentation technique du « Trigger Processor » TP se trouve sur le site wiki du GANIL :

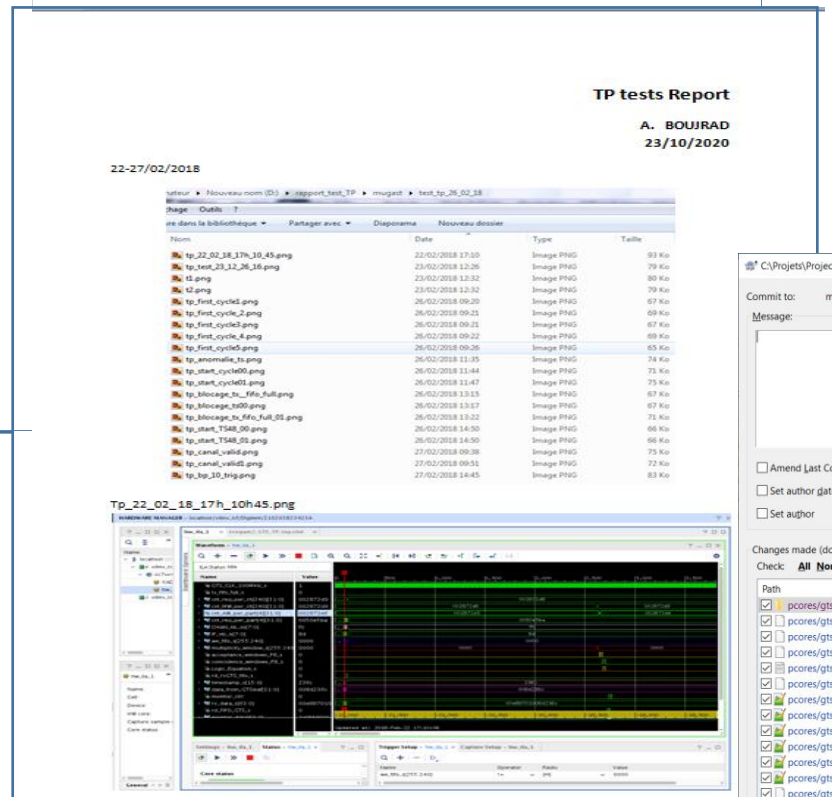
http://wiki.ganil.fr/cgap/GAMMA/attachment/wiki/EXOGAM2/Projet/TP/STP-439A%20-%20SP%20Exogam%20Trigger%20Processor.pdf

I-Présentation de la carte TP

Le TP est base sur le kit d'évaluation Xilinx VC707 (**Figure 1**). Le manuel d'utilisateur de la VC707 se trouve à l'adresse :

https://www.xilinx.com/support/documentation/boards_and_kits/vc707/ug885_VC707_Eval_Bd.pdf

Figure 1 Photo et Block Diagramme du Kit d'évaluation VC707

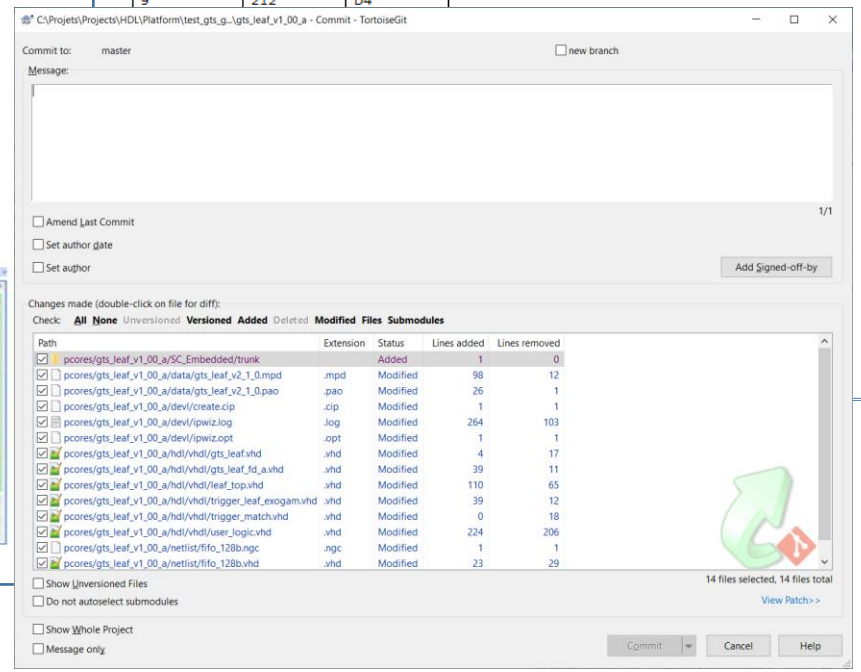


TP tests Report

A. BOUJRAD
23/10/2020

22-27/02/2018

Tp_22_02_18_17h_10h45.png



Tests TP du 1/12/2020

A. BOUJRAD

Tests effectués dans le laboratoire Electronique (Abderrahman et Chiheb).
Puis tests sur AGATA (Emmanuel, Abderrahman et Chiheb).

A/ Test en Labo

avec le module Numexo2-106 _IP=206) et PC ganp879.

Les canaux sont les suivants :

Channel	IP (Décimal)	IP (Hexa)
0	221	DD
1	220	DC
2	219	DB
3	218	DA
4	217	D9
5	216	D8
6	215	D7
7	214	D6
8	213	D5
9	212	D4

C:\Projets\Projects\HDL\Platform\test_gts_g..\gts_leaf_v1_00_a - Commit - TortoiseGit

Commit to: master — new branch

Message:

Amend Last Commit
Set author date
Set author — Add Signed-off-by

Changes made (double-click on file for diff):

Check: All None Unversioned Versioned Added Deleted Modified Files Submodules

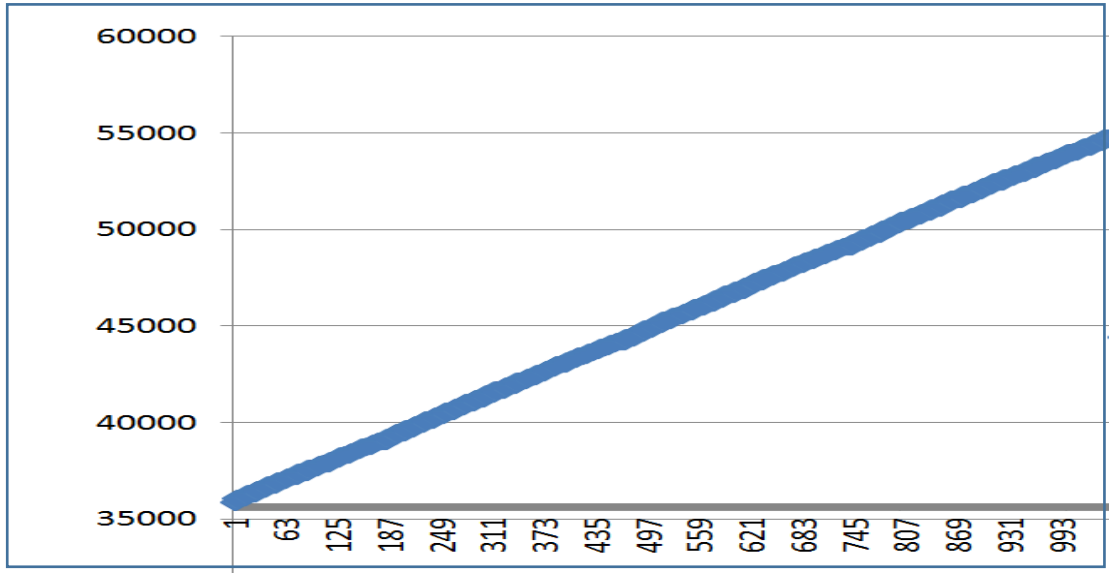
Path	Extension	Status	Lines added	Lines removed
pcores/gts_leaf_v1_00_a/SC_Embedded/trunk		Added	1	0
pcores/gts_leaf_v1_00_a/data/gts_leaf_v2_1_0.mpd	.mpd	Modified	98	12
pcores/gts_leaf_v1_00_a/data/gts_leaf_v2_1_0.pao	.pao	Modified	26	1
pcores/gts_leaf_v1_00_a/devl/create.cip	.cip	Modified	1	1
pcores/gts_leaf_v1_00_a/devl/ipwiz.log	.log	Modified	264	103
pcores/gts_leaf_v1_00_a/devl/ipwiz.opt	.opt	Modified	1	1
pcores/gts_leaf_v1_00_a/hdl/vhdl/gts_leaf.vhd	.vhd	Modified	4	17
pcores/gts_leaf_v1_00_a/hdl/vhdl/gts_leaf_fd_a.vhd	.vhd	Modified	39	11
pcores/gts_leaf_v1_00_a/hdl/vhdl/leaf_top.vhd	.vhd	Modified	110	65
pcores/gts_leaf_v1_00_a/hdl/vhdl/trigger_leaf_exogam.vhd	.vhd	Modified	39	12
pcores/gts_leaf_v1_00_a/hdl/vhdl/trigger_match.vhd	.vhd	Modified	0	18
pcores/gts_leaf_v1_00_a/hdl/vhdl/user_logic.vhd	.vhd	Modified	224	206
pcores/gts_leaf_v1_00_a/netlist/fifo_128b.ngc	.ngc	Modified	1	1
pcores/gts_leaf_v1_00_a/netlist/fifo_128b.vhd	.vhd	Modified	23	29

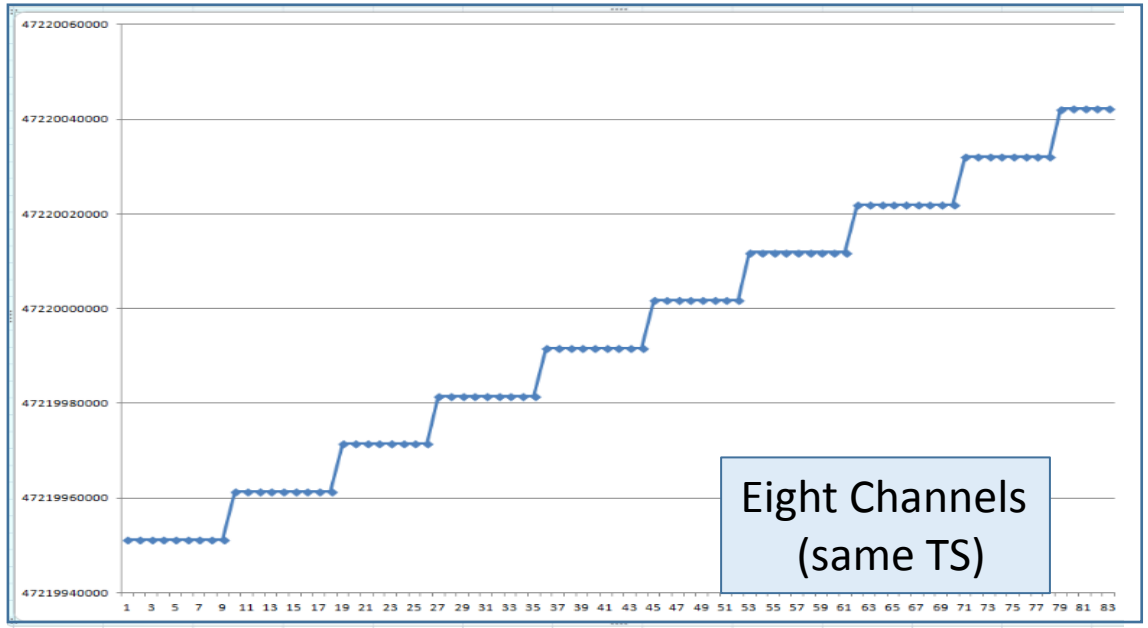
14 files selected, 14 files total

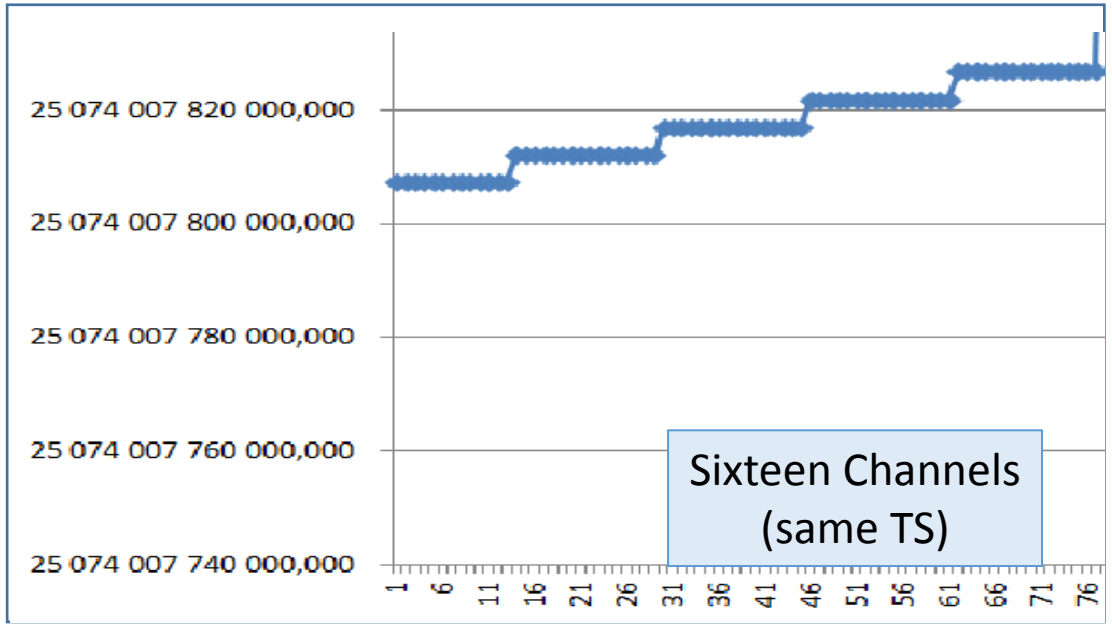
Show Unversioned Files — View Patch>>
Do not autoselect submodules
Show Whole Project
Message only

Commit | Cancel | Help

Time Stamp verification example
Tests in Lab







Example of tests on AGATA
December 2020

	ATCA	GGP	Accept	Reject	Equation
1	1 channel in P1		100%		
2	2 channels in P1		100%		
3	19 channels in P1		100%		
4		1 channel in P1	100%		
5		2 channels in P1	100%		
6		20 channels in P1	100%		
7	19 channels in P1	20 channels in P2		0.2 % (GGP)	P1 OR P2

8 **2 adjacent ATCA** Cristals (Compton event) associated to **P1** (multiplicity **> 2)** :
Result : 10 to 20% of coincidence as expected

9 **2 GGP** with Synchro Pulser associated to **P1** (muliplicity **> 2)** :
Result : 2% of rejection (to be explained)

For tests **8 & 9** if multiplicity threshold is set to 3 a 0% validation is obtained as expected

TP development ressources

- Trigger Processor IP developments
  - *Chiheb Belkhiria*
  - *Abderrahman Boujrad*

- Python *(Slow control, Statistics…)*
  - *Laurent Charles*
  - *Sébastien Coudert*
  - *Chiheb Belkhiria*

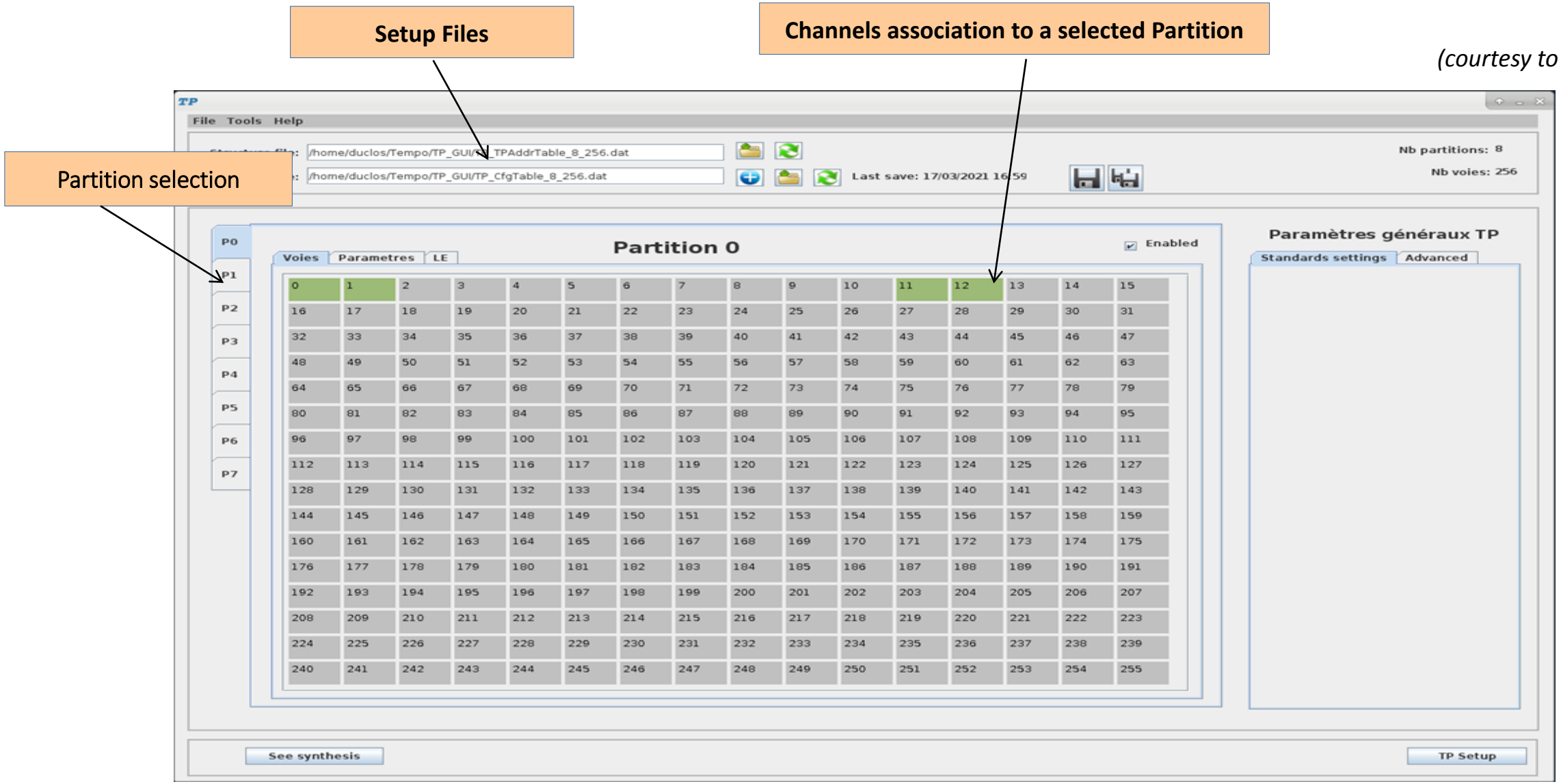
- IPBUS
  - *Laurent Charles*
  - *Chiheb Belkhiria*

- GUI
  - *Blandine Duclos*

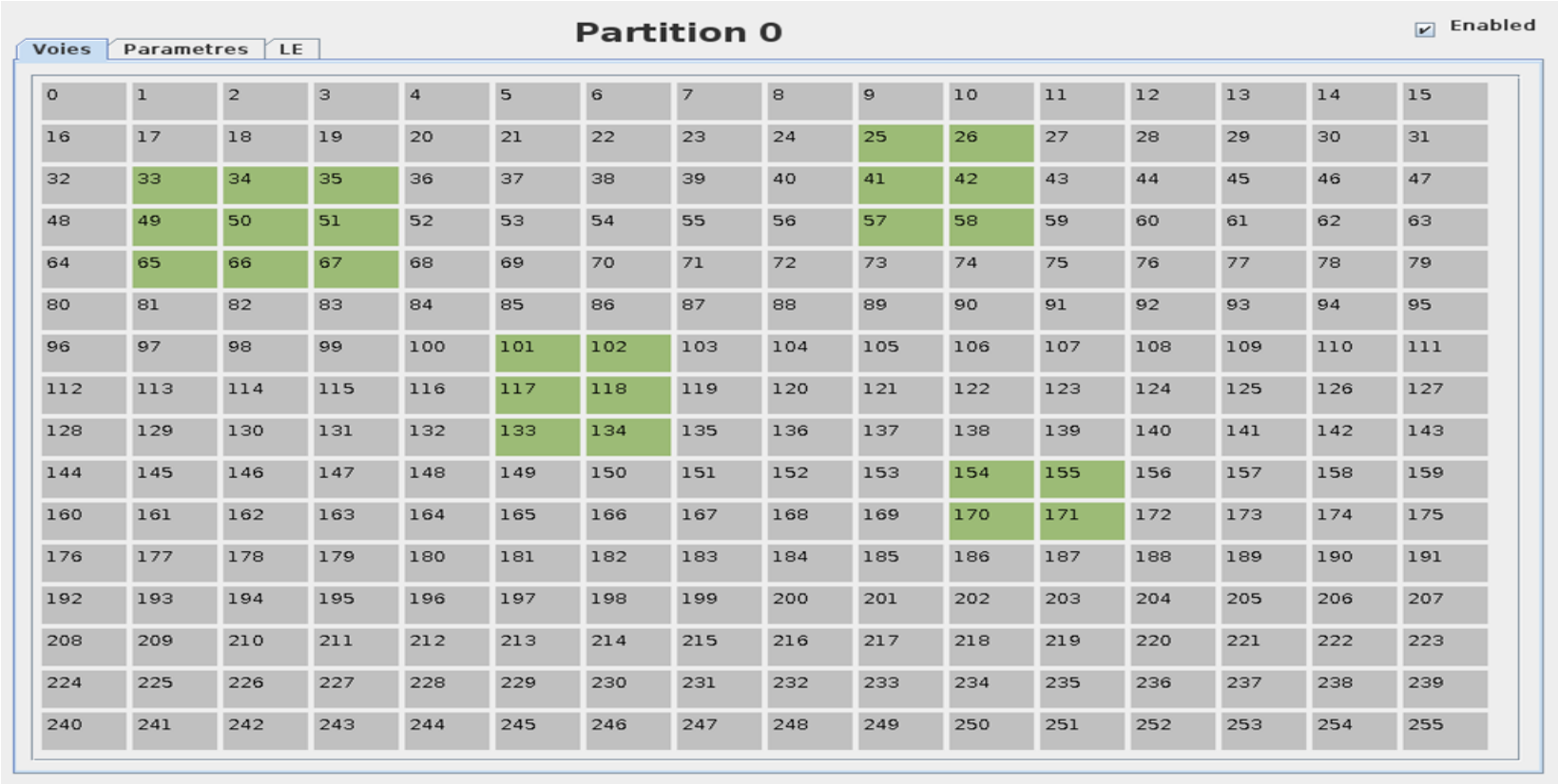
- TP tests
  - *Abderrahman Boujrad*
  - *Emmanuel Clement*
  - *Chiheb Belkhiria*

Trigger Processor
Graphical User Interface

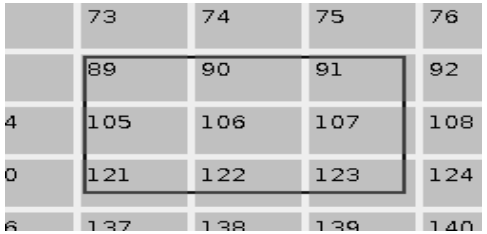
(courtesy to B. Duclos)



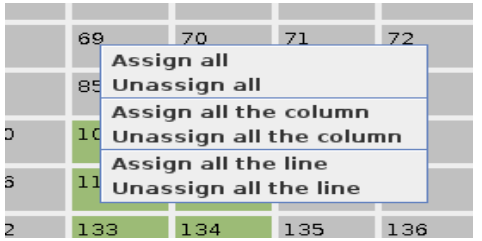
Channels assignment to a partition

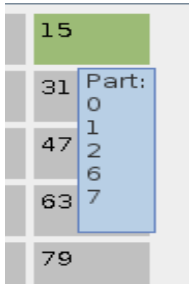


- By shape selection (in green) :

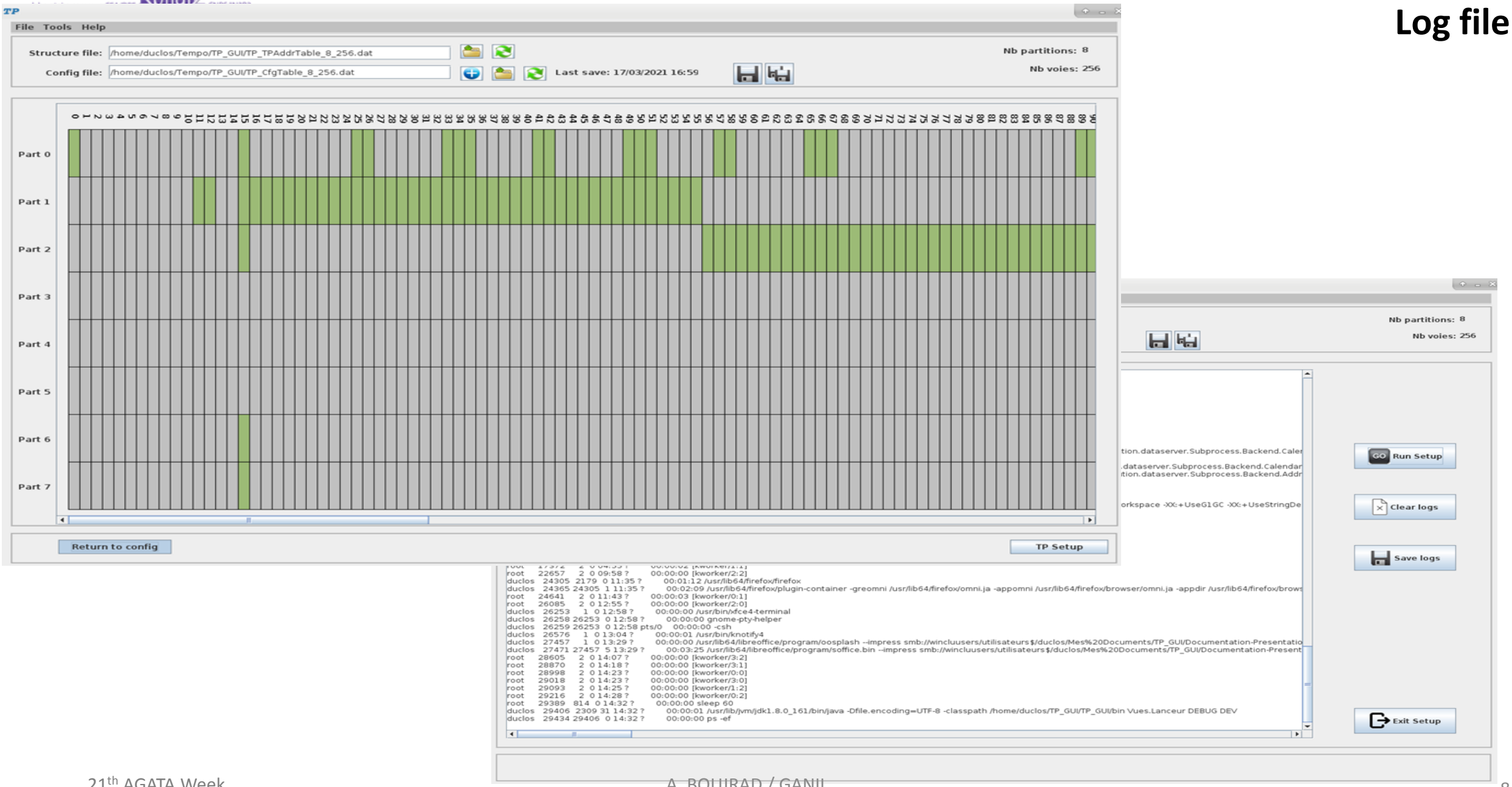


- By using the context Menu :

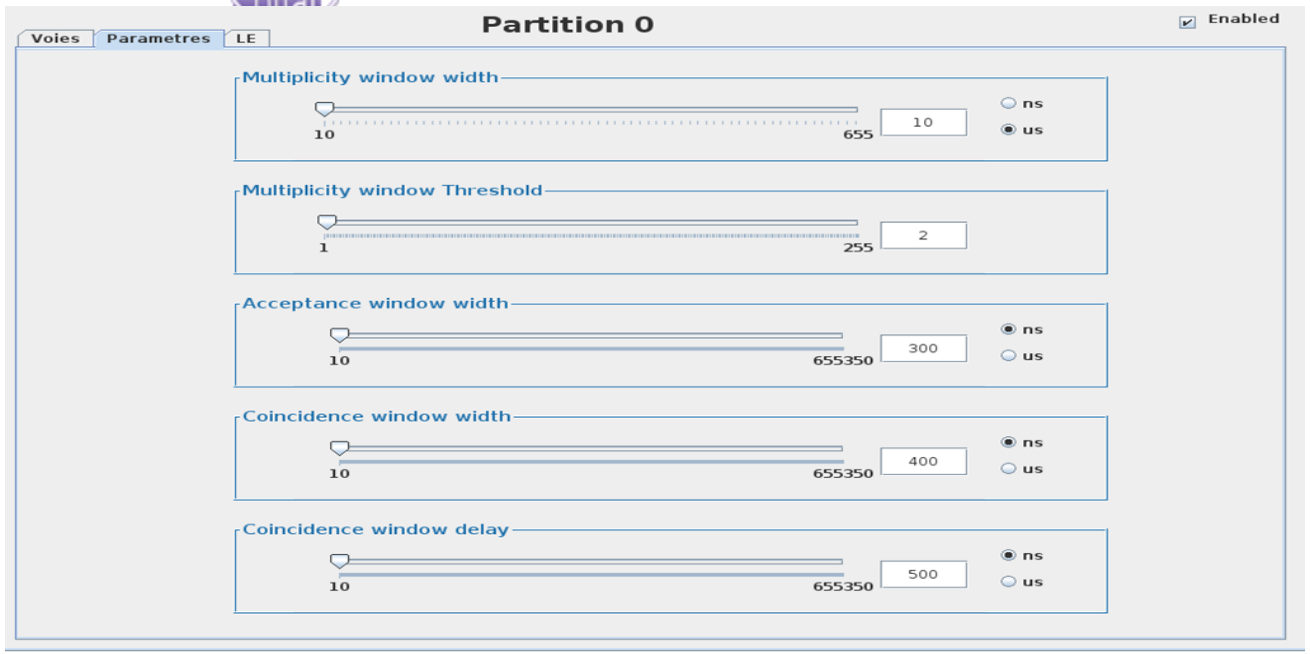


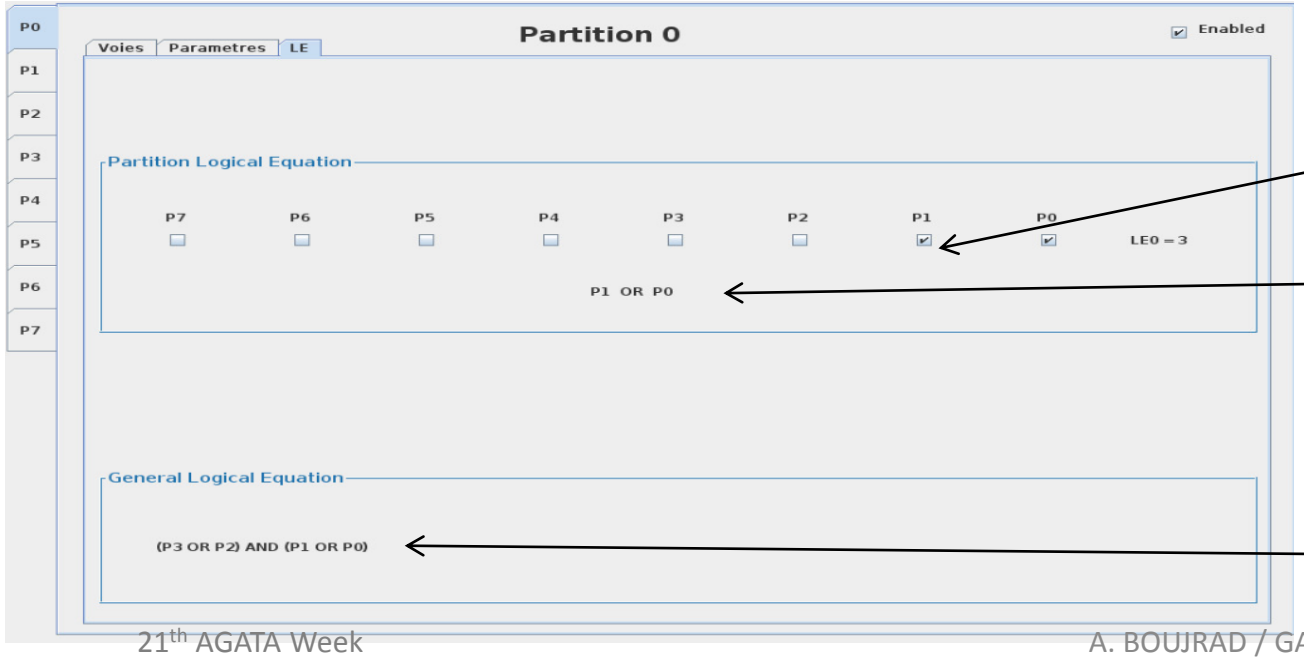


A Global view
Log file



TP setup





TP Windows

- Multiplicity window width
- Multiplicity window threshold
- Acceptance window
- Coincidence window width
- Coincidence window delay

Logic equation

- Partition selection
- LE Formula
- Logic equation expression

TO DO

- **Continuation of the TP tests With AGATA system's**
  - High counting rate on April 2021
  - AGATA/NUMEXO2 coupling

- **Tests and validation of The GUI**
  - In the next weeks
- **Document finalization**