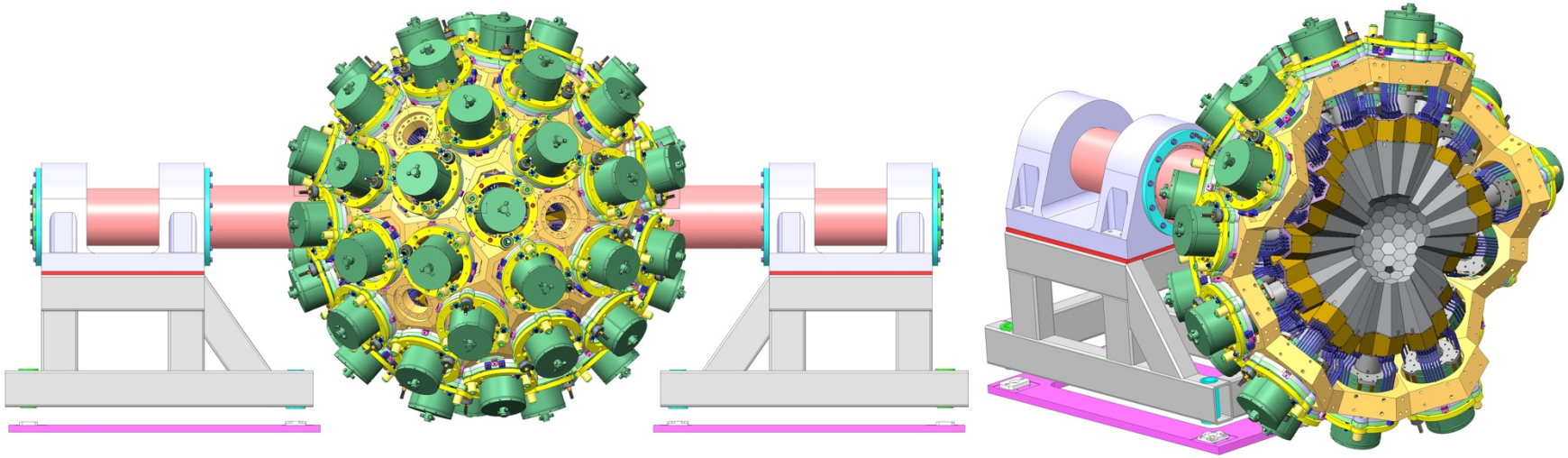
Introduction to the Electronics AGATA Week Session: towards 2π

Andres Gadea (IFIC-CSIC, Spain)
on behalf the AGATA Electronics Working Group



21st AGATA Week, February-March, 2021

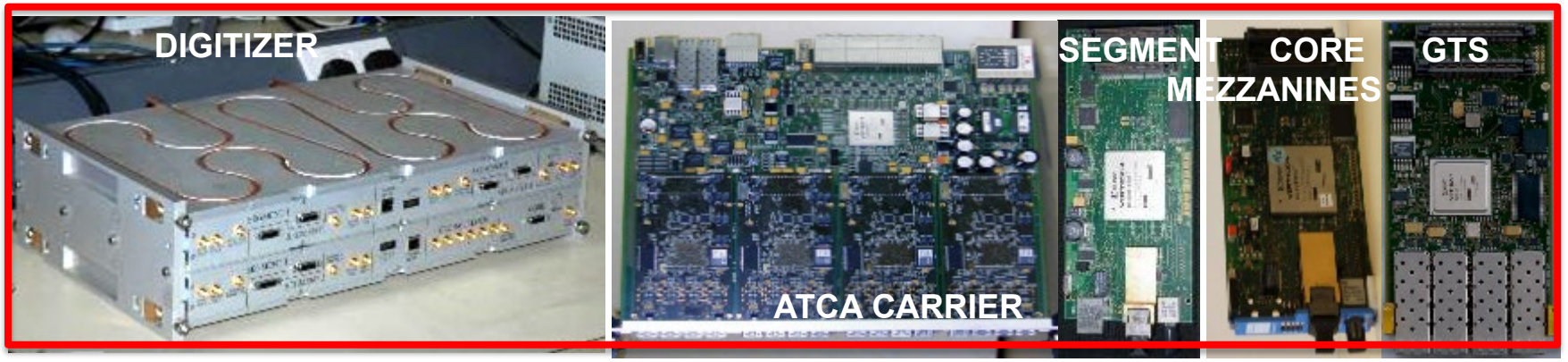
IFIC INSTITUT DE FÍSICA CORPUSCULAR

CSIC CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

AGATA ADVANCED GAMMA TRACKING ARRAY

AGATA Electronics Phase 0

Designed: 2005-2007
Last Produced: 2011



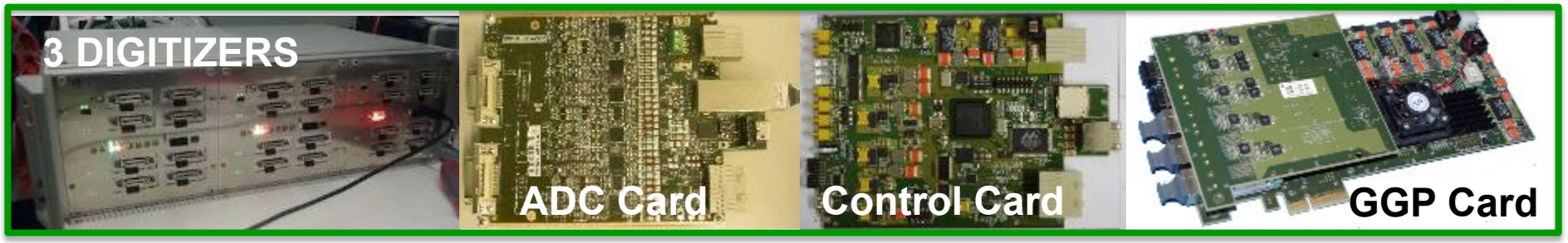
19 channels available and working (initially 25)

- Transceiver Synchronization issues: 9 Core DIGITIZER cards.
- Severe issues with obsolescence, maintenance expensive.
- The PCIe interface LINCO2 requires obsolete servers with obsolete O.S. No solution for update found.
- High Power consumption prevents it use at the beginning of the LNL campaign

AGATA Electronics Phase 1

Designed: 2010-2013

Last produced: 2017/2018

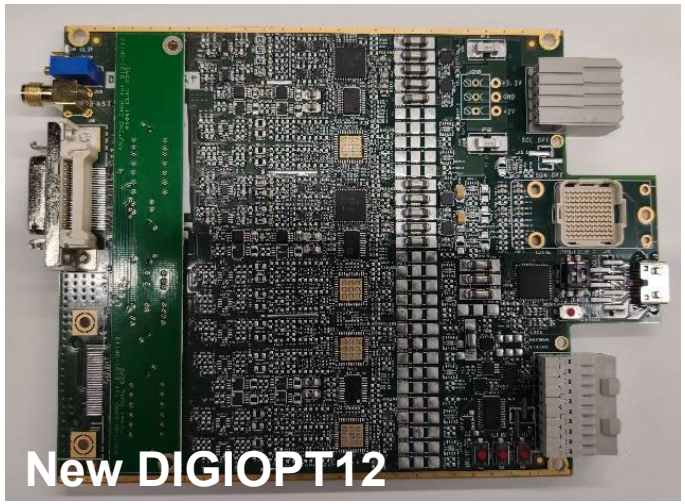


19 Channels working + 3 to be installed (total procured of 28)

- 1st production batch (14) only 9 GGP (4 GALILEO) & 13 Digitizers available
- 2nd production batch (14) 13 GGP and 14 Digitizers (3 GGP with issues)
- GGP Motherboard production for maintenance (11) 3 GGP sent to GANIL.
- Issues with the obsolescence of the Transceivers: QSFP (used in two boards) had to be bought from 2nd hand providers.
- Still uses 4 long MPO-MPO fibres per capsule, while reduced compared with the Phase 0 electronics (7).
- GGP PCIe pre-processing board sits inside the processing server, not every server supports the board.

INFN-Milano INFN-Padova INFN-LNL IFIC-Valencia ETSE-Uni-Valencia

AGATA Electronics Phase 2



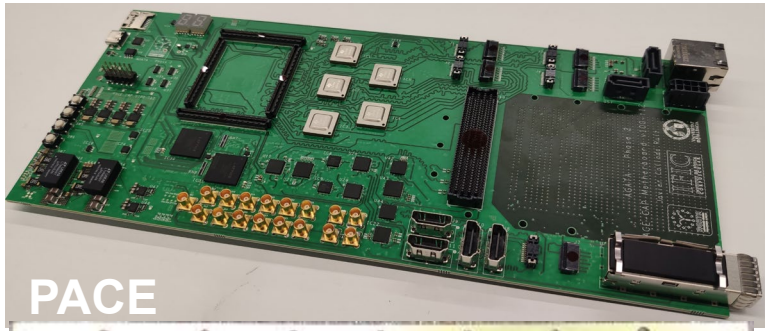
Digitizer Board Upgraded for Phase 2

- New analogue signal conditioning: lower noise larger bandwidth
- Dealing with DNL using Sliding Scale corrections
- Copper connection to the neighbouring pre-processing board
- 33 Segment and 11 Core boards already delivered

Designed by INFN-Milano. Produced by EOS S.r.l.

Pre-Processing Board for Phase 2

- Data pre-processing and Ethernet boards designed with SoM commercial Mezzanines
- ADC input using the time-multiplexing concept
- Ethernet: read-out, monitoring & control
- Hardware being validated
- Firmware under development (mostly completed)

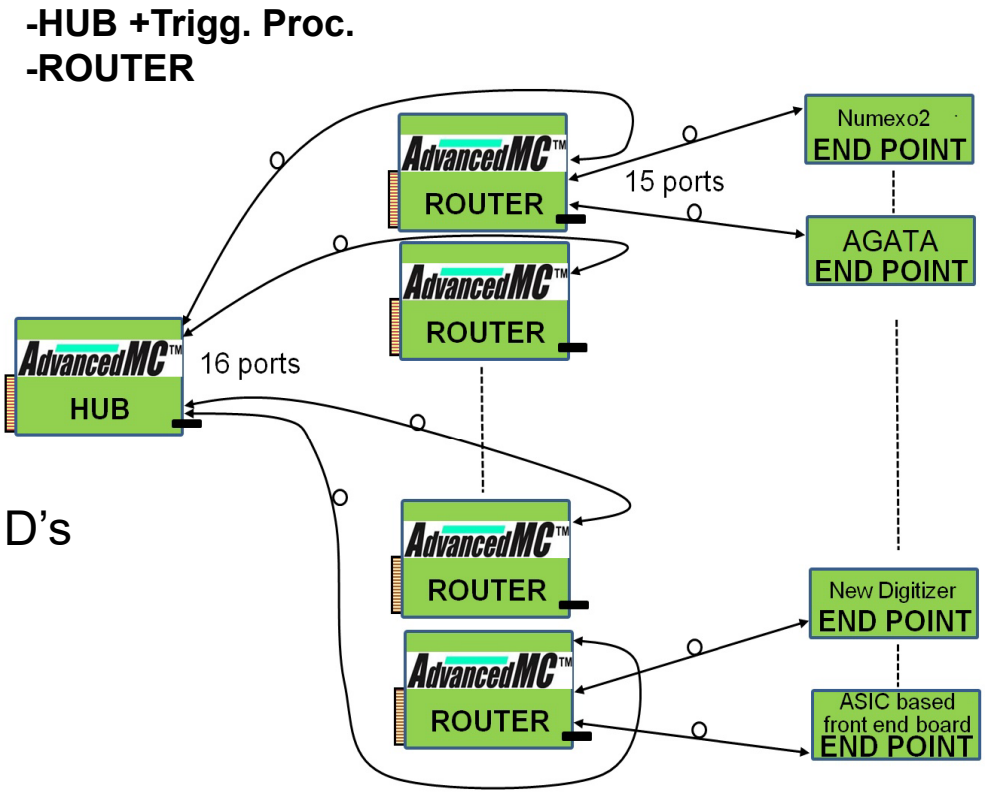


Ethernet board & Firmware: IJCLab-Orsay
Pre-processing board IFIC & ETSE-Valencia
Pre-processing Firmware: IPHC-Strasbourg, STFC-Daresbury
Monitoring, Read-out & Control: IPHC-Strasbourg, IJCLab-Orsay, STFC-Daresbury

Global Trigger & Synchronization: SMART

To be implemented in 2024

- AGATA GTS system broadly used
- New (hardware compatible) SMART system designed by GANIL (G. Wittwer et al.)
- Increased number of Trigger Request ID's
- Adapted to AGATA + Complementary Instruments.
- Trigger Processor with larger logic equation capabilities and flexibility in the trigger partitions
- First prototypes produced



Responsibility of GANIL GAP
See Contributions of G.Wittwer for SMART and A.Boujrad for the new Trigger Processor

Programme

- 09:00 Electronics Introduction
  Andres Gadea (IFIC, Spain) , Ian Lazarus (STFC, UK)
- 09:05 Phase 2 electronics : introduction, mecanics and PS
  Vicente Gonzalez (IFIC, Spain)
- 09:20 Status of the new DIGIOPT12 production
  Alberto Pullia (INFN Milan, Italy)
- 09:25 Status of the PACE Hardware
  Javier Collado (IFIC, Italy)
- 09:40 Status of the STARE Hardware and Firmware
  Nabil Karkour (IJCLab Orsay, France)
- 09:55 Report on the status of the SMART development
  Gilles Wittwer (Ganil, France)
- 10:10 Report on the status of the GANIL Trigger Processor
  Abderrahman Boujrad (GANIL, France)
- 10:25 Discussion on present and future Firmware
  Chairperson: Ian Lazarus (STFC, UK)

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