DICE project status report
-Développement pixels pour les taux de comptage et niveau de radiation extrêmes-

2nd FCC France Workshop – January 20-21 2021

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CPPM, Aix-Marseille Université, CNRS / IN2P3, France

DICE project lead by: M. Barbero (CPPM), Jérôme Baudot (IPHC)

Plan of talk

- Introduction: The DICE project
- Historical implications
- WP “Hybrid Pixels”
- WP “Depleted CMOS”
- Timeline of project
- Development and scope of project
- Conclusion

The DICE project

- Joint project carried by CPPM and IPHC labs.
- General theme: "Pixel detectors for tracking and vertexing developed in the relevant technologies for future projects in which the hit rate and the radiation hardness are critical parameters"
- Structure:

  2 Work Packages:

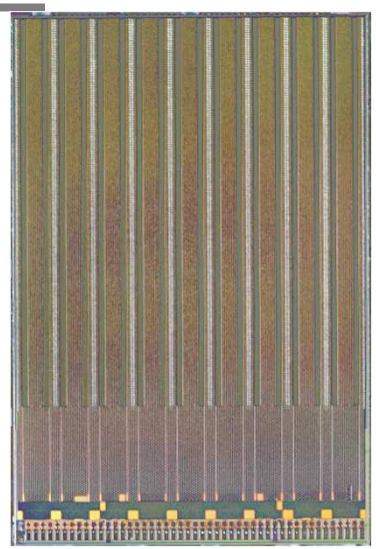
  - **Hybrid pixels** (Resp. Sci. M. Barbero CPPM/ Resp. Tech. M. Menouni CPPM)
    - Techno exploration at advanced process node -e.g. 28 nm-
  - **Monolithic pixels** (Resp. Sci. J. Baudot IPHC/ Resp. Tech. P. Pangaud CPPM)
    - Depleted MAPS technology exploration in two main directions: exploitation of already developed achievements and study of new technologies
- Start date: January 2021 / 3 year planning

- In this talk: Previous implications and link to DICE + scope and planning for the project

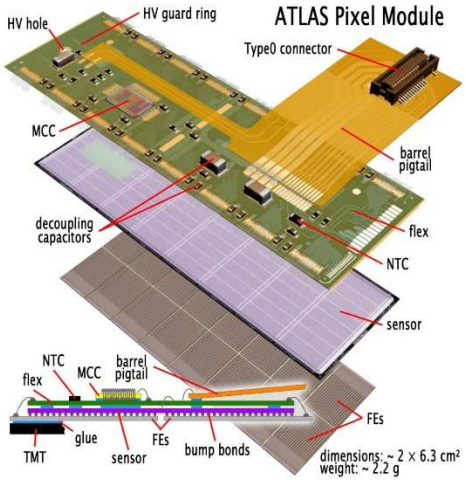
WP Hybrid Pixels

Hybrid pixels at CPPM

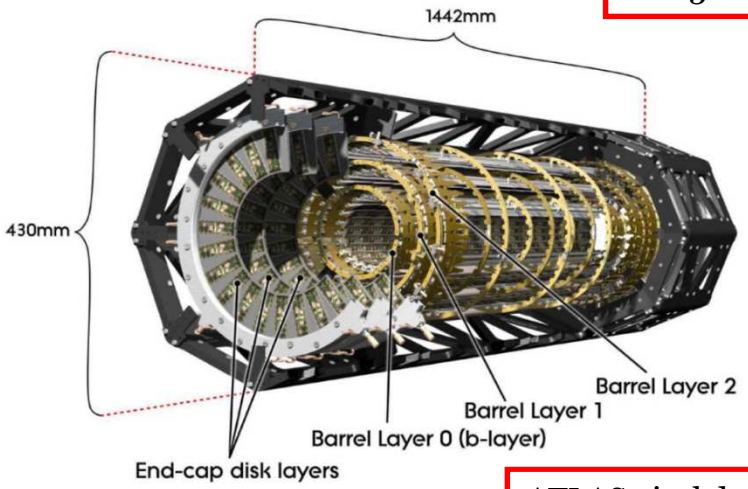
- **CPPM: Historical player on the ATLAS project**.
  - Part of the collab. for FE-I3 hybrid pixel IC for the original 3-layer pixel detector (IBM ¼ µm techno.).



FE-I3 chip - IBM ¼ µm



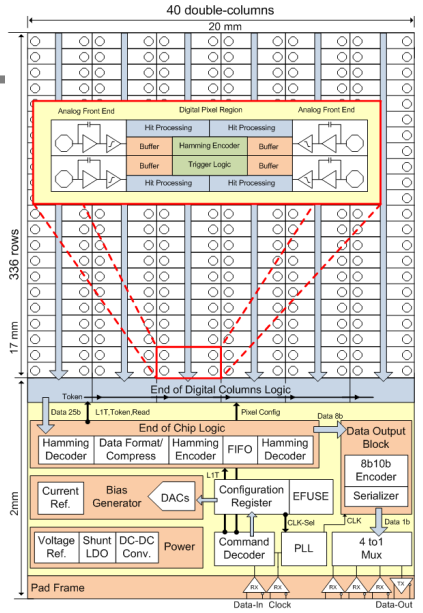
ATLAS pixel module



ATLAS pixel detector (<2014)

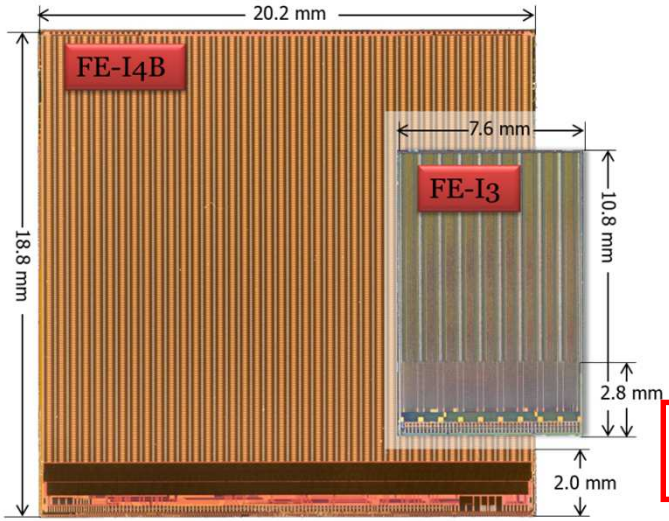
Hybrid pixels at CPPM

- **CPPM: Historical player on the ATLAS project**.
  - Part of the collab. for FE-I3 hybrid pixel IC for the original 3-layer pixel detector (IBM ¼ µm techno.).
  - Part of the collab. for FE-I4 for the ATLAS Insertable B-Layer IBL Upgrade (IBM 130nm techno.).



FE-I4 architecture - IBM 130nm

IBL insertion -2014-



FE-I4 / FE-I3 to scale

Hybrid pixels at CPPM

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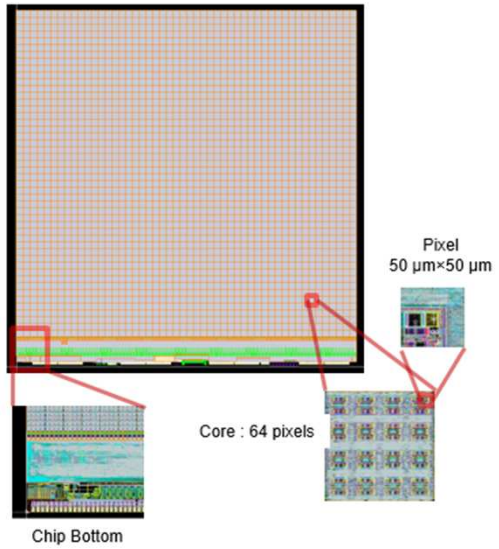
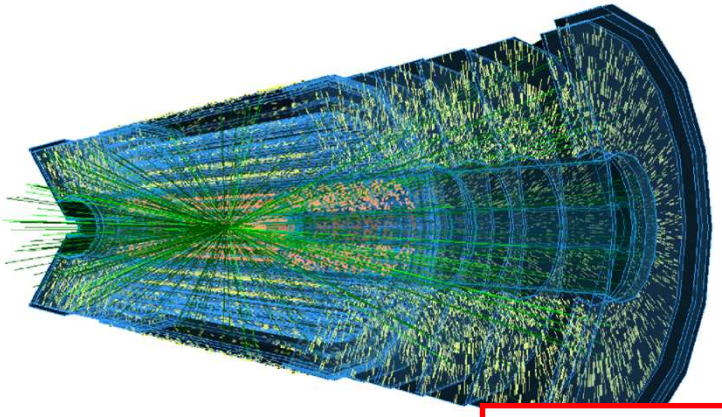
  - Part of the collab. for FE-I4 for the ATLAS Insertable B-Layer IBL Upgrade (IBM 130nm techno.).
  - Part of the joint CERN ATLAS-CMS RD53 collab. to develop ATLAS (ITkPixV1) et CMS (CROC) ICs (TSMC 65nm techno.).



RD53 IC organization

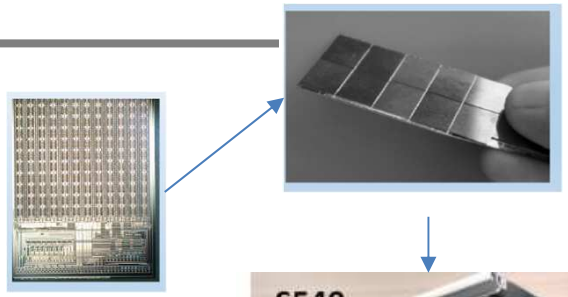
RD53 : ITkPixV1



ATLAS ITk (installation 2026)

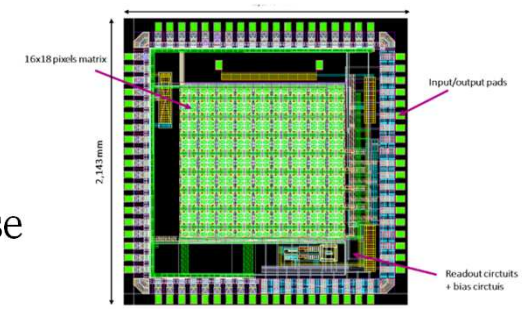
e.g. current non-HEP

- XPAD project:
  - Readout Chip for hybrid pixel detectors based on photon counting
    - IBM 0.25 µm process
    - 130µm × 130µm pixel size
  - Used for X-ray detection applications
  - Creation of the ImXPAD Start-up
  - A new CPPM-Industry collaboration is currently on the way
    - Development of the pixel readout circuits expected for the future generation of these detectors.



Active area 12 x 7.5 cm²
537 600 pixels

- DEMON project:
  - Hybrid Pixels for plasma diagnostics in the Tokamak Tore Supra at CEA-Cadarache
    - Design compliant with high flux and low noise
    - TSMC 0.13 µm process
    - 70 µm × 70 µm pixel size



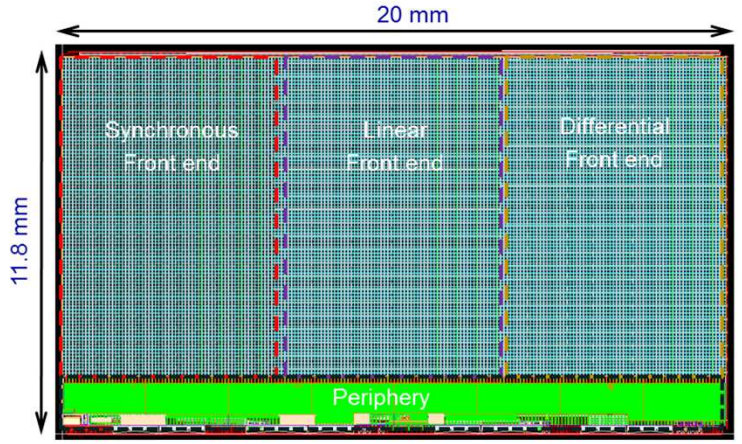
DEMON chip prototype

Plans for 28nm DICE

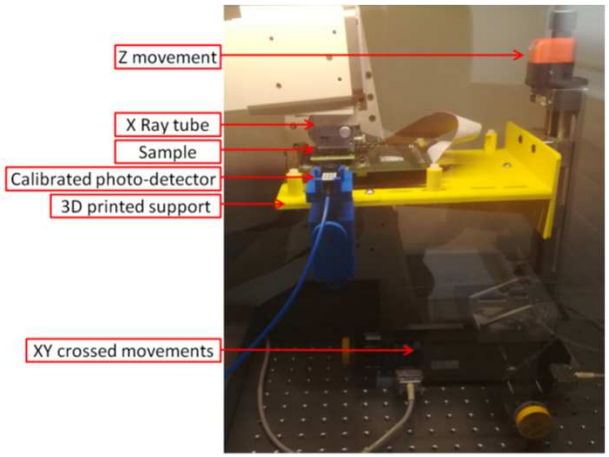
- **Challenges for tracking in future colliders:**
  - Pixel size / integration density, radiation tolerance, spatial resolution, time resolution, power consumption → Need more advanced process than what HEP currently uses (state of the art 65 nm RD53)
  - Process node: 28 nm node is foreseen for the design of these circuits
    - But challenging designs because of process complexity (reduced gain, low power voltage…).
- **Goal of DICE:**
  - 3 years:
    - Qualify the 28 nm CMOS process
    - Develop a first small pixel array (64×64 pixels of 25µm × 25µm)
  - Timeline of developments:
  - **June 2021** : first DICE-supported 28 nm run scheduled
    - TID and SEU tolerance testing
    - Design of basic analog blocks
  - **Mid-2022** : Submission of small pixel array
  - **Mid-2023** : Hybridization
- **Link to community: 28nm part of CERN Strategic R&D roadmap** (see 28nm forum kickoff meeting Nov. 12th 2020: https://indico.cern.ch/event/970389/)

Themes for 28nm DICE

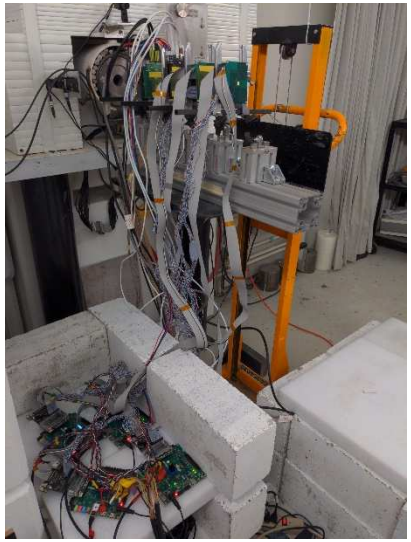
- Analog design.
- Design for high radiation level.
  - TID
  - SEU
- Characterization of technology
  - In the lab
  - Under irradiation
  - Against SEE



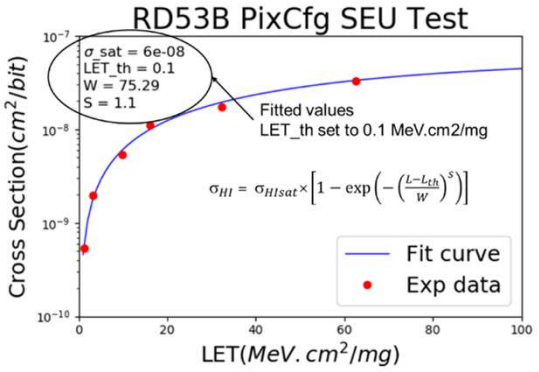
RD53A Front-End



AMU-based LDR TID effect test setup



Dec 2020 SEU tests at TRIUMF

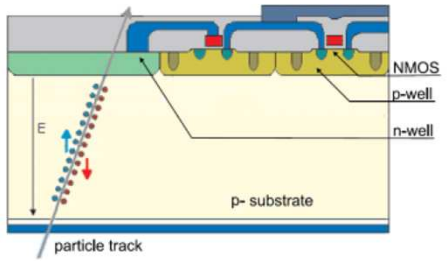


SEU Xsection vs. LET

WP Monolithic DepCMOS

Monolithic depleted CMOS

- In some context, could provide advantageous alternative to hybrid pixels or be the best monolithic option.



Depleted active monolithic CMOS Pixels

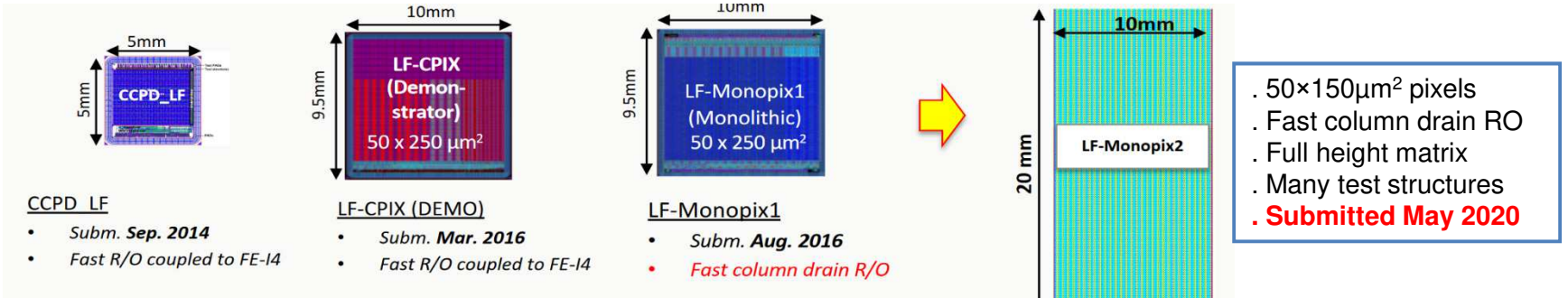
- Key ingredients:
  - Charges collected by drift.
    - to go above ~ 10^{13} $n_{eq}.cm^{-2}$, collecting charge by diffusion is problematic → drift (hence standard MAPS → Depleted MAPS).
  - Consequence → Fast signal response & radiation hardness.
  - Technology requirements → High Voltage process (apply 10s-200 V), High Resistive wafers (>100Ωcm) and multiple nested wells (for full CMOS & shield)

(depleted layer: $d \sim \sqrt{\rho . V}$)

- Advantages:
  - Usage of commercial process: production capability, reliability, low cost…
  - Simple less expensive module (wrt hybrid): no hybridization and much easier production! Can be used for larger area applications
  - Small pixel size possible (in some process, e.g. TJ)
  - Less power, less material…

DMAPS developments

- DMAPS Monopix dvp based on original specs for ATLAS ITk outer pixel layer: NIEL >10^{15} $n_{eq}.cm^{-2}$, TID >80 Mrad, 25ns bx, Hit Rate >100 $MHz.cm^{-2}$
- Higher radiation hardness & faster readout need:
  - → Cope with NIEL / trapping:
    - Fast collection by drift
  - → Have high time resolution:
    - Fast collection by drift
    - Fast analog FE
    - Time stamping on chip
  - → Cope with high TID:
    - Process + design methodology
  - → Cope with high hit rate:
    - Fast return to baseline in analog FE (<~ 1 µs, avoids pile-up)
    - High logic density
    - High output bandwidth



LF 150nm development line / LF-Monopix2 latest prototype submitted to date

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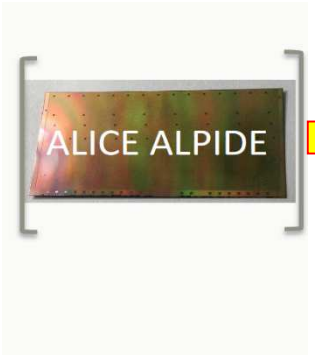

Mimosis development (TJ180) -talk A. Besson juste before-

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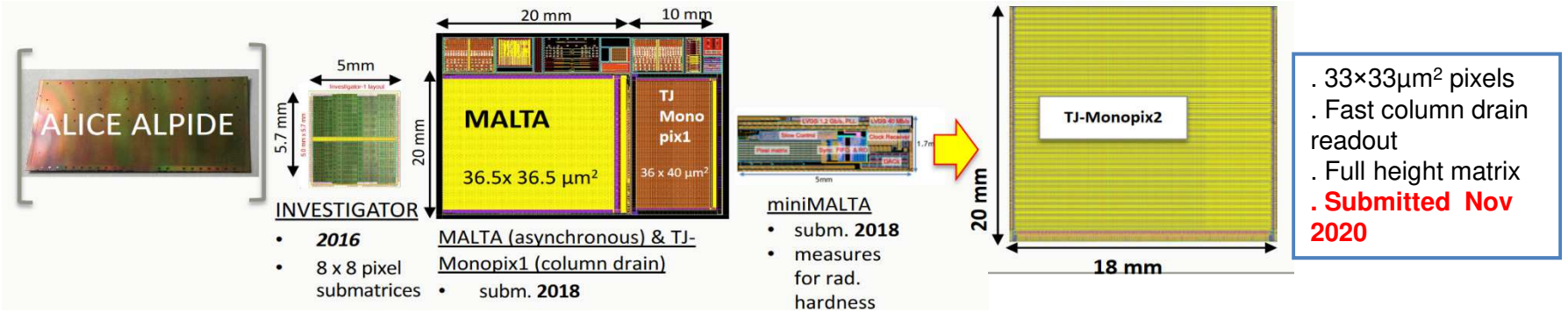
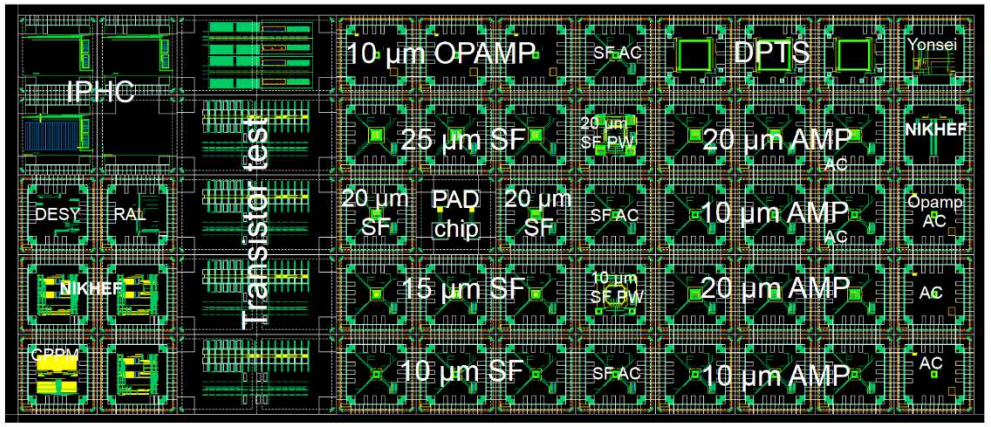


TJ 180nm development line / TJ-Monopix2 latest prototype submitted to date

TJ65

- Dec 2020: 1st CERN-lead MLR in TJ65 nm techno. circuit went for fabrication.
- FR: Implication of the CPPM (ring oscillators) and of the IPHC (rolling shutter large matrices).



- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.

MLR1 submission Dec. 2020

- This is a **run test of the TJ65nm technology**:
  - Participation of CERN, IPHC, DESY, RAL, NIKHEF, CPPM, Yonsei)
  - Analog structure designs (matrices, LVDS/CML rec./driv., amplifiers, bandgap…
  - Test devices for characterization of technology (collection diodes, transistor test structures, ring-oscill.)

- Common interest of CPPM-IPHC-IP2I towards this technology.

DICE plans for DepMAPS

- **Challenges for tracking in future colliders:**
  - Monolithic integration allows large area application (cost reduction, ease of production, system level simplifications…), yet high voltage and depletion allows charge collection by drift, rather good radiation tolerance and high hit rate → DepMAPS
  - Process node: DICE supports implications on LF150, TJ180 and TJ65
    - LF150 / TJ180 well established / TJ65 more prospective…
- **Goal of DICE:**
  - 3 years:
    - Build on work done on LF150/TJ180 for short term application (Belle VXD)
    - Qualify TJ65nm for future applications. If issues, identify other technology of interest
  - Timeline of developments:
  - **2021** : characterization of available large prototypes (LF150 / TJ180) and TJ65

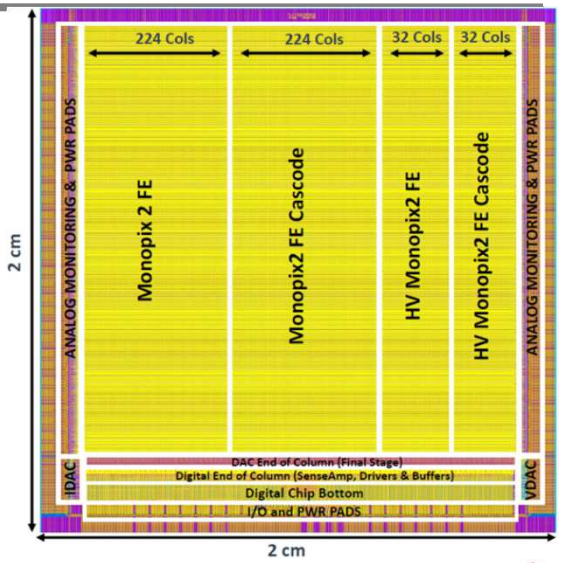
    1- LF-Monopix2 & TJ-Monopix2 (+ test structures) → support designs in LF150/TJ180

    2- TJ65 MLR1 characterization (among which TID / NIEL)→ design MLR2
  - **2022** : 1- TJ180/LF150 → Link to Belle VXD effort / other applications.

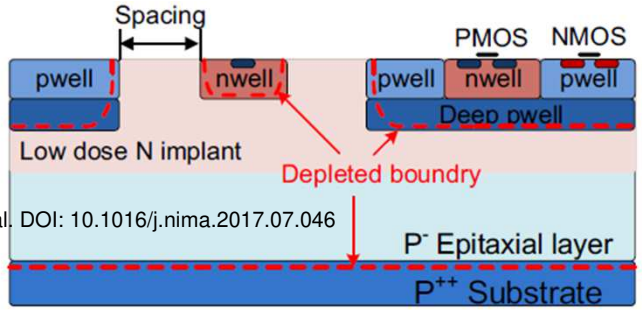
    2- TJ65 → Validation of technology / Submission of more complex structures
  - **Mid-2023** : Validation of TJ65 techno for future applications
- **Link to community: CERN R&D roadmap (focus on TJ180 and TJ65), RD50 (LF), CERN, U-Bonn, CEA-IRFU, Belle II VXD community, …**

Themes for DepMAPS DICE

- Design for high radiation level (TID / SEU) and high rate.
- Design complex large application specific large IC (Belle VXD upgrade? → 1st full-CMOS tracker on e+e- collider!).
- Characterization of TJ65 technology for future application
  - In the lab
  - Under irradiation
  - Against SEE

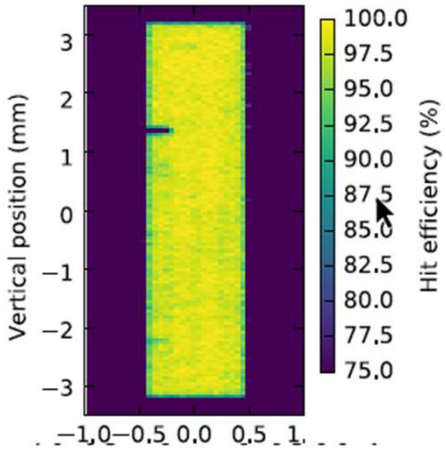


TJ-Monopix2 Subm. Nov. 2020

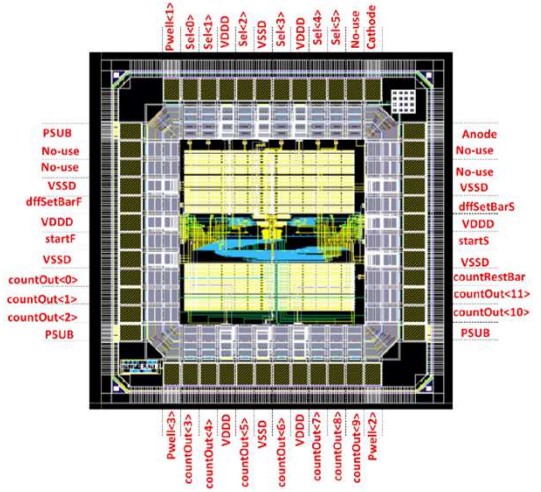


W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046

Process modification TJ180



Measured LF150 efficiency at 10^{15} n.cm^{-2} ~98.9%



RingO test structures TJ 65 – Dec 2020

Conclusion

- **DICE supports**:
  - Pixel developments for high radiation and high hit rate environment
  - Needs of experiments at future hadron colliders (post-ITk ATLAS, FCC-hh…)
  - Needs of Belle VXD upgrade at e+e- collider for very high luminosity
  - Allows to keep specific expertise present in the IN2P3 community
  - Allows to keep an active prospective towards future projects

- DICE (high radiation and high hit rate pixels) contrasts with the main specifications of heavy ion and FCC-ee sensors (very small pixel and low power), and is in this sense complementary to the CMOS R&D project presented just before.

A. Besson, same session

- There is an expertise and a synergy between efforts in the IN2P3 community on which to build towards applications to future pixel projects.

- Our partners in related efforts: RD53, RD50, collaboration Bonn / CPPM / CERN / IRFU, KIT Karlsruhe, AIDAinnova…