DICE project status
-Développement pIxels pour les taux de Comptage et niveau de radiation Extrêmes-

3rd FCC-France /Higgs & EW Factory worshop, Annecy
30/11 - 2/12 /2021

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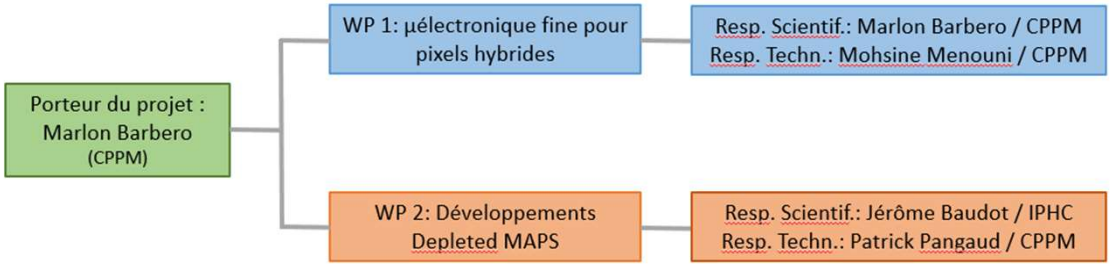
Talk plan

1. Introduction
2. WP1 - Hybrid Pixels (28 nm)
3. WP2 - Depleted MAPS :
   a) TJ65
   b) LF150
   c) TJ180
4. Conclusions

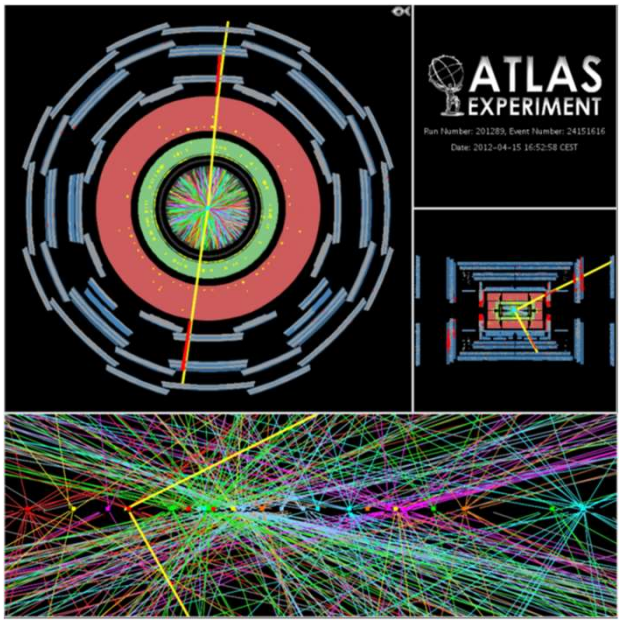
DICE project

- A project involving CPPM and IPHC, carried by M. Barbero / CPPM (+ involvement IPHC -J. Baudot et al-). Start: beginning 2021.
- General theme :
  - Tracking / vertexing with pixel detector in relevant technologies for futures projects with main emphasis on:
    - **High counting rates/ high hit rates**.
    - **Radiation hardness** middle to high.
- 2 Work Packages:
  - **Hybrid Pixels**: Exploring advanced process nodes technologies -e.g. 28 nm- (RS: Barbero / RT: Menouni)
  - **Monolithic Pixels**: Focus on Depleted MAPS technologies Depleted MAPS in two main directions → exploitation of mature R&D and potential of new technologies (RS: Baudot / RT: Pangaud)



WP1: Hybrid Pixels for future trackers

- Next generation pixel readout circuits for inner detectors:
  - Severe radiation levels
  - Unprecedented hit rates
  - Complex trigger management technics
  - High data transfer - several tens Gbit/s -
  - Small pixel size integrating complex digital functions (high integration density)
  - Higher temporal resolution → 4D tracking
  - Low power and small material budget



- 28 nm CMOS process standard:
  - Excellent compromise in terms of integration density vs. TID tolerance
  - Potential candidate to succeed to 65 nm CMOS node used for hybrid pixel development in framework of HL-LHC

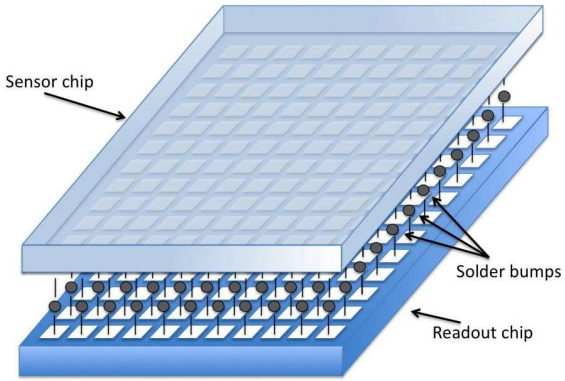
- Higher instantaneous luminosity:
  - Higher pile-up
  - e.g. HL-LHC: ~ 200 pile-up events / bunch-crossing
  - Small pixel size a must / time information would help separating tracks

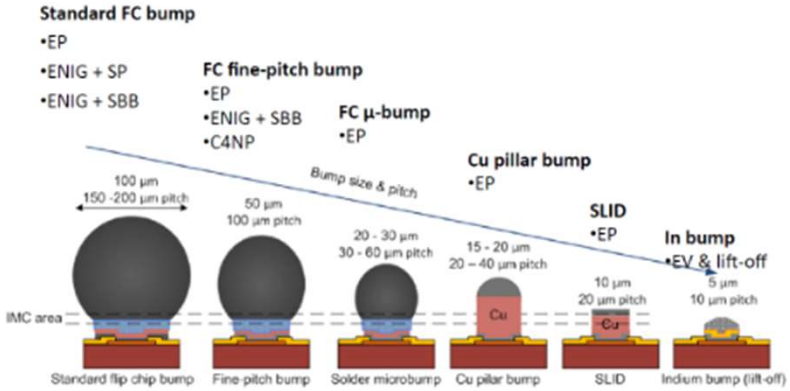
WP1: Short term plans

- **Investigation of 28 nm** process node:
  - Process advocated by CERN
  - "Standard" planar process → TID effect resistant
- Study: Compatibility with analog parts conception (as necessary for pixel circuits):
  - Base circuits simulations
  - Process qualification in terms of performances for analog design, low power and low noise
- TID-resistance process qualification:
  - Compatibility with high TID necessary for futures projects
  - TID effects modelling:
    - Analog and digital simulation taking TID effects
- SEE studies:
  - Prototype circuits to study SEU/SET effects
  - Very small node capacitance:
    - Will it need new architectures for higher tolerance?

WP1: Middle/Long term plans

- Conception of a small 64×64 pixel matrix with 25µm×µm pixels :
  - "Digital on top" approach
    - Mastering digital conception tools a must
    - Prototype analog blocks with high constraints (low noise ampli, precision ADC, PLL, high speed serializer…)
- Prospection work planned on advanced hybridization techniques:
  - Advacam proposes hybridization techniques at 10-20µm level
  - IZM?
  - 3D techniques?
- Ambitious project in terms of manpower and budget:
  - Conception cycles in these process types are longer and need more verifications
  - Needs to be done in **collaborations**
    - Potential interest in other IN2P3 laboratories through DICE
    - First discussions in framework of RDR53



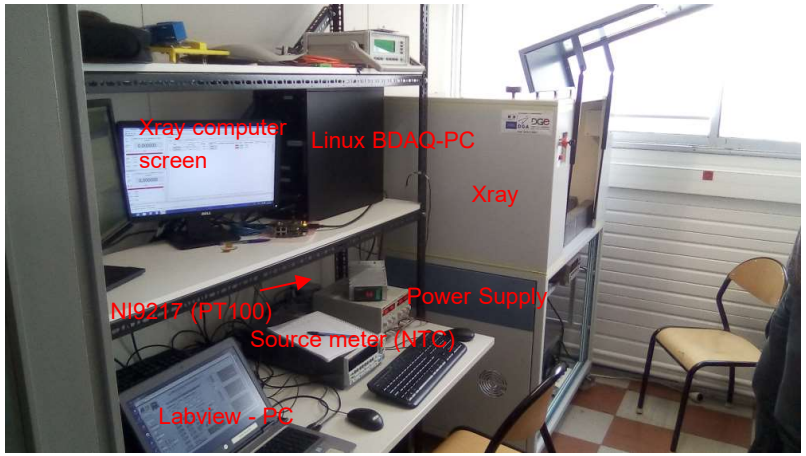


Very high density interconnection techniques (from Vahanen Advacam)

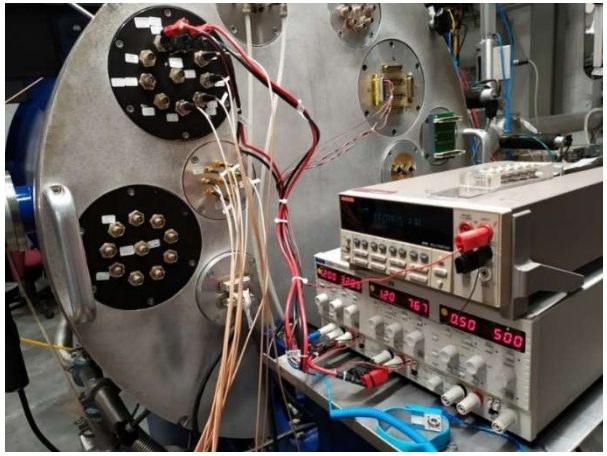
WP1: Perspectives

- In CPPM:
  - Small 3-person team of designers → approx. 1FTE equiv

  → Collaboration needed
- ~ March 2022: Chip prototype submission
  - Single transistors (TID studies)
  - Ring Oscillators (TID testing of digital libraries)
  - SEU test architectures
  - Analog block: Fast amplifier
- Q1/Q2-2022: Test preparation
- Q2/Q3-2022: Functional testing
- Q3-2022: Irradiation tests (TID / SEE)
- End 2022 / Beginning 2023:
  - **Submission of a 25µm² , 64×64 pixels matrix**



TID testing at AMU - Saint Jerome



Heavy ion testing at UCL - Louvain la Neuve

WP2: Pixels depMAPS

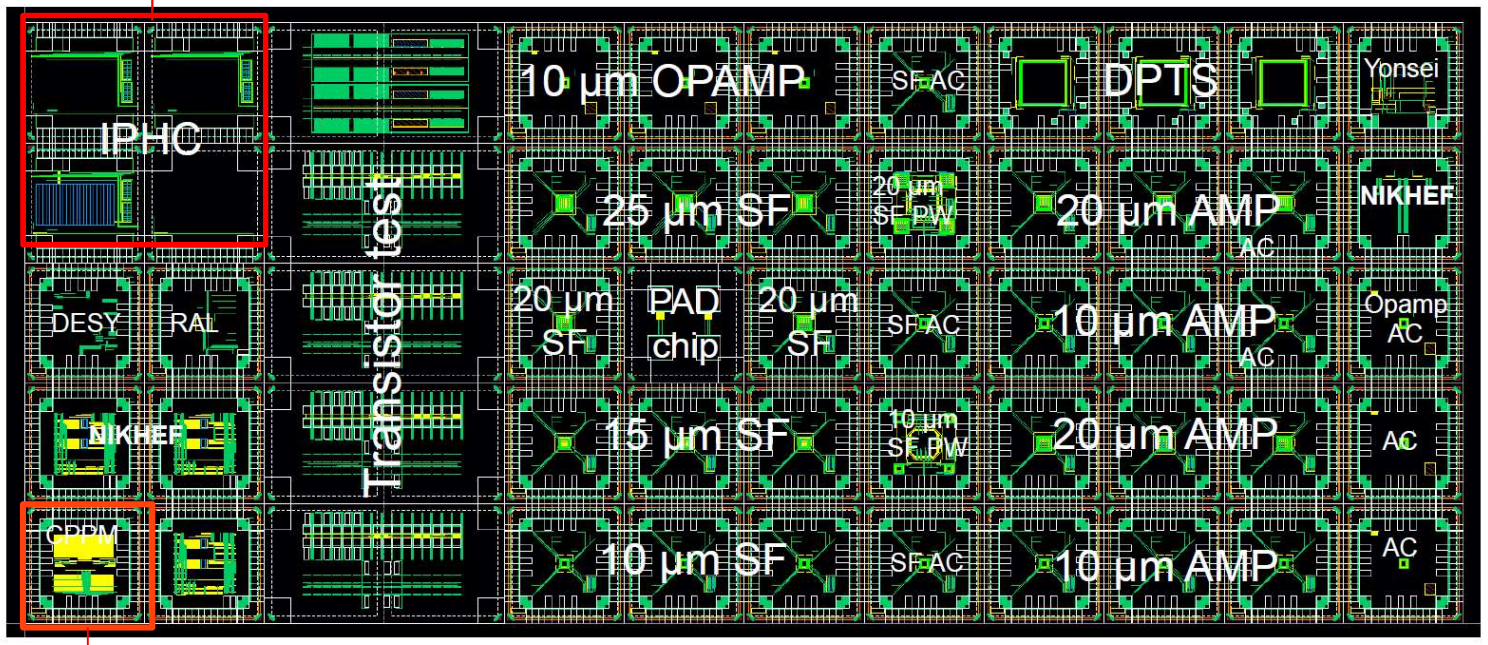
- **<u>Exploiting mature R&D</u>**:
  - Short term
    - Validation of large size prototypes LF-/TJ- Monopix2, work in LF150 and TJ180 technologies
  - Middle term
    - Adapt TJ-Monopix2 the Belle II context: OBELIX-v1 demonstrator

- **<u>New R&D</u>**: Exploring new technology TJ-65 nm
  - Short term
    - Verification of basic performances
    - Check adequacy with DICE objectives
  - Middle term
    - Prototype(s) dedicated to
      - High hit rates (>> 100 MHz/cm^2)
      - Temporal resolution of order 100 ps
      - Coping with NIEL >>10^{15} n_{eq}/cm^2

WP2: TJ65 / MLR1

- MLR1 submitted in Dec 2020 → back summer 2021

IPHC has contributed with analog Front-Ends CE65, conceived to study charge collection in this technology .



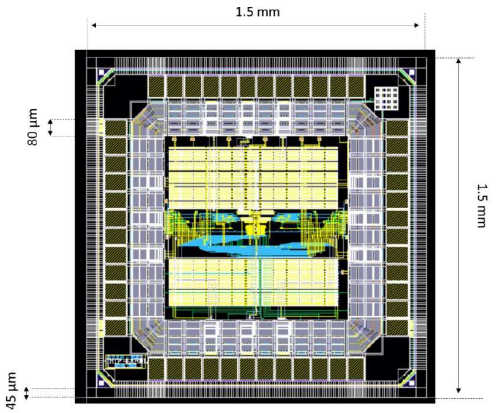
CPPM has contributed with a series of Ring Oscillators, conceived to characterize how the standard cells of the digital library cope with ionizing radiations in this technology .

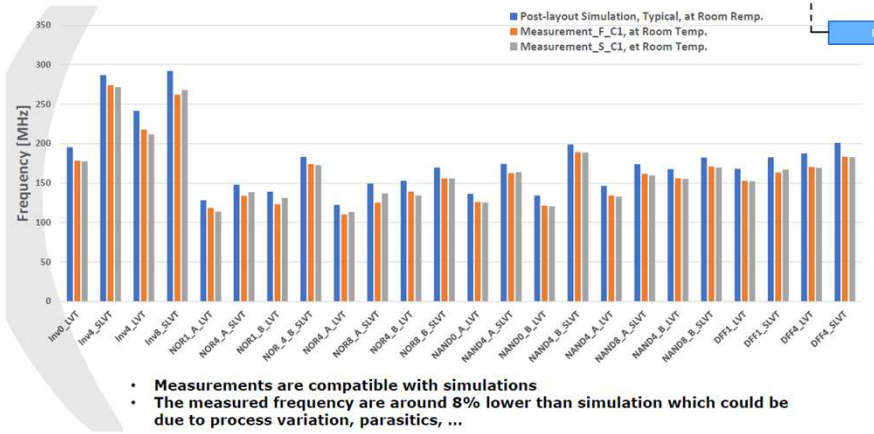
WP2: TJ65 - CPPM / Ring-Oscillator

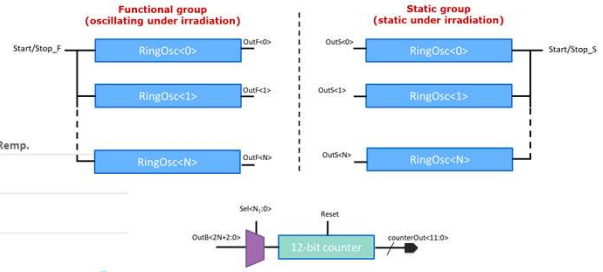
- In short: A prototype test IC containing 24 × 2 ring oscillators, with various cell types (Inv, Nand, Nor, DFF), various sizes and two different V_T (low, super-low).

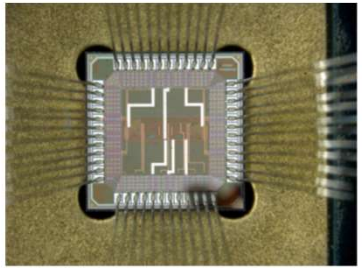
- Oscillation frequency depends on:
  - Temperature
  - Polarization
  - TID and Dose rates
- But other factors observed (in TSMC 65m) that can be tested here too:
  - Dynamic vs. Static cells.
  - Asymmetric cell entries

Low V_T		Super Low V_T	
Size Min	Size+	Size Min	Size+
INV0_LVT	INV4_LVT	INV4_SLVT	INV8_SLVT
NOR1_LVT_A	NOR4_LVT_A	NOR4_SLVT_A	NOR8_SLVT_A
NOR1_LVT_B	NOR4_LVT_B	NOR4_SLVT_B	NOR8_SLVT_B
NAND0_LVT_A	NAND4_LVT_A	NAND4_SLVT_A	NAND4_SLVT_A
NAND0_LVT_B	NAND4_LVT_B	NAND4_SLVT_B	NAND4_SLVT_B
DFF1_LVT	DFF4_LVT	DFF1_SLVT	DFF4_SLVT





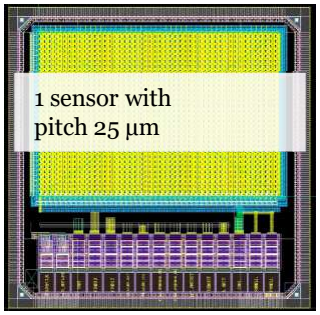


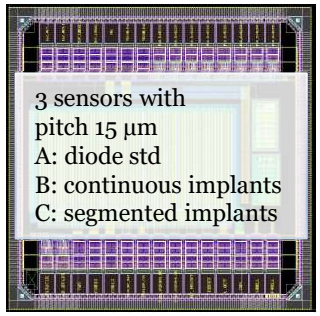


WP2: TJ65 - IPHC / CE65

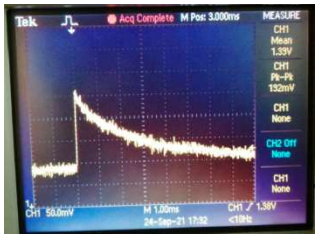
- **CE65 targets**:
  - Understand charge collection properties in TJ65
    - SNR, charge sharing, signal speed
    - Unirradiated and irradiated sensors
  - Common activity with MP R&D CMOS

See A. Besson's talk just before



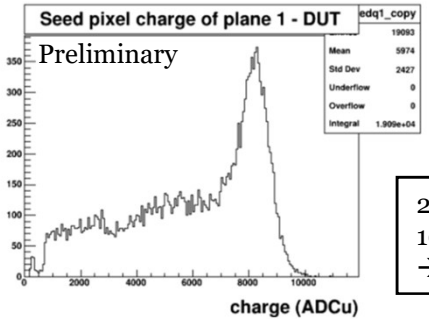


- **4 different CE65 sensors**:
  - Small matrices with analog output: 64/48×32
  - 12 versions each:
    - Front-end: DC ampli, DC follower…
    - Doping profiles: std & 3 modifications (steered by CERN)



1st ^{55}Fe signals

- Next step: Conception starting in 2021 for submission ER1 in Q1-2022:
  - Big sensors to study stitching (ALICE-inspired)
  - In this framework:
    - Work on MOST IC (CERN steered), low power, temporal info preserving.
    - Optimization of pixels with new CE65+ matrices!



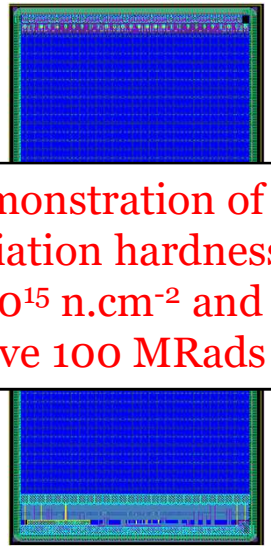
Unirradiated B4 DC Amp

2 B4 splits irradiated to 100 Mrad and 500 Mrad → testing will follow

MP DICE & MP CMOS interests!

WP2: Monopix developments

LF-Monopix2:



Demonstration of radiation hardness to 10^{15} n.cm^{-2} and above 100 MRads

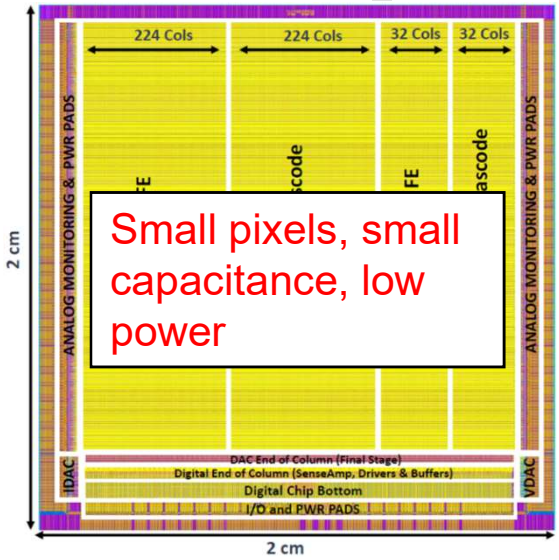
2×1 cm², 340×56 pixels, 50×150 µm²

Analog and digital FE improvements, reduced pixel size, better layout

Submitted in June 2020

→ Back dec. 2020

TJ-Monopix2:



2×2 cm², 512×512 pixels, 33×33 µm²

New implants for better charge collection after irrad., low threshold

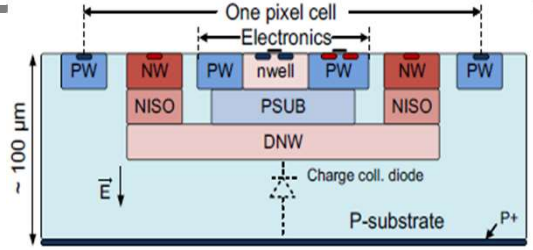
Submitted in October 2020

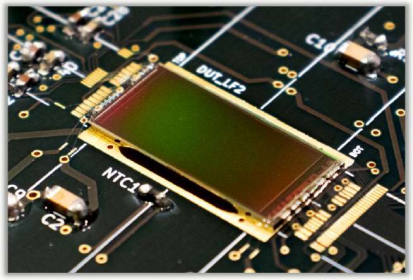
→ Back Feb. 2021

WP2: LFOUNDRY 150nm techno

Circuit **LF-MONOPIX2** (Bonn, CPPM, IRFU)

12 wafers back end 2020





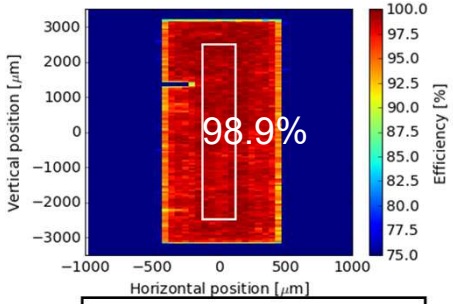
Test bench and firmware developed by Univ Bonn : MIO3 + GPAC card.

Tests realized by Bonn and CPPM (on-going) show a functional IC with results close to specifications

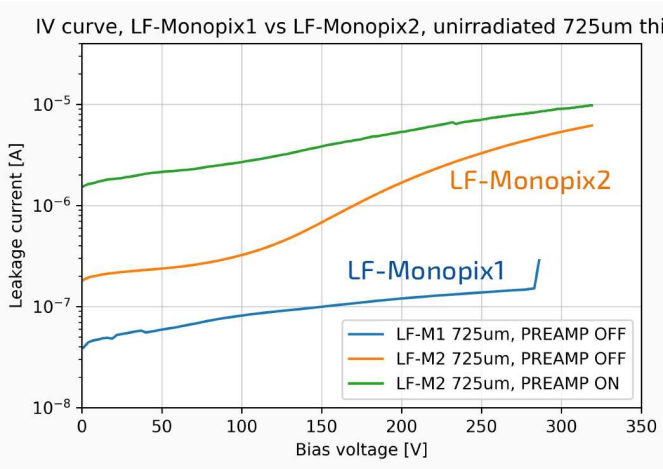
This second LF-MONOPIX version (LF-MONOPIX2) fixes some crosstalk and threshold adjustment problems.

Tests on-going : sensor characterization, threshold ajustments. New irradiation tests will come in 2022

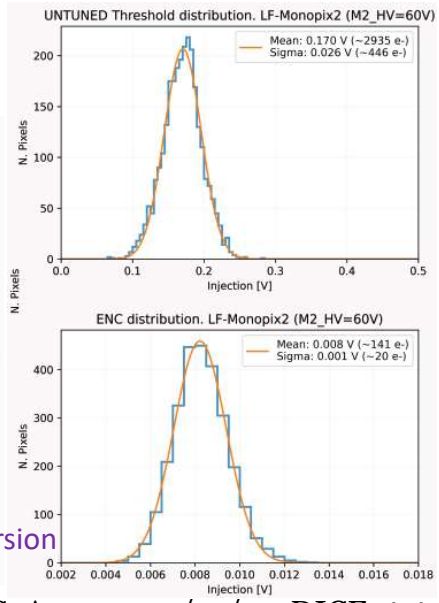
Below: Previous LF-MONOPIX1 results



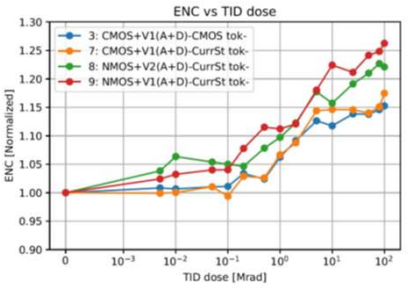
Monopix1: ELSA test beam. Efficiency @ 10^{15} n.cm^{-2} : 98.9%!



Measurements at Room Temperature in a laboratory desk

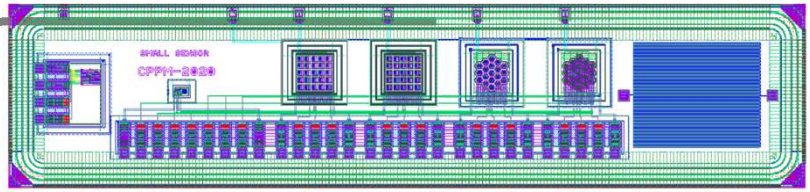


Threshold dispersion for 1 pixel type



Monopix1: ENC vs TID

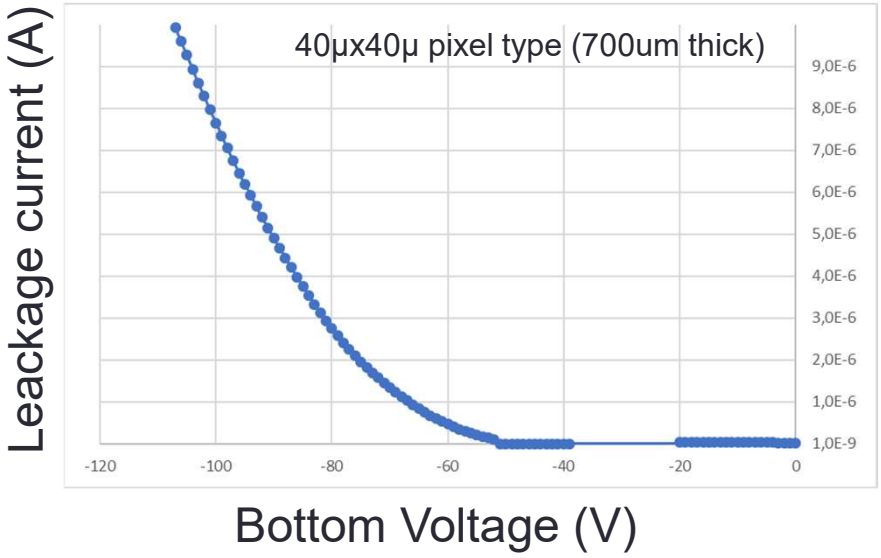
WP2: LF150nm



LF-MONOPIX2 circuit (Bonn, CPPM, IRFU)

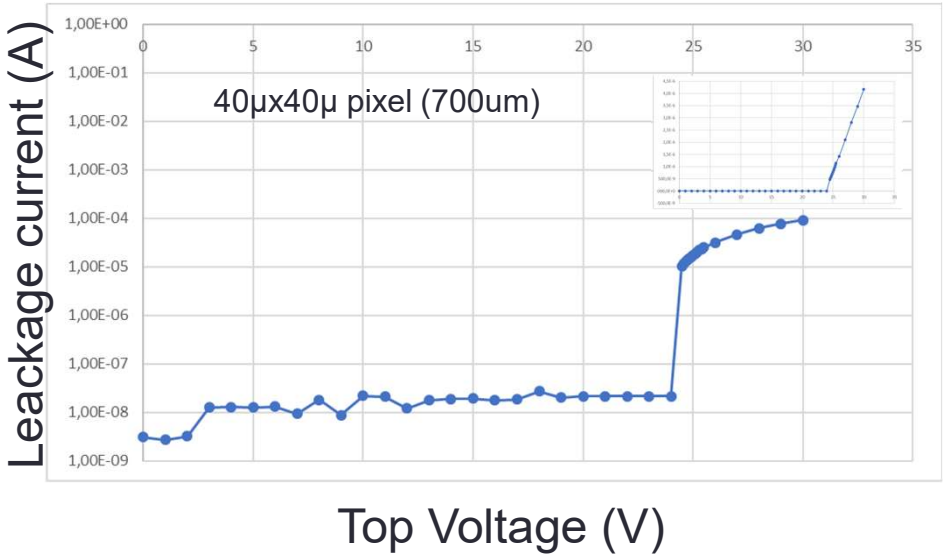
+ Test Structures : Small circuit with various test structures

- Small pixels (50µ × 50µ) : 1st result show that small pixels could be depleted up to ΔV~80V. Tests on-going
- Bandgap conceptual implementation flaw. Submitted again through RD50-MPW3 (Nov 2021 / test in 2022)
- Guard ring circuits 3GR and APD studies: IHEP visitor Zhao Mei : test on going



30nA/4px global leakage current for different diode (DNW) sizes, for a top bias @24 V

BV at 54V (2kohms substrate)



10nA/4px leakage current for different diode (DNW) sizes, for a bottom bias @0 V

BV at 24V (2kohms substrate)

The total Voltage potential (top to bottom) at **78 V** is achieved

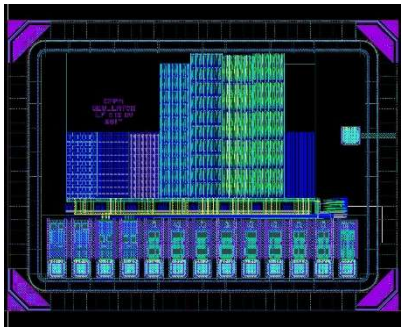
WP2: LF150nm

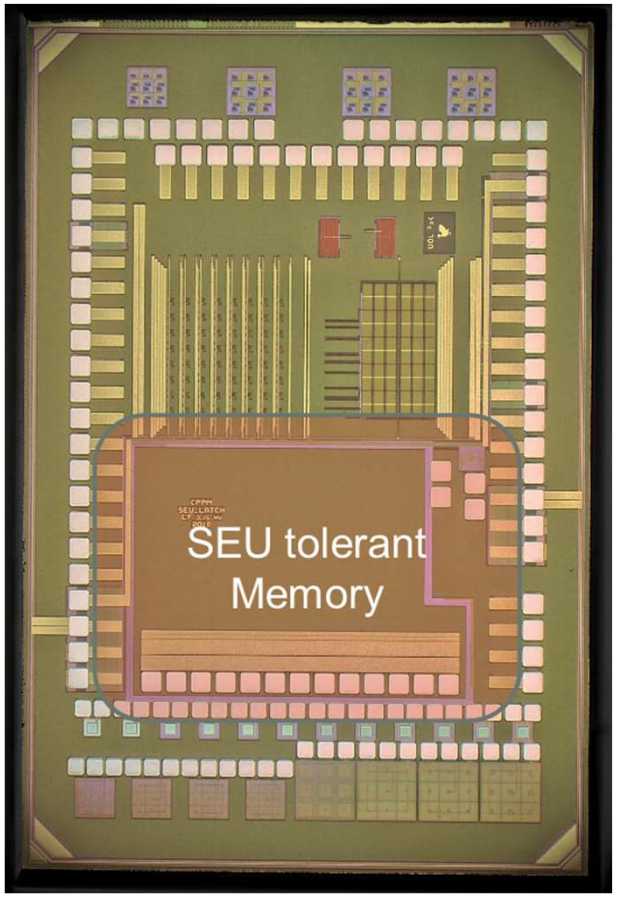
Circuit RD50-MPW2 (RD50 collaboration)

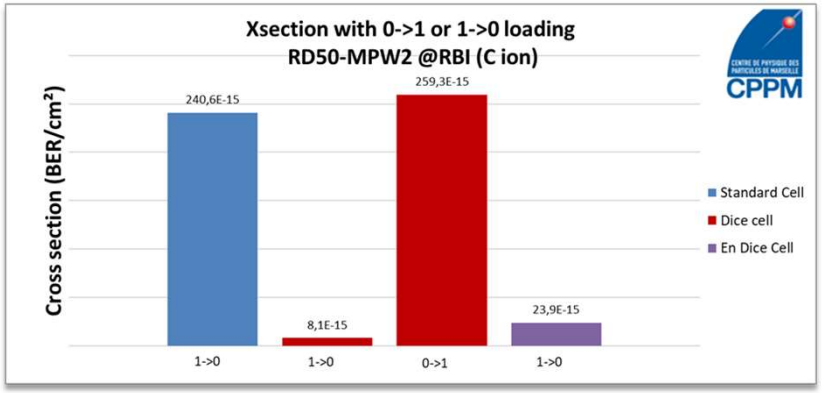
+ SEU hard structures

Recently tested in Ganil (France) and RBI (Croatie) in 2021! First results show that LF is a SEU-hard technology (comparable or better than comparable prototypes in other technologies)

Cellules: SRAM (col8), split TRL + DICE cell (col7), split TRL + standard cell (col6), TRL + DICE cell (col5), TRL + standard cells (col4), enhanced DICE cell (col3), DICE cell (col2), standard cell Col1)







SEU-hardness vs. architecture type (0 to 1 and 1 to 0 transitions)

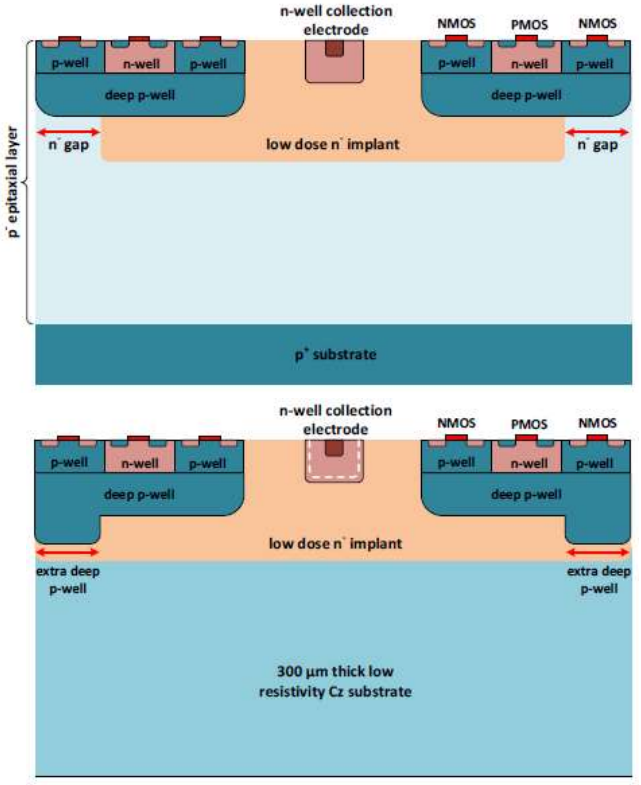
WP2: TOWERJAZZ 180nm CIS technology

TJ-MONOPIX2 circuit (CERN, BONN, CPPM)

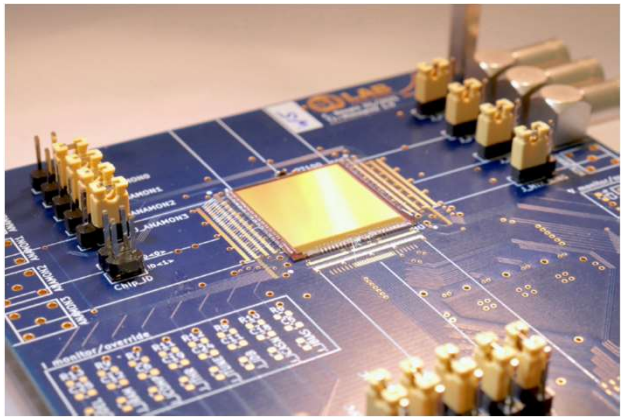
IC developed and submitted in 2020. Back in January 2021.

- 2×2cm² IC with 33 µm×µm pixels
- TJ-Monopix2 features a high rate digital architecture (column drain / trigger / 40MHz clock)
- This 2nd version of the TJ-MONOPIX (TJ-MONOPIX2) should fix some threshold adjustment issues. Test on-going
- Basis for a candidate VTX Belle-II upgrade → OBELIX

Uses a test bench and firmware developed by Univ Bonn : MIO3+GPAC cards or BDAQ.



2021 : started TJ-MONOPIX2 characterization
Test bench still in developments (firmware, software). Few bonding issues.



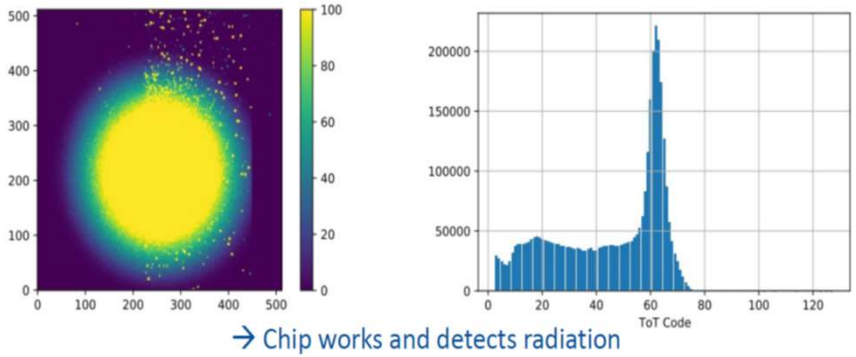
2022:

Development of **OBELIX** prototype from TJ-MONOPIX2. On-going: specification defination / TJ-MONOPIX2 test

A lot still to be done for characterization (in the lab, but also under beam + irradiation)

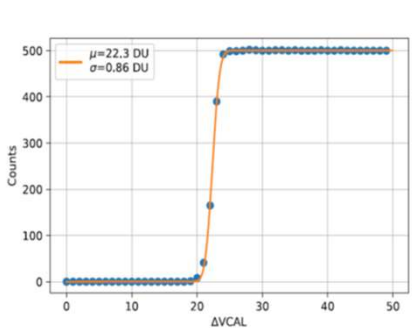
WP2: TJ-Monopix2 recent results

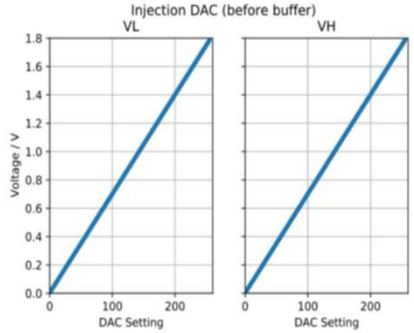
- ^{55}Fe source detection:



→ Chip works and detects radiation

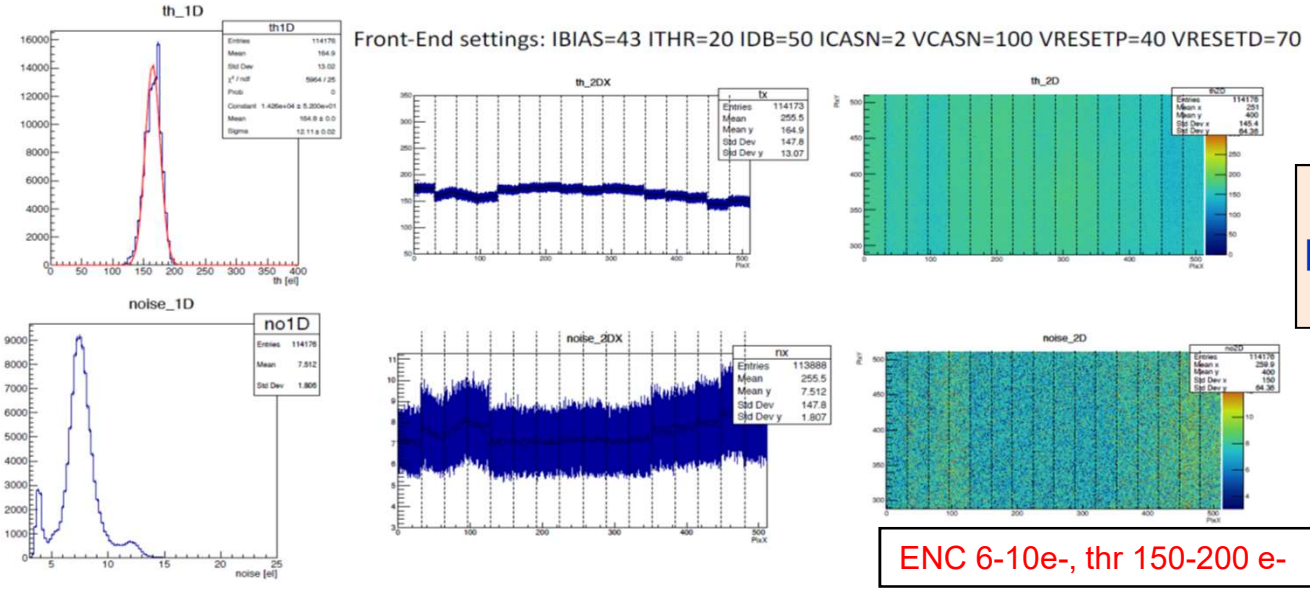
- S-curves & DAC lineary:





- TJ-Malta2 results (indentical FE!):

W5R10 EPI NGAP - Total scan of the matrix



TJ-Monopix2 could be precursor for OBELIX → VTX Belle-II upgrade…

ENC 6-10e-, thr 150-200 e-

Conclusion, perspectives 2022

- **WP hybride**:
  - **28 nm**: prototype finalization (transistors, R-O, SEU-hard cells, ampli) → March 2022 submission / functional tests / irradiation test / pixel matrix: end 2022 / beginning 23
  - Support: IN2P3 / AIDAinnova / RD53? (28nm session in Sept. in RD53 collab week)

- **WP DepCMOS**:
  - **TJ65**:
    - Tests CE65 & RO / irradiations / CE65+ conception
    - Support: AIDAinnova/ CERN strategic R&D WP1.2 / Participation to ER1 through DICE
  - **LF 150**:
    - Finalization LF-Monopix2 tests / small pixels / RD50-MPW3 / tbd small pixel matrice
    - AIDAinnova / RD50 framework
  - **TJ180**:
    - TJ-Monopix2 functional tests / irradiation tests / OBELIX transition for potential Belle-II VTX Upgrade (v1 in 2022, targets 100 MHz/cm², ~50 MRad, ~3.10^{14} n_{eq}/cm²).
    - AIDAinnova / CERN strategic R&D WP1.2 / transition Belle II upgrade
  - Synergies on DepCMOS with CMOS MP (A. Besson's talk)

DICE contributes to cutting edge R&D for future tracking and vertexing applications