# CALICE Si-W ECAL status

Daniel Jeans, LLR Ecole Polytechnique

for the SiW-ECAL groups
Clermont-Ferrand, Grenoble, LAL, LLR, OMEGA

SOCLE, 9 nov 2009

Develop of ECAL for LC “particle flow” detector

-> high granularity calorimeter
-> modest energy resolution

Calorimeter for ILC

## Physics prototype

- Data analysis

## EUDET technological prototype

- Mechanics
- Thermal
- Silicon
- FE electronics
- DAQ (David's talk)
- plans

# Data analysis of physics prototype

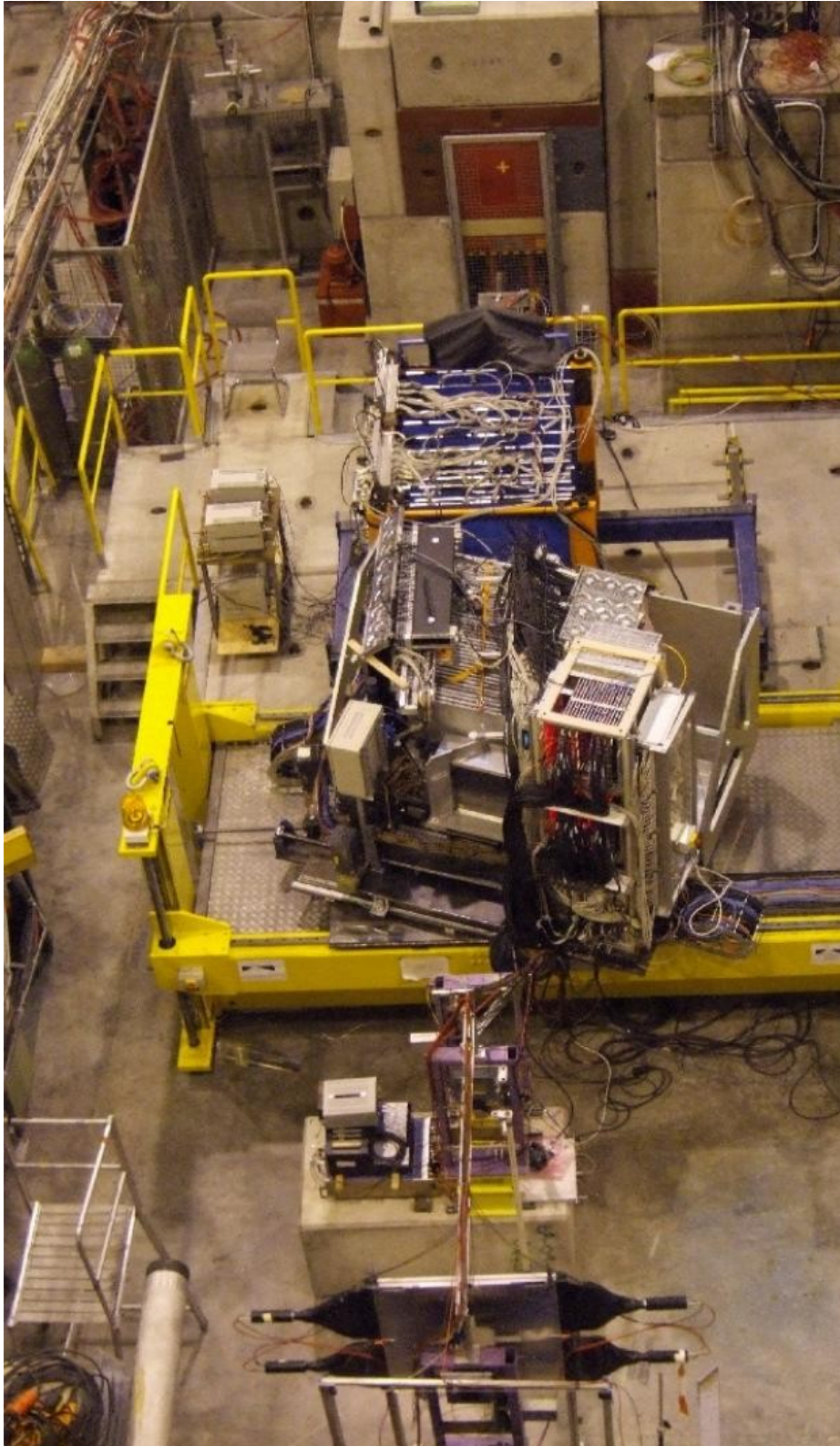
Data taken in 2006-8, combined runs with analogue HCAL & tail catcher

- published:
  - * ECAL commissioning
  - * Response to electrons in homogeneous detector region

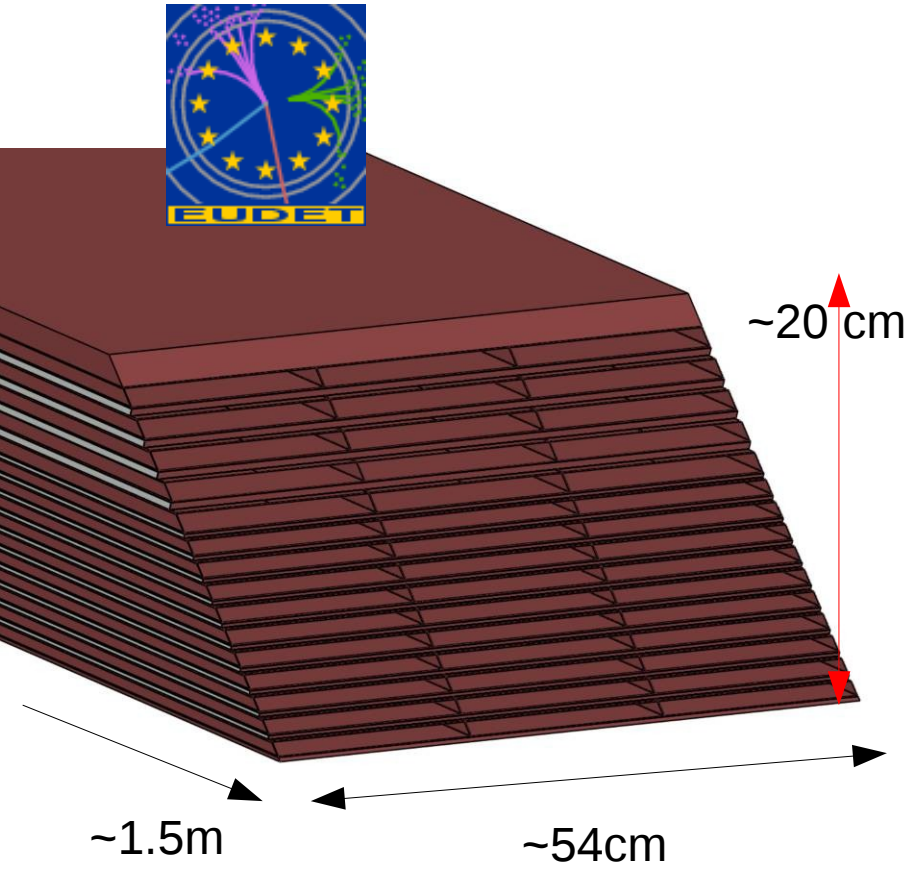
- almost published
  - * readout chip in shower maximum

- analyses in progress
  - * shower profiles (electrons)
  - * angular and position resolution (electrons)
  - * response to pions
  - * uniformity
  - * shower fluctuations and correlations

Need to organise effort rather better

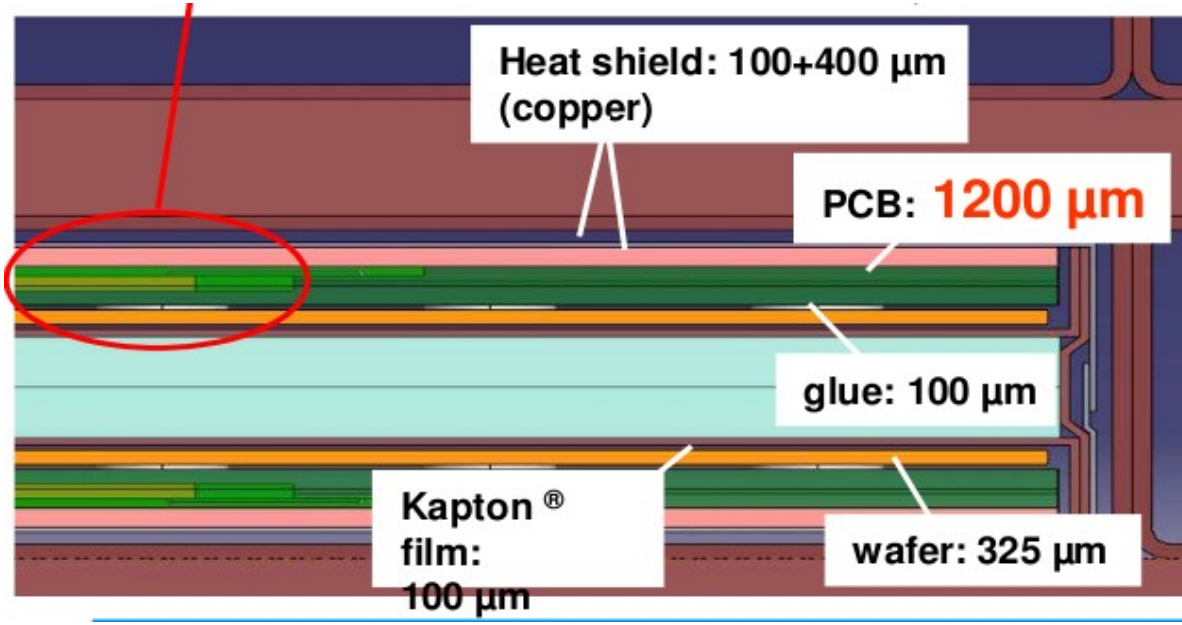


# EUDET (technological) prototype




* Close to shape size of ILD module
* FE electronics embedded
* Higher granularity
  10X10 -> 5x5 mm2

Instrument 18x18 cm2 tower with silicon sensors

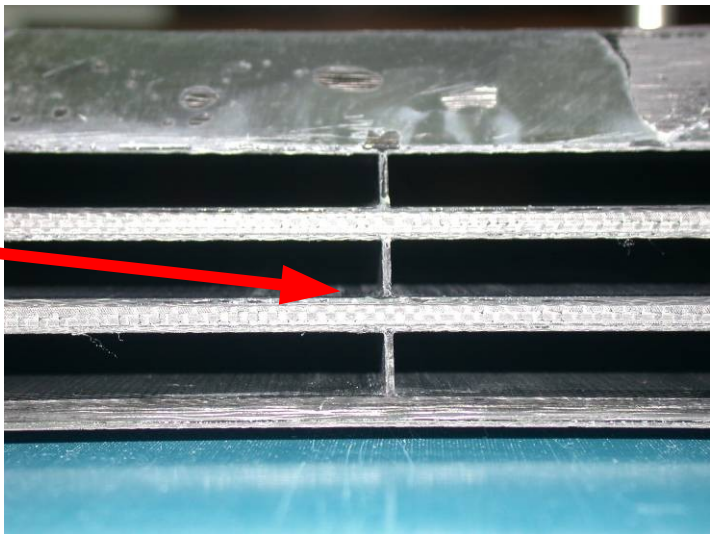


# Mechanical structure

Small demonstrator alveolar structure built

One full-sized layer constructed
more layers will follow in next months

Assembly of layers
Moulds being designed



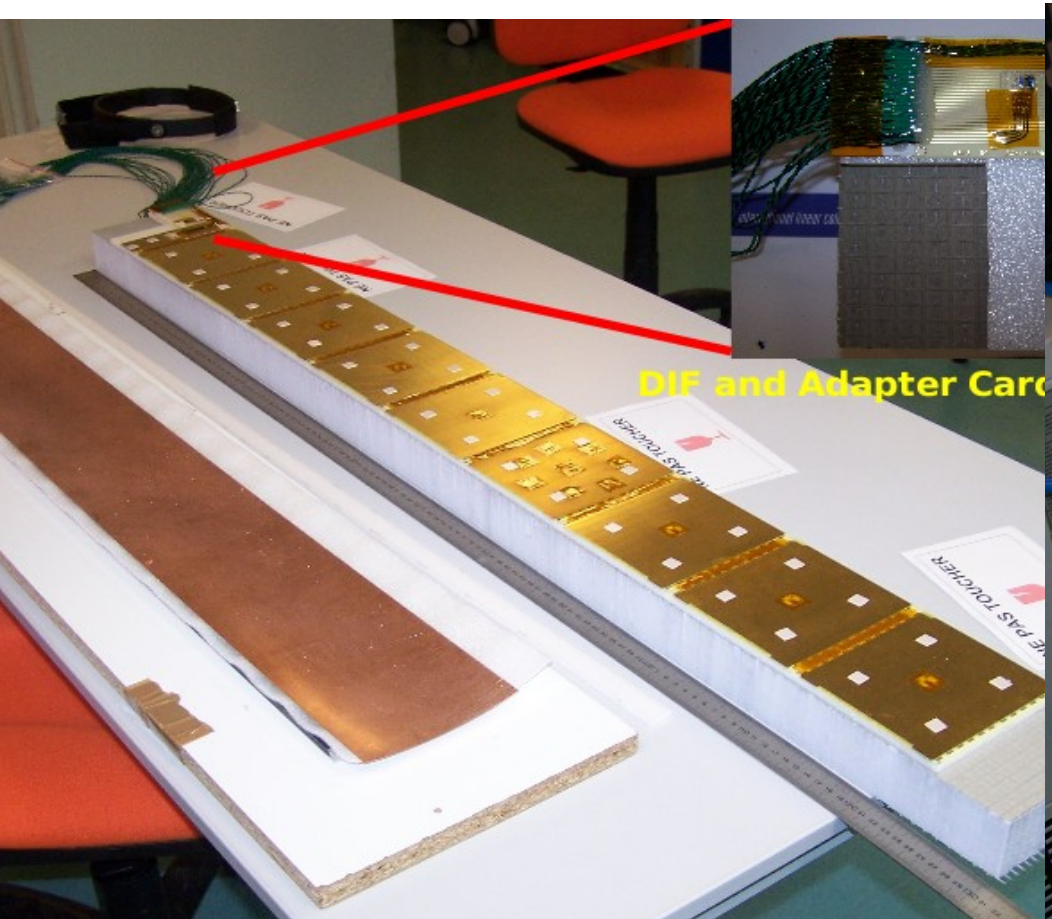
# Thermal characteristics / detector integration

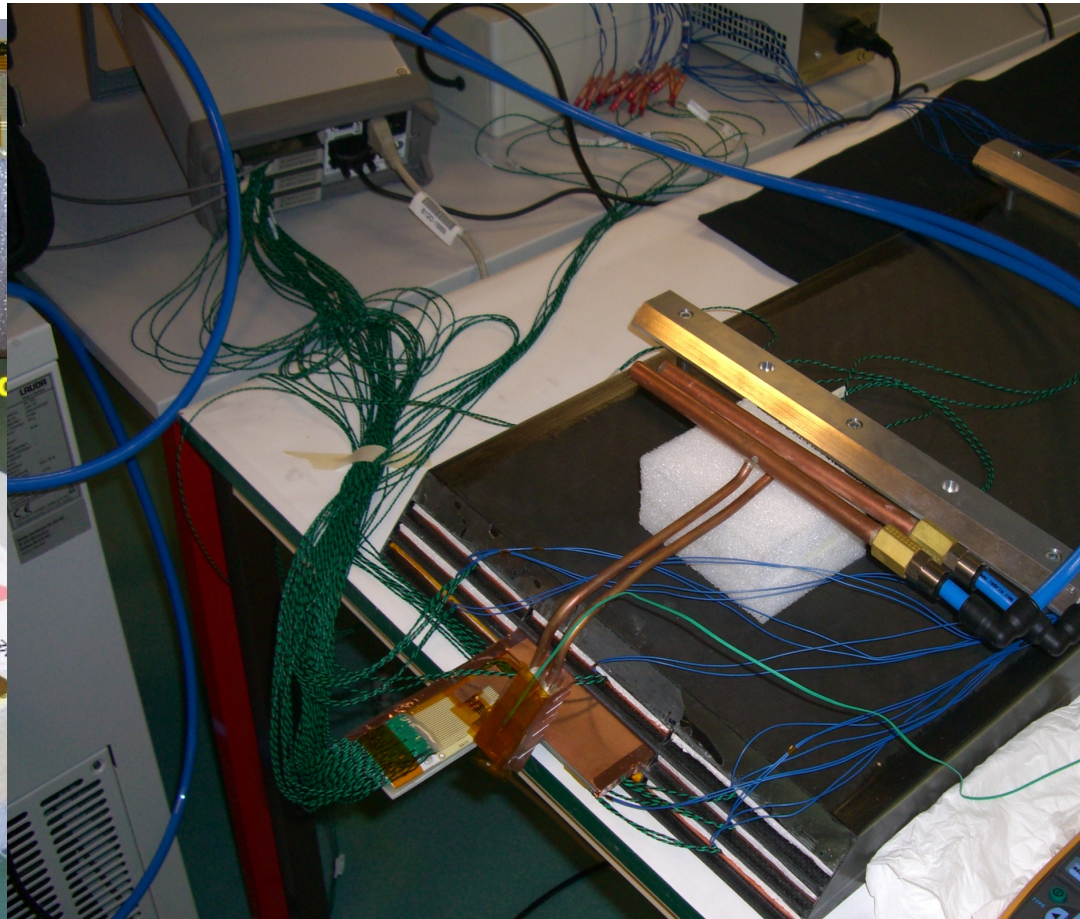
“thermal slabs” deliver 1W in midpoint of each alveola, measure temperature

Slabs constructed in similar way to real layers:
Thin PCB, soldered into long chain

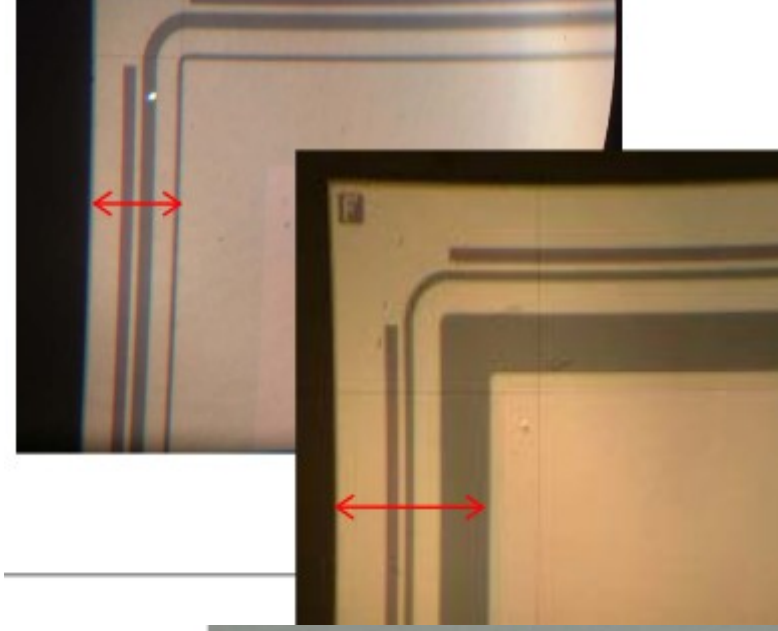
Data taken in thermal tests under analysis: use to tune simulation

Detector integration:
Various tools developed, works well, tolerances OK



# Silicon detectors



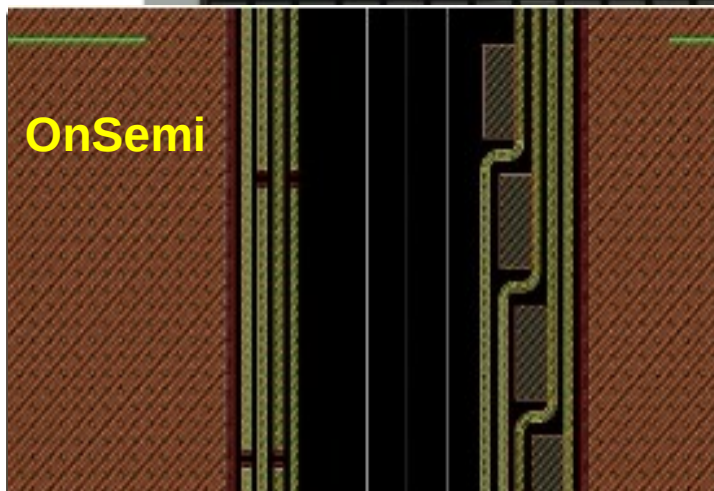
Have ~40 9x9 cm2 detectors in hand (5x5mm2 cells)
- Will instrument part of technological proto (Hammamatsu)

Developing new sensor design
- Particularly the troublesome guard ring region
- Working with other manufacturers OnSemi, BRC

Present cost of silicon detectors >> acceptable for LC detector
- Most important open question

Opening new collaboration...
- Writing MOU to develop sensor with Korea
- Widening links with Japanese colleagues

Links with industry could be developed within AIDA programme

# Front End electronics

SKIROC2 ASIC for technological proto
- being designed

First tests using SPIROC2 chip
Designed for A-HCAL
Many common features with SKIROC2
Less channels, smaller dynamic range

Can run in “SKIROC” mode

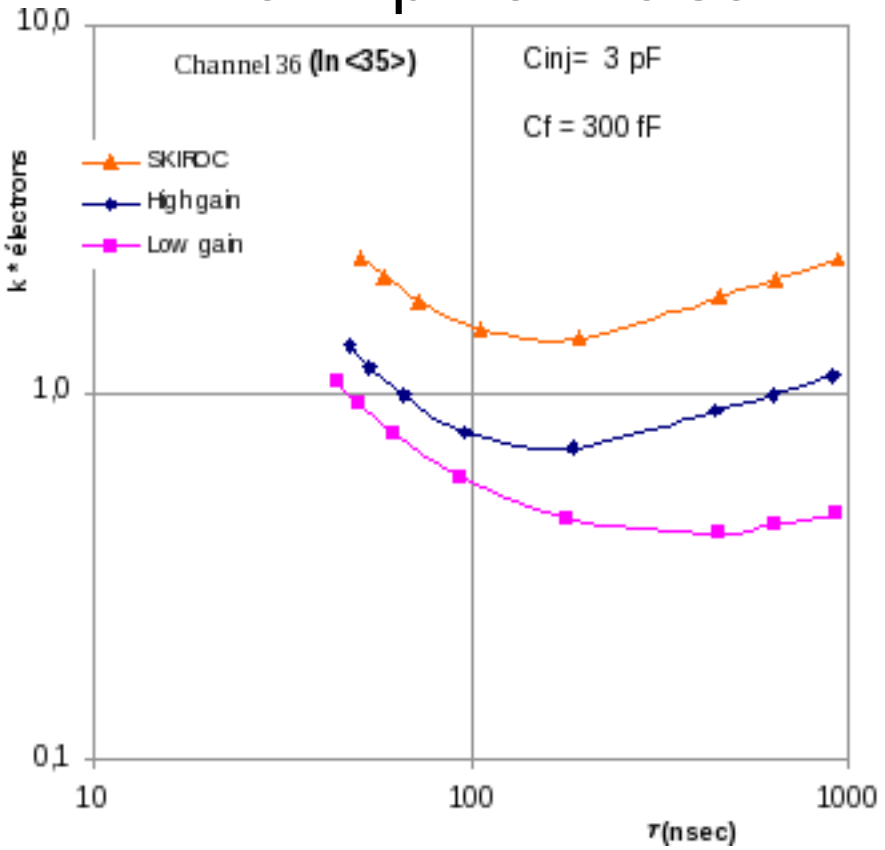
Slides from Stephane Callier/OMEGA

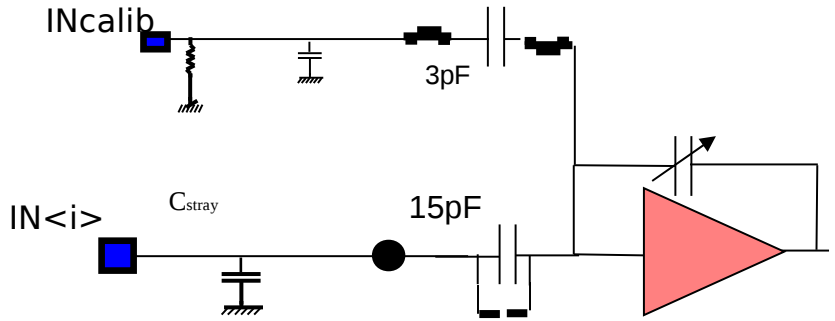
# Tests of SPIROC2 (in SKIROC mode)

SPIROC in SKIROC mode

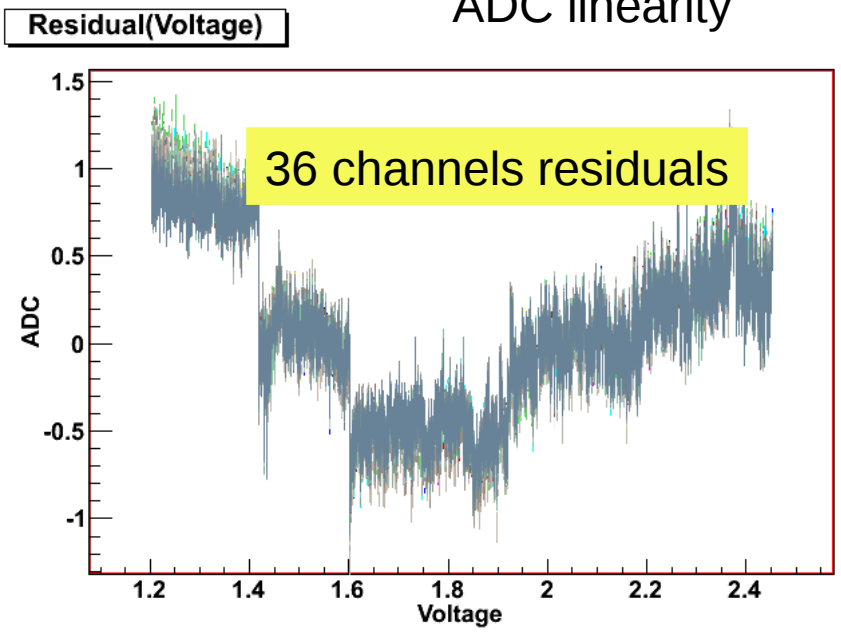
By Maurice Cohen-Solal (LAL)

## PreAmplifier Noise




## ADC linearity




Slides from Stephane Callier/OMEGA

- If SKIROC 2 is validated →
  - production in hand for EUDET module
  - Backup solution: SPIROC2

- Sharing of the HARDROC2 and SKIROC2 production
  - Cheaper than an engineering run for prototyping due to large silicon area (60mm² ie ~60k€)

Slides from Stephane Callier/OMEGA

# PCB: to mount Si detectors & FE electronics

Test board with packaged chip (fev7_CIP)

Ready to be used in cosmic tests with whole DAQ chain

Board with encapsulated chip

First PCB prototypes arrived, second version underway

Chip bonding at CERN (?)

# DAQ

Hardware ready (CALICE UK);
firmware & software under development & debugging (UK, LLR)

See David Decotigny's talk for details

# Future plans

Continue manufacture & assembly of technological proto

Cosmic tests during 2010
- Si detector -> DAQ chain
- Power pulsing

Partially instrumented structure with a few layers ~ start 2011
- Progressively add active layers -> funding

Combined testbeam programme with HCALs and/or trackers
- Within possible AIDA program

Aim: “proved technology” by ~2012

# Summary

Physics proto: data collected, further analysis effort required

Technological proto:

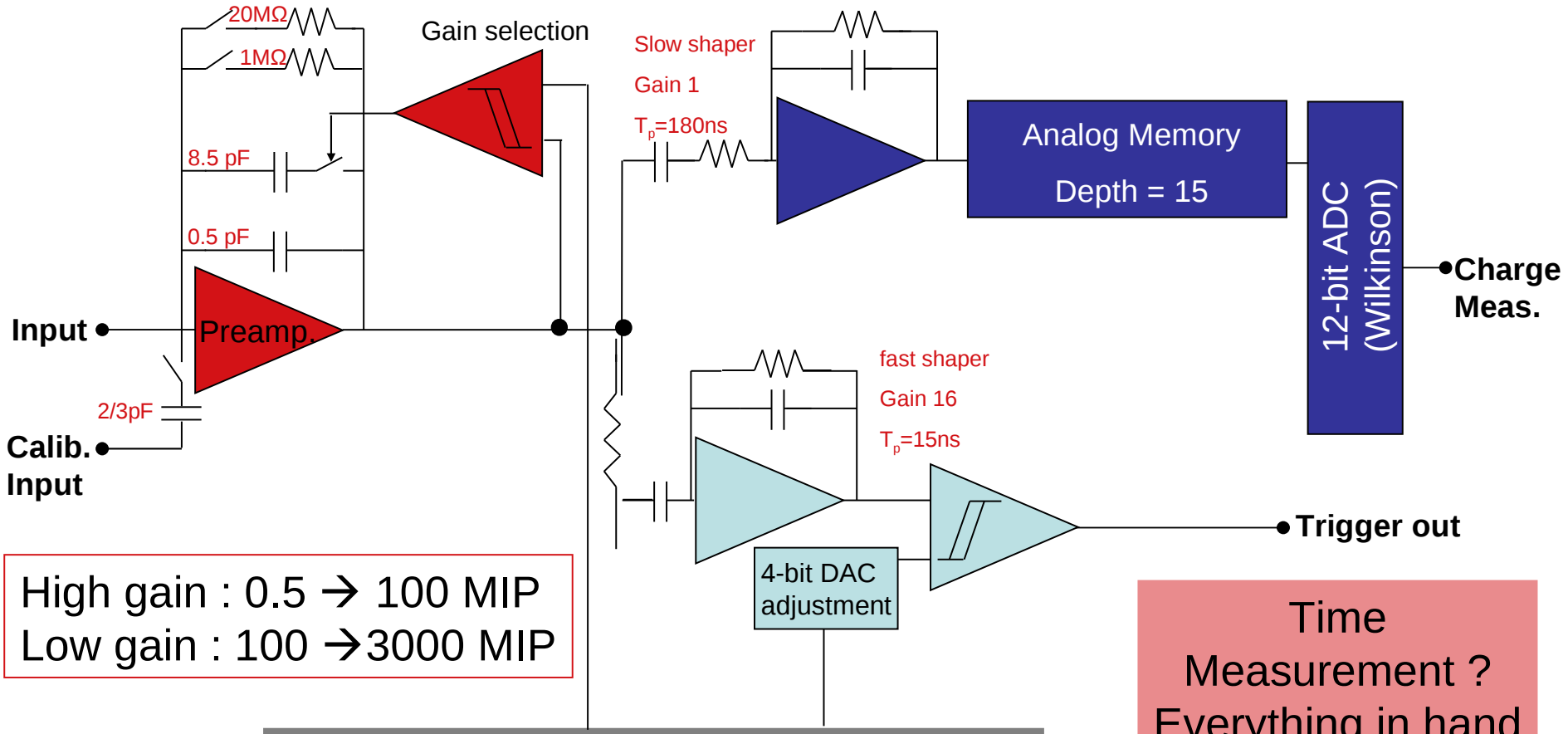
- Mechanics ~ understood
- Thermal: under study
- Slab construction & Integration: ~ understood
- Silicon wafers: have solution, need to reduce cost
- FE electronics: SPIROC2 for tests, waiting for SKIROC2..
- DAQ: firmware development, debugging

Prove Si-W ECAL technology by 2012

- * at reasonable price *

backups

# SKIROC 2 analogue block scheme




High gain : 0.5 → 100 MIP
Low gain : 100 →3000 MIP

Time Measurement ? Everything in hand (from spiroc)

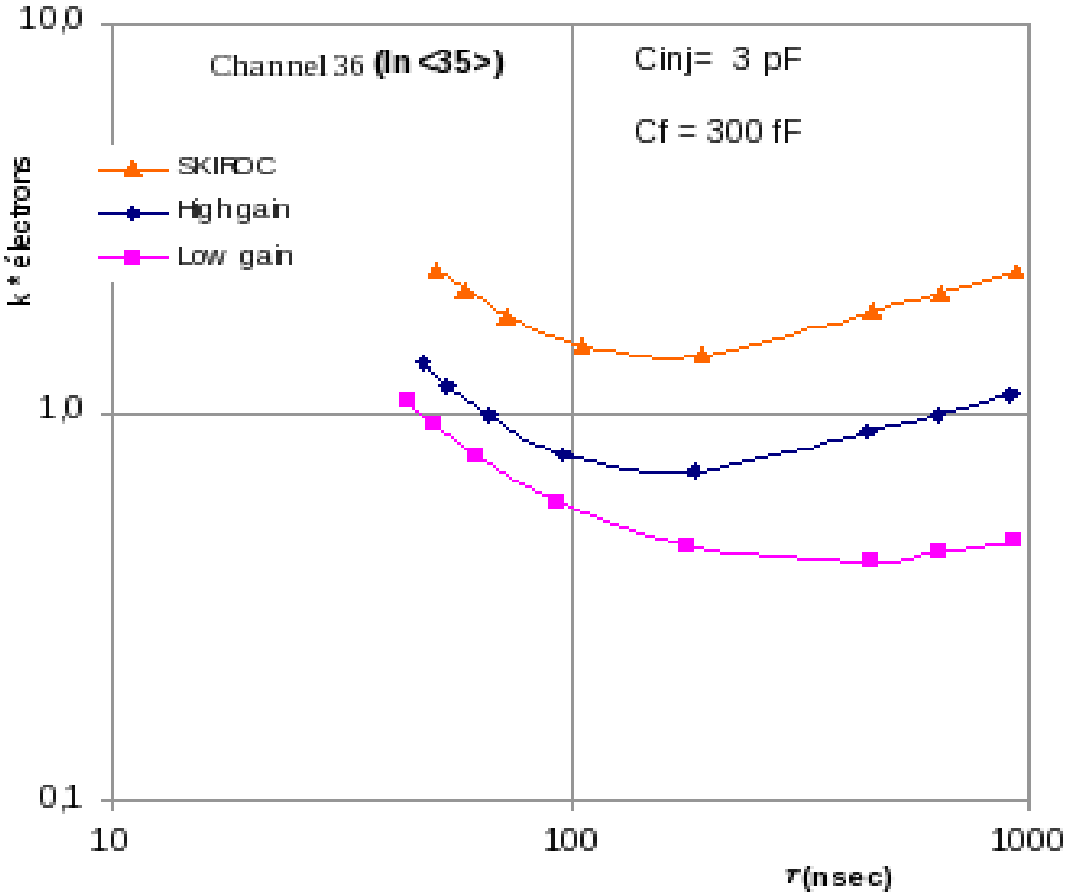
Slides from Stephane Callier/OMEGA

# Tests of SPIROC2 (in SKIROC mode)

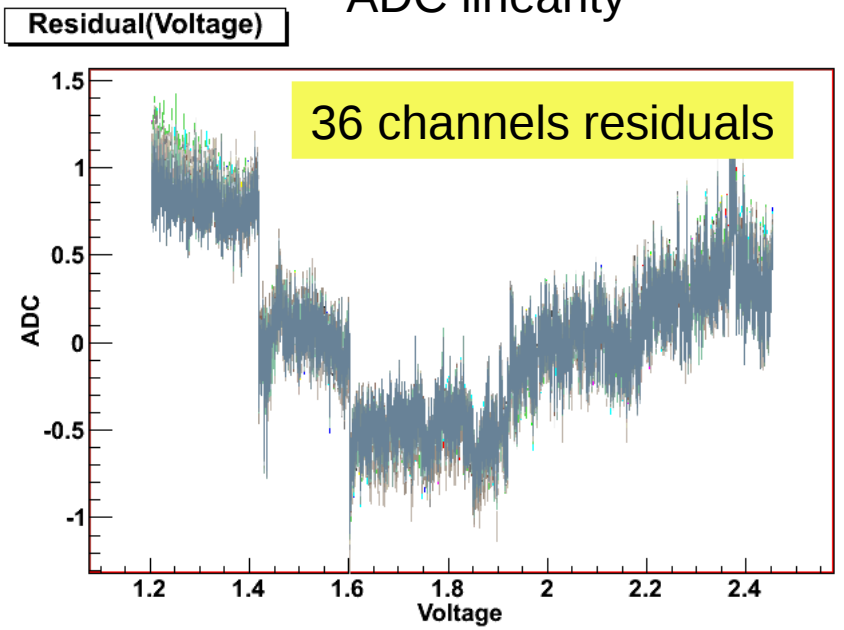
SPIROC in SKIROC mode

By Maurice Cohen-Solal (LAL)

## PreAmplifier Noise

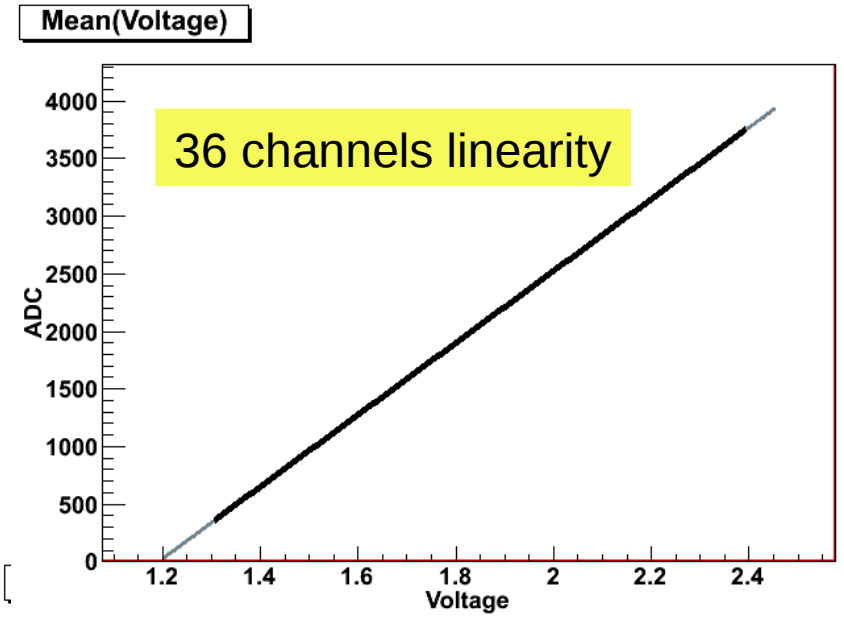


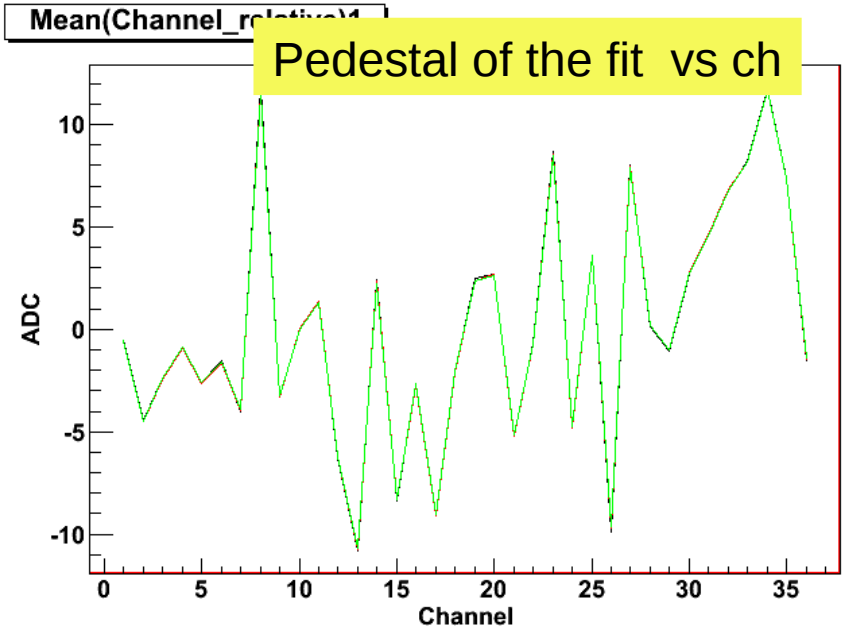

## ADC linearity

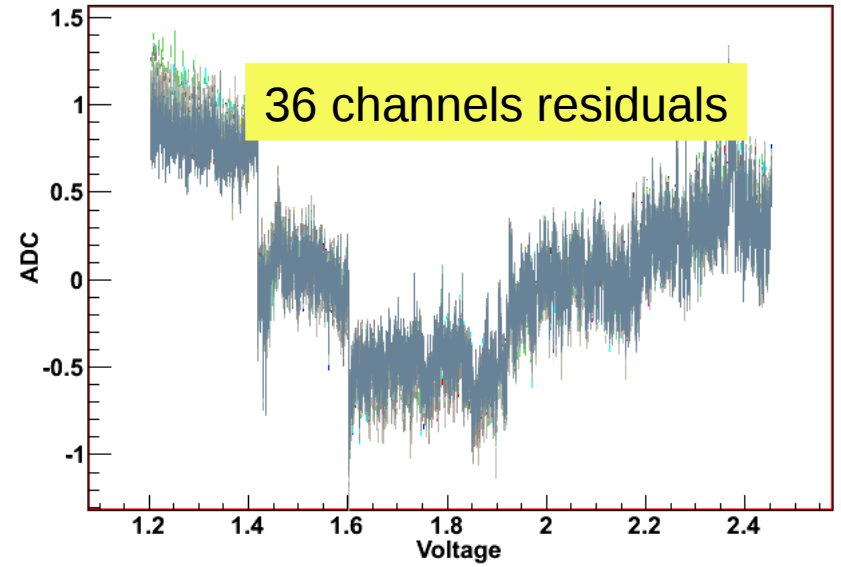


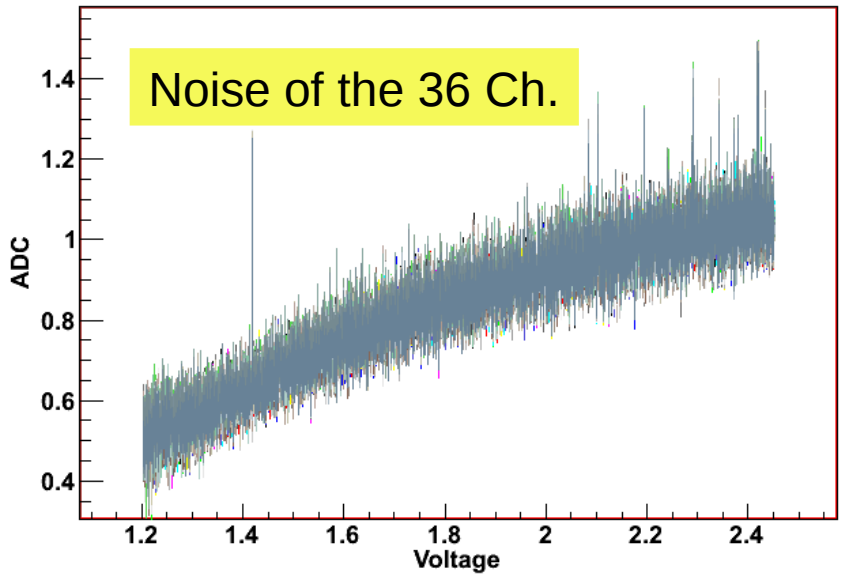

Slides from Stephane Callier/OMEGA

# Internal 12-bit ADC performance




Slides from Stephane Callier/OMEGA