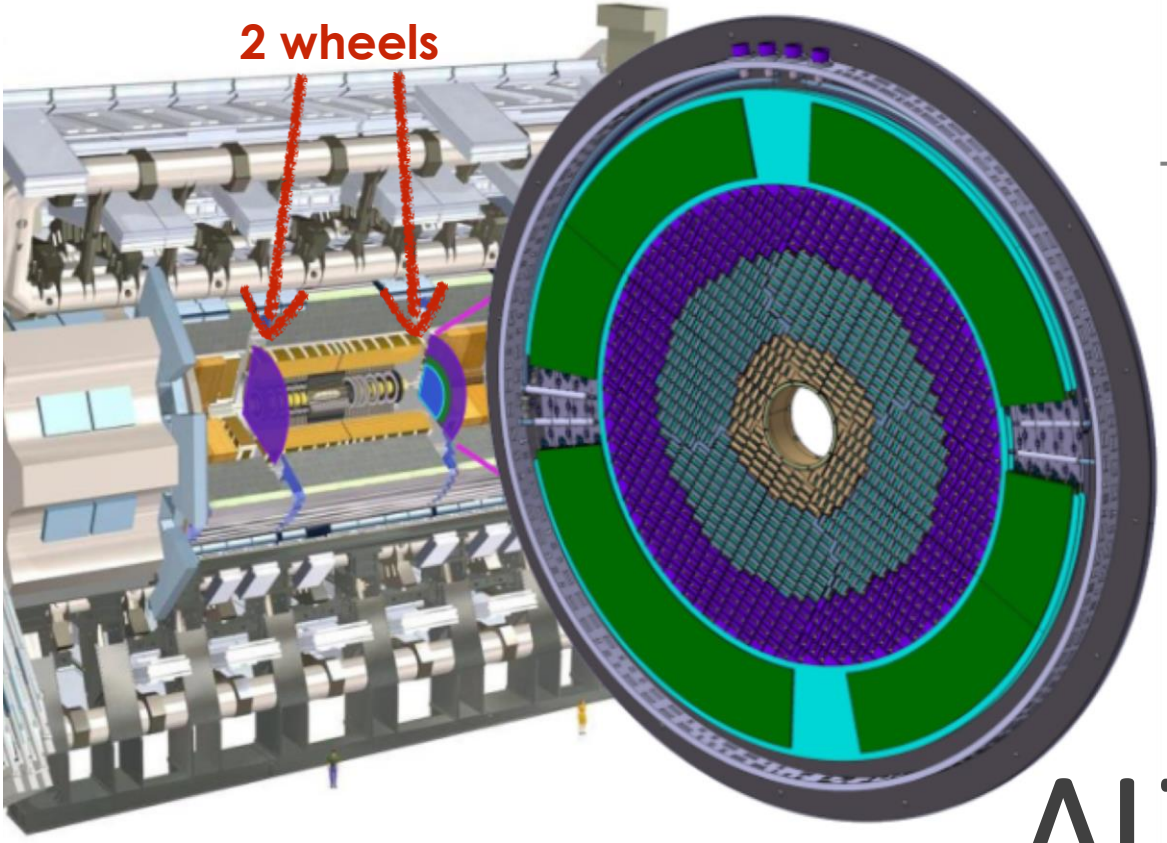
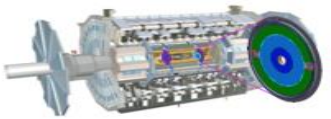


Maxime Morenas/OMEGA on behalf of ATLAS HGTD

IEEE NSS, 5 October 2020

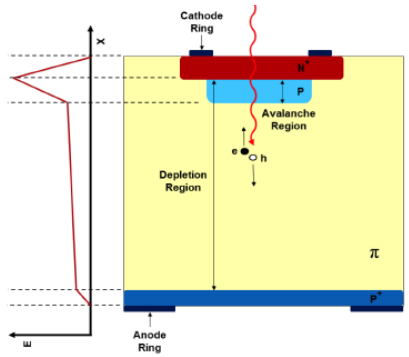
ALTIROC1

A 25 pico-second time resolution ASIC for the ATLAS High Granularity Timing Detector (HGTD)

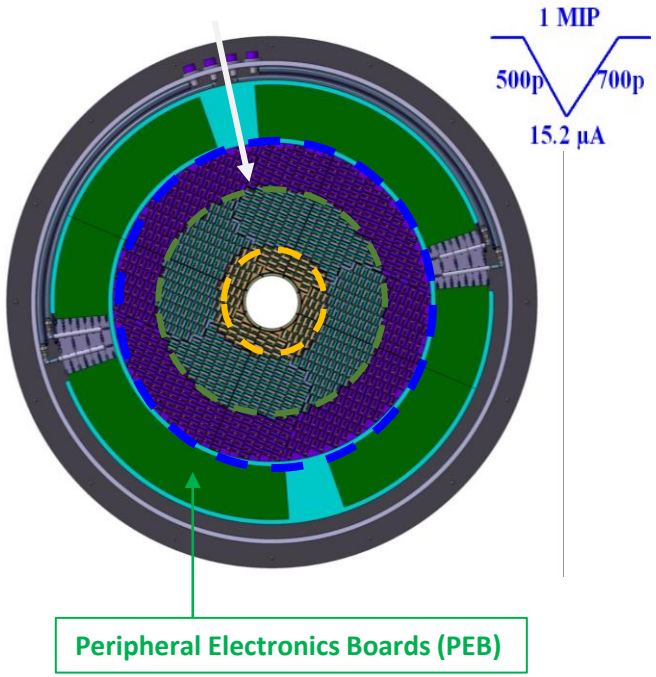


ATLAS HGTD

High Granularity Timing Detector in HL-LHC



LGAD sensors
1.3 x 1.3 mm^2
Thickness = 50 µm

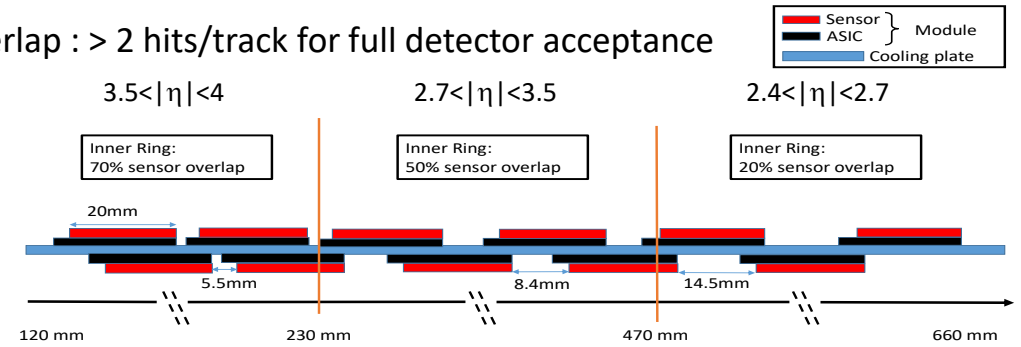


REQUIREMENTS of the HGTD DETECTOR

- **Luminosity measurement**: sum of the hits for each Bunch Crossing
- **Time measurement** for minimum ionizing particle

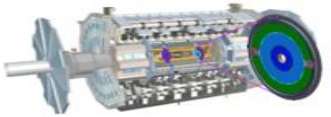
with a resolution between **25 ps to 50 ps per track** over the detector's lifetime
35 ps to 70 ps per hit

Overlap : > 2 hits/track for full detector acceptance



Active area: LGAD sensor bump-bonded onto **2 ASICs (225 channels/ASIC)**
- **Inner ring** : 12 cm< R< 23 cm (3.5 < η < 4.0) replaced each 1000 fb^{-1}
- **Middle ring** : 23 cm< R< 47 cm (2.7 < η < 3.5) replaced at 2000 fb^{-1}
- **Outer ring** : 47 cm< R< 64 cm (2.4 < η < 2.7) never replaced

Rings replacement allows to keep:
- 2.5x10^{15} n_{eq}/cm^2 max (w/SF=1.5) and TID 2 MGy max (w/SF=2.25)
- Charge in irradiated sensor > 4fC



ATLAS HGTD

Requirements for the ASIC

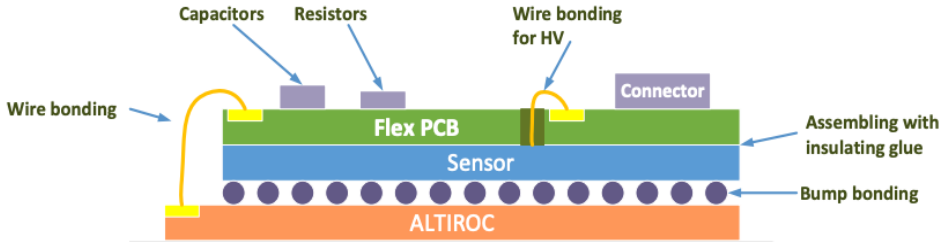
Maximum jitter (σ_{elec})	**25 ps at 10 fC at the start of the HL-LHC and 70 ps for 4 fC at the end**
TDC contribution	**< 10 ps**
Time walk contribution	**< 10 ps**
Clock contribution	**< 15 ps**

TDC conversion time	**< 25 ns**

PAD size	1.3 x 1.3 mm^2 x 50 µm => **Cdet = 4 pF**
ASIC size and channels /ASIC	2x2 cm^2 15x15=225 channels/ASIC
Single PAD noise (ENC)	**< 3000 e- or 0.5 fC**
Minimum threshold	**2 fC**
Dynamic range	**4 fC** to 50 fC

Main contributors to time resolution

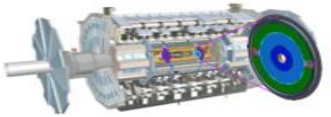
$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$
$$\text{with } \sigma_{elec}^2 = \sigma_{Time\ walk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2$$



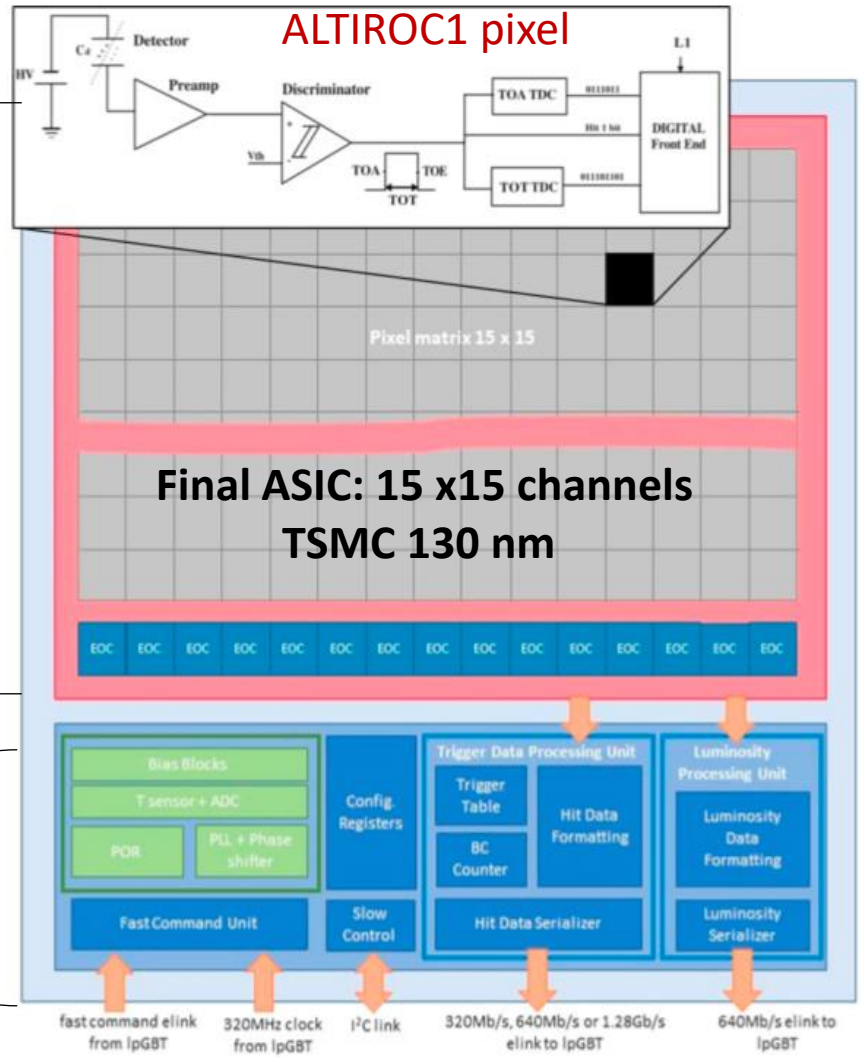
TID Tolerance	**2 MGy** (inner modules replaced after each 1000 fb^{-1} , middle ring after 2000 fb^{-1})
Full chip SEU probability	< 5 % / hour

ASIC designed in CMOS 130 nm

Voltage and Power dissipation per ASIC	1.2V and 300 mW cm^{-2} => 1.2 W/ASIC (225 ch) or **4.4 mW/channel** and 200 mW for the common part



Front end electronics-ASIC: ALTIROC, analog part



Analog part
Pixels tested with Altiroc1

Digital blocks
Under design

- Main challenge = small jitter (low noise/capacitance) down to 4 fC

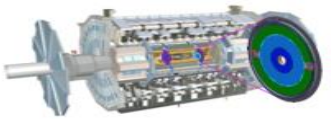
⇒ **Analog FE performance crucial**

$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

C_d: sensor cap (~4 pF)
t_d: LGAD drift time, 600 ps
Q_{in}: MIP charge (10 fC at start, 4 fC at end)
e_n: noise spectral density of input trans.

⇒ **ALTIROC1 prototypes** (5x5 ch), which integrate

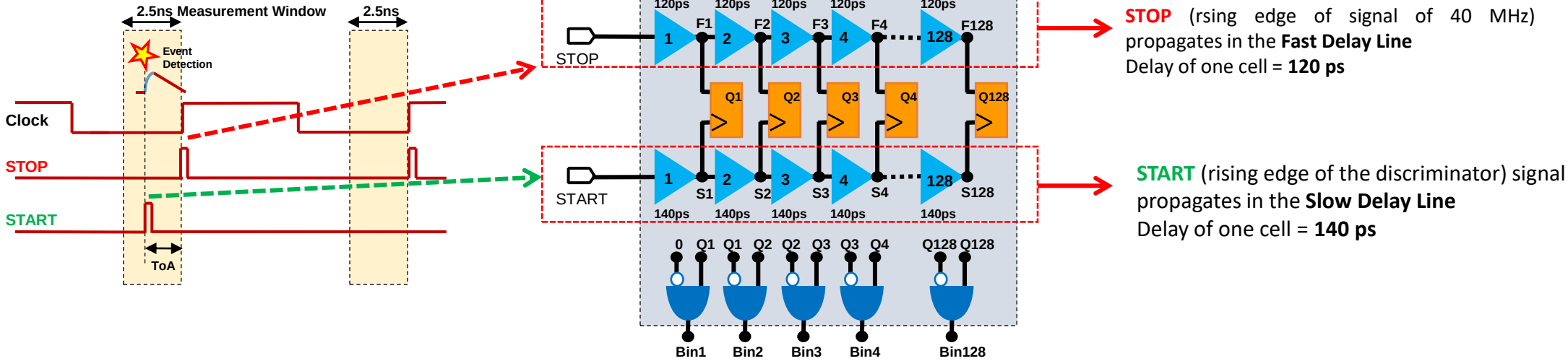
- A voltage **preamplifier** followed by a **discriminator**:
  - Time walk correction made with a Time over Threshold (TOT) architecture
- **Two TDC** (Time to Digital Converter) to provide digital **Hit data** =Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
  - TOA TDC: bin of 20 ps (7 bits), range of 2.5 ns, to be centered on the bunch crossing
  - TOT TDC: bin of 160 ps (9 bits), range of 20 ns
- One local memory (**SRAM**):
  - 17 bits of the time measurement (Hit data) stored until L0/L1 trigger (~ 1 MHz) if hit detected (otherwise 1 bit stored), trigger latency = 10 µs in Altiroc1, will be 35 µs in full size ASIC (Altiroc2)
- **Phase shifter**



TOA TDC Architecture : Vernier Delay Line

TOA TDC
- Resolution: 20 ps
- Range: 2.5 ns
- 7 bits

TDC Power consumption 0.4 mA *1.2 V = 0,5 mW @ 10% occupancy



STOP (rsing edge of signal of 40 MHz) propagates in the **Fast Delay Line**
Delay of one cell = **120 ps**

START (rising edge of the discriminator) signal propagates in the **Slow Delay Line**
Delay of one cell = **140 ps**

Differential shunt capacitor voltage-controlled delay cells

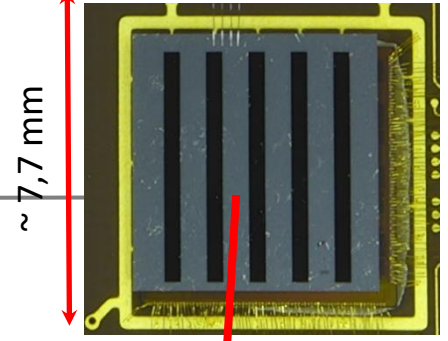
- START pulse comes first and initializes the TDC operation. STOP pulse follows the START with a delay that represents the time interval to be digitalized.
- At each tap of the Delay Line, STOP signal catches up to the START signal by the difference of the propagation delays of cells in Slow and Fast branches: i.e. 140ps – 120ps = 20ps (LSB).
- The number of cells necessary for STOP signal to surpass the START signal represents the result of TDC conversion
- Cycling configuration used in order to reduce the total number of Delay Cells.
- TDC range is equal to 128 * 20 ps = 2.56 ns

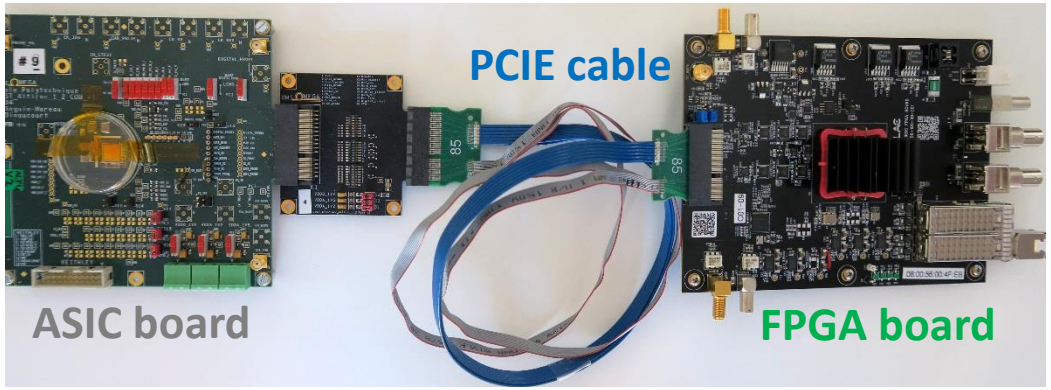
TESTBENCH

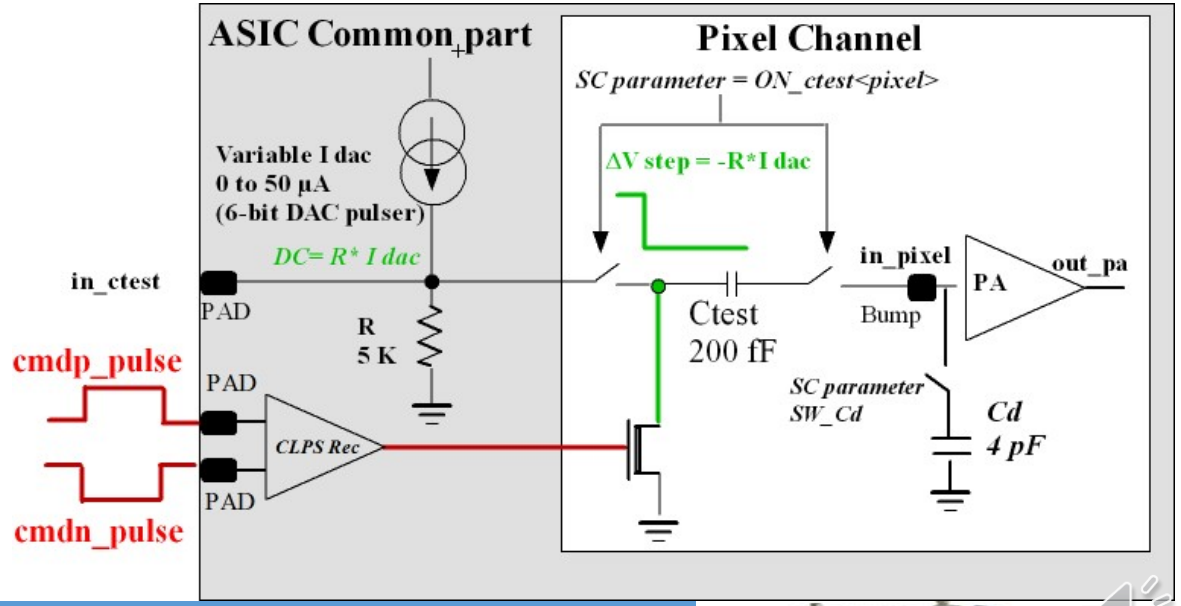
- **ALTIROC1** : testbench measurements (ASIC alone or with sensor), irradiation tests, testbeam

- **Setup:** ASIC board (ASIC alone or bump bonded onto sensor) + FPGA board

- Charge injection (0 up to 50 fC) using **ASIC internal calibration pulser** controlled by **cmd_pulse** input, generated by the FPGA, synchronous to 40 MHz clock
- ASIC alone: Cd=4 pF can be set by SC to mimic sensor capacitor
- **External trigger,** width and delay tunable by 10 ps steps **:** used to characterize the TOA and TOT TDC alone

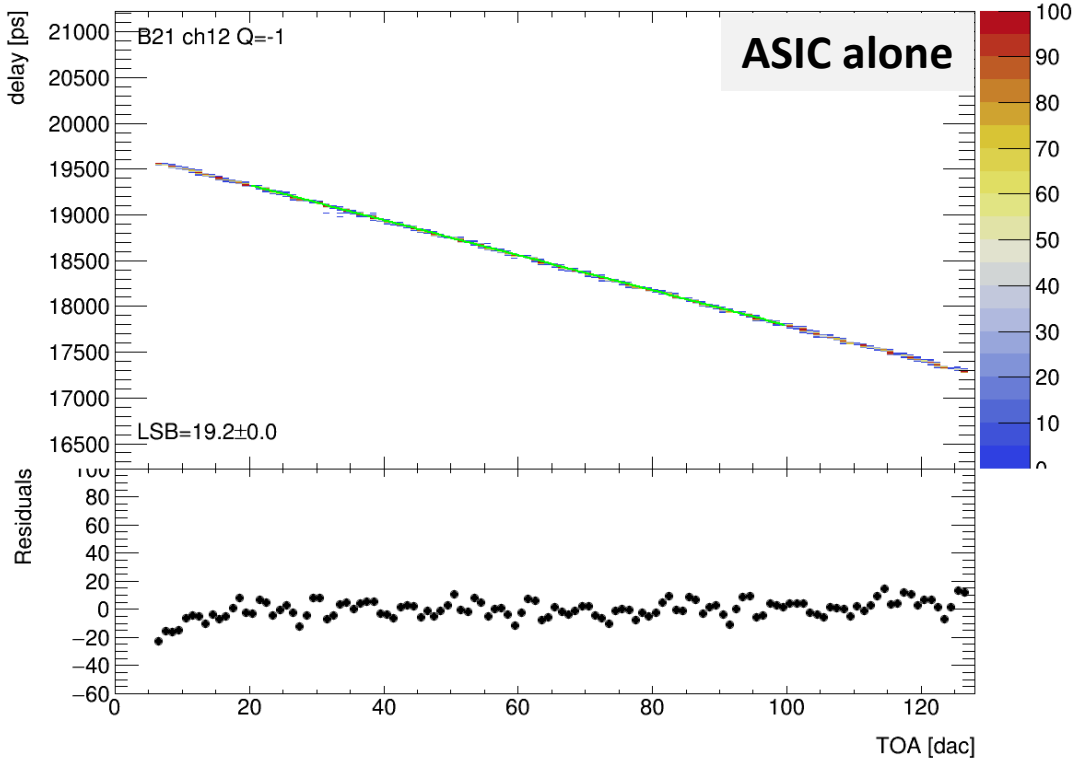




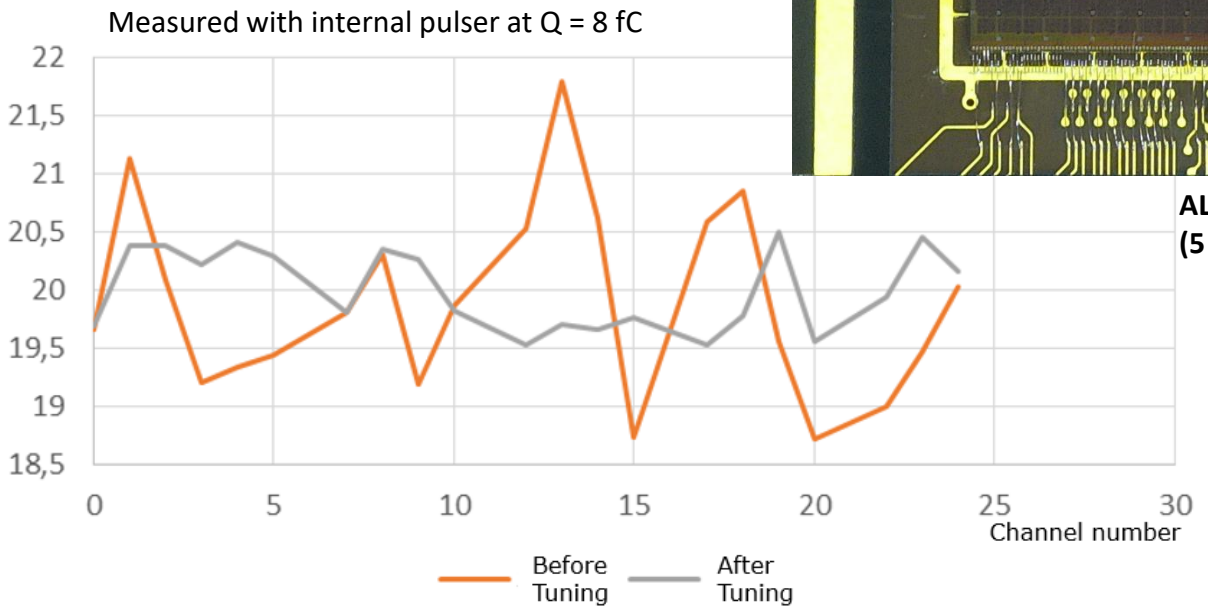


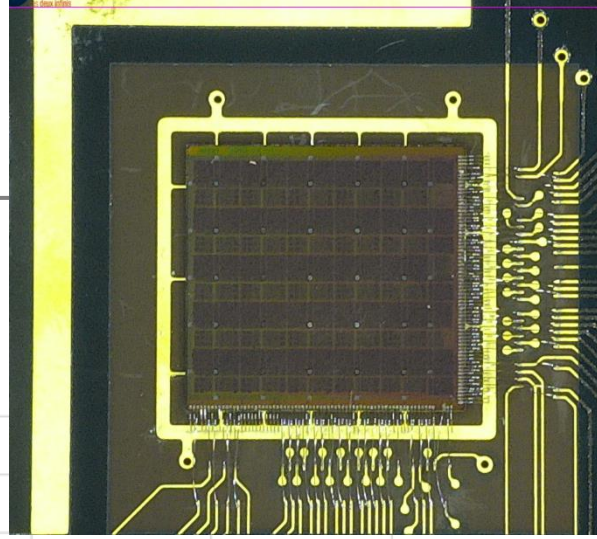
ALTIROC1 – TOA TDC performance

Delay versus <TOA>



<TOA LSB> vs channel





ALTIROC1
(5 × 5 channels)

<TOA_LSB> = 19 ps

<TOA_LSB> = 20 ps
Rms jitter = 0,35 ps

- TOA_LSB and TOT_LSB can be adjusted to 20 ps and 160 ps per channel using Slow Control parameters

ALTIROC1 - DLL performance in temperature

3 DLL : **Fast** (120 ps), **Slow** (140 ps), **Coarse** (160 ps)

TDC for TOA

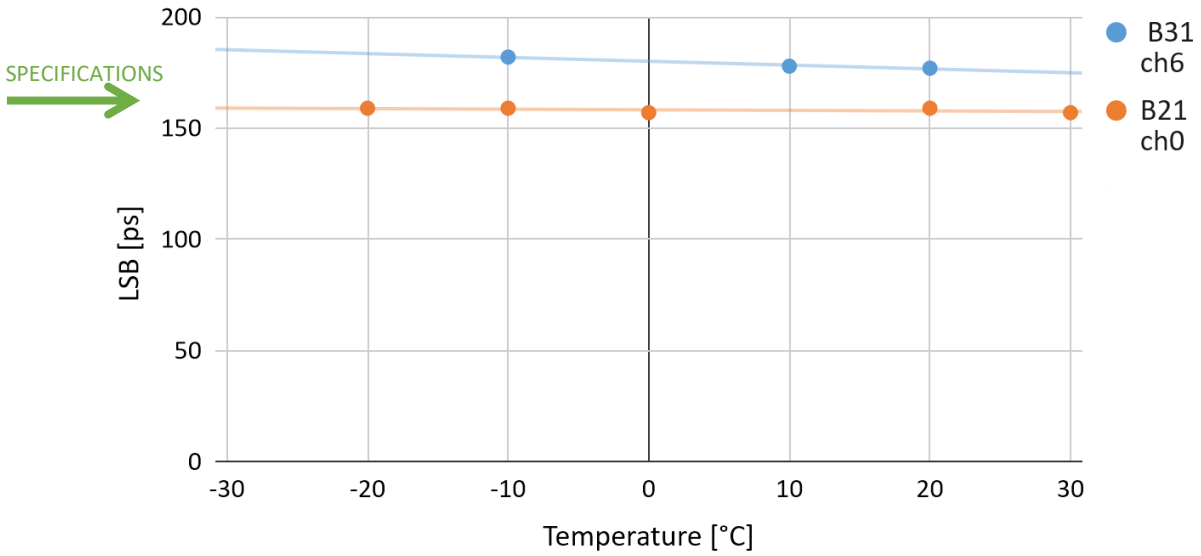
Achieving 20 ps LSB

TDC for TOT

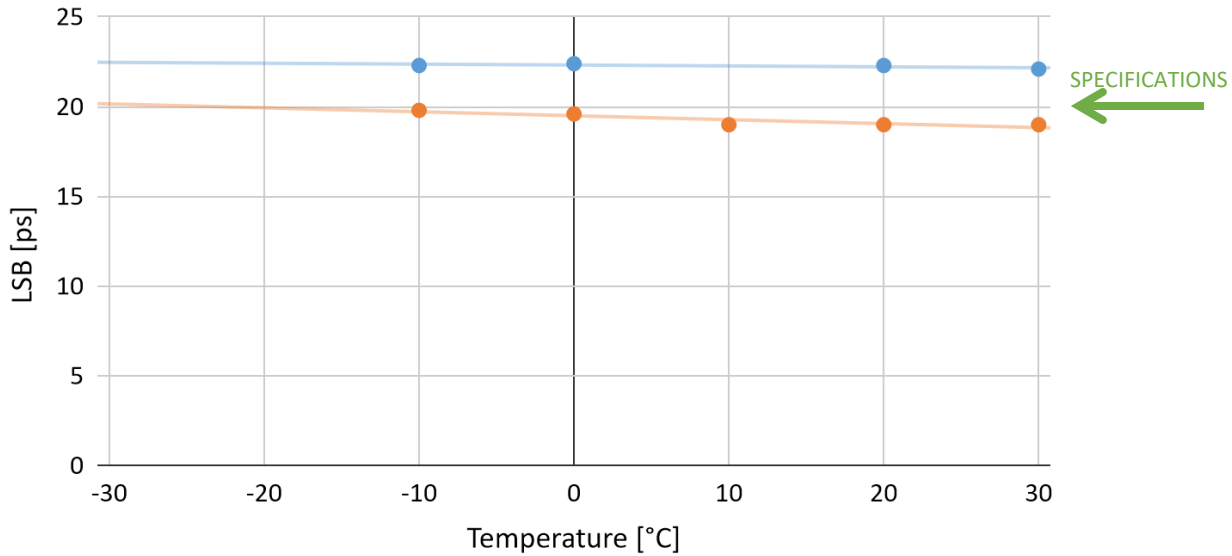
Achieving 160 ps LSB

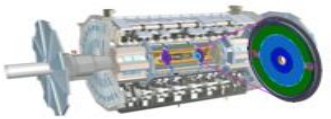
- Different <LSB> because not tuned
- Average temperature variability : below 3%

TOT LSB



TOA LSB

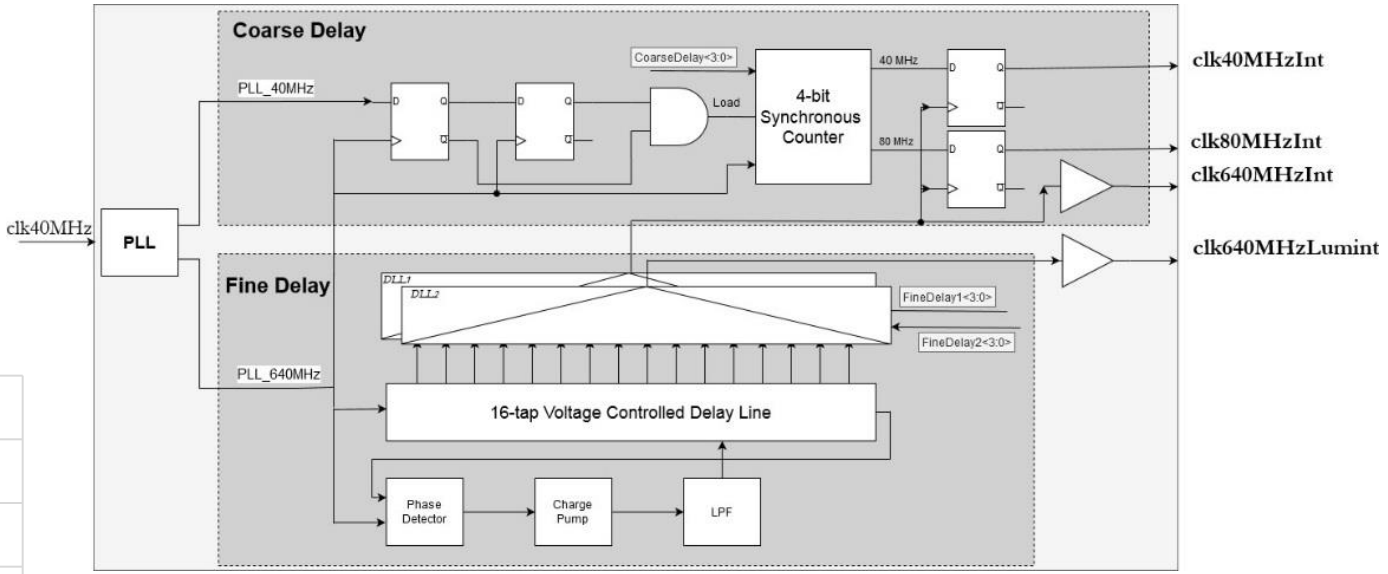




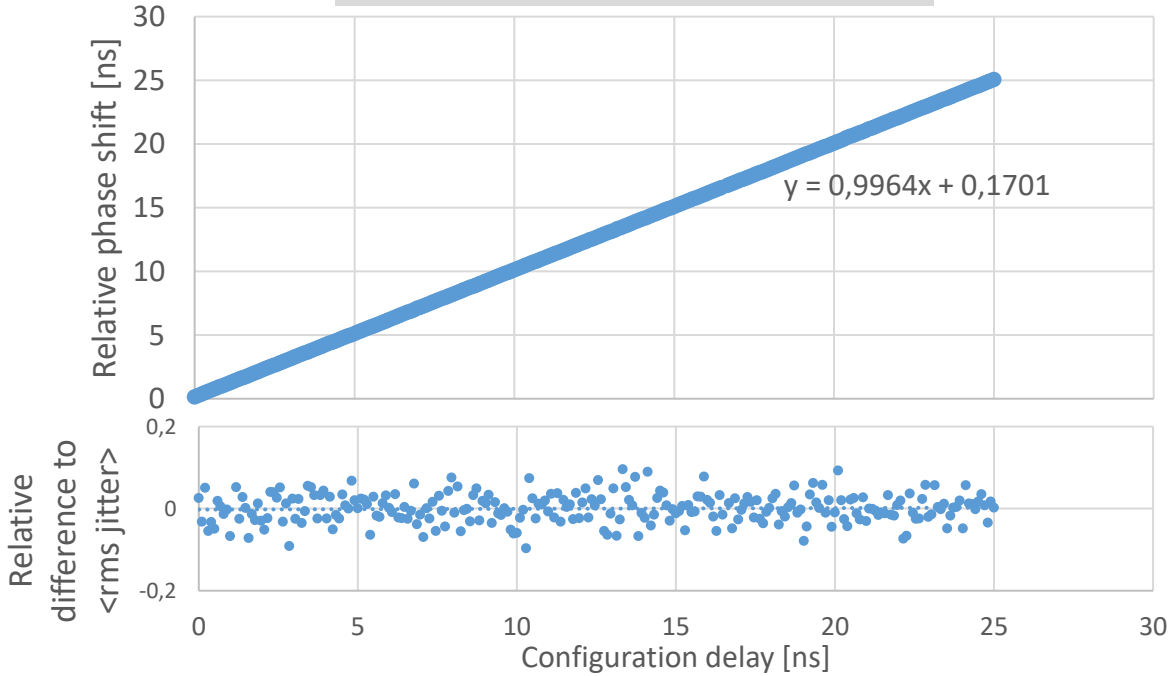
ATLAS HGTD

ALTIROC1 – Phase shifter performance

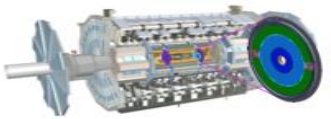
- Used to center the 2.5 ns measurement time window of the TOA TDC on the Bunch Crossing
- Requirements:
  - **Step 100 ps ± 10 ps, range 25 ns**
  - Power dissipation < 10 mW



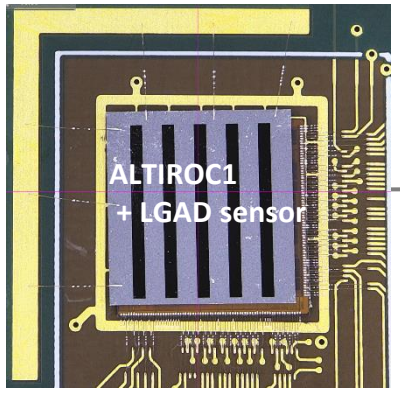
Phase shift vs delay at +20°C



- Results :
  - Shift the 40 MHz clock by steps of 98 ps LSB and range achieved
  - **<output clock rms jitter>**$_{temperature,range}$: 14 ps



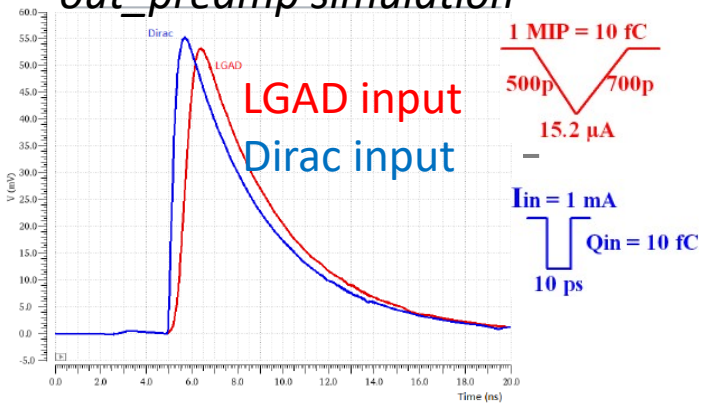
ATLAS HGTD

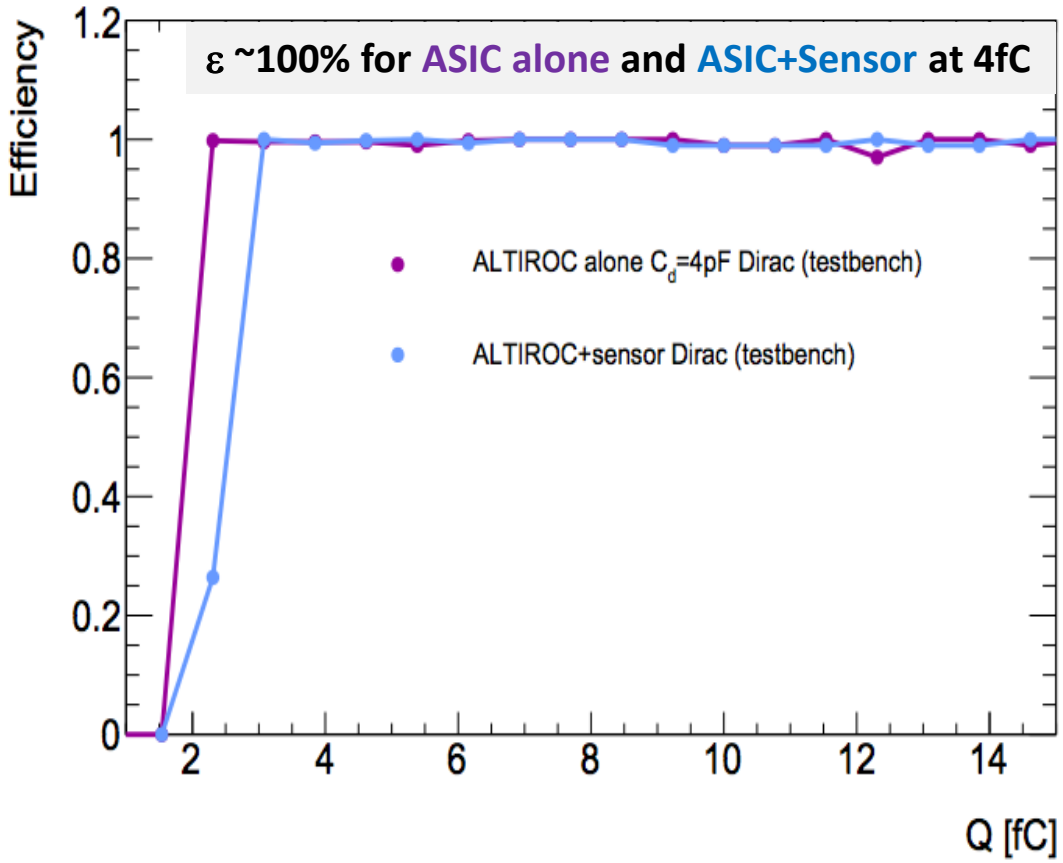


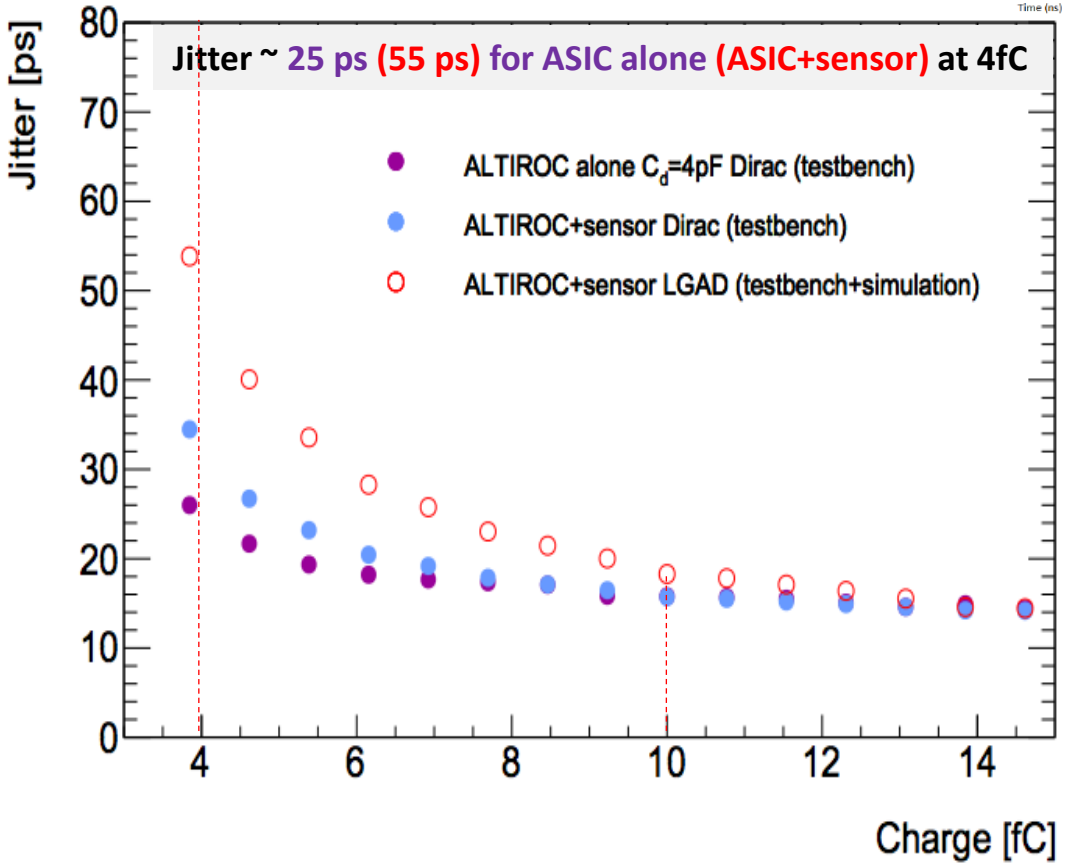
ALTIROC1 - Analog performance at system level

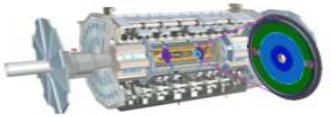
System level = ASIC bump-bonded onto a 5x5 LGAD sensor (1.3 mm x 1.3 mm x 50 µm)

out_preamp simulation



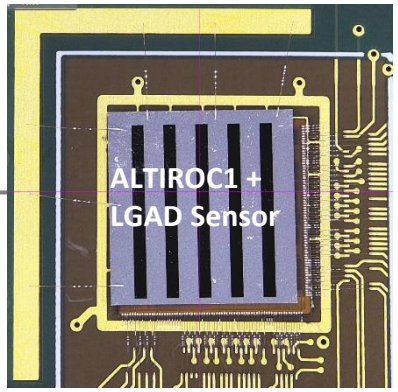




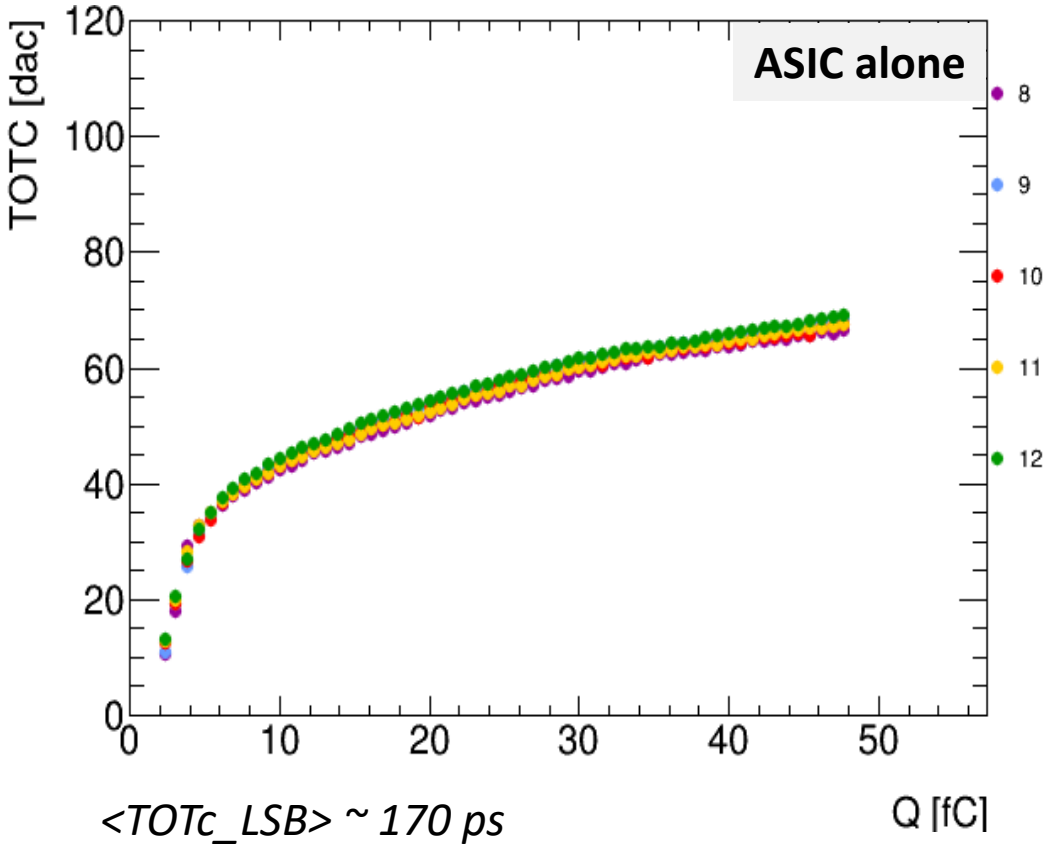


ATLAS HGTD

ALTIROC1 - Analog performance at system level

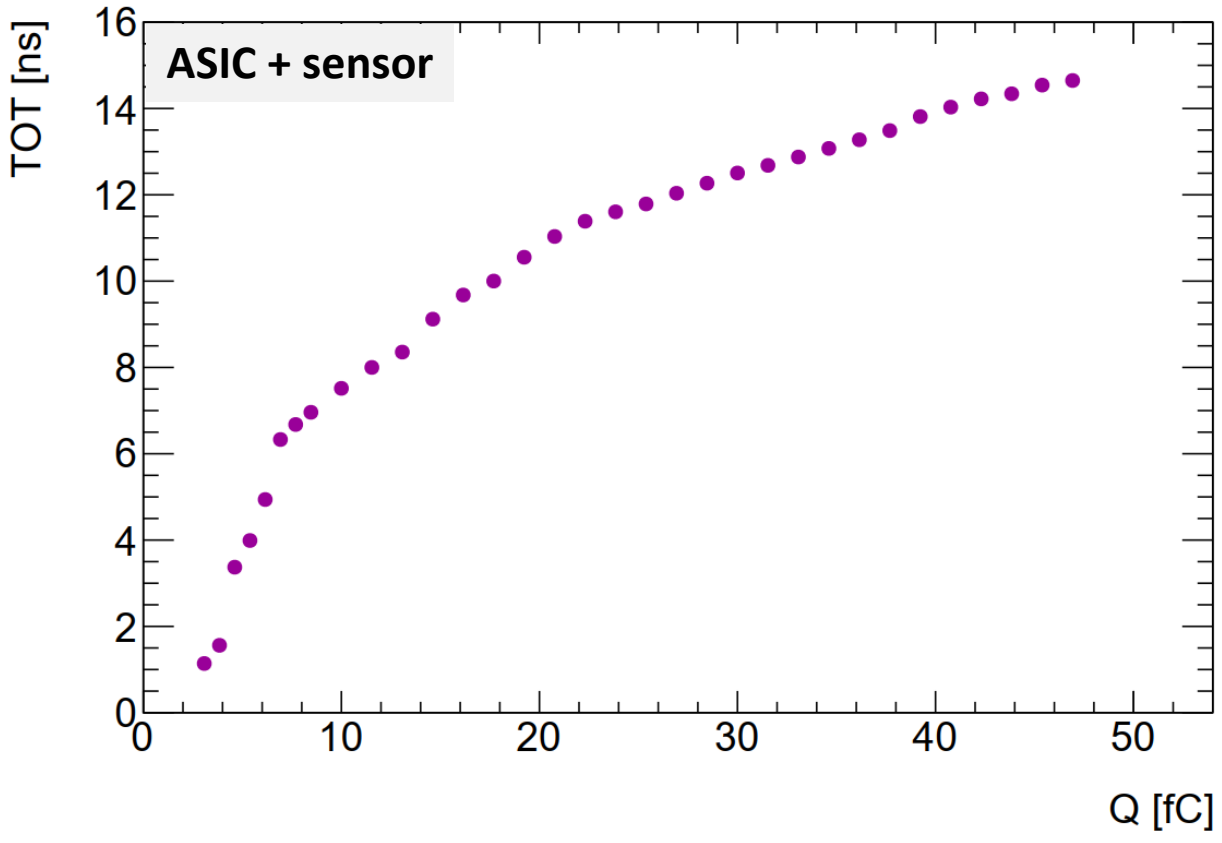


TOTc of Ch4, Cd =4 pF vs Qinj for several boards



<TOTc_LSB> ~ 170 ps

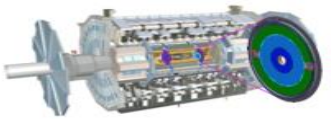
TOTc vs Qinj



SUMMARY & CONCLUSIONS

- Good analog performance demonstrated with ALTIROC1 prototypes
  - Very useful to understand system issues with sensor
  - Jitter (ASIC+sensor) < 35 ps at 4 fC with calibration pulse
  - Vth (ASIC+sensor) can be set at 2 fC
  - More results about under irradiation tests and testbeam presented by **Dr. Yusheng Wu (2 nov.)**

- Design of first full size ASIC (ALTIROC2) is on going, submission end 2020
  - Mix of Digital On Top (DOT) and Analog On Top (AOT), compromise between power dissipation, timing verifications, analog performance
  - Analog performance crucial , floor plan (power distribution, grounding) done AoT
  - Tests at system level will be done

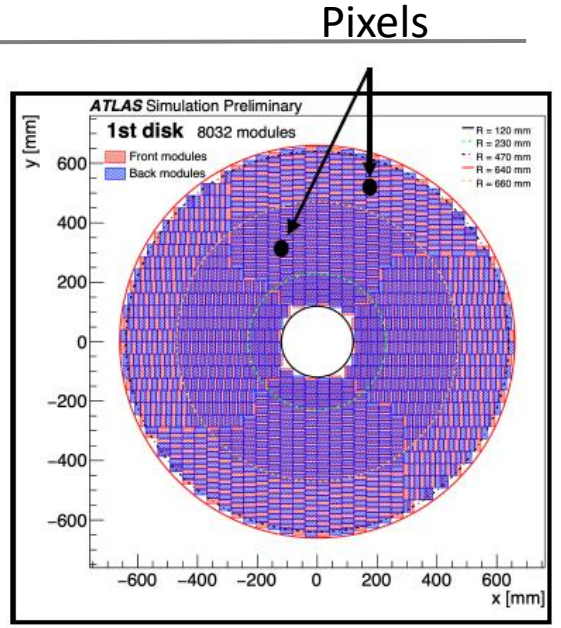


BACK UP : TOA calibration

Goal: measure the same hit time for tracks from the same interaction

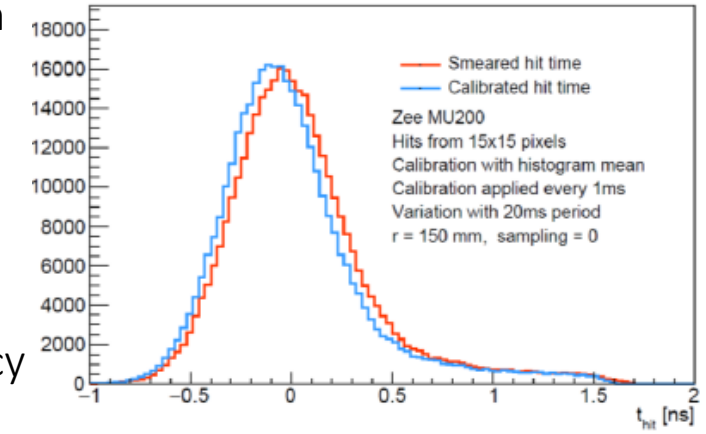
⇒ Need to correct various effects :

hit time = TOA_t0 = t0_static_ASIC + t0_static_online + t0_dynamic_offline



- t0 dispersion inside one ASIC: t0_static_ASIC
  - Due to ck skew between channels, static dispersion. Offline correction using ASIC internal calibration pulser to have **t0_static_ASIC** better than 5 ps

- t0 dispersion between ASICs: **t0_static_online** and **t0_dynamic_offline**
  - Due to TOF (η, ϕ, flex cable length), static dispersion. Online correction using each ASIC phase shifter to adjust the TOA window and so to get **t0_static_online** within ~ 100 ps.



  - Due to dynamic variations (drift of 40 MHz clock-RF, temperature …). Offline correction using minimum bias physics events to re-adjust each ASIC t0 and so to have **t0_dynamic_offline** within the needed accuracy of 10 ps (average of hits done over different integration windows)