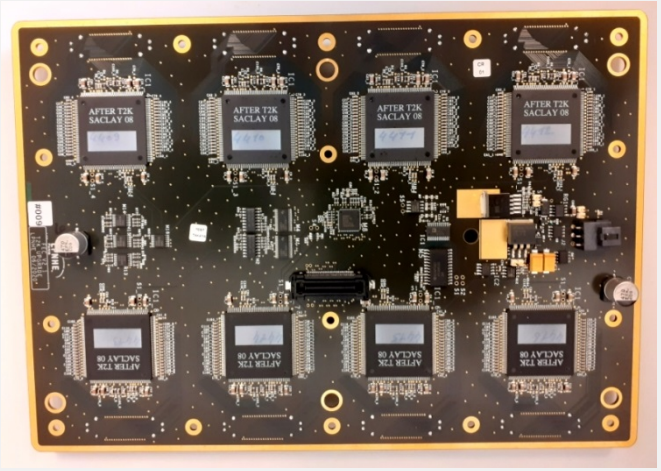
HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

Front End Card - **FEC** / T2K Phase2



LPNHE electronics staff : *Eric Pierre*
François Toussenel
Jean-Marc Parraud

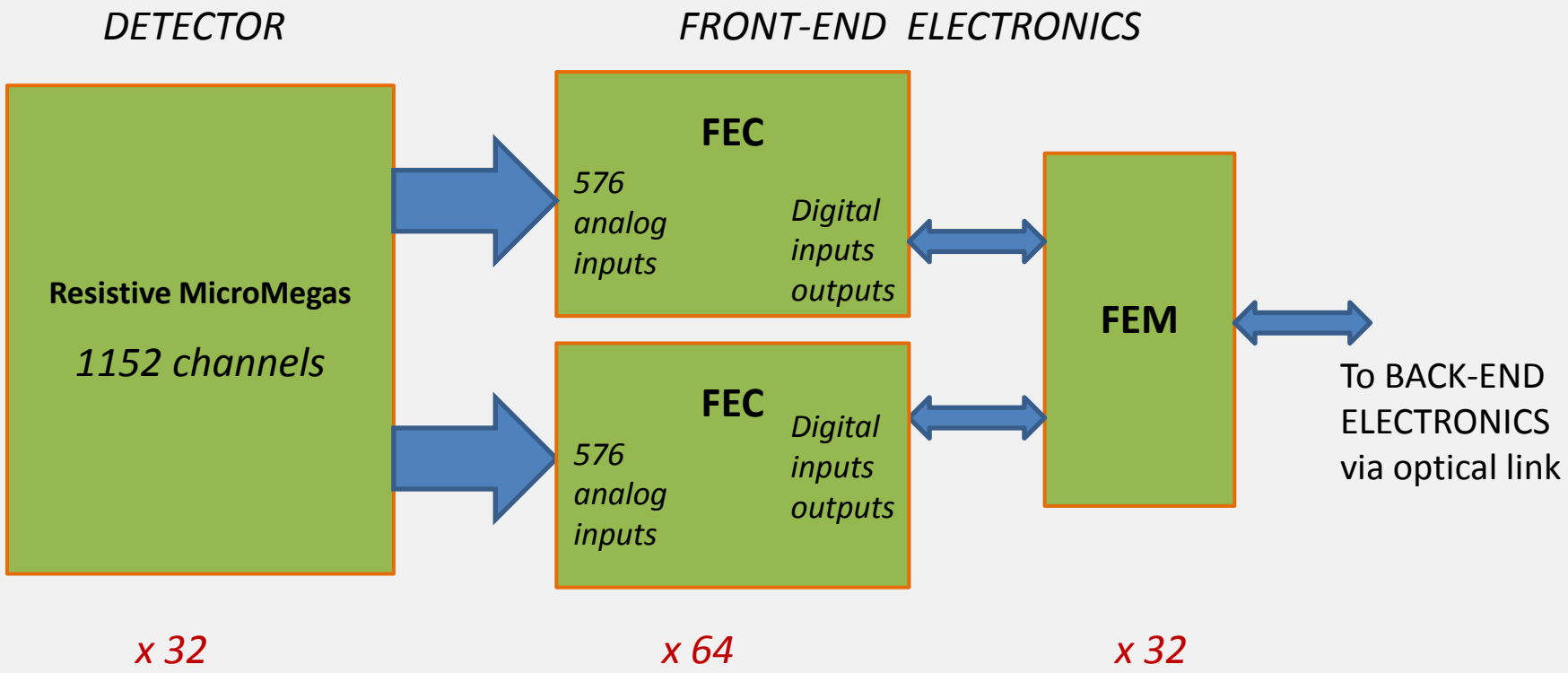
LPNHE scientist Manager : *Boris Popov*

Acknowledgements to *Denis Calvet* and all the *IRFU T2K team members* for their collaboration

HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

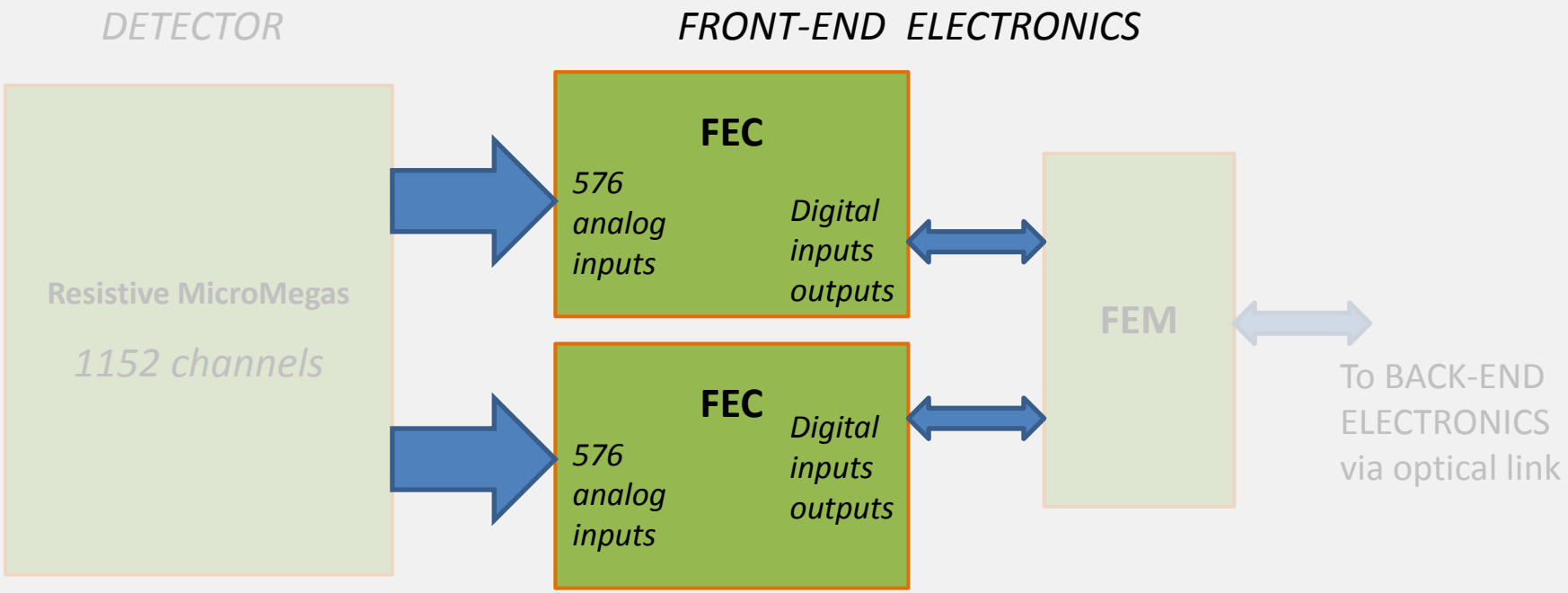
Preliminary



HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

Preliminary



⇩ *64 x FEC needed for on-site integration + spares*

LPNHE contribution

→ Production of **84 cards**: 12 x pre-prod cards
72 x prod cards

HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

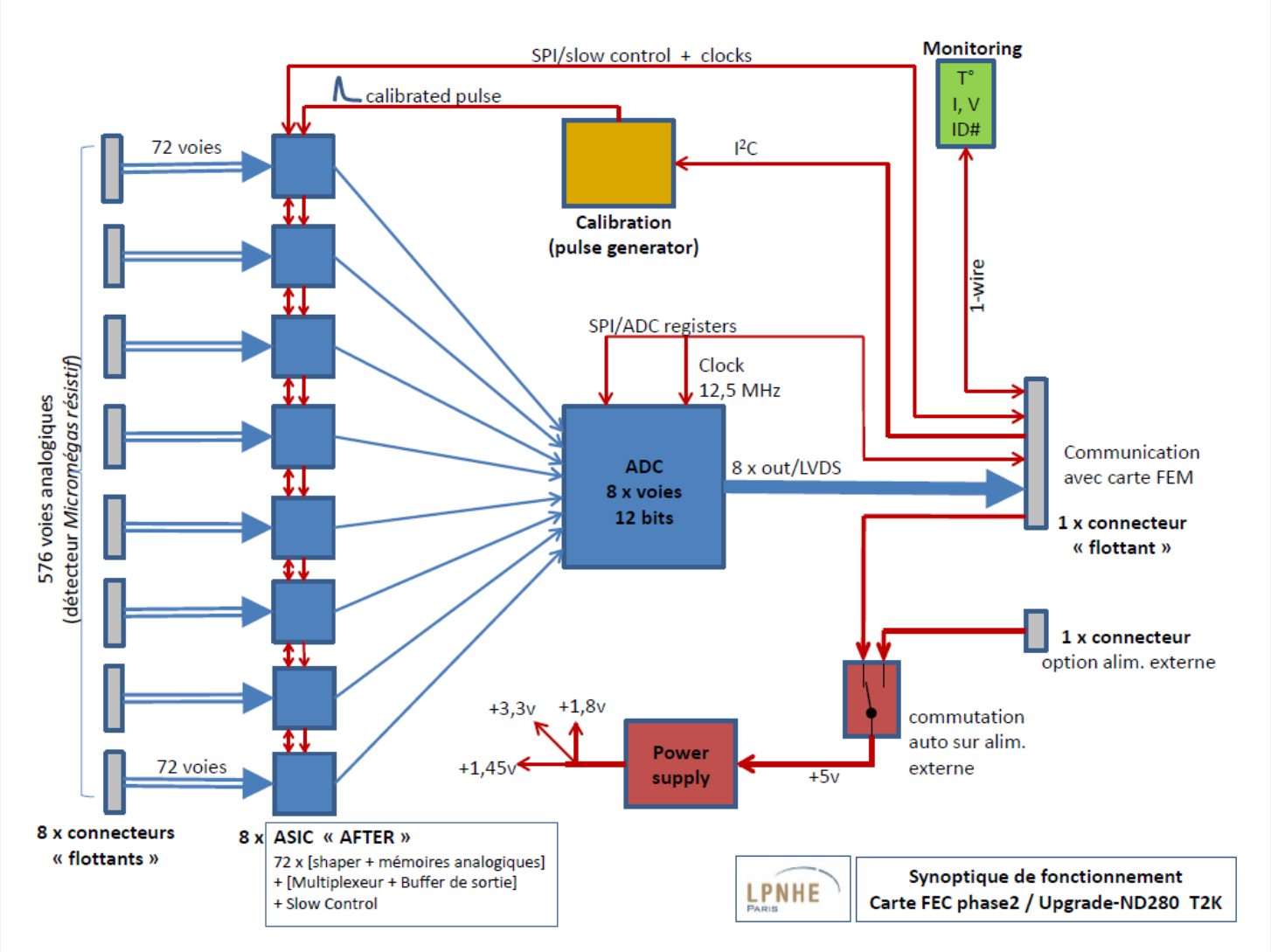
FEC / Phase2 :

Based on FEC/Phase1 that works fine for more than 10 years at T2K-Tokai site.

Use of the **same ASIC** (→ « **After** » / IRFU) for the read out and processing of analog signals coming from the detector.
Qty=8 (qty=4 in Phase1)

Use of an **8 channel ADC** (**AD9637-40**), instead of a 4 channel ADC.

The **global architecture remains the same** as it was in Phase1.



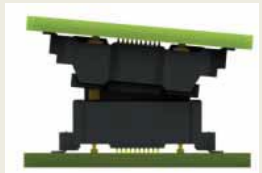
HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

How did it go till now :

- *December 2018* : **1st FEC mock-up** *without active components*
- *March 2019* : **2nd FEC mock-up** " " "
  - ⇨ These mock-ups allowed the validation of **floating connectors** intended for connecting signals : **MicroMegas detector ←→ FEC** (8 connectors)
    FEM ←→ FEC (1 connector)

HIROSE FX23 series
80 contacts
+ 4 power contacts



- *October 2019* : Design of the **FEC prototype schematics**, ***including all final functionnalities***

- *February 2020* : **FEC prototype manufacturing**
  February to June 2020 : Tests at IRFU with FEM prototype and acquisition system
  worked fine *after few fixes (2 wrong footprints, 1 missing connection on eFuse)*

- *August 2020* : **12 x pre-prod FEC manufacturing**, ***few changes*** *versus* ***prototype*** *mentioned above*
  - ⇨ September 2020 : 4 x tested at IRFU with pre-prod FEM and acquisition system
    2 x tested at Warsaw with their new testbench
    work fine / now waiting for production, qty = 72

HA-TPC front-end electronics PRR

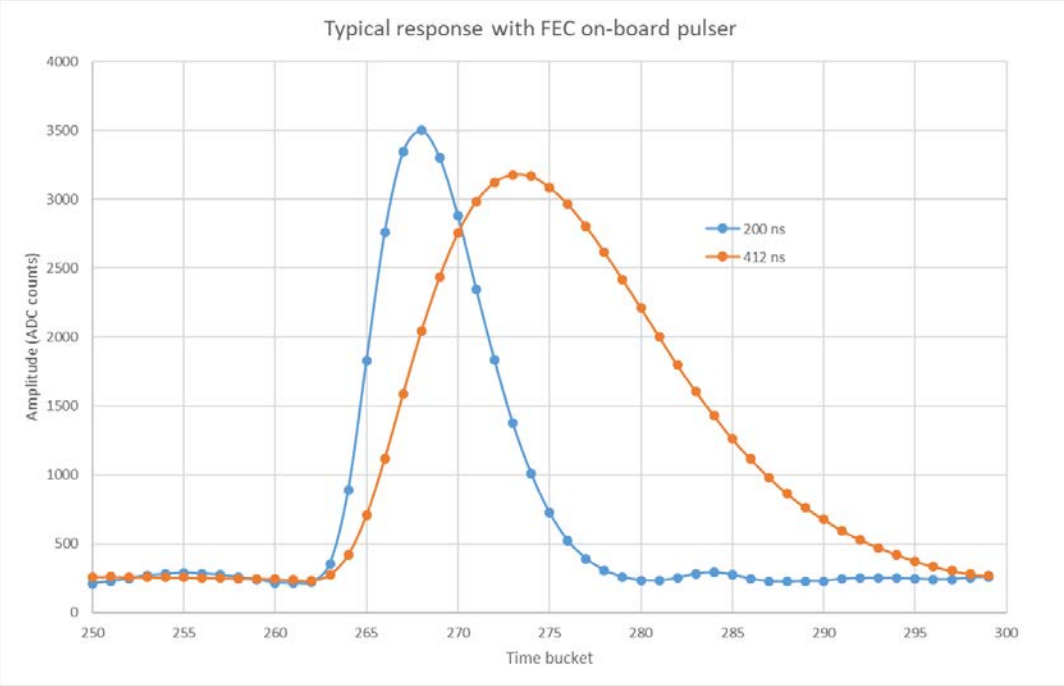
⇨ FEC 2020/10/29

Tests made on FEC prototypes at IRFU → Thanks to Denis Calvet !

→ *Power consumption measurement : ≈ 1,5 A / board*

→ *Calibration pulse response measurements*

2 pulse widths injected :
- *> 200 ns*
- *> 412 ns*



FEC-Proto-V1 n°05

HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

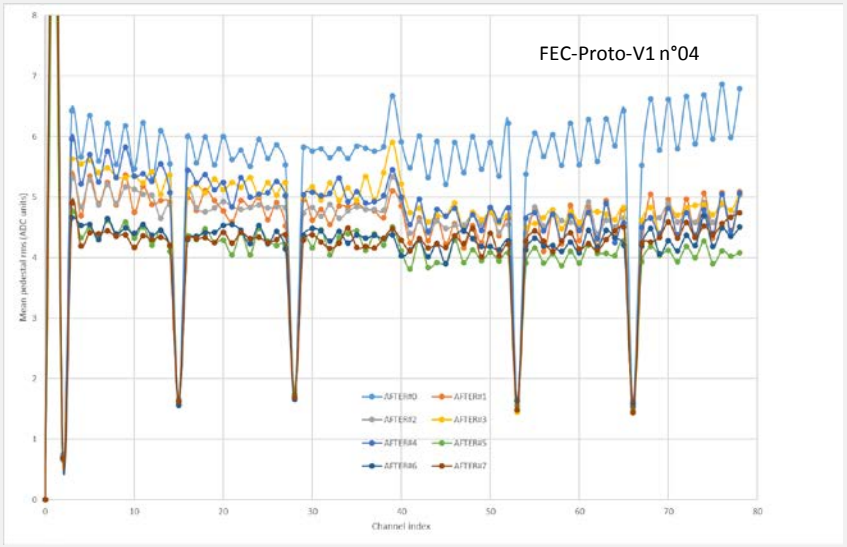
Tests made on FEC prototypes at IRFU

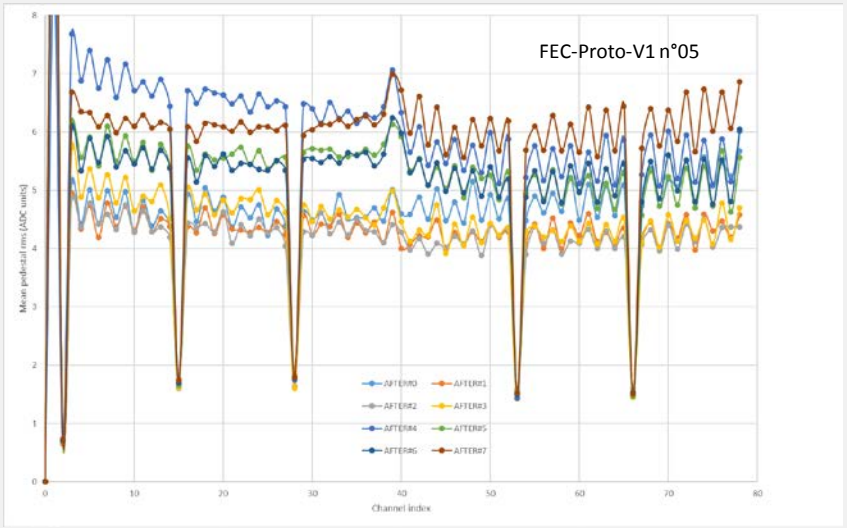
→ *Pedestals measurement*

> without shielding
> inputs not connected

! AFTER ASIC channels # 0, 1, 2, 15, 28, 53, 66 are NOT data channels

(see document "ASIC After datasheet", P. Baron and E. Delagnes).





HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

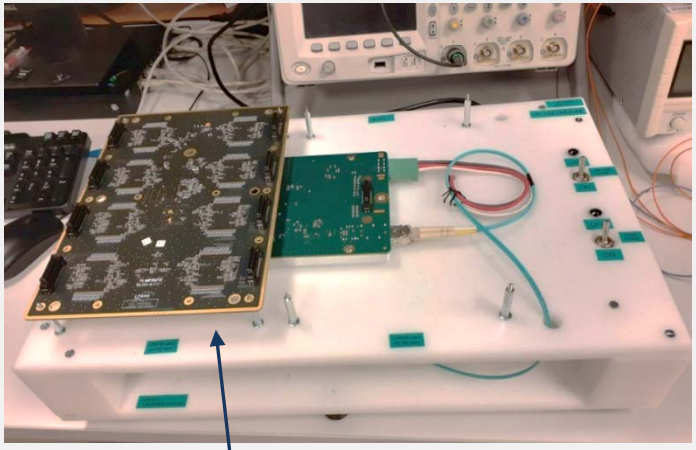
Test Bench intended
for FEC production

This testbench has been developed by our colleagues of Warsaw University of Technology, and *delivered to LPNHE one week ago.*

→ *Many thanks to our Warsaw colleagues for their good job.*

This testbench, including *hardware* and *software*, has been **successfully turned on at LPNHE**.
A few FEC tests have been performed.

>> In order to test the forthcoming FEC, this testbench will be installed at the manufacturer site (*Ouestronic-Rennes*).



FEC in test

HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

Test Bench intended for FEC production

« Passed » example
FEC 007 test report / page #1

Fec test report:
Date: 2020-10-26 16:01:30
Tester name: Diego

Test#1 Monitoring values — Passed

0	FEC label	007	OK
1	FEC DC2438 ID	e30000024da8fa26	OK
2	FEC_T (to 35°C)	29.469	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	1.396	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers: Passed
Test#3 Pedestal run: Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns — Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run — Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2974	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3069	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2966	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3078	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3029	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3045	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3025	OK

FEC test final result: Passed

« Failed » example
FEC 009 test report / page #1

Fec test report:
Date: 2020-10-26 16:13:43
Tester name: Diego

Test#1 Monitoring values — Failed

0	FEC label	009	OK
1	FEC DC2438 ID	6c0000024dc35c26	OK
2	FEC_T (to 35°C)	25.156	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.1A to 1.5A)	1.401	OK
5	FEC_Vad (1.9V to 2.0V)	1.330	FAIL

Test#2 Slow control registers: Passed
Test#3 Pedestal run: Passed

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns — Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run — Failed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 69	FAIL
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 64	FAIL
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 72	FAIL
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 63	FAIL
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 74	FAIL
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 66	FAIL
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 71	FAIL
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 70	FAIL

FEC test final result: Failed

Range of acceptance may need to be revised

SUMMARY of the first tests already done (qty : 8)

FEC #	*Result*	*Comments*
002	*Passed*	*Tests made by Andrzej at Warsaw*
003	*Passed*	
007	*Passed*	
008	*Passed*	
009	*Failed*	*Faulty **calibration pulse** → To be solved*
010	*Passed*	
011	*Failed*	*I monitoring=1,501A **NOT a failure** (max = 1,5A)*
012	*Failed*	*too high **pedestals** on 5 channels / same Asic → needs more investigations*

HA-TPC front-end electronics PRR

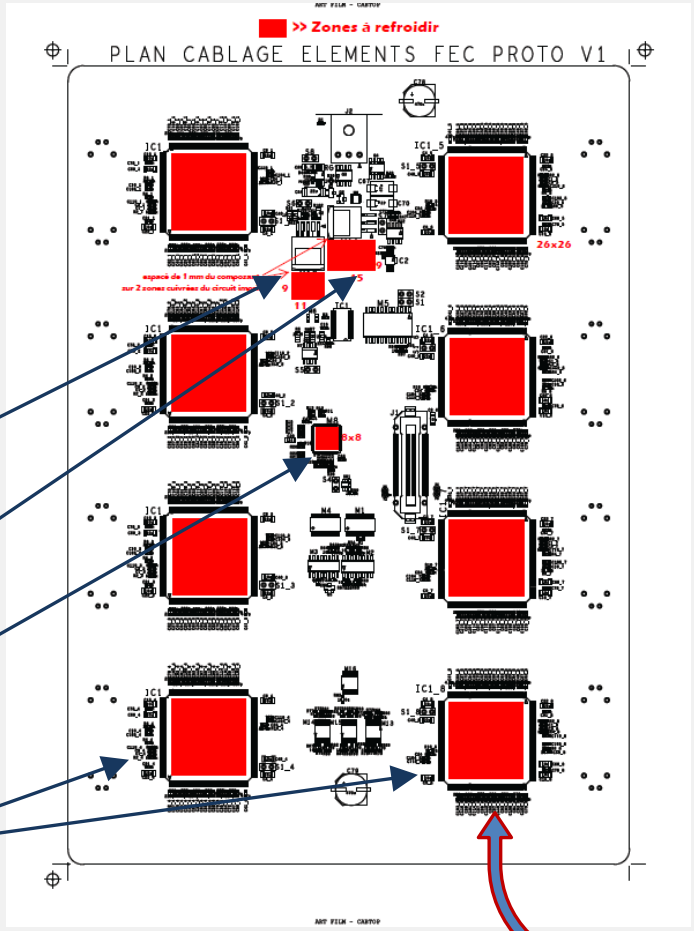
⇨ FEC 2020/10/29

FEC cooling :

In order to keep a temperature of 25~30°C , cooling is required.

Components requiring cooling are :

- Regulator *MIC29502*
  P≈2,5W
- Regulator *LM1086*
  P≈0,7W
- ADC *AD9637*
  P≈0,5W
- Asic *AFTER (x8)*
  P≈0,5W each



Shielding/cooling plate

Thanks to the IRFU mechanical team !

Silicone pads

HA-TPC front-end electronics PRR

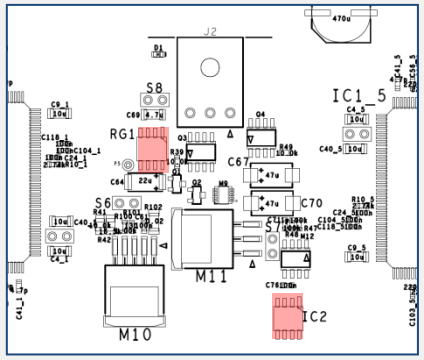
⇨ FEC 2020/10/29

Improvements made on FEC

Following the prototype tests :

> Change of improper **footprints** → IC2 / DS2438 (1-wire monitoring device)
RG1 / LP2951 (linear regulator / +1,45v)

> Connection GND ←→ Pad M9 / STEF05 (eFuse) that was missing !



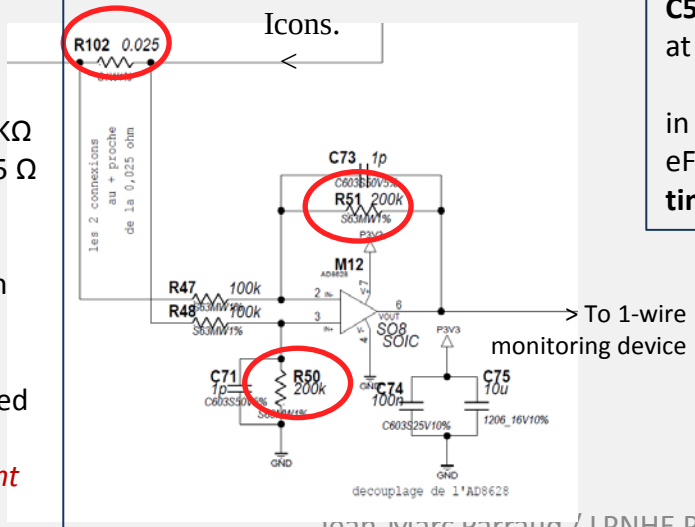
Following the pre-prod FEC tests :

Current consumption Monitoring :

Value adjustment of :
R50/R51 : 499 KΩ → 200 KΩ
R102 : 0,02 Ω → 0,025 Ω

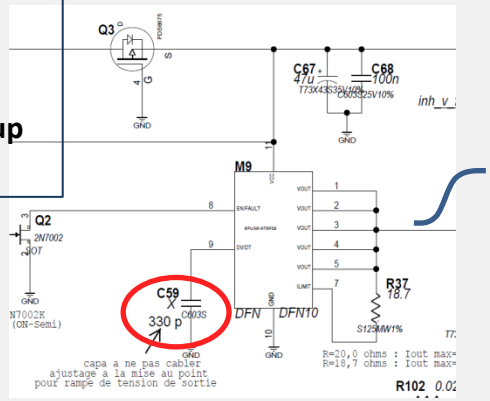
in order to keep an ideal common mode voltage on M12 inputs

… But op-amp gain is divised per 2
→ *To be taken into account in the acquisition part*



C59 : value adjustment at 330 pF

in order to set the eFuse **output ramp-up time** at ~10 ms



HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

Topics to keep an eye on

Tests in magnetic field :

Because of *Covid-19 pandemic*, beam tests could not take place in October 2020 (DESY) as planned. Thus, pre-prod FEC could not have been tested in a 0,2 T magnetic field.

→ There is an alternative to do this magnetic test at *IJCLab-Orsay*. Date to be determined. (? Covid ?)
→ We are rather confident to the issue : *FEC/Phase1* was insensitive to this environment.
FEC/Phase2 : no magnetic component, only 1 inductor-22 nH for the ADC/1,8v filtering.
This inductor is not mandatory and has been placed *as a precaution.*
>> It can safely be *replaced by a 0 Ω* resistor if necessary.

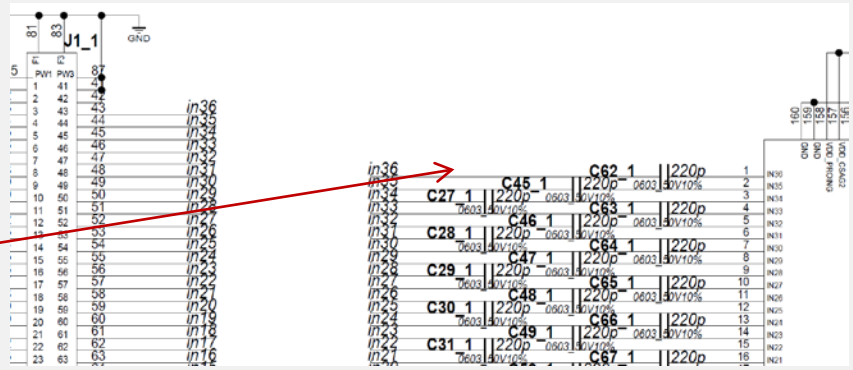
Analog inputs are not voltage-referenced :

Input pads towards AFTER Asic are not referenced, and may *eventually* be charged at a potential greater than the one accepted by the Asic input.

→ Existing leakage currents on PCB must eliminate this possibility
→ No damage has never been observed till now

>> In series capacitors may be replaced by *1 kv* ones

>> As a last resort, a *100 MΩ to GND* can be added at each input pad (qty=576 !)



HA-TPC front-end electronics PRR

⇨ FEC 2020/10/29

Planned schedule : *(before Covid-19 containment annoucement)*

FEC Boards

- *November 2020* : **Launch of FEC prod** (qty=72) to external company (*Ouestronic*)
- *End of February 2021* : 1st batch of **16 FEC** tested and delivered
  - ⇨ *These 16 boards are intended to equip the first ½ HA-TPC planned for March 2021*
- *April 2021* : Last batch of **56 FEC** tested and delivered

FEC Cooling plates

- *November 2020* : **8 plates** manufactured at LPNHE workshop
- *December 2020* : **8 plates** manufactured by external company (*Chanteloup Associés*)
  - ⇨ *These 16 cooling plates are intended to equip the first ½ HA-TPC planned for March 2021*
- *April 2021 :* **64 plates** manufactured by external company (*Chanteloup Associés*)

Risks of delay on the schedule :

- ***COVID-19 !*** Delay on our work at LPNHE in case of sanitary containment

  Delay on FEC production →  ***Ouestronic*** *was open during previous containment, … maybe the same for next one*

  Delay on cooling plates production. *No information about* ***Chanteloup Associés*** *in that case*