

Fec test report:

Date: 2020-10-26 12:56:54

Tester name: Diego

Test#1 Monitoring values

Passed

0	FEC label	010	OK
1	FEC DC2438 ID	5d0000024d9c7026	OK
2	FEC_T (to 35°C)	27.625	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	1.482	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3001	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3122	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3122	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3114	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3095	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3028	OK

FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdc(2) Fem(00) FEC_T: 27.625 degC
2	fe 0 moni V 1	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 1	0	0 Tdc(2) Fem(00) FEC_I: 1.482 A
8	fe 0 moni S 1	0	0 Tdc(2) Fem(00) FEC_Serial: 5d0000024d9c7026

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x2088000 (34111488) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0xb0b 0xb0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0xc0c 0xc0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0xd0d 0xd0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdc(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdc(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdc(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdc(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdc(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdc(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdc(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdc(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xefff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xefff0000
168	fe 0 after 12 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
189	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.3	1 r	511.0	0.0	1 r	491.4	10.9	1 r	511.0	0.0	1 r	511.0	0.0
2 r	321.9	0.7	2 r	284.7	0.7	2 r	273.8	0.7	2 r	265.1	0.7	2 r	307.3	0.7	2 r	309.2	0.7	2 r	268.2	0.7	2 r	334.2	0.7
3	306.2	4.7	3	207.5	4.7	3	259.4	4.8	3	229.0	5.3	3	271.1	4.7	3	210.3	4.3	3	255.2	4.5	3	335.9	4.7
4	198.6	4.6	4	286.4	4.1	4	207.4	4.2	4	306.9	4.9	4	317.7	4.4	4	275.1	4.0	4	177.0	4.4	4	272.9	4.2
5	248.2	4.6	5	212.7	4.6	5	224.9	4.5	5	241.1	5.6	5	340.1	4.7	5	282.4	4.4	5	271.1	4.2	5	264.4	4.3
6	123.7	4.3	6	244.3	4.3	6	274.9	4.3	6	195.4	4.6	6	334.4	4.6	6	288.9	4.2	6	166.2	4.5	6	182.8	4.2
7	220.5	4.4	7	190.5	4.5	7	261.6	4.7	7	210.6	5.4	7	220.0	4.6	7	267.4	4.2	7	230.0	4.2	7	309.4	4.3
8	160.2	4.3	8	155.5	4.3	8	151.0	4.5	8	197.3	4.8	8	316.5	4.7	8	268.8	4.2	8	253.7	4.5	8	234.7	4.0
9	130.4	4.7	9	209.9	4.4	9	243.0	4.7	9	281.7	5.2	9	272.1	4.5	9	204.0	4.4	9	184.0	4.2	9	282.3	3.9
10	181.6	4.4	10	280.3	4.4	10	197.6	4.6	10	287.5	4.7	10	311.6	4.4	10	253.0	4.2	10	210.2	4.2	10	312.8	4.2
11	210.6	4.3	11	178.3	4.6	11	204.2	4.7	11	182.6	5.0	11	280.9	4.6	11	174.3	4.3	11	218.5	4.3	11	233.8	4.2
12	260.4	4.4	12	203.7	4.3	12	269.6	4.4	12	195.8	4.7	12	351.3	4.7	12	245.8	4.3	12	192.8	4.0	12	259.0	3.9
13	177.9	4.3	13	192.4	4.3	13	169.3	4.5	13	222.1	4.9	13	217.1	4.4	13	220.8	4.4	13	104.9	4.3	13	261.0	4.0
14	139.9	4.3	14	121.5	4.5	14	188.8	4.3	14	185.9	4.6	14	257.5	4.3	14	292.1	4.2	14	230.4	4.2	14	252.1	4.7
15 f	258.7	1.7	15 f	115.7	1.7	15 f	130.8	1.8	15 f	126.1	1.7	15 f	255.8	1.6	15 f	174.2	1.6	15 f	170.7	1.6	15 f	279.3	1.6
16	181.9	4.3	16	214.9	4.3	16	194.2	4.5	16	203.9	4.9	16	267.0	4.2	16	158.8	4.1	16	211.6	4.4	16	285.7	4.0
17	216.0	4.3	17	236.7	4.5	17	245.6	4.2	17	196.7	4.5	17	208.2	4.4	17	362.4	4.1	17	224.3	4.2	17	302.2	4.1
18	166.7	4.4	18	212.4	4.2	18	198.6	4.5	18	297.0	4.7	18	286.4	4.4	18	342.8	4.0	18	235.9	4.3	18	262.1	4.1
19	161.6	4.6	19	155.6	4.5	19	269.6	4.5	19	212.3	4.8	19	241.8	4.4	19	241.9	4.2	19	260.9	4.1	19	280.1	4.2
20	218.4	4.3	20	281.4	4.3	20	165.6	4.5	20	232.5	4.8	20	261.8	4.5	20	93.7	4.3	20	203.8	4.4	20	203.0	4.0
21	257.0	4.2	21	206.2	4.3	21	252.0	4.4	21	102.9	4.6	21	297.4	4.6	21	283.2	4.3	21	235.2	4.1	21	203.0	4.0
22	249.2	4.3	22	196.8	4.5	22	235.1	4.7	22	201.2	5.0	22	247.8	4.5	22	248.0	4.1	22	166.2	4.2	22	266.6	4.3
23	248.6	4.3	23	222.8	4.2	23	296.6	4.3	23	198.1	4.5	23	235.7	4.1	23	265.9	4.1	23	191.6	4.1	23	285.6	4.1
24	202.5	4.1	24	179.0	4.5	24	213.9	4.4	24	233.1	4.8	24	274.9	4.5	24	262.1	4.1	24	248.0	4.3	24	170.8	4.2
25	125.9	4.4	25	159.3	4.3	25	264.7	4.3	25	152.7	4.7	25	265.7	4.2	25	297.2	4.1	25	190.3	4.1	25	287.0	4.0
26	271.6	4.4	26	207.4	4.2	26	240.2	4.3	26	227.4	4.9	26	327.4	4.5	26	254.7	4.1	26	203.7	4.2	26	187.9	4.1
27	226.0	4.3	27	244.8	4.2	27	216.3	4.4	27	298.3	4.7	27	226.6	4.3	27	205.4	4.3	27	189.1	4.1	27	233.6	4.0
28 f	277.1	1.7	28 f	249.0	1.8	28 f	149.1	1.9	28 f	205.9	1.7	28 f	289.8	1.8	28 f	146.4	1.9	28 f	201.3	1.7	28 f	210.3	1.7
29	205.3	4.4	29	122.1	4.4	29	237.4	4.1	29	226.9	4.6	29	269.8	4.3	29	283.5	4.2	29	231.6	4.3	29	327.1	4.1
30	177.9	4.2	30	314.3	4.4	30	244.2	4.2	30	233.3	4.5	30	215.5	4.3	30	227.8	4.0	30	254.7	4.0	30	266.6	4.1
31	186.7	4.1	31	181.0	4.3	31	136.0	4.4	31	225.7	4.8	31	241.0	4.2	31	265.3	4.2	31	276.2	4.4	31	215.0	4.7
32	173.0	4.2	32	190.6	4.3	32	280.5	4.3	32	202.2	4.3	32	250.6	4.3	32	169.9	4.2	32	140.3	4.0	32	241.1	4.2
33	201.6	4.3	33	154.8	4.3	33	318.3	4.8	33	221.4	4.9	33	240.5	4.3	33	251.1	4.2	33	198.8	4.2	33	263.4	4.0
34	250.5	4.1	34	227.3	4.0	34	213.4	4.2	34	206.8	4.9	34	244.5	4.3	34	268.6	4.0	34	233.4	4.2	34	171.3	4.1
35	254.5	4.2	35	132.4	4.1	35	228.1	4.5	35	230.0	4.5	35	256.9	4.4	35	357.3	4.2	35	165.3	4.3	35	238.8	4.1
36	232.1	4.2	36	231.0	4.3	36	209.6	4.3	36	292.1	4.6	36	305.9	4.2	36	216.4	4.1	36	218.6	4.2	36	248.0	3.9
37	263.7	4.4	37	117.1	4.6	37	146.9	4.5	37	159.8	4.7	37	304.0	4.2	37	253.4	4.2	37	156.0	4.5	37	321.6	4.1
38	206.5	4.2	38	119.6	4.1	38	164.3	4.1	38	243.8	4.8	38	288.5	4.2	38	299.5	4.2	38	317.9	4.3	38	266.1	4.0
39	283.3	4.4	39	237.9	4.3	39	213.6	5.1	39	208.8	4.9	39	213.8	4.6	39	174.2	4.4	39	179.0	4.4	39	161.6	4.1
40	229.8	4.1	40	204.5	4.2	40	173.1	4.2	40	210.5	4.3	40	245.2	4.3	40	244.3	4.0	40	326.4	4.2	40	217.1	4.1
41	224.4	4.0	41	255.4	4.0	41	153.0	4.0	41	161.4	4.2	41	228.1	4.2	41	296.6	3.8	41	170.1	3.9	41	277.6	3.8
42	242.4	3.9	42	137.6	4.1	42	173.3	4.2	42	230.5	4.5	42	282.3	4.2	42	235.2	4.0	42	175.9	4.2	42	230.8	4.2
43	211.5	3.9	43	243.9	4.0	43	266.0	4.0	43	181.0	4.2	43	169.2	4.0	43	317.7	4.0	43	184.6	3.8	43	257.1	3.8
44	203.3	4.2	44	195.3	3.8	44	255.5	4.0	44	252.7	4.1	44	267.0	3.9	44	207.5	3.9	44	244.3	4.1	44	243.2	4.0
45	263.1	4.0	45	246.6	3.9	45	200.9	4.2	45	286.8	4.1	45	248.3	4.1	45	257.3	3.9	45	212.5	4.1	45	246.4	4.2
46	229.2	4.0	46	143.6	4.0	46	231.0	4.1	46	194.9	4.3	46	224.2	4.1	46	174.8	4.0	46	237.3	4.0	46	243.5	3.9
47	204.9	3.8	47	209.6	3.6	47	172.4	4.0	47	212.3	4.2	47	251.9	3.9	47	354.9	4.0	47	213.3	3.9	47	308.7	4.1
48	230.8	4.1	48	163.0	4.1	48	201.8	4.0	48	173.2	4.5	48	210.0	4.0	48	191.1	4.2	48	213.8	4.1	48	245.6	4.0
49	203.0	4.1	49	191.1	4.2	49	237.4	4.0	49	189.0	4.1	49	282.9	4.0	49	198.1	3.8	49	220.6	3.9	49	266.1	4.1
50	258.1	4.2	50	195.0	3.8	50	243.2	4.2	50	216.5	4.4	50	302.6	4.0	50	250.1	3.9	50	152.3	4.0	50	354.8	4.3
51	238.7	4.0	51	250.0	3.9	51	162.9	4.0	51	267.3	4.0	51	158.1	4.1	51	199.0	3.9	51	213.8	4.0	51	325.4	4.1
52	251.2	3.9	52	151.6	4.4	52	245.0	4.3	52	251.9	4.2	52	296.6	4.0	52	256.9	3.9	52	154.9	4.0	52	308.2	4.3
53 f	219.7	1.6	53 f	185.6	1.6	53 f	238.6	1.6	53 f	199.1	1.6	53 f	296.1	1.6	53 f	215.7	1.4	53 f	211.7	1.4	53 f	258.5	1.4
54	254.1	4.0	54	167.3	4.2	54	207.1	4.1	54	211.1	4.2	54	296.7	4.3	54	320.7	4.0	54	235.2	3.9	54	225.8	4.0
55	123.0	3.9	55	284.4	4.1	55	237.7	4.1	55	170.8	4.3	55	296.1	4.0	55	252.4	4.0	55	189.2	4.1	55	308.9	4.1
56	242.1	3.9	56	190.7	4.0	56	180.2	4.1	56	317.7	4.1	56	256.8	4.3	56	237.4	3.9	56	224.5	3.8	56	298.2	4.2
57	297.6	4.2	57	173.4	4.0	57	206.0	4.1	57	218.5	4.2	57	191.2	4.2	57	247.2	3.9	57	99.7	4.0	57	224.3	4.1
58	214.5	4.1	58	221.4	3.9	58	192.6	4.4	58	297.1	3.9	58	302.7										

Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	404.6	10.9	1 r	332.3	8.6	1 r	303.5	11.1	1 r	276.6	12.3	1 r	338.2	11.8	1 r	250.6	12.2	1 r	322.6	9.3	1 r	481.9	7.0
2 r	249.7	0.7	2 r	249.8	0.7	2 r	249.8	0.7	2 r	250.0	0.7	2 r	250.3	0.7	2 r	250.1	0.7	2 r	250.2	0.7	2 r	250.0	0.7
3	248.2	4.5	3	248.8	4.6	3	251.1	5.0	3	250.6	5.9	3	248.8	4.5	3	249.8	4.5	3	249.5	4.5	3	250.4	4.4
4	251.3	4.2	4	249.3	4.5	4	249.6	4.4	4	249.2	5.1	4	250.3	4.4	4	249.7	4.4	4	250.1	4.4	4	251.4	4.2
5	248.7	4.7	5	249.3	4.5	5	251.4	4.7	5	248.7	5.6	5	250.8	4.7	5	250.7	4.4	5	251.1	4.5	5	251.6	4.3
6	249.7	4.3	6	251.6	4.2	6	249.9	4.5	6	251.0	5.0	6	250.7	4.5	6	249.8	4.4	6	249.8	4.3	6	248.6	4.5
7	249.8	4.4	7	250.2	4.7	7	249.1	4.9	7	249.8	5.6	7	249.5	4.7	7	250.1	4.2	7	249.5	4.6	7	249.1	4.2
8	248.6	4.4	8	249.5	4.4	8	249.7	4.2	8	249.3	4.8	8	249.8	4.4	8	248.4	4.2	8	250.1	4.3	8	249.7	4.1
9	248.9	4.5	9	251.0	4.3	9	249.1	4.7	9	249.0	5.5	9	249.1	4.5	9	248.4	4.2	9	251.0	4.2	9	251.4	4.5
10	250.8	4.6	10	250.9	4.4	10	250.4	4.4	10	248.5	5.1	10	249.5	4.3	10	250.0	4.1	10	250.1	4.2	10	248.5	4.1
11	250.1	4.4	11	251.2	4.3	11	249.8	4.7	11	249.1	4.9	11	251.3	4.5	11	251.0	4.5	11	250.6	4.4	11	249.0	4.2
12	248.7	4.0	12	249.9	4.2	12	249.6	4.5	12	249.8	4.9	12	251.1	4.4	12	249.7	4.2	12	250.2	4.3	12	250.0	4.2
13	249.0	4.3	13	251.3	4.5	13	249.6	4.5	13	250.7	5.1	13	249.5	4.7	13	249.7	4.3	13	250.6	4.3	13	249.1	4.2
14	248.9	4.2	14	251.3	4.7	14	247.8	4.5	14	249.2	4.6	14	249.6	4.3	14	249.8	4.2	14	250.1	4.1	14	248.7	4.3
15 f	249.2	1.6	15 f	249.6	1.7	15 f	249.5	1.8	15 f	249.7	1.7	15 f	249.3	1.7	15 f	250.2	1.7	15 f	250.2	1.7	15 f	250.3	1.6
16	249.6	4.3	16	249.4	4.4	16	249.2	4.3	16	250.0	5.0	16	249.7	4.5	16	249.9	4.2	16	249.1	4.2	16	249.1	4.1
17	250.3	4.4	17	249.2	4.1	17	250.6	4.4	17	249.8	4.8	17	250.3	4.2	17	252.4	4.1	17	250.8	4.0	17	249.3	4.2
18	248.2	4.2	18	251.1	4.3	18	248.2	4.4	18	248.9	5.0	18	249.6	4.3	18	248.8	4.2	18	250.4	4.2	18	250.2	4.2
19	249.9	4.4	19	249.9	4.2	19	250.3	4.5	19	249.4	4.7	19	251.9	4.5	19	249.8	4.2	19	251.1	4.1	19	249.5	4.0
20	250.3	4.2	20	250.5	4.4	20	250.0	4.5	20	250.2	5.0	20	250.1	4.5	20	249.9	4.5	20	249.5	4.2	20	249.1	4.3
21	250.2	4.4	21	249.5	4.7	21	247.4	4.4	21	250.1	4.6	21	249.4	4.3	21	251.0	4.1	21	250.4	4.1	21	250.4	4.1
22	250.2	4.3	22	249.6	4.3	22	250.3	4.4	22	249.9	5.0	22	249.8	4.5	22	249.2	4.1	22	249.9	4.1	22	249.8	4.3
23	249.7	4.5	23	249.2	4.3	23	248.8	4.3	23	250.6	4.7	23	248.3	4.3	23	249.9	4.3	23	250.1	4.1	23	249.3	4.0
24	249.5	4.5	24	250.1	4.2	24	249.0	4.5	24	249.9	4.9	24	248.8	4.6	24	251.2	4.2	24	249.8	4.1	24	250.1	4.3
25	248.7	4.3	25	250.2	4.0	25	249.3	4.3	25	250.2	4.6	25	248.9	4.8	25	249.5	4.3	25	251.2	4.1	25	249.8	3.8
26	248.0	4.3	26	250.4	4.3	26	249.4	4.6	26	248.8	4.8	26	250.2	4.3	26	248.4	4.1	26	248.9	4.2	26	249.3	4.3
27	249.7	4.2	27	248.6	4.1	27	251.3	4.2	27	250.1	4.6	27	248.7	4.3	27	250.3	4.1	27	248.8	4.1	27	249.6	4.0
28 f	250.3	1.6	28 f	249.8	1.8	28 f	249.6	1.7	28 f	249.6	1.8	28 f	249.6	1.7	28 f	249.9	1.9	28 f	250.3	1.7	28 f	250.7	1.6
29	249.8	4.2	29	250.4	4.2	29	250.0	4.4	29	249.2	5.0	29	250.7	4.3	29	251.7	4.3	29	249.6	4.1	29	250.4	4.2
30	249.6	4.2	30	249.0	4.2	30	250.3	4.3	30	251.3	4.9	30	250.0	4.3	30	248.5	4.2	30	249.2	4.2	30	249.7	4.0
31	250.2	4.3	31	249.2	4.2	31	250.1	4.4	31	249.0	4.6	31	249.8	4.4	31	248.1	4.0	31	250.1	4.3	31	249.4	4.2
32	250.7	4.2	32	250.2	4.3	32	250.2	4.3	32	250.2	4.6	32	250.0	4.2	32	249.5	4.0	32	249.4	4.3	32	249.6	4.1
33	248.5	4.1	33	250.4	4.3	33	248.8	4.4	33	249.3	4.9	33	250.8	4.6	33	250.8	4.0	33	250.5	4.3	33	249.8	4.3
34	250.4	4.5	34	250.4	4.3	34	251.9	4.2	34	249.9	4.5	34	251.1	4.5	34	249.2	4.2	34	248.9	4.4	34	249.8	4.3
35	250.2	4.0	35	251.2	4.2	35	250.0	4.2	35	249.0	4.6	35	250.0	4.2	35	248.3	4.0	35	251.5	4.3	35	250.2	4.1
36	249.2	4.5	36	250.2	4.0	36	249.1	4.5	36	250.8	4.6	36	251.2	4.4	36	250.7	4.2	36	248.4	4.3	36	249.2	4.1
37	247.9	4.2	37	248.8	4.2	37	248.7	4.3	37	249.7	4.8	37	250.2	4.4	37	250.4	4.2	37	250.0	4.1	37	249.2	4.0
38	248.0	4.2	38	249.0	4.2	38	249.8	4.1	38	250.4	4.9	38	248.7	4.4	38	248.7	4.2	38	250.4	4.0	38	249.0	4.1
39	250.1	4.4	39	249.1	4.5	39	247.6	4.7	39	249.1	5.1	39	249.1	4.8	39	250.2	4.4	39	250.1	4.5	39	249.5	4.4
40	249.9	4.2	40	247.4	4.0	40	249.3	4.3	40	248.7	4.8	40	249.9	4.3	40	248.6	4.1	40	250.6	4.1	40	249.2	4.2
41	249.7	3.8	41	251.0	3.9	41	249.1	3.9	41	249.6	4.3	41	249.8	4.1	41	248.2	3.8	41	249.2	4.0	41	250.0	4.0
42	247.8	4.2	42	248.8	4.0	42	251.3	4.0	42	250.0	4.5	42	249.6	4.1	42	250.9	4.0	42	249.8	4.0	42	250.1	4.2
43	250.0	4.0	43	248.3	3.9	43	249.1	4.1	43	249.7	4.2	43	250.7	4.0	43	249.9	3.8	43	249.9	3.8	43	249.7	4.2
44	249.4	4.1	44	249.9	4.0	44	248.4	4.2	44	249.7	4.4	44	249.8	4.1	44	250.5	4.0	44	250.7	3.9	44	250.8	4.3
45	248.4	4.0	45	248.2	4.1	45	250.6	4.1	45	248.4	4.1	45	251.9	3.9	45	249.7	4.0	45	250.7	4.0	45	250.3	4.2
46	251.6	3.9	46	249.5	4.0	46	249.4	4.2	46	248.1	4.3	46	250.5	4.2	46	247.6	4.0	46	251.2	4.0	46	250.1	4.2
47	249.2	4.0	47	248.5	3.8	47	250.8	4.0	47	250.8	4.4	47	249.5	4.4	47	248.2	3.9	47	252.7	4.1	47	248.5	4.1
48	248.0	4.0	48	249.9	4.3	48	248.4	4.1	48	249.5	4.6	48	249.5	4.1	48	249.5	4.0	48	250.3	3.9	48	248.1	4.3
49	249.7	4.1	49	250.8	3.8	49	251.1	3.9	49	250.5	4.2	49	250.7	4.2	49	249.6	3.9	49	249.4	3.9	49	250.8	4.0
50	249.7	4.1	50	249.2	4.0	50	249.1	4.2	50	248.9	4.3	50	249.3	4.2	50	249.0	4.1	50	250.9	4.0	50	249.5	4.3
51	248.6	4.0	51	248.4	4.3	51	249.7	4.0	51	250.3	4.2	51	249.3	4.2	51	250.7	4.0	51	251.4	4.0	51	249.1	3.9
52	249.4	4.0	52	248.9	4.3	52	250.4	4.3	52	250.2	4.1	52	249.3	4.2	52	249.8	4.1	52	249.8	4.1	52	250.7	4.2
53 f	249.1	1.6	53 f	249.3	1.5	53 f	250.1	1.6	53 f	250.2	1.6	53 f	250.2	1.6	53 f	249.1	1.5	53 f	249.7	1.5	53 f	249.9	1.4
54	250.5	4.1	54	248.6	4.1	54	248.6	4.0	54	249.8	4.3	54	250.3	4.2	54	250.5	3.8	54	251.1	4.1	54	248.8	4.3
55	249.9	4.0	55	251.5	4.0	55	250.3	4.6	55	249.2	4.4	55	251.2	3.9	55	250.7	4.0	55	250.0	4.0	55	250.1	4.3
56	250.2	4.0	56	250.3	4.0	56	249.2	4.1	56	249.2	4.2	56	249.2	4.2	56	249.2	3.9	56	247.6	3.9	56	250.4	4.1
57	249.3	4.1	57	250.3	4.3	57	249.3	4.4	57	248.7	4.7	57	249.4	4.4	57	250.6	4.0	57	249.2	4.0	57	250.2	4.4
58	249.3	4.1	58	250.5	4.0	58	249.0	4.0	58	250.4													