

Fec test report:

Date: 2020-10-26 16:01:30

Tester name: Diego

Test#1 Monitoring values

Passed

0	FEC label	007	OK
1	FEC DC2438 ID	e30000024da8fa26	OK
2	FEC_T (to 35°C)	29.469	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	1.396	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2974	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3069	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2966	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3078	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3029	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3045	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3025	OK

FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdc(2) Fem(00) FEC_T: 29.469 degC
2	fe 0 moni V 1	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 1	0	0 Tdc(2) Fem(00) FEC_I: 1.396 A
8	fe 0 moni S 1	0	0 Tdc(2) Fem(00) FEC_Serial: e30000024da8fa26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12088000 (302546944) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0b0b 0x0b0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0c0c 0x0c0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0d0d 0x0d0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdc(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdc(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdc(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdc(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdc(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdc(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdc(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdc(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 TdcM(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 TdcM(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 TdcM(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xefff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xefff0000
168	fe 0 after 12 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
189	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.3	1 r	511.0	0.0	1 r	511.0	0.0
2 r	392.9	0.7	2 r	344.5	0.7	2 r	306.6	0.7	2 r	353.2	0.7	2 r	288.9	0.7	2 r	330.8	0.7	2 r	326.1	0.7	2 r	307.9	0.7
3	333.3	4.6	3	340.4	4.5	3	257.2	5.1	3	265.8	5.6	3	243.9	4.8	3	205.9	4.5	3	276.5	4.7	3	328.2	4.9
4	355.3	4.4	4	341.5	4.3	4	330.0	4.3	4	206.7	5.0	4	268.6	4.4	4	229.2	4.2	4	295.8	4.6	4	251.7	4.6
5	361.3	4.3	5	321.5	4.7	5	159.7	4.6	5	281.7	5.6	5	260.5	4.7	5	212.8	4.3	5	279.0	4.4	5	240.8	4.9
6	318.0	4.3	6	214.1	4.0	6	293.6	4.4	6	246.3	4.6	6	153.8	4.5	6	211.4	4.3	6	278.3	4.6	6	261.1	4.3
7	334.6	4.2	7	295.9	4.3	7	246.2	4.6	7	271.4	5.5	7	251.8	4.8	7	248.1	4.4	7	293.1	4.5	7	208.3	4.8
8	326.2	4.0	8	266.3	4.6	8	256.4	4.1	8	203.1	4.7	8	283.7	4.5	8	168.8	4.2	8	307.7	4.4	8	266.2	4.3
9	265.7	4.5	9	332.5	4.1	9	260.8	4.8	9	351.6	5.0	9	187.7	4.5	9	284.1	4.2	9	306.5	4.5	9	251.9	4.8
10	285.2	4.2	10	267.8	4.4	10	229.0	4.4	10	227.0	4.8	10	188.8	4.5	10	237.9	4.1	10	274.1	4.6	10	229.6	4.6
11	274.0	4.3	11	308.7	4.2	11	282.2	4.8	11	257.2	4.8	11	182.1	4.7	11	207.1	4.3	11	253.3	4.5	11	277.2	4.6
12	331.0	4.5	12	277.9	4.2	12	325.9	4.6	12	264.0	4.8	12	270.2	4.5	12	252.3	4.1	12	350.3	4.1	12	239.9	4.5
13	243.6	4.4	13	293.2	4.2	13	251.1	4.5	13	232.1	5.1	13	256.5	4.6	13	229.5	4.2	13	289.4	4.4	13	315.3	4.9
14	272.8	4.2	14	276.8	4.1	14	235.1	4.6	14	269.6	4.6	14	232.7	4.6	14	226.1	4.2	14	267.6	4.1	14	224.8	4.6
15 f	312.7	1.5	15 f	223.8	1.8	15 f	249.1	1.7	15 f	308.2	1.6	15 f	296.7	1.7	15 f	321.9	1.6	15 f	308.4	1.7	15 f	237.7	1.7
16	305.8	4.1	16	211.0	4.0	16	331.9	4.3	16	212.3	5.0	16	184.8	4.6	16	246.6	4.1	16	368.2	4.6	16	262.3	4.9
17	362.7	4.0	17	318.8	4.0	17	249.1	4.6	17	283.0	4.7	17	178.5	4.6	17	203.0	4.1	17	182.8	4.4	17	225.5	4.6
18	435.5	4.2	18	196.6	4.1	18	293.0	4.8	18	244.9	5.4	18	167.2	4.5	18	172.0	4.2	18	330.2	4.5	18	222.3	4.7
19	343.6	4.3	19	283.0	4.1	19	241.4	4.5	19	284.8	4.5	19	202.2	4.4	19	220.3	4.1	19	287.8	4.3	19	290.5	4.9
20	261.1	4.1	20	278.8	4.1	20	266.9	4.3	20	239.6	4.7	20	240.6	4.5	20	131.4	4.3	20	319.2	4.7	20	236.6	5.0
21	321.0	4.1	21	284.3	4.3	21	260.8	4.3	21	262.1	4.6	21	172.6	4.4	21	240.1	4.1	21	291.4	4.2	21	229.2	4.6
22	250.6	4.2	22	332.8	4.1	22	239.0	4.4	22	249.5	5.0	22	225.8	4.5	22	238.6	3.9	22	233.7	4.2	22	282.9	4.8
23	301.7	4.1	23	275.9	4.1	23	234.9	4.3	23	269.9	4.7	23	153.9	4.4	23	201.7	4.2	23	261.8	4.1	23	263.0	4.4
24	296.5	4.4	24	254.2	4.0	24	224.0	4.5	24	260.2	5.0	24	137.6	4.5	24	136.0	4.2	24	263.9	4.7	24	241.1	4.4
25	297.2	4.5	25	212.5	4.2	25	224.3	4.7	25	265.8	4.6	25	217.2	4.6	25	213.2	4.2	25	338.6	4.3	25	294.4	4.5
26	354.9	4.2	26	261.4	4.6	26	204.5	4.5	26	226.6	5.1	26	273.9	4.3	26	274.1	4.1	26	288.6	4.2	26	224.0	4.5
27	274.0	4.0	27	306.4	4.1	27	247.5	4.2	27	304.9	4.9	27	235.9	4.4	27	287.9	4.0	27	283.3	4.2	27	228.3	4.5
28 f	338.1	1.7	28 f	274.9	1.7	28 f	301.7	1.9	28 f	248.9	1.7	28 f	121.8	1.8	28 f	224.2	1.7	28 f	205.2	1.9	28 f	180.8	1.9
29	320.9	4.6	29	223.3	4.1	29	205.9	4.4	29	348.9	4.8	29	267.4	4.8	29	220.9	4.3	29	227.1	4.3	29	271.5	4.6
30	246.7	4.2	30	238.2	4.0	30	231.1	4.3	30	302.1	4.5	30	154.8	4.3	30	195.2	4.1	30	291.0	4.5	30	270.0	4.4
31	243.6	4.3	31	211.5	4.2	31	202.2	4.4	31	235.8	4.7	31	200.2	4.7	31	273.9	4.1	31	323.2	4.5	31	191.8	4.6
32	350.1	4.2	32	269.7	4.3	32	307.6	4.3	32	238.1	4.6	32	144.2	4.2	32	244.6	4.1	32	249.7	4.4	32	271.5	4.5
33	276.8	4.2	33	324.1	4.2	33	242.7	4.4	33	248.5	4.9	33	192.5	4.6	33	253.6	4.2	33	232.0	4.6	33	251.0	4.7
34	228.2	4.2	34	244.8	3.9	34	243.7	4.8	34	357.4	4.6	34	275.7	4.3	34	292.7	4.2	34	287.6	4.4	34	280.2	4.8
35	303.9	4.2	35	315.9	4.3	35	237.4	4.4	35	408.2	4.8	35	241.8	4.4	35	248.8	4.1	35	293.9	4.4	35	257.7	4.5
36	306.6	4.1	36	205.4	3.9	36	221.8	4.4	36	307.4	4.5	36	183.7	4.4	36	222.0	4.3	36	325.6	4.2	36	172.2	4.5
37	331.2	4.2	37	222.0	4.0	37	211.4	4.2	37	269.1	4.7	37	217.9	4.5	37	286.3	4.4	37	271.4	4.8	37	342.6	4.6
38	301.4	4.2	38	255.7	4.0	38	262.5	4.2	38	314.2	4.5	38	116.6	4.2	38	229.9	4.1	38	249.7	4.3	38	302.5	4.7
39	411.2	4.6	39	348.1	4.2	39	273.1	4.9	39	226.9	5.2	39	276.6	4.6	39	207.4	4.3	39	293.8	4.5	39	363.3	4.8
40	359.4	4.0	40	299.0	4.0	40	248.7	4.1	40	300.1	4.5	40	161.6	4.4	40	313.2	4.2	40	272.2	4.4	40	249.2	4.5
41	389.4	3.9	41	186.8	3.9	41	252.5	3.9	41	249.8	4.1	41	228.7	4.3	41	334.1	3.9	41	187.8	4.1	41	260.8	4.3
42	334.3	4.0	42	314.6	3.8	42	284.5	4.0	42	364.2	4.3	42	226.2	4.0	42	223.1	4.0	42	197.2	4.2	42	287.1	4.8
43	315.4	3.9	43	289.8	3.8	43	228.2	3.9	43	270.5	3.9	43	232.3	4.1	43	278.8	3.8	43	269.8	4.1	43	261.2	4.4
44	305.4	3.9	44	229.7	4.0	44	253.0	4.0	44	379.1	4.3	44	176.1	4.2	44	235.4	4.1	44	199.9	4.1	44	257.3	4.6
45	359.7	4.0	45	286.6	3.8	45	203.9	3.9	45	283.1	4.2	45	206.9	4.0	45	302.4	4.2	45	255.8	4.3	45	363.9	4.3
46	372.3	4.1	46	225.7	3.7	46	258.8	4.0	46	297.5	4.3	46	269.4	4.2	46	223.9	4.1	46	201.2	4.3	46	259.1	4.9
47	296.1	4.0	47	242.3	3.8	47	240.2	4.0	47	337.5	4.1	47	247.4	4.1	47	279.6	4.0	47	372.5	4.2	47	192.7	4.7
48	343.6	4.1	48	307.3	3.9	48	228.4	4.1	48	232.1	4.3	48	281.4	4.1	48	254.2	3.9	48	277.6	4.5	48	294.8	4.9
49	316.2	3.9	49	252.3	3.8	49	218.1	4.1	49	280.0	4.3	49	225.6	4.0	49	166.7	3.9	49	342.0	3.9	49	208.7	4.3
50	242.7	4.1	50	239.1	4.0	50	196.3	4.2	50	333.8	4.3	50	238.7	4.2	50	216.1	4.2	50	249.2	4.5	50	202.5	4.8
51	285.4	4.0	51	312.6	3.9	51	227.1	4.2	51	286.6	4.0	51	242.6	4.2	51	291.3	4.2	51	235.6	4.2	51	322.6	4.4
52	273.6	4.4	52	192.3	3.8	52	232.4	4.2	52	254.9	4.3	52	197.4	4.1	52	160.8	4.9	52	285.5	4.4	52	313.2	4.9
53 f	205.4	1.6	53 f	343.9	1.7	53 f	219.5	1.6	53 f	348.5	1.5	53 f	190.0	1.7	53 f	282.1	1.7	53 f	229.7	1.6	53 f	202.9	1.6
54	311.9	3.9	54	214.5	3.8	54	194.7	4.3	54	275.4	4.1	54	154.9	4.1	54	161.2	4.0	54	211.9	4.3	54	288.9	4.6
55	355.7	3.9	55	252.5	4.0	55	285.0	4.1	55	235.5	4.3	55	210.2	4.2	55	302.1	4.2	55	290.7	4.3	55	275.4	4.7
56	337.2	4.0	56	231.5	3.9	56	226.0	3.8	56	303.8	4.2	56	128.5	4.3	56	177.1	4.0	56	302.9	4.0	56	323.5	4.6
57	310.3	4.0	57	294.4	4.2	57	256.6	4.2	57	294.5	4.5	57	197.4	4.0	57	270.4	4.1	57	294.7	4.4	57	194.2	4.7
58	268.1	3.9	58	273.9	3.9	58	237.9	4.3	58	241.8	4.1	58	237.3										

Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	463.1	8.0	1 r	425.2	7.9	1 r	347.0	10.3	1 r	378.8	8.5	1 r	365.9	10.4	1 r	271.0	9.5	1 r	327.3	11.4	1 r	503.9	5.8
2 r	249.4	0.7	2 r	249.5	0.7	2 r	249.7	0.7	2 r	249.9	0.7	2 r	250.0	0.7	2 r	249.7	0.7	2 r	250.2	0.7	2 r	249.8	0.7
3	250.0	4.5	3	250.0	4.4	3	250.2	4.8	3	248.7	5.4	3	250.4	4.7	3	249.3	4.3	3	250.4	4.6	3	249.8	4.8
4	249.8	4.3	4	248.2	4.0	4	250.2	4.2	4	249.0	4.8	4	250.7	4.5	4	250.8	4.2	4	251.1	4.4	4	249.8	4.4
5	250.3	4.4	5	250.8	4.1	5	249.8	4.5	5	249.6	5.2	5	250.5	4.8	5	250.5	4.2	5	249.8	4.3	5	249.7	4.8
6	249.6	4.2	6	249.7	4.1	6	250.0	4.2	6	249.2	4.7	6	250.7	4.5	6	251.3	4.2	6	250.9	4.6	6	249.9	4.4
7	249.8	4.3	7	250.9	4.1	7	248.6	4.6	7	251.8	5.0	7	249.6	4.6	7	251.1	4.2	7	252.2	4.3	7	250.5	4.5
8	249.6	4.2	8	250.0	4.1	8	250.6	4.5	8	250.2	4.5	8	249.1	4.8	8	249.3	4.2	8	249.2	4.4	8	250.7	4.3
9	249.6	4.4	9	248.7	4.4	9	249.6	4.7	9	250.2	5.0	9	250.8	4.5	9	249.6	4.2	9	250.2	4.5	9	249.7	4.5
10	250.0	4.2	10	248.9	4.4	10	250.8	4.4	10	248.7	4.7	10	250.2	4.7	10	250.4	4.5	10	250.7	4.5	10	251.0	4.5
11	249.7	4.2	11	249.2	4.1	11	251.0	4.4	11	251.2	4.6	11	250.2	4.5	11	251.3	4.4	11	251.2	4.2	11	250.0	4.7
12	249.5	4.2	12	251.4	4.2	12	248.9	4.3	12	249.7	4.8	12	249.9	4.2	12	249.7	4.2	12	251.8	4.3	12	250.4	4.5
13	250.0	4.4	13	250.7	4.1	13	249.9	4.2	13	251.8	4.9	13	250.1	4.7	13	249.7	4.3	13	250.6	4.3	13	250.8	4.7
14	249.7	4.1	14	249.7	4.1	14	249.9	4.2	14	249.0	4.5	14	250.3	4.5	14	252.1	4.2	14	249.2	4.2	14	249.2	4.3
15 f	249.2	1.6	15 f	249.9	1.8	15 f	249.9	1.7	15 f	249.4	1.6	15 f	250.1	1.7	15 f	249.9	1.6	15 f	250.6	1.7	15 f	249.8	1.8
16	250.0	4.1	16	250.3	4.2	16	250.4	4.3	16	249.1	4.8	16	249.5	4.5	16	248.1	4.0	16	250.9	4.5	16	249.0	4.6
17	248.9	4.7	17	250.3	3.9	17	249.8	4.3	17	249.2	4.7	17	249.3	4.3	17	249.6	4.3	17	250.3	4.4	17	249.3	4.5
18	250.1	4.5	18	248.3	4.1	18	251.3	4.4	18	249.8	4.8	18	251.4	4.2	18	251.0	4.4	18	251.7	4.4	18	250.8	4.8
19	248.3	4.1	19	250.8	4.0	19	251.4	4.4	19	249.5	4.6	19	250.4	4.1	19	249.8	4.2	19	249.5	4.3	19	250.6	4.6
20	250.0	4.3	20	250.6	4.1	20	249.4	4.2	20	249.5	4.6	20	249.6	4.4	20	249.2	4.2	20	249.9	4.5	20	249.2	4.7
21	249.2	4.1	21	252.3	4.2	21	250.1	4.3	21	248.9	4.7	21	249.8	4.4	21	250.2	4.1	21	249.5	4.4	21	249.9	4.4
22	248.9	3.9	22	249.8	4.5	22	250.8	4.3	22	250.0	4.7	22	250.1	4.5	22	250.8	4.2	22	248.8	4.2	22	248.6	4.4
23	249.4	4.0	23	249.7	3.9	23	250.2	4.2	23	249.3	4.2	23	249.9	4.2	23	250.6	4.2	23	250.1	4.1	23	250.6	4.5
24	250.7	4.2	24	250.9	4.0	24	249.8	4.2	24	250.4	4.5	24	249.5	4.2	24	248.9	4.4	24	250.9	4.5	24	249.9	4.4
25	250.3	4.0	25	251.3	3.9	25	249.6	4.5	25	249.1	4.4	25	250.4	4.3	25	250.2	4.1	25	249.7	4.1	25	249.8	4.3
26	250.4	4.1	26	251.2	4.1	26	250.0	4.5	26	247.3	4.5	26	251.5	4.3	26	249.2	4.2	26	249.1	4.4	26	250.9	4.6
27	250.0	4.1	27	252.0	4.0	27	250.2	4.2	27	249.9	4.4	27	250.2	4.3	27	250.3	4.2	27	251.2	4.3	27	250.8	4.2
28 f	249.2	1.6	28 f	250.3	1.7	28 f	250.6	1.8	28 f	249.3	1.8	28 f	250.1	1.7	28 f	250.6	1.6	28 f	250.6	1.9	28 f	250.1	1.8
29	250.1	4.1	29	250.3	4.2	29	249.8	4.1	29	250.2	4.6	29	248.7	4.3	29	249.7	4.4	29	250.1	4.2	29	251.3	4.5
30	249.2	3.9	30	251.2	4.2	30	250.5	4.2	30	249.7	4.4	30	250.7	4.8	30	251.4	4.3	30	249.9	4.3	30	249.6	4.5
31	249.9	4.1	31	249.9	4.0	31	249.3	4.3	31	248.5	4.5	31	250.3	4.2	31	249.6	4.0	31	249.9	4.4	31	249.5	4.5
32	250.3	4.2	32	250.0	4.0	32	249.5	4.2	32	251.2	4.2	32	250.7	4.4	32	250.3	4.2	32	248.9	4.5	32	250.4	4.3
33	249.2	4.1	33	250.1	4.0	33	248.3	4.2	33	250.4	4.6	33	248.7	4.6	33	250.7	4.2	33	251.6	4.3	33	248.8	4.6
34	250.2	4.1	34	250.1	3.9	34	249.3	4.1	34	250.0	4.2	34	251.1	4.3	34	249.8	4.1	34	251.2	4.4	34	249.8	4.5
35	248.8	4.1	35	249.2	4.3	35	249.8	4.3	35	250.1	4.6	35	249.3	4.5	35	248.9	4.3	35	250.3	4.5	35	250.0	4.5
36	249.7	4.3	36	249.0	4.0	36	250.2	4.1	36	248.9	4.4	36	249.2	4.6	36	249.5	3.9	36	249.4	4.5	36	250.1	4.4
37	251.2	4.0	37	251.8	4.0	37	249.8	4.3	37	250.2	4.6	37	248.8	4.3	37	251.1	4.4	37	250.8	4.5	37	248.6	4.7
38	250.0	4.1	38	249.2	4.0	38	251.4	4.1	38	250.2	4.4	38	249.7	4.3	38	250.1	4.1	38	250.4	4.2	38	249.3	4.3
39	250.3	4.3	39	250.2	4.3	39	251.1	4.7	39	249.0	4.8	39	249.0	4.7	39	250.8	4.2	39	249.4	4.4	39	251.1	4.7
40	249.5	4.0	40	250.0	4.0	40	251.3	4.3	40	250.0	4.4	40	249.8	4.4	40	251.5	4.1	40	250.9	4.3	40	250.0	4.6
41	250.6	4.0	41	250.3	4.2	41	251.5	3.9	41	249.0	4.1	41	249.6	4.0	41	250.4	4.0	41	250.6	4.1	41	248.3	4.3
42	249.3	3.9	42	250.1	3.8	42	250.8	4.2	42	250.8	4.1	42	249.7	4.1	42	251.4	4.4	42	248.8	4.2	42	249.7	4.5
43	250.2	4.0	43	249.5	3.8	43	251.2	4.0	43	249.2	4.1	43	251.0	4.0	43	250.2	3.9	43	250.2	4.1	43	250.6	4.3
44	249.8	3.7	44	251.1	3.9	44	251.1	4.1	44	249.4	4.1	44	250.6	4.2	44	249.1	3.8	44	250.2	4.5	44	250.3	4.5
45	250.2	3.8	45	250.5	3.9	45	249.9	4.4	45	250.8	4.1	45	250.4	4.1	45	249.6	3.9	45	249.3	4.1	45	250.6	4.4
46	248.5	4.0	46	249.5	4.1	46	251.3	4.2	46	249.5	4.1	46	249.9	4.1	46	250.3	4.1	46	250.4	4.3	46	249.3	4.6
47	248.9	3.9	47	249.3	3.8	47	249.9	3.9	47	249.4	4.1	47	250.2	4.0	47	250.1	4.0	47	250.2	4.0	47	249.4	4.7
48	247.8	3.9	48	251.1	3.9	48	249.9	4.0	48	250.1	4.3	48	250.2	4.1	48	250.1	4.0	48	250.6	4.6	48	249.2	4.7
49	250.3	3.9	49	249.8	3.9	49	250.7	3.9	49	249.2	4.2	49	250.0	4.0	49	249.7	3.8	49	250.3	4.5	49	249.3	4.6
50	248.5	4.0	50	250.1	3.8	50	251.9	4.0	50	249.3	4.1	50	249.4	4.1	50	250.2	4.3	50	250.9	4.5	50	249.7	4.5
51	248.8	3.9	51	249.6	3.7	51	251.6	4.1	51	249.3	4.2	51	249.1	4.2	51	252.0	4.1	51	249.4	3.9	51	249.1	4.4
52	250.5	4.2	52	250.2	4.0	52	250.3	4.3	52	248.2	4.0	52	251.2	4.5	52	250.2	4.1	52	249.7	4.3	52	249.5	4.7
53 f	250.1	1.6	53 f	250.6	1.6	53 f	250.2	1.6	53 f	250.6	1.7	53 f	250.0	1.6	53 f	249.6	1.7	53 f	249.7	1.8	53 f	250.0	1.6
54	249.3	4.1	54	248.9	3.9	54	248.8	4.0	54	250.6	4.1	54	250.2	4.1	54	250.4	4.0	54	249.6	4.2	54	249.6	4.5
55	249.7	3.8	55	250.2	4.0	55	249.9	4.3	55	250.0	4.2	55	249.1	4.3	55	250.7	4.1	55	249.4	4.4	55	250.2	4.7
56	249.0	3.9	56	249.6	4.1	56	250.5	3.9	56	249.5	4.0	56	249.5	4.0	56	249.8	4.0	56	249.3	4.2	56	250.7	4.5
57	250.9	4.0	57	249.8	3.8	57	249.3	4.0	57	249.7	4.2	57	251.7	4.3	57	249.7	4.2	57	250.0	4.3	57	248.9	4.6
58	248.4	4.0	58	251.6	3.7	58	250.5	4.0	58	249.2													