

## Fec test report:

Date: 2020-10-26 15:22:27

Tester name: Diego

### Test#1 Monitoring values

Passed

0	FEC label	008	OK
1	FEC DC2438 ID	ec0000024d999d26	OK
2	FEC_T (to 35°C)	23.656	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.1A to 1.5A)	1.497	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3053	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2995	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3085	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3005	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3173	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3064	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3040	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3058	OK

## FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdc(2) Fem(00) FEC_T: 23.656 degC
2	fe 0 moni V 1	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 1	0	0 Tdc(2) Fem(00) FEC_I: 1.497 A
8	fe 0 moni S 1	0	0 Tdc(2) Fem(00) FEC_Serial: ec0000024d999d26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12088000 (302546944) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0b0b 0x0b0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0c0c 0x0c0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0d0d 0x0d0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdc(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdc(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdc(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdc(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdc(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdc(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdc(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdc(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 ( Aligned SCA_Write )
6	daq 0xFFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 1 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 Tdc(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 Tdc(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 Tdc(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xefff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xefff0000
168	fe 0 after 12 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
189	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

# Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	501.1	8.3	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	299.2	0.7	2 r	270.0	0.7	2 r	298.0	0.7	2 r	315.9	0.7	2 r	250.8	0.7	2 r	333.2	0.7	2 r	300.7	0.7	2 r	286.5	0.7
3	299.8	4.4	3	214.6	4.4	3	330.4	4.5	3	301.6	5.1	3	206.5	4.9	3	321.0	4.6	3	244.1	4.6	3	212.8	4.9
4	228.4	4.1	4	156.2	4.4	4	300.3	4.3	4	184.1	4.8	4	146.4	4.5	4	288.4	4.3	4	258.1	4.3	4	132.1	4.5
5	225.2	4.4	5	183.5	4.6	5	285.4	4.4	5	201.2	5.1	5	208.3	4.6	5	284.9	4.4	5	241.6	4.5	5	195.5	4.7
6	257.5	4.4	6	176.5	4.1	6	187.5	4.3	6	239.9	4.6	6	143.7	4.8	6	326.9	4.2	6	197.0	4.2	6	175.7	4.3
7	258.7	4.5	7	142.5	4.2	7	275.2	4.5	7	181.3	5.0	7	266.9	4.4	7	276.5	4.4	7	180.9	4.5	7	267.6	4.5
8	202.6	4.2	8	114.1	4.1	8	233.5	4.3	8	258.1	4.4	8	147.2	4.4	8	280.0	4.5	8	151.2	4.2	8	187.4	4.4
9	293.8	4.5	9	185.6	4.2	9	258.1	4.3	9	271.6	4.8	9	240.2	4.8	9	383.1	4.3	9	253.7	4.2	9	254.3	4.6
10	328.6	4.4	10	204.3	4.0	10	250.9	4.3	10	159.7	4.5	10	122.7	4.3	10	336.4	4.1	10	180.1	4.1	10	170.9	4.4
11	259.8	4.3	11	183.4	4.2	11	268.3	4.1	11	211.3	4.9	11	221.7	4.5	11	352.8	4.4	11	216.7	4.4	11	256.5	4.5
12	293.0	4.3	12	172.8	4.3	12	339.4	4.0	12	278.1	4.7	12	177.2	4.5	12	339.2	4.3	12	199.0	4.0	12	171.2	4.3
13	287.6	4.3	13	174.0	4.0	13	254.9	4.3	13	205.9	4.6	13	214.4	4.3	13	269.1	4.1	13	288.4	4.6	13	216.8	4.5
14	254.7	4.0	14	151.8	4.3	14	272.4	4.3	14	245.3	5.0	14	132.7	4.6	14	338.8	4.3	14	231.7	4.0	14	297.0	4.3
15 f	237.3	1.6	15 f	213.8	1.7	15 f	248.8	1.7	15 f	217.8	1.7	15 f	266.1	1.8	15 f	267.6	1.6	15 f	326.0	1.7	15 f	265.1	1.6
16	304.8	4.2	16	140.8	4.4	16	241.1	4.0	16	231.3	4.8	16	143.7	4.6	16	288.6	4.1	16	203.7	4.1	16	289.0	4.4
17	215.8	4.3	17	128.5	4.1	17	261.6	4.5	17	165.5	4.4	17	115.1	4.4	17	313.6	4.0	17	318.2	4.3	17	168.6	4.4
18	165.8	4.2	18	191.3	4.0	18	251.5	4.2	18	145.6	4.5	18	237.1	4.7	18	317.5	4.2	18	246.6	4.2	18	221.6	4.4
19	243.8	4.0	19	184.9	4.1	19	259.3	4.0	19	224.7	4.4	19	128.2	4.5	19	232.9	4.1	19	288.7	4.1	19	279.7	4.6
20	285.9	4.1	20	133.5	4.2	20	261.6	4.6	20	166.5	4.8	20	167.2	4.3	20	268.9	4.2	20	187.5	4.3	20	253.6	4.4
21	47.0	4.0	21	208.7	4.2	21	216.1	4.2	21	224.9	4.4	21	196.6	4.3	21	292.1	4.0	21	217.4	4.1	21	241.2	4.4
22	231.8	4.2	22	136.0	4.1	22	159.1	4.1	22	185.8	4.6	22	209.2	4.3	22	315.4	4.2	22	245.1	4.2	22	198.8	4.6
23	276.2	4.2	23	285.6	4.0	23	215.2	4.1	23	253.5	4.4	23	161.5	4.6	23	344.4	4.2	23	225.2	4.2	23	200.5	4.5
24	300.2	4.0	24	172.8	4.4	24	318.6	4.2	24	255.7	4.6	24	183.2	4.5	24	309.4	4.2	24	186.0	4.3	24	293.2	4.4
25	225.9	4.2	25	148.1	4.3	25	259.8	4.2	25	279.2	4.5	25	172.6	4.6	25	253.2	4.0	25	187.2	4.0	25	196.7	4.4
26	273.7	4.2	26	121.8	4.1	26	196.3	4.3	26	272.2	4.3	26	240.3	4.4	26	314.7	4.2	26	181.6	4.2	26	225.9	4.2
27	266.0	4.1	27	120.5	4.0	27	208.2	4.0	27	209.2	4.1	27	224.1	4.9	27	289.3	4.0	27	294.2	4.1	27	242.1	4.2
28 f	194.0	1.8	28 f	121.3	1.9	28 f	230.9	2.0	28 f	199.6	1.7	28 f	210.5	1.9	28 f	236.1	1.7	28 f	219.7	1.7	28 f	205.0	1.8
29	341.1	4.2	29	152.6	4.1	29	234.8	4.0	29	196.6	4.7	29	248.4	4.3	29	247.1	4.1	29	127.8	3.9	29	201.6	4.5
30	195.6	4.1	30	222.0	3.9	30	275.4	4.1	30	301.1	4.2	30	126.8	4.3	30	340.4	4.2	30	166.9	4.2	30	256.3	4.3
31	234.4	4.1	31	180.4	4.2	31	311.3	4.3	31	205.8	4.6	31	162.5	4.8	31	265.2	4.3	31	153.4	4.2	31	182.9	4.5
32	215.8	4.2	32	188.3	4.1	32	253.9	4.3	32	236.3	4.5	32	186.5	4.1	32	263.9	4.5	32	295.1	4.2	32	234.2	4.2
33	259.4	4.2	33	193.6	4.3	33	191.0	4.3	33	345.8	4.6	33	156.1	4.3	33	280.1	4.2	33	207.9	4.1	33	271.7	4.3
34	253.4	4.2	34	201.2	3.9	34	260.1	4.1	34	198.5	4.3	34	187.0	4.3	34	283.4	4.1	34	194.5	4.2	34	269.1	4.5
35	276.8	4.2	35	211.7	4.1	35	289.2	4.3	35	251.5	4.8	35	128.5	4.4	35	296.2	4.3	35	251.7	4.3	35	168.4	4.6
36	168.0	4.4	36	152.6	4.0	36	189.8	4.0	36	203.2	4.2	36	207.7	4.5	36	273.9	4.0	36	210.5	4.1	36	273.8	4.4
37	165.3	4.1	37	162.5	4.1	37	323.5	4.3	37	182.1	4.4	37	122.4	4.3	37	286.0	4.3	37	281.1	4.1	37	223.2	4.3
38	203.8	4.3	38	186.8	4.1	38	209.4	4.0	38	218.4	4.6	38	211.0	4.3	38	258.4	4.1	38	190.9	4.1	38	199.4	4.2
39	162.1	4.5	39	202.8	4.4	39	285.2	4.3	39	251.5	4.8	39	167.7	4.5	39	303.8	4.2	39	237.5	4.4	39	184.9	4.8
40	254.7	4.0	40	243.5	4.0	40	251.1	4.4	40	153.0	4.2	40	219.0	4.8	40	234.0	4.1	40	306.6	4.2	40	237.1	4.6
41	175.5	3.9	41	275.8	3.8	41	204.3	3.8	41	228.3	4.0	41	217.6	4.0	41	341.0	3.8	41	179.9	3.8	41	233.1	4.4
42	206.7	4.0	42	163.7	3.9	42	265.7	4.0	42	232.7	4.0	42	217.7	4.1	42	225.1	3.9	42	182.6	3.9	42	144.0	4.2
43	129.0	4.0	43	228.3	3.8	43	237.9	4.1	43	320.1	4.0	43	144.7	4.1	43	271.4	3.8	43	288.5	3.8	43	196.2	4.1
44	179.2	4.0	44	105.1	4.0	44	179.5	3.8	44	227.4	4.1	44	217.3	4.1	44	254.1	3.8	44	213.2	4.0	44	268.1	4.4
45	133.1	4.0	45	203.3	3.7	45	225.3	4.1	45	292.9	4.2	45	216.8	4.1	45	269.1	3.7	45	287.2	4.4	45	209.3	4.1
46	251.8	4.0	46	150.6	4.0	46	311.6	3.8	46	243.7	4.2	46	186.9	4.3	46	322.4	3.9	46	267.2	4.0	46	284.1	4.4
47	247.9	4.0	47	206.9	4.0	47	234.8	4.1	47	221.1	3.8	47	114.6	4.1	47	368.0	3.8	47	301.7	4.0	47	213.7	4.4
48	258.2	3.6	48	197.9	3.8	48	236.0	3.8	48	209.6	4.2	48	160.9	4.1	48	242.1	3.8	48	235.0	3.9	48	246.6	4.4
49	169.0	4.1	49	91.3	3.6	49	223.1	3.9	49	221.2	4.1	49	220.9	4.0	49	218.6	3.8	49	258.7	3.7	49	237.6	4.2
50	244.3	3.9	50	169.8	3.9	50	336.4	3.9	50	177.8	4.3	50	130.8	4.1	50	240.6	4.0	50	259.4	3.9	50	281.9	4.6
51	161.0	4.3	51	124.7	4.1	51	266.4	3.8	51	251.4	4.3	51	158.7	4.1	51	306.7	3.8	51	232.8	4.1	51	329.2	4.2
52	258.8	4.0	52	172.7	3.9	52	278.3	4.1	52	208.7	4.0	52	162.4	4.5	52	242.5	3.8	52	239.8	4.2	52	303.0	4.4
53 f	286.3	1.6	53 f	135.5	1.5	53 f	269.9	1.7	53 f	235.9	1.4	53 f	115.5	1.6	53 f	319.5	1.5	53 f	204.3	1.5	53 f	230.7	1.5
54	222.4	3.9	54	283.2	3.8	54	230.3	3.9	54	182.6	4.2	54	146.7	3.9	54	286.7	3.8	54	270.9	3.9	54	247.3	3.9
55	172.1	4.3	55	213.2	3.8	55	250.1	3.8	55	202.5	4.1	55	250.5	4.1	55	366.1	3.7	55	242.3	4.0	55	225.6	4.7
56	215.6	3.9	56	131.6	4.0	56	216.9	4.0	56	220.3	3.9	56	112.8	4.0	56	271.5	4.2	56	217.1	3.8	56	248.8	4.2
57	279.9	4.0	57	114.1	3.9	57	331.6	3.9	57	282.9	4.1	57	211.5	4.2	57	283.5	4.1	57	265.7	3.8	57	262.4	4.5
58	280.8	4.0	58	171.9																			



Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	378.2	10.2	1 r	306.7	9.2	1 r	427.2	10.3	1 r	383.0	9.2	1 r	253.1	11.5	1 r	443.0	9.6	1 r	291.5	8.6	1 r	283.9	10.2
2 r	250.9	0.7	2 r	250.5	0.7	2 r	250.4	0.7	2 r	250.3	0.7	2 r	250.4	0.7	2 r	250.6	0.6	2 r	250.1	0.7	2 r	250.4	0.7
3	251.7	4.6	3	250.8	4.5	3	251.2	4.6	3	250.1	4.8	3	251.5	4.7	3	251.0	4.5	3	250.3	4.5	3	252.0	4.7
4	253.2	4.3	4	250.9	4.1	4	251.3	4.2	4	251.5	5.0	4	251.7	4.4	4	251.3	4.1	4	251.2	4.3	4	251.5	4.5
5	248.9	4.2	5	251.4	4.2	5	251.3	4.3	5	251.5	4.8	5	249.8	4.6	5	251.6	4.2	5	250.6	4.5	5	251.7	4.6
6	252.2	4.3	6	250.3	4.1	6	250.1	4.3	6	250.3	4.1	6	249.5	4.6	6	250.1	4.3	6	250.0	4.1	6	250.5	4.3
7	250.1	4.3	7	250.5	4.4	7	251.0	4.6	7	251.4	4.7	7	250.0	4.4	7	250.4	4.3	7	251.3	4.3	7	250.8	4.4
8	250.4	4.2	8	250.1	4.3	8	248.2	4.5	8	250.5	4.6	8	250.1	4.4	8	249.4	4.1	8	249.7	4.3	8	251.5	4.4
9	250.5	4.3	9	249.7	4.2	9	250.9	4.2	9	250.3	4.6	9	250.6	4.4	9	250.4	4.0	9	251.0	4.3	9	249.8	4.7
10	250.7	4.3	10	251.1	4.1	10	250.7	4.2	10	251.5	4.3	10	248.5	4.6	10	251.7	4.1	10	250.6	4.1	10	249.6	4.3
11	251.2	4.3	11	250.1	4.1	11	252.6	4.3	11	250.4	4.6	11	252.0	4.5	11	249.1	4.5	11	250.7	4.2	11	250.4	4.5
12	250.2	4.0	12	250.6	4.1	12	252.0	4.1	12	251.4	4.3	12	251.2	4.3	12	250.0	4.1	12	249.4	4.4	12	252.3	4.2
13	250.8	4.2	13	250.2	4.1	13	249.6	4.1	13	250.3	4.2	13	250.2	4.3	13	250.4	4.5	13	250.6	4.3	13	250.1	4.4
14	250.1	4.0	14	249.6	4.2	14	251.4	4.1	14	250.6	4.3	14	253.2	4.4	14	250.8	4.1	14	251.5	4.0	14	249.7	4.2
15 f	251.2	1.8	15 f	250.4	1.6	15 f	250.7	1.7	15 f	249.8	1.7	15 f	250.5	1.8	15 f	249.8	1.7	15 f	250.8	1.7	15 f	250.9	1.8
16	249.0	4.3	16	249.9	4.3	16	250.9	4.2	16	250.3	4.4	16	249.1	4.6	16	249.9	4.3	16	250.1	4.2	16	250.9	4.6
17	251.2	4.1	17	249.2	4.2	17	249.0	4.2	17	251.0	4.4	17	250.6	4.5	17	249.7	4.2	17	251.9	4.2	17	250.6	4.4
18	249.9	4.1	18	252.4	4.1	18	251.3	4.1	18	249.3	4.7	18	249.7	4.4	18	251.1	4.3	18	249.9	4.2	18	250.3	4.3
19	250.0	4.2	19	250.1	4.0	19	250.4	4.1	19	250.1	4.1	19	249.9	4.6	19	250.6	4.0	19	250.2	4.3	19	250.1	4.4
20	251.9	4.2	20	250.5	4.0	20	250.5	4.6	20	251.1	4.3	20	250.7	4.4	20	250.8	4.0	20	249.8	4.0	20	251.2	4.3
21	249.8	4.2	21	250.4	4.1	21	251.5	4.2	21	251.2	4.3	21	250.2	4.3	21	250.4	4.1	21	250.9	4.1	21	249.4	4.2
22	249.8	4.1	22	249.8	4.3	22	250.2	4.2	22	251.4	4.5	22	250.1	4.3	22	250.3	4.1	22	251.7	4.2	22	250.8	4.2
23	251.1	4.2	23	251.1	4.0	23	251.1	4.0	23	248.6	4.3	23	252.2	4.7	23	251.3	4.1	23	250.5	4.0	23	250.7	4.4
24	250.3	4.2	24	249.2	4.0	24	250.1	3.9	24	250.4	4.4	24	251.6	4.5	24	250.0	4.1	24	251.8	4.5	24	252.1	4.3
25	252.1	4.2	25	250.0	4.1	25	249.7	4.2	25	251.0	4.2	25	250.8	4.7	25	250.9	4.3	25	251.3	4.2	25	250.8	4.3
26	251.2	4.1	26	249.9	3.8	26	251.9	4.4	26	250.6	4.4	26	252.0	4.3	26	249.6	4.1	26	250.3	4.2	26	251.5	4.3
27	249.8	4.1	27	252.2	4.0	27	251.1	4.4	27	251.6	4.2	27	251.0	4.4	27	250.9	4.3	27	251.9	4.2	27	251.9	4.7
28 f	250.9	1.7	28 f	250.3	1.8	28 f	250.4	1.8	28 f	250.1	1.8	28 f	251.6	1.8	28 f	250.8	1.7	28 f	250.6	1.8	28 f	250.6	1.8
29	250.7	4.2	29	250.3	4.2	29	249.6	4.2	29	248.8	4.3	29	249.4	4.3	29	250.3	4.1	29	250.0	4.4	29	250.6	4.3
30	251.4	4.1	30	251.0	3.9	30	252.3	4.3	30	252.3	4.2	30	250.9	4.3	30	250.6	4.4	30	250.1	4.1	30	251.4	4.3
31	251.2	4.2	31	249.8	4.1	31	249.9	4.3	31	249.9	4.3	31	252.0	4.4	31	250.9	4.3	31	251.2	4.0	31	251.1	4.4
32	251.6	4.0	32	251.6	4.2	32	250.0	4.1	32	252.1	4.2	32	251.5	4.4	32	251.0	4.1	32	250.2	4.1	32	252.0	4.3
33	251.0	4.0	33	250.9	4.2	33	251.7	4.1	33	250.4	4.4	33	250.6	4.3	33	250.4	4.1	33	251.9	4.1	33	250.4	4.3
34	251.9	4.0	34	249.5	4.0	34	249.7	4.2	34	251.0	4.0	34	251.1	4.4	34	250.4	4.2	34	249.3	4.2	34	250.7	4.0
35	250.9	4.1	35	250.3	4.3	35	250.3	4.3	35	249.2	4.4	35	251.9	4.3	35	251.2	4.0	35	249.6	4.0	35	251.8	4.4
36	250.1	4.0	36	250.2	4.1	36	250.1	4.1	36	250.4	4.5	36	252.2	4.5	36	249.4	4.3	36	251.8	4.0	36	251.1	4.3
37	251.3	4.0	37	248.9	4.1	37	252.0	4.2	37	249.2	4.1	37	252.1	4.5	37	250.5	4.0	37	249.9	4.2	37	251.6	4.2
38	251.2	4.1	38	250.3	4.0	38	250.9	4.1	38	251.1	4.2	38	251.4	4.2	38	250.8	4.4	38	251.1	4.1	38	250.8	4.2
39	250.0	4.3	39	250.5	4.2	39	251.7	4.4	39	250.7	4.6	39	251.4	4.6	39	250.6	4.5	39	250.4	4.5	39	250.6	4.5
40	251.9	4.1	40	250.1	4.0	40	251.3	4.3	40	250.4	4.3	40	251.9	4.4	40	249.9	3.9	40	249.4	4.2	40	250.4	4.2
41	252.7	4.0	41	251.8	3.9	41	252.1	3.9	41	250.8	4.0	41	250.0	4.0	41	250.1	4.0	41	250.0	4.0	41	249.3	4.2
42	250.6	4.0	42	250.2	3.9	42	250.2	3.9	42	250.3	3.6	42	250.9	4.1	42	251.0	3.9	42	251.4	3.8	42	251.5	4.0
43	251.1	3.8	43	249.7	4.2	43	250.1	3.8	43	251.5	3.8	43	250.3	4.0	43	251.2	4.0	43	249.9	3.9	43	251.6	4.1
44	250.1	3.9	44	250.5	3.8	44	250.7	3.8	44	251.8	3.8	44	251.0	4.1	44	251.2	3.6	44	250.7	4.0	44	252.4	4.0
45	251.8	3.8	45	250.3	3.6	45	251.3	3.9	45	250.5	3.8	45	250.1	4.1	45	250.5	3.7	45	251.4	4.0	45	251.6	4.1
46	250.0	3.8	46	251.1	3.8	46	251.4	4.0	46	250.9	4.0	46	249.7	4.0	46	249.8	3.9	46	250.5	4.1	46	252.2	4.1
47	250.6	3.8	47	250.9	3.8	47	250.6	3.9	47	250.7	4.0	47	249.4	4.6	47	249.9	3.9	47	249.1	3.9	47	251.8	4.2
48	249.3	3.8	48	250.0	3.9	48	249.3	4.0	48	249.8	4.2	48	250.1	4.1	48	251.2	3.9	48	249.7	3.9	48	251.2	4.3
49	250.5	4.0	49	251.7	3.9	49	250.2	3.9	49	251.5	4.0	49	251.1	4.1	49	251.4	3.7	49	249.1	4.0	49	249.2	4.0
50	252.2	4.2	50	250.7	4.2	50	251.2	3.8	50	249.9	3.8	50	250.7	4.0	50	251.2	4.1	50	252.3	3.9	50	249.8	4.2
51	250.9	4.2	51	250.1	3.8	51	249.6	4.1	51	251.7	4.0	51	249.9	4.2	51	250.6	3.8	51	250.8	3.7	51	251.2	4.3
52	250.5	3.9	52	250.8	3.8	52	251.2	4.0	52	251.3	3.9	52	251.1	4.2	52	250.3	4.0	52	249.6	3.9	52	250.6	4.3
53 f	251.1	1.4	53 f	249.9	1.5	53 f	250.8	1.6	53 f	250.7	1.5	53 f	251.1	1.5	53 f	249.9	1.5	53 f	251.2	1.6	53 f	250.2	1.4
54	251.5	3.9	54	250.2	4.0	54	250.0	4.1	54	249.6	4.2	54	249.4	3.8	54	249.4	3.8	54	249.2	3.8	54	251.0	4.0
55	251.8	4.0	55	251.5	3.8	55	250.8	3.9	55	250.7	3.8	55	248.9	4.0	55	249.9	3.9	55	251.1	4.2	55	251.4	4.2
56	249.1	3.7	56	249.8	4.0	56	249.8	4.0	56	251.4	3.9	56	251.4	4.0	56	249.0	3.9	56	250.3	4.0	56	250.8	4.1
57	250.7	4.2	57	250.0	3.8	57	249.4	4.0	57	250.9	4.2	57	249.3	4.2	57	249.3	3.9	57	249.8	4.0	57	251.6	4.3
58	251.4	4.0	58	251.4	3.9	58	248.7	3.9	58	251.2													