

Fec test report:

Date: 2020-10-26 15:52:11

Tester name: Boris

Test#1 Monitoring values

Failed

0	FEC label	011	OK
1	FEC DC2438 ID	630000024da7d926	OK
2	FEC_T (to 35°C)	28.688	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	1.501	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3023	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3010	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3052	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3031	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3012	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3061	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3058	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3060	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdcm(2) Fem(00) FEC_T: 28.688 degC
2	fe 0 moni V 1	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 1 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 1	0	0 Tdcm(2) Fem(00) FEC_I: 1.501 A
8	fe 0 moni S 1	0	0 Tdcm(2) Fem(00) FEC_Serial: 630000024da7d926

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2088000 (34111488) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdcm(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdcm(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdcm(2) Fem(00) After(10) Reg(3) <- 0x0 0xb0b 0xb0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0xc0c 0xc0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0xd0d 0xd0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdcm(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(15) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdcm(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdcm(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdcm(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdcm(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdcm(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdcm(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdcm(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdcm(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 Tdc(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 Tdc(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 Tdc(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xefff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xefff0000
168	fe 0 after 12 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
189	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	500.5	8.3	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	462.1	11.0	1 r	511.0	0.0
2 r	391.5	0.7	2 r	319.1	0.7	2 r	372.5	0.7	2 r	365.7	0.7	2 r	361.1	0.7	2 r	312.6	0.7	2 r	286.3	0.7	2 r	321.8	0.7
3	326.9	4.4	3	176.8	4.5	3	378.4	4.5	3	302.9	5.6	3	340.9	4.7	3	380.3	4.3	3	217.4	4.6	3	265.5	4.9
4	308.6	4.1	4	202.7	4.1	4	329.7	4.2	4	275.0	4.7	4	310.9	4.4	4	343.2	4.5	4	297.7	4.3	4	222.1	4.5
5	352.7	4.1	5	193.1	4.3	5	360.1	4.2	5	310.9	5.0	5	321.2	4.4	5	344.4	4.2	5	168.7	4.4	5	277.3	4.9
6	278.9	4.0	6	217.2	4.2	6	331.9	4.3	6	220.9	4.9	6	257.1	4.5	6	308.8	4.2	6	241.5	4.2	6	246.9	4.8
7	273.4	4.0	7	164.5	4.5	7	352.7	4.3	7	300.4	5.1	7	233.8	4.5	7	275.7	4.4	7	253.3	4.5	7	178.7	4.4
8	349.1	3.9	8	166.8	4.2	8	330.8	4.2	8	265.3	4.6	8	326.4	4.3	8	233.2	4.2	8	310.3	4.3	8	232.2	4.5
9	229.1	4.2	9	188.3	4.4	9	364.8	4.5	9	271.5	4.9	9	250.2	4.6	9	338.8	4.1	9	222.2	4.3	9	195.1	4.5
10	274.2	4.0	10	225.1	4.3	10	363.5	4.1	10	253.0	4.5	10	248.0	4.5	10	290.2	4.2	10	205.6	4.3	10	210.0	4.5
11	276.6	4.2	11	184.0	4.3	11	324.5	4.3	11	218.7	4.7	11	264.7	4.3	11	293.4	4.2	11	320.6	4.2	11	257.1	4.7
12	356.8	3.9	12	272.7	4.5	12	441.4	4.2	12	266.5	4.3	12	265.7	4.2	12	360.6	4.2	12	290.1	4.5	12	329.9	4.3
13	290.8	4.0	13	115.9	4.3	13	312.7	4.2	13	243.8	4.7	13	285.5	4.3	13	282.7	4.4	13	296.1	4.3	13	173.7	4.2
14	220.9	4.4	14	200.4	4.3	14	346.4	4.2	14	237.8	4.4	14	284.1	4.2	14	373.7	4.3	14	243.0	4.2	14	171.7	4.4
15 f	323.2	1.6	15 f	209.6	1.7	15 f	359.3	1.6	15 f	256.6	1.6	15 f	197.8	1.6	15 f	304.6	1.6	15 f	184.8	1.8	15 f	273.0	1.7
16	354.4	4.2	16	175.3	4.3	16	326.4	4.3	16	275.7	4.7	16	276.2	4.5	16	207.6	4.1	16	235.3	4.3	16	231.3	4.7
17	251.7	3.9	17	159.4	4.4	17	276.2	4.2	17	269.2	4.3	17	190.8	4.2	17	328.6	4.3	17	267.4	4.2	17	265.3	4.4
18	292.9	4.0	18	178.4	4.2	18	355.6	4.0	18	208.0	4.8	18	289.4	4.5	18	262.7	4.3	18	208.3	4.3	18	180.0	4.5
19	227.7	4.2	19	292.6	4.2	19	361.2	4.1	19	269.2	4.5	19	293.6	4.2	19	254.7	4.1	19	228.7	4.2	19	185.6	4.4
20	339.1	4.1	20	187.3	4.0	20	342.5	4.5	20	295.2	4.6	20	265.7	4.3	20	262.3	4.2	20	348.1	4.2	20	171.9	4.3
21	351.5	4.5	21	198.9	4.2	21	293.8	3.9	21	258.8	4.5	21	184.3	4.5	21	282.7	4.2	21	225.7	4.1	21	291.6	4.4
22	316.4	4.0	22	215.0	4.3	22	278.2	4.3	22	182.3	4.6	22	273.7	4.2	22	281.1	4.0	22	217.8	4.2	22	183.0	4.3
23	291.6	3.8	23	245.7	4.3	23	353.9	4.3	23	266.2	4.4	23	266.1	4.3	23	317.9	4.4	23	111.5	4.3	23	198.2	4.4
24	288.5	4.1	24	203.9	4.4	24	347.6	4.2	24	274.3	4.7	24	268.7	4.4	24	246.3	4.3	24	173.8	4.4	24	313.0	4.5
25	354.5	4.5	25	206.0	4.1	25	334.8	4.0	25	265.9	4.5	25	220.7	4.2	25	194.8	4.0	25	260.8	4.1	25	224.5	4.7
26	337.6	4.1	26	217.6	4.3	26	312.9	4.3	26	289.9	4.7	26	251.5	4.2	26	273.0	4.3	26	227.1	4.3	26	219.4	4.5
27	245.4	3.9	27	167.6	4.0	27	299.2	4.1	27	275.4	4.5	27	258.0	4.2	27	306.6	4.1	27	149.1	3.9	27	276.3	4.4
28 f	294.7	1.7	28 f	192.4	1.7	28 f	352.8	1.8	28 f	313.7	1.7	28 f	284.9	1.8	28 f	214.4	1.7	28 f	200.2	1.7	28 f	130.8	1.9
29	295.9	4.2	29	273.8	4.0	29	322.8	4.4	29	252.2	4.8	29	186.2	4.3	29	337.3	4.3	29	268.1	4.2	29	219.5	4.3
30	310.1	4.3	30	197.9	4.2	30	304.8	4.1	30	352.2	4.2	30	285.8	4.2	30	248.0	4.3	30	343.3	4.2	30	312.5	4.6
31	337.8	4.2	31	211.5	4.2	31	357.3	4.3	31	316.9	4.6	31	328.3	4.2	31	297.5	4.3	31	207.3	4.2	31	268.1	4.5
32	319.1	4.0	32	160.2	4.2	32	344.7	3.9	32	313.9	4.3	32	347.1	4.3	32	295.1	4.5	32	188.8	4.3	32	245.4	4.4
33	269.8	4.1	33	274.4	4.1	33	285.1	4.0	33	228.8	4.5	33	219.4	4.3	33	138.7	4.3	33	178.8	4.2	33	247.2	4.4
34	310.6	4.0	34	251.0	3.9	34	367.3	4.1	34	236.8	4.4	34	268.5	4.1	34	341.0	4.1	34	120.1	4.2	34	273.1	4.3
35	278.4	4.0	35	278.9	4.1	35	294.1	4.0	35	315.5	4.6	35	185.9	4.2	35	327.0	4.3	35	318.2	4.3	35	244.7	4.4
36	309.1	3.9	36	274.3	4.2	36	303.4	4.2	36	279.0	4.3	36	297.2	4.1	36	306.4	4.1	36	259.6	4.1	36	266.0	4.5
37	318.9	3.8	37	207.3	4.2	37	374.4	4.2	37	200.2	4.4	37	360.4	4.3	37	294.8	4.1	37	213.6	4.2	37	286.1	4.5
38	318.5	3.9	38	240.7	4.0	38	233.6	3.9	38	288.2	4.5	38	248.5	4.1	38	174.6	4.3	38	199.7	4.0	38	241.8	4.4
39	300.4	4.3	39	185.7	4.0	39	276.7	4.2	39	269.1	4.7	39	323.7	4.4	39	329.6	4.3	39	168.1	4.5	39	240.2	4.7
40	323.2	4.4	40	204.9	4.1	40	316.5	3.8	40	302.4	4.3	40	322.1	4.2	40	185.4	4.0	40	242.3	3.9	40	256.2	4.3
41	349.8	3.7	41	211.2	4.1	41	315.3	3.8	41	278.1	3.9	41	237.8	4.1	41	317.7	3.8	41	237.7	4.0	41	223.5	4.5
42	366.2	3.8	42	264.4	4.1	42	313.1	3.7	42	248.4	4.4	42	315.2	4.3	42	287.0	4.0	42	233.2	4.2	42	202.7	4.5
43	388.7	3.5	43	266.9	3.9	43	238.1	3.7	43	305.7	4.0	43	295.3	3.8	43	228.9	4.0	43	147.5	4.0	43	221.6	4.6
44	350.6	3.7	44	241.5	3.8	44	295.2	3.9	44	309.0	4.0	44	265.2	4.1	44	196.5	4.1	44	171.0	4.2	44	246.2	4.5
45	282.3	3.7	45	188.6	3.8	45	323.5	4.4	45	256.8	3.8	45	270.4	3.8	45	304.7	3.8	45	238.0	4.0	45	256.5	4.4
46	337.7	4.2	46	208.3	3.8	46	298.1	4.1	46	303.3	4.0	46	234.0	3.8	46	258.0	4.1	46	267.0	4.0	46	292.2	4.5
47	228.1	3.8	47	236.1	4.0	47	312.0	3.8	47	287.6	4.3	47	277.5	4.0	47	203.9	3.9	47	240.2	4.1	47	270.0	4.2
48	232.5	3.9	48	273.3	3.9	48	318.6	3.8	48	299.8	4.5	48	278.4	3.9	48	245.3	4.1	48	206.6	3.9	48	237.8	4.6
49	371.8	3.8	49	191.0	4.0	49	318.1	3.8	49	211.1	4.0	49	276.9	3.9	49	250.6	4.2	49	235.0	4.0	49	277.6	4.2
50	360.6	3.8	50	217.0	4.0	50	365.7	4.1	50	269.2	4.1	50	273.5	3.9	50	310.5	4.2	50	306.4	4.2	50	257.2	4.5
51	385.6	3.9	51	190.9	4.0	51	368.0	3.9	51	259.3	4.0	51	231.4	3.9	51	328.9	4.2	51	302.6	4.1	51	272.5	4.3
52	255.5	4.1	52	245.6	4.0	52	291.1	4.1	52	269.9	4.1	52	242.2	4.0	52	169.2	4.1	52	172.7	4.2	52	355.8	4.7
53 f	303.1	1.4	53 f	205.2	1.6	53 f	319.6	1.6	53 f	335.3	1.6	53 f	224.2	1.6	53 f	357.0	1.7	53 f	227.1	1.7	53 f	243.5	1.7
54	292.2	4.1	54	140.6	4.0	54	344.6	3.9	54	279.4	4.3	54	269.2	4.0	54	250.7	4.1	54	235.7	4.1	54	173.3	4.5
55	316.7	3.9	55	248.1	4.0	55	351.3	4.0	55	210.7	4.1	55	242.2	4.0	55	263.5	4.2	55	127.4	4.4	55	275.5	4.6
56	332.9	3.7	56	208.2	4.0	56	386.0	3.7	56	303.6	3.9	56	331.6	4.0	56	271.6	3.9	56	312.1	4.3	56	206.2	4.6
57	344.1	3.8	57	268.2	4.0	57	380.1	4.0	57	272.1	4.3	57	170.3	4.3	57	241.8	4.0	57	147.5	4.2	57	285.5	4.7
58	297.7	4.0	58	175.9	4.2	58	354.5	3.8	58	258.9	3.9	58	258.7</										

Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	511.0	0.0	1 r	249.9	11.3	1 r	461.7	10.3	1 r	494.7	6.2	1 r	466.2	8.9	1 r	454.4	10.9	1 r	251.3	11.3	1 r	316.2	11.7
2 r	250.3	0.7	2 r	250.1	0.7	2 r	249.6	0.7	2 r	249.8	0.7	2 r	250.2	0.7	2 r	249.8	0.7	2 r	250.4	0.7	2 r	249.8	0.7
3	249.4	4.5	3	248.2	4.5	3	251.9	4.7	3	250.3	5.6	3	250.2	5.0	3	249.6	4.6	3	251.5	4.4	3	252.4	4.7
4	250.5	4.3	4	249.9	4.1	4	250.3	4.3	4	250.2	4.8	4	249.8	4.2	4	250.1	4.2	4	250.3	4.2	4	251.3	4.6
5	250.5	4.3	5	251.0	4.4	5	248.7	4.3	5	250.3	5.2	5	249.5	4.6	5	250.2	4.3	5	249.5	4.4	5	252.9	4.7
6	250.5	4.2	6	250.8	4.3	6	249.7	4.1	6	250.0	4.9	6	248.5	4.4	6	250.6	4.3	6	251.1	4.5	6	251.2	4.4
7	250.4	4.3	7	249.8	4.4	7	249.6	4.3	7	249.9	5.5	7	249.1	4.4	7	250.2	4.3	7	251.8	4.4	7	249.9	4.6
8	249.6	4.3	8	249.8	4.0	8	249.4	4.2	8	250.9	5.0	8	251.6	4.4	8	250.4	4.2	8	250.8	4.4	8	250.9	4.2
9	250.1	4.3	9	251.3	4.4	9	250.6	4.5	9	251.1	4.9	9	250.3	4.6	9	249.7	4.4	9	250.9	4.5	9	249.5	4.4
10	250.8	4.2	10	251.3	4.2	10	250.7	4.3	10	250.9	4.5	10	249.9	4.5	10	250.6	4.2	10	252.0	4.2	10	249.6	4.4
11	248.9	4.3	11	250.0	4.3	11	250.4	4.3	11	250.5	4.9	11	249.3	4.4	11	251.1	4.5	11	249.4	4.3	11	251.5	4.7
12	250.1	4.0	12	250.3	4.2	12	252.0	4.2	12	249.1	4.4	12	249.9	4.2	12	248.8	4.2	12	250.1	4.4	12	248.7	4.3
13	248.3	4.2	13	250.0	4.3	13	250.6	4.3	13	250.1	4.7	13	251.6	4.3	13	249.6	4.4	13	250.7	4.4	13	248.0	4.7
14	250.4	4.0	14	250.9	4.2	14	250.1	4.2	14	251.1	4.6	14	250.5	4.3	14	249.7	4.3	14	249.6	4.2	14	249.1	4.4
15 f	250.3	1.6	15 f	250.2	1.7	15 f	250.9	1.6	15 f	249.6	1.7	15 f	250.4	1.7	15 f	249.8	1.5	15 f	249.8	1.7	15 f	249.7	1.7
16	250.9	4.1	16	250.8	4.1	16	251.4	4.3	16	249.6	4.9	16	250.9	4.4	16	249.7	4.3	16	250.3	4.4	16	250.7	4.5
17	249.7	4.0	17	250.9	4.3	17	250.3	4.0	17	250.0	4.5	17	249.6	4.2	17	250.0	4.4	17	250.2	4.2	17	250.2	4.3
18	249.2	4.2	18	249.6	4.0	18	248.6	4.1	18	249.9	4.7	18	251.0	4.5	18	249.9	4.3	18	250.7	4.3	18	249.6	4.7
19	249.6	4.0	19	250.0	4.2	19	251.3	4.2	19	251.3	4.4	19	250.6	4.0	19	249.5	4.1	19	250.2	4.1	19	249.0	4.6
20	250.8	4.3	20	250.4	4.1	20	250.6	4.3	20	250.9	5.0	20	249.0	4.4	20	250.7	4.2	20	248.8	4.5	20	249.3	4.3
21	250.4	4.1	21	249.6	4.3	21	249.7	4.3	21	251.9	4.5	21	250.4	4.4	21	250.4	4.4	21	248.8	4.1	21	249.0	4.5
22	249.9	4.1	22	249.7	4.1	22	250.4	4.1	22	250.4	4.4	22	249.6	4.3	22	250.4	4.3	22	248.5	4.3	22	250.7	4.7
23	249.5	4.4	23	249.3	4.1	23	249.4	4.1	23	249.8	4.5	23	250.0	4.1	23	250.9	4.2	23	250.8	4.4	23	250.8	4.5
24	250.3	4.1	24	250.3	4.1	24	251.1	4.2	24	249.7	4.7	24	251.4	4.3	24	250.1	4.4	24	250.1	4.3	24	250.6	4.7
25	251.0	4.0	25	250.1	3.9	25	250.7	4.1	25	249.4	4.7	25	249.2	4.3	25	249.0	4.1	25	250.0	4.3	25	250.2	4.3
26	250.6	4.0	26	249.9	4.1	26	249.7	4.3	26	250.3	4.6	26	249.5	4.2	26	249.8	3.9	26	250.4	4.5	26	251.4	4.7
27	250.6	3.8	27	249.1	4.1	27	250.1	4.1	27	250.7	4.5	27	250.5	4.2	27	251.4	4.2	27	251.0	4.5	27	251.2	4.5
28 f	249.8	1.7	28 f	250.3	1.8	28 f	249.8	1.6	28 f	250.0	1.7	28 f	250.1	1.6	28 f	250.7	1.7	28 f	250.4	1.9	28 f	250.5	1.8
29	250.7	3.8	29	249.3	4.2	29	248.5	4.2	29	251.8	4.6	29	250.7	4.2	29	250.8	4.4	29	251.6	4.2	29	249.2	4.5
30	249.4	3.9	30	250.6	4.1	30	250.1	4.0	30	249.8	4.5	30	250.5	4.1	30	249.9	4.2	30	249.8	4.4	30	249.5	4.3
31	249.3	4.0	31	249.3	4.3	31	250.0	4.2	31	249.4	4.5	31	250.5	3.9	31	248.7	4.2	31	251.6	4.3	31	249.7	5.1
32	251.3	4.0	32	250.2	4.4	32	249.0	4.0	32	249.2	4.4	32	251.3	4.1	32	249.6	4.2	32	250.9	4.1	32	251.1	4.4
33	249.7	4.0	33	250.7	4.4	33	251.1	4.0	33	249.7	4.4	33	251.2	4.8	33	250.4	4.2	33	249.1	4.3	33	247.9	4.5
34	249.4	4.0	34	250.4	4.2	34	249.9	4.0	34	250.8	4.3	34	250.2	4.3	34	250.8	4.2	34	249.8	4.4	34	251.3	4.3
35	250.2	4.0	35	250.1	4.2	35	251.2	4.2	35	249.7	4.7	35	249.8	4.1	35	250.0	4.2	35	248.9	4.4	35	248.5	4.5
36	250.4	4.0	36	251.2	4.4	36	250.7	4.0	36	250.6	4.5	36	251.3	4.1	36	251.1	4.3	36	250.2	4.3	36	249.7	4.5
37	250.2	4.1	37	250.2	4.1	37	251.2	4.2	37	250.9	4.7	37	251.0	4.4	37	250.1	4.1	37	250.7	4.3	37	249.5	4.6
38	249.2	3.9	38	250.2	4.2	38	249.5	4.1	38	249.5	4.1	38	249.4	4.1	38	249.9	4.2	38	249.0	4.2	38	249.9	4.5
39	250.0	4.3	39	249.5	4.5	39	249.3	4.3	39	250.1	4.8	39	249.2	4.4	39	248.7	4.3	39	250.6	4.3	39	250.0	4.7
40	249.8	3.9	40	249.8	4.0	40	250.0	3.9	40	250.6	4.4	40	250.5	4.0	40	250.0	4.2	40	250.2	3.9	40	250.2	4.4
41	251.2	4.1	41	250.4	3.9	41	250.1	3.9	41	250.9	4.0	41	249.7	4.2	41	250.9	4.0	41	250.4	4.1	41	250.6	4.5
42	249.8	3.9	42	251.3	4.1	42	251.0	4.0	42	250.1	4.2	42	250.4	4.0	42	248.9	4.0	42	249.7	4.2	42	250.5	4.4
43	251.1	3.8	43	250.3	4.2	43	249.8	3.9	43	250.2	3.9	43	250.7	3.8	43	249.8	4.1	43	249.0	3.9	43	249.0	4.3
44	247.7	3.8	44	250.1	4.0	44	252.1	3.9	44	250.1	4.3	44	250.2	4.0	44	248.7	4.1	44	250.0	4.2	44	248.9	4.7
45	250.4	4.0	45	250.6	4.0	45	250.3	3.8	45	251.1	4.1	45	251.9	3.8	45	249.8	4.0	45	249.5	4.0	45	248.5	4.5
46	250.0	3.7	46	250.9	4.3	46	250.4	3.8	46	251.2	4.1	46	250.3	4.0	46	249.3	4.0	46	250.2	4.2	46	250.9	4.7
47	249.4	3.8	47	250.0	4.0	47	251.5	3.8	47	249.9	4.0	47	250.6	4.1	47	250.0	3.8	47	248.5	4.0	47	249.9	4.6
48	248.5	3.9	48	251.0	4.1	48	250.7	3.9	48	249.8	4.2	48	251.3	4.0	48	250.4	4.1	48	249.5	4.3	48	249.6	4.7
49	249.9	3.9	49	250.5	3.9	49	250.6	3.9	49	250.6	3.9	49	248.9	4.1	49	249.8	3.9	49	249.3	4.1	49	248.7	4.4
50	247.9	4.2	50	250.2	4.0	50	249.0	3.9	50	250.0	4.1	50	251.0	3.9	50	248.7	4.2	50	249.9	4.3	50	249.7	4.8
51	248.9	3.9	51	249.9	4.2	51	249.9	3.9	51	249.6	4.3	51	250.2	4.2	51	249.6	4.0	51	248.5	4.0	51	250.3	4.4
52	250.8	3.9	52	250.1	4.1	52	250.4	3.8	52	249.6	4.3	52	251.3	4.2	52	250.2	4.0	52	250.4	4.3	52	249.0	4.8
53 f	249.6	1.5	53 f	250.4	1.6	53 f	249.7	1.6	53 f	250.1	1.6	53 f	250.4	1.5	53 f	249.9	1.8	53 f	251.1	1.7	53 f	249.4	1.7
54	250.7	3.7	54	249.3	4.0	54	250.2	4.0	54	250.4	4.0	54	249.5	3.9	54	249.1	4.1	54	249.6	4.2	54	249.8	4.5
55	248.5	3.9	55	249.1	3.9	55	250.3	4.4	55	250.7	4.2	55	249.6	4.0	55	251.2	4.2	55	251.9	4.5	55	248.1	4.9
56	250.4	3.7	56	251.5	4.0	56	249.8	3.9	56	248.7	4.1	56	249.4	3.9	56	249.3	4.1	56	251.6	4.3	56	249.7	4.6
57	250.2	3.9	57	250.3	4.2	57	250.1	4.1	57	249.3	4.2	57	251.4	4.0	57	251.2	4.0	57	250.7	4.5	57	249.3	4.9
58	249.0	4.1	58	249.7	4.0	58	249.2	4.3	58	250.8													