

Fec test report:

Date: 2020-10-26 15:30:01

Tester name: Boris

Test#1 Monitoring values

Passed

| | | | |
|---|------------------------|------------------|----|
| 0 | FEC label | 008 | OK |
| 1 | FEC DC2438 ID | ec0000024d999d26 | OK |
| 2 | FEC_T (to 35°C) | 29.156 | OK |
| 3 | FEC_Vdd (3.2V to 3.4V) | 3.270 | OK |
| 4 | FEC_I (1.1A to 1.5A) | 1.492 | OK |
| 5 | FEC_Vad (1.9V to 2.0V) | 1.940 | OK |

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

| | | | | |
|----|----------------|---------|-----------|----|
| 8 | After chip #8 | Mean OK | STDDEV OK | OK |
| 9 | After chip #9 | Mean OK | STDDEV OK | OK |
| 10 | After chip #10 | Mean OK | STDDEV OK | OK |
| 11 | After chip #11 | Mean OK | STDDEV OK | OK |
| 12 | After chip #12 | Mean OK | STDDEV OK | OK |
| 13 | After chip #13 | Mean OK | STDDEV OK | OK |
| 14 | After chip #14 | Mean OK | STDDEV OK | OK |
| 15 | After chip #15 | Mean OK | STDDEV OK | OK |

Test#4 AD9637 test patterns

Passed

| | | | | |
|---|----------------|--|-------------------|----|
| 0 | ADC channel #0 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 1 | ADC channel #1 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 2 | ADC channel #2 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 3 | ADC channel #3 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |
| 4 | ADC channel #4 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 5 | ADC channel #5 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 6 | ADC channel #6 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 7 | ADC channel #7 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |

Test#5 Pulser run

Passed

| | | | | |
|----|----------------|-----------------------------------|----------------|----|
| 8 | After chip #8 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3048 | OK |
| 9 | After chip #9 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 2994 | OK |
| 10 | After chip #10 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3110 | OK |
| 11 | After chip #11 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 2991 | OK |
| 12 | After chip #12 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3168 | OK |
| 13 | After chip #13 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3046 | OK |
| 14 | After chip #14 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3080 | OK |
| 15 | After chip #15 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3068 | OK |

FEC test final result:

Passed

| Monitoring test | | | |
|-----------------|---------------------------|-------|---|
| NO | Command | Error | Response |
| 0 | fe fec_enable 2 | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x80000 |
| 1 | fe 0 moni T 1 | 0 | 0 Tdc(2) Fem(00) FEC_T: 29.156 degC |
| 2 | fe 0 moni V 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vdd: 3.270 V |
| 3 | fe 0 pulser 1 model T2K2 | 0 | 0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 4 | fe 0 pulser 1 base 0x3FFF | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 5 | fe 0 pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 6 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.940 V |
| 7 | fe 0 moni I 1 | 0 | 0 Tdc(2) Fem(00) FEC_I: 1.492 A |
| 8 | fe 0 moni S 1 | 0 | 0 Tdc(2) Fem(00) FEC_Serial: ec0000024d999d26 |

| Slow control registers test | | | |
|-----------------------------|---|-------|--|
| NO | Command | Error | Response |
| 0 | fe 0 mode after | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe fec_enable 2 | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x80000 |
| 2 | fe fec_enable | 0 | 0 Tdc(2) Fem(00) Reg(1) = 0x12088000 (302546944) FEC_Enable: 2 |
| 3 | fe 0 after 8 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 4 | fe 0 after 9 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 5 | fe 0 after 10 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 6 | fe 0 after 11 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 7 | fe 0 after 12 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 8 | fe 0 after 13 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 9 | fe 0 after 14 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 10 | fe 0 after 15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 11 | fe 0 after 8 wrchk 3 0x0 0x0909 0x0909 | 0 | 0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified) |
| 12 | fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a | 0 | 0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified) |
| 13 | fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b | 0 | 0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0b0b 0x0b0b (1 chip verified) |
| 14 | fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c | 0 | 0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0c0c 0x0c0c (1 chip verified) |
| 15 | fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d | 0 | 0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0d0d 0x0d0d (1 chip verified) |
| 16 | fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e | 0 | 0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified) |
| 17 | fe 0 after 14 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 18 | fe 0 after 15 wrchk 3 0x0 0x0101 0x0101 | 0 | 0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified) |
| 19 | fe 0 after 8 read 3 | 0 | 0 Tdc(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909 |
| 20 | fe 0 after 9 read 3 | 0 | 0 Tdc(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a |
| 21 | fe 0 after 10 read 3 | 0 | 0 Tdc(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b |
| 22 | fe 0 after 11 read 3 | 0 | 0 Tdc(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c |
| 23 | fe 0 after 12 read 3 | 0 | 0 Tdc(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d |
| 24 | fe 0 after 13 read 3 | 0 | 0 Tdc(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e |
| 25 | fe 0 after 14 read 3 | 0 | 0 Tdc(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0 |
| 26 | fe 0 after 15 read 3 | 0 | 0 Tdc(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101 |
| 27 | fe 0 after 8 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 28 | fe 0 after 9 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 29 | fe 0 after 10 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 30 | fe 0 after 11 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 31 | fe 0 after 12 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 32 | fe 0 after 13 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 33 | fe 0 after 14 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 34 | fe 0 after 15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |

| ADC pattern test | | | |
|------------------|--------------------------|-------|--|
| NO | Command | Error | Response |
| 0 | fe 0 mode after | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe 0 test_mode | 0 | 0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0 |
| 2 | be 0 state eb | 0 | 0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current |
| 3 | be 0 state tg | 0 | 0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG) |
| 4 | be 0 state pm | 0 | 0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE) |
| 5 | fe 0 state | 0 | 0 Tdc(2) Fem(00) State = 0x3 (Aligned_SCA_Write) |
| 6 | daq 0xFFFFF F | 0 | 0 Tdc(2): daq paused |
| 7 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 8 | fe 0 emit_empty_ch 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 10 | fe 0 keep_rst 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 11 | fe 0 skip_rst 2 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x40000 |
| 12 | fe adc 1 model AD9637 | 0 | 0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637) |
| 13 | fe adc 1 write 0x14 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0) |
| 14 | fe adc 1 write 0x4 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 15 | fe adc 1 write 0x5 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1) |
| 16 | fe adc 1 write 0xD 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 17 | fe adc 1 write 0x4 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 18 | fe adc 1 write 0x5 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2) |
| 19 | fe adc 1 write 0xD 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 20 | fe adc 1 write 0x4 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |

| | | | |
|----|-------------------------|---|--|
| 21 | fe adc 1 write 0x5 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4) |
| 22 | fe adc 1 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 23 | fe adc 1 write 0x4 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 24 | fe adc 1 write 0x5 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8) |
| 25 | fe adc 1 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 26 | fe adc 1 write 0x4 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1) |
| 27 | fe adc 1 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 28 | fe adc 1 write 0xD 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 29 | fe adc 1 write 0x4 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2) |
| 30 | fe adc 1 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 31 | fe adc 1 write 0xD 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 32 | fe adc 1 write 0x4 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4) |
| 33 | fe adc 1 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 34 | fe adc 1 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 35 | fe adc 1 write 0x4 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8) |
| 36 | fe adc 1 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 37 | fe adc 1 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 38 | fe 0 subtract_ped 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 39 | fe 0 zero_suppress 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 40 | fe 0 zs_pre_post 4 8 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0xc4 |
| 41 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdc(2) Reg(0) <- 0x0 |
| 42 | be 0 eb check_ev_nb 1 | 0 | 0 Tdc(2) Reg(0) <- 0x800000 |
| 43 | be 0 eb check_ev_ts 1 | 0 | 0 Tdc(2) Reg(0) <- 0x1000000 |
| 44 | be 0 eb ts_tolerance 0 | 0 | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 45 | be 0 event_limit 0x0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 46 | be 0 trig_rate 0 50 | 0 | 0 Tdc(2) Reg(6) <- 0x32 |
| 47 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 48 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 49 | be 0 trig_ena 1 | 0 | 0 Tdc(2) Reg(6) <- 0x1000 |
| 50 | be 0 trig_ena 0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 51 | be 0 state eb | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current) |
| 52 | be 0 state tg | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS) |
| 53 | be 0 state pm | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE) |
| 54 | fe 0 state | 0 | 0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready) |
| 55 | fe adc 1 write 0x4 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15) |
| 56 | fe adc 1 write 0x5 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15) |
| 57 | fe adc 1 write 0xD 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0) |

| Pulser test | | | |
|-------------|-------------------------------------|-------|--|
| NO | Command | Error | Response |
| 0 | daq 0xFFFF F | 0 | 0 Tdc(2): daq paused |
| 1 | fe 0 after 8:15 wrchk 3 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 2 | fe 0 after 8:15 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 3 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 4 | fe 0 emit_empty_ch 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 5 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 6 | fe 0 keep_rst 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 7 | fe 0 skip_rst 2 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x40000 |
| 8 | fe 0 test_enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 test_mode 1 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x400 |
| 10 | fe 0 tdata A 0x1FF | 0 | 0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510 |
| 11 | fe 0 test_zbt 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 12 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 13 | fe 0 asic_mask | 0 | 0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0 |
| 14 | fe 0 pulser 1 enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x0 |
| 15 | fe 0 pulser 1 ft_enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x0 |
| 16 | fe 0 pulser 1 model T2K2 | 0 | 0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 17 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 18 | fe 0 pulser 1 ampl 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff |
| 19 | fe 0 pulser 1 delay 3000 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0xbb8 |
| 20 | fe pulser load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 21 | fe 0 pulser 1 enable 1 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x10000 |
| 22 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdc(2) Reg(0) <- 0x0 |
| 23 | be 0 eb check_ev_nb 1 | 0 | 0 Tdc(2) Reg(0) <- 0x800000 |
| 24 | be 0 eb check_ev_ts 1 | 0 | 0 Tdc(2) Reg(0) <- 0x1000000 |
| 25 | be 0 eb ts_tolerance 0 | 0 | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 26 | be 0 event_limit 0x0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 27 | be 0 trig_rate 0 50 | 0 | 0 Tdc(2) Reg(6) <- 0x32 |
| 28 | be 0 trig_delay 0 0 | 0 | 0 Tdc(2) Reg(8) <- 0x0 |
| 29 | be 0 trig_delay 1 0 | 0 | 0 Tdc(2) Reg(8) <- 0x0 |
| 30 | be 0 trig_delay 2 0 | 0 | 0 Tdc(2) Reg(9) <- 0x0 |
| 31 | be 0 trig_delay 3 0 | 0 | 0 Tdc(2) Reg(9) <- 0x0 |
| 32 | be 0 ss_trig_delay 0x4 | 0 | 0 Tdc(2) Reg(14) <- 0x4 |
| 33 | be 0 ss_trig_ena 1 | 0 | 0 Tdc(2) Reg(6) <- 0x10000 |
| 34 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 35 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 36 | be 0 isobus 0x0C | 0 | 0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear) |

| | | | |
|-----|---|---|---|
| 37 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 38 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 39 | fe 0 asic_mask 0xfeff | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfeff0000 |
| 40 | fe 0 after 8 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration |
| 41 | fe 0 after 8 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 42 | fe 0 after 8 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 43 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 44 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 45 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 46 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 47 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 48 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 49 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 50 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 51 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 52 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 53 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 54 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 55 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 56 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 57 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 58 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 59 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 60 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 61 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 62 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 63 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 64 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 65 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 66 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 67 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 68 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 69 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 70 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 71 | fe 0 asic_mask 0xfdf | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfdf0000 |
| 72 | fe 0 after 9 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration |
| 73 | fe 0 after 9 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 74 | fe 0 after 9 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 75 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 76 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 77 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 78 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 79 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 80 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 81 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 82 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 83 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 84 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 85 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 86 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 87 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 88 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 89 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 90 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 91 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 92 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 93 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 94 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 95 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 96 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 97 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 98 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 99 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 100 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 101 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 102 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 103 | fe 0 asic_mask 0xfbff | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfbff0000 |
| 104 | fe 0 after 10 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration |
| 105 | fe 0 after 10 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 106 | fe 0 after 10 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 107 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 108 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 109 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 110 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 111 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 112 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 113 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 114 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |

| | | | |
|-----|---|---|--|
| 115 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 116 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 117 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 118 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 119 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 120 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 121 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 122 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 123 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 124 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 125 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 126 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 127 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 128 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 129 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 130 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 131 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 132 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 133 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 134 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 135 | fe 0 asic_mask 0xf7ff | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xf7ff0000 |
| 136 | fe 0 after 11 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration |
| 137 | fe 0 after 11 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 138 | fe 0 after 11 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 139 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 140 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 141 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 142 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 143 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 144 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 145 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 146 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 147 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 148 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 149 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 150 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 151 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 152 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 153 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 154 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 155 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 156 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 157 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 158 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 159 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 160 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 161 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 162 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 163 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 164 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 165 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 166 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 167 | fe 0 asic_mask 0xefff | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xefff0000 |
| 168 | fe 0 after 12 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration |
| 169 | fe 0 after 12 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 170 | fe 0 after 12 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 171 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 172 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 173 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 174 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 175 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 176 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 177 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 178 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 179 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 180 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 181 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 182 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 183 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 184 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 185 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 186 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 187 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 188 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 189 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 190 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 191 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 192 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |

| | | | |
|-----|---|---|---|
| 193 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 194 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 195 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 196 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 197 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 198 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 199 | fe 0 asic_mask 0xdfff | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000 |
| 200 | fe 0 after 13 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration |
| 201 | fe 0 after 13 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 202 | fe 0 after 13 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 203 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 204 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 205 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 206 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 207 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 208 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 209 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 210 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 211 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 212 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 213 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 214 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 215 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 216 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 217 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 218 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 219 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 220 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 221 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 222 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 223 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 224 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 225 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 226 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 227 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 228 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 229 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 230 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 231 | fe 0 asic_mask 0xbfff | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000 |
| 232 | fe 0 after 14 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration |
| 233 | fe 0 after 14 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 234 | fe 0 after 14 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 235 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 236 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 237 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.940 V |
| 238 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 239 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 240 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 241 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 242 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 243 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 244 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 245 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 246 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 247 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 248 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 249 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 250 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 251 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 252 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 253 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 254 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 255 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 256 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 257 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 258 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 259 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 260 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 261 | fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 262 | fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 263 | fe 0 asic_mask 0x7fff | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000 |
| 264 | fe 0 after 15 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration |
| 265 | fe 0 after 15 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 266 | fe 0 after 15 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 267 | fe 0 pulser 1 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 268 | fe pulser 1 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 269 | fe 0 moni A 1 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 270 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |

| | | | |
|-----|--------------------------|---|--|
| 271 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 272 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 273 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 274 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 275 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 276 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 277 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 278 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 279 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 280 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 281 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 282 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 283 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 284 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 285 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 286 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 287 | fe 0 pulser 1 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 288 | fe pulser 1 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 289 | fe 0 moni A 1 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 290 | fe 0 pulser 1 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 291 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 292 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 293 | be 0 trig_ena 0 | 0 | 0 Tdcm(2) Reg(6) <- 0x0 |

Pedestal data before centermean

| CHIP 8 | | | CHIP 9 | | | CHIP 10 | | | CHIP 11 | | | CHIP 12 | | | CHIP 13 | | | CHIP 14 | | | CHIP 15 | | |
|--------|-------|-----|--------|-------|-----|---------|-------|-----|---------|-------|-----|---------|-------|-----|---------|-------|-----|---------|-------|-----|---------|-------|-----|
| CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD |
| 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 |
| 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 505.6 | 6.2 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 |
| 2 r | 300.8 | 0.7 | 2 r | 272.6 | 0.7 | 2 r | 299.2 | 0.6 | 2 r | 317.9 | 0.6 | 2 r | 253.1 | 0.7 | 2 r | 333.0 | 0.6 | 2 r | 302.2 | 0.7 | 2 r | 288.5 | 0.7 |
| 3 | 303.6 | 4.5 | 3 | 219.3 | 4.3 | 3 | 332.4 | 4.4 | 3 | 304.7 | 5.3 | 3 | 209.0 | 4.8 | 3 | 320.8 | 4.5 | 3 | 244.5 | 4.5 | 3 | 216.2 | 4.6 |
| 4 | 230.2 | 4.3 | 4 | 158.2 | 4.3 | 4 | 304.2 | 4.3 | 4 | 187.1 | 4.7 | 4 | 149.4 | 4.7 | 4 | 288.4 | 4.3 | 4 | 259.6 | 4.4 | 4 | 133.8 | 4.6 |
| 5 | 225.8 | 4.2 | 5 | 186.2 | 4.3 | 5 | 287.3 | 4.6 | 5 | 205.1 | 5.0 | 5 | 211.7 | 4.4 | 5 | 284.7 | 4.7 | 5 | 244.5 | 4.4 | 5 | 196.8 | 4.5 |
| 6 | 260.1 | 4.1 | 6 | 179.7 | 4.1 | 6 | 189.2 | 4.4 | 6 | 241.7 | 4.6 | 6 | 145.7 | 4.7 | 6 | 326.1 | 4.1 | 6 | 197.6 | 4.3 | 6 | 178.9 | 4.2 |
| 7 | 260.9 | 4.2 | 7 | 146.7 | 4.4 | 7 | 276.7 | 4.5 | 7 | 184.4 | 5.0 | 7 | 269.9 | 4.6 | 7 | 276.9 | 4.2 | 7 | 183.8 | 4.5 | 7 | 271.9 | 4.6 |
| 8 | 205.1 | 4.4 | 8 | 116.6 | 4.2 | 8 | 234.2 | 4.3 | 8 | 260.4 | 4.2 | 8 | 150.4 | 4.5 | 8 | 279.8 | 4.1 | 8 | 152.0 | 4.3 | 8 | 188.9 | 4.4 |
| 9 | 296.3 | 4.2 | 9 | 188.4 | 4.3 | 9 | 260.6 | 4.5 | 9 | 274.3 | 4.8 | 9 | 242.7 | 4.5 | 9 | 383.0 | 4.3 | 9 | 257.0 | 4.3 | 9 | 256.2 | 4.6 |
| 10 | 330.4 | 4.6 | 10 | 207.9 | 4.2 | 10 | 252.4 | 4.1 | 10 | 161.8 | 4.7 | 10 | 124.6 | 4.6 | 10 | 337.3 | 4.2 | 10 | 181.9 | 4.2 | 10 | 172.9 | 4.2 |
| 11 | 261.1 | 4.4 | 11 | 184.9 | 4.2 | 11 | 271.5 | 4.2 | 11 | 214.4 | 4.6 | 11 | 226.1 | 4.3 | 11 | 352.8 | 4.3 | 11 | 217.5 | 4.2 | 11 | 258.9 | 4.3 |
| 12 | 294.2 | 4.1 | 12 | 176.3 | 4.2 | 12 | 341.9 | 4.2 | 12 | 280.5 | 4.5 | 12 | 179.2 | 4.6 | 12 | 338.9 | 4.5 | 12 | 199.8 | 4.2 | 12 | 173.4 | 4.5 |
| 13 | 289.8 | 4.5 | 13 | 176.8 | 4.0 | 13 | 257.4 | 4.2 | 13 | 208.3 | 4.6 | 13 | 216.3 | 4.5 | 13 | 268.9 | 4.4 | 13 | 291.3 | 4.3 | 13 | 217.9 | 4.4 |
| 14 | 257.2 | 4.1 | 14 | 155.8 | 4.3 | 14 | 275.1 | 4.0 | 14 | 247.8 | 4.5 | 14 | 137.3 | 4.7 | 14 | 339.0 | 4.1 | 14 | 235.6 | 4.3 | 14 | 298.9 | 4.3 |
| 15 f | 239.2 | 1.6 | 15 f | 216.5 | 1.6 | 15 f | 251.0 | 1.6 | 15 f | 220.1 | 1.6 | 15 f | 269.1 | 1.7 | 15 f | 267.4 | 1.6 | 15 f | 328.2 | 1.6 | 15 f | 267.4 | 1.8 |
| 16 | 306.8 | 4.1 | 16 | 143.2 | 4.0 | 16 | 241.8 | 4.3 | 16 | 233.3 | 4.9 | 16 | 145.4 | 4.3 | 16 | 288.2 | 4.3 | 16 | 204.7 | 4.1 | 16 | 290.1 | 4.5 |
| 17 | 218.6 | 4.2 | 17 | 131.5 | 4.3 | 17 | 262.6 | 4.3 | 17 | 169.7 | 4.3 | 17 | 118.2 | 4.5 | 17 | 312.3 | 4.2 | 17 | 322.0 | 4.2 | 17 | 170.8 | 4.2 |
| 18 | 167.1 | 4.2 | 18 | 193.4 | 4.1 | 18 | 252.6 | 4.2 | 18 | 147.6 | 4.6 | 18 | 240.3 | 4.7 | 18 | 317.4 | 4.2 | 18 | 247.7 | 4.2 | 18 | 224.5 | 4.4 |
| 19 | 245.0 | 4.1 | 19 | 187.3 | 4.3 | 19 | 260.5 | 4.5 | 19 | 227.9 | 4.4 | 19 | 129.5 | 4.7 | 19 | 233.0 | 4.3 | 19 | 289.9 | 4.2 | 19 | 282.1 | 4.3 |
| 20 | 288.7 | 4.1 | 20 | 135.1 | 4.1 | 20 | 264.0 | 4.3 | 20 | 169.8 | 4.5 | 20 | 170.3 | 4.6 | 20 | 268.4 | 4.2 | 20 | 188.7 | 4.2 | 20 | 256.8 | 4.3 |
| 21 | 48.4 | 4.0 | 21 | 213.0 | 4.2 | 21 | 217.6 | 4.0 | 21 | 228.7 | 4.5 | 21 | 198.7 | 4.3 | 21 | 292.2 | 4.5 | 21 | 219.5 | 4.1 | 21 | 243.6 | 4.2 |
| 22 | 233.7 | 4.3 | 22 | 139.4 | 4.0 | 22 | 161.3 | 4.2 | 22 | 189.7 | 4.6 | 22 | 212.2 | 4.3 | 22 | 315.2 | 4.2 | 22 | 246.0 | 4.2 | 22 | 200.9 | 4.4 |
| 23 | 279.4 | 4.3 | 23 | 289.4 | 4.0 | 23 | 217.6 | 4.1 | 23 | 254.2 | 4.3 | 23 | 164.7 | 4.5 | 23 | 344.6 | 4.3 | 23 | 226.0 | 4.0 | 23 | 202.3 | 4.5 |
| 24 | 301.6 | 3.9 | 24 | 176.3 | 3.9 | 24 | 319.4 | 4.3 | 24 | 258.3 | 4.4 | 24 | 185.8 | 4.4 | 24 | 309.2 | 4.5 | 24 | 188.4 | 4.2 | 24 | 294.9 | 4.5 |
| 25 | 227.9 | 4.2 | 25 | 151.3 | 4.1 | 25 | 261.4 | 4.4 | 25 | 282.0 | 4.4 | 25 | 176.0 | 4.8 | 25 | 254.5 | 4.4 | 25 | 190.1 | 4.1 | 25 | 198.2 | 4.3 |
| 26 | 275.6 | 4.0 | 26 | 124.3 | 4.1 | 26 | 199.1 | 4.3 | 26 | 275.1 | 4.4 | 26 | 243.4 | 4.6 | 26 | 314.2 | 4.2 | 26 | 183.0 | 4.4 | 26 | 227.6 | 4.8 |
| 27 | 266.9 | 4.3 | 27 | 123.0 | 4.0 | 27 | 210.6 | 4.0 | 27 | 213.7 | 4.2 | 27 | 227.5 | 4.3 | 27 | 289.3 | 4.3 | 27 | 297.4 | 4.1 | 27 | 244.4 | 4.3 |
| 28 f | 196.3 | 1.8 | 28 f | 124.4 | 1.8 | 28 f | 232.8 | 1.7 | 28 f | 202.3 | 1.7 | 28 f | 213.5 | 1.6 | 28 f | 236.8 | 1.6 | 28 f | 221.6 | 1.7 | 28 f | 207.1 | 1.9 |
| 29 | 343.0 | 4.2 | 29 | 155.0 | 4.2 | 29 | 236.1 | 4.0 | 29 | 199.1 | 4.5 | 29 | 250.8 | 4.3 | 29 | 246.7 | 4.2 | 29 | 128.5 | 4.0 | 29 | 203.7 | 4.4 |
| 30 | 196.8 | 4.2 | 30 | 225.9 | 4.2 | 30 | 277.7 | 4.1 | 30 | 304.7 | 4.5 | 30 | 130.1 | 4.6 | 30 | 340.9 | 4.2 | 30 | 168.6 | 4.1 | 30 | 258.8 | 4.3 |
| 31 | 236.8 | 4.0 | 31 | 182.3 | 4.2 | 31 | 312.9 | 4.2 | 31 | 208.2 | 4.3 | 31 | 166.4 | 4.6 | 31 | 265.7 | 4.2 | 31 | 156.4 | 4.3 | 31 | 186.0 | 4.6 |
| 32 | 218.2 | 4.2 | 32 | 192.2 | 4.0 | 32 | 254.1 | 4.4 | 32 | 239.8 | 4.2 | 32 | 190.1 | 4.4 | 32 | 264.6 | 4.1 | 32 | 296.2 | 4.3 | 32 | 237.0 | 4.1 |
| 33 | 261.2 | 4.2 | 33 | 196.3 | 4.2 | 33 | 194.4 | 4.3 | 33 | 348.8 | 4.2 | 33 | 160.4 | 4.4 | 33 | 280.6 | 4.2 | 33 | 210.6 | 4.2 | 33 | 272.4 | 4.5 |
| 34 | 255.5 | 4.1 | 34 | 203.8 | 4.0 | 34 | 261.1 | 4.3 | 34 | 202.5 | 4.2 | 34 | 188.9 | 4.5 | 34 | 284.8 | 4.1 | 34 | 195.0 | 4.1 | 34 | 271.7 | 4.6 |
| 35 | 280.7 | 4.2 | 35 | 215.7 | 4.2 | 35 | 291.2 | 4.2 | 35 | 252.3 | 4.6 | 35 | 131.4 | 4.6 | 35 | 296.8 | 4.1 | 35 | 253.2 | 4.2 | 35 | 171.3 | 4.3 |
| 36 | 168.5 | 4.0 | 36 | 155.2 | 4.3 | 36 | 191.1 | 4.8 | 36 | 204.6 | 4.1 | 36 | 211.8 | 4.3 | 36 | 273.8 | 4.2 | 36 | 211.7 | 4.2 | 36 | 276.6 | 4.0 |
| 37 | 168.6 | 4.2 | 37 | 165.4 | 4.2 | 37 | 325.8 | 4.1 | 37 | 184.4 | 4.6 | 37 | 126.0 | 4.6 | 37 | 285.8 | 4.0 | 37 | 283.3 | 4.1 | 37 | 225.5 | 4.4 |
| 38 | 206.0 | 4.1 | 38 | 190.2 | 3.9 | 38 | 210.1 | 4.2 | 38 | 220.6 | 4.3 | 38 | 214.2 | 4.1 | 38 | 258.6 | 4.1 | 38 | 192.8 | 4.2 | 38 | 201.9 | 4.2 |
| 39 | 164.6 | 4.3 | 39 | 205.8 | 4.3 | 39 | 287.1 | 4.3 | 39 | 254.8 | 4.5 | 39 | 171.1 | 4.7 | 39 | 305.1 | 4.2 | 39 | 239.5 | 4.4 | 39 | 186.5 | 4.7 |
| 40 | 257.7 | 3.9 | 40 | 246.8 | 4.0 | 40 | 252.5 | 4.2 | 40 | 154.6 | 4.3 | 40 | 222.8 | 4.4 | 40 | 234.8 | 4.1 | 40 | 309.0 | 4.3 | 40 | 238.5 | 4.3 |
| 41 | 178.4 | 4.0 | 41 | 280.9 | 3.9 | 41 | 207.7 | 3.9 | 41 | 231.1 | 3.9 | 41 | 220.8 | 4.1 | 41 | 339.3 | 3.9 | 41 | 179.8 | 4.1 | 41 | 234.6 | 4.1 |
| 42 | 209.2 | 3.8 | 42 | 166.9 | 3.9 | 42 | 268.5 | 4.1 | 42 | 235.0 | 3.8 | 42 | 221.4 | 4.1 | 42 | 224.8 | 4.0 | 42 | 184.7 | 4.1 | 42 | 147.1 | 4.2 |
| 43 | 130.5 | 3.9 | 43 | 230.4 | 3.9 | 43 | 239.4 | 4.1 | 43 | 321.3 | 4.0 | 43 | 148.3 | 4.2 | 43 | 271.6 | 3.9 | 43 | 290.9 | 3.9 | 43 | 199.4 | 4.1 |
| 44 | 181.8 | 4.0 | 44 | 108.1 | 3.9 | 44 | 181.4 | 3.9 | 44 | 231.5 | 3.8 | 44 | 220.5 | 4.3 | 44 | 255.1 | 3.8 | 44 | 214.4 | 3.9 | 44 | 270.3 | 4.5 |
| 45 | 135.7 | 3.9 | 45 | 206.8 | 3.8 | 45 | 225.7 | 4.3 | 45 | 294.4 | 3.7 | 45 | 221.0 | 4.2 | 45 | 269.6 | 3.9 | 45 | 289.8 | 4.0 | 45 | 211.8 | 4.2 |
| 46 | 253.7 | 4.1 | 46 | 154.9 | 3.6 | 46 | 312.8 | 3.9 | 46 | 245.0 | 4.2 | 46 | 189.1 | 4.3 | 46 | 322.5 | 4.1 | 46 | 267.5 | 4.2 | 46 | 288.0 | 4.4 |
| 47 | 250.2 | 4.1 | 47 | 209.8 | 4.0 | 47 | 236.7 | 3.8 | 47 | 223.8 | 4.0 | 47 | 116.0 | 4.1 | 47 | 367.1 | 3.8 | 47 | 302.3 | 4.0 | 47 | 216.5 | 4.2 |
| 48 | 258.7 | 4.0 | 48 | 200.3 | 3.9 | 48 | 236.5 | 3.8 | 48 | 212.2 | 4.1 | 48 | 164.3 | 4.2 | 48 | 243.5 | 3.9 | 48 | 236.0 | 3.9 | 48 | 249.4 | 4.3 |
| 49 | 171.9 | 3.9 | 49 | 94.5 | 3.7 | 49 | 225.1 | 4.0 | 49 | 223.9 | 4.0 | 49 | 225.0 | 4.0 | 49 | 219.1 | 3.8 | 49 | 260.2 | 3.9 | 49 | 239.1 | 4.1 |
| 50 | 246.8 | 3.9 | 50 | 171.6 | 3.9 | 50 | 338.2 | 3.9 | 50 | 180.3 | 4.0 | 50 | 134.2 | 4.3 | 50 | 241.5 | 3.9 | 50 | 261.7 | 3.9 | 50 | 283.0 | 4.5 |
| 51 | 162.9 | 4.0 | 51 | 126.7 | 3.9 | 51 | 269.1 | 4.1 | 51 | 254.3 | 4.0 | 51 | 160.9 | 4.5 | 51 | 307.3 | 3.9 | 51 | 234.8 | 3.9 | 51 | 331.5 | 4.1 |
| 52 | 260.9 | 4.2 | 52 | 175.5 | 4.1 | 52 | 280.2 | 3.9 | 52 | 211.6 | 4.1 | 52 | 165.8 | 4.2 | 52 | 242.8 | 4.0 | 52 | 240.9 | 4.6 | 52 | 304.4 | 4.5 |
| 53 f | 287.8 | 1.6 | 53 f | 139.2 | 1.6 | 53 f | 272.8 | 1.5 | 53 f | 238.2 | 1.6 | 53 f | 118.6 | 1.4 | 53 f | 319.9 | 1.5 | 53 f | 205.8 | 1.6 | 53 f | 233.0 | 1.5 |
| 54 | 224.5 | 3.9 | 54 | 285.2 | 4.0 | 54 | 230.6 | 4.0 | 54 | 186.2 | 4.1 | 54 | 149.1 | 4.0 | 54 | 287.2 | 3.9 | 54 | 272.8 | 3.9 | 54 | 248.2 | 4.0 |
| 55 | 175.7 | 4.2 | 55 | 216.1 | 3.9 | 55 | 251.4 | 3.7 | 55 | 204.8 | 3.8 | 55 | 253.6 | 4.1 | 55 | 366.2 | 3.9 | 55 | 243.8 | 4.3 | 55 | 228.2 | 4.5 |
| 56 | 216.2 | 4.0 | 56 | 134.3 | 3.9 | 56 | 218.5 | 3.9 | 56 | 222.6 | 4.0 | 56 | 115.7 | 4.0 | 56 | 272.0 | 4.2 | 56 | 218.0 | 4.2 | 56 | 251.2 | 4.1 |
| 57 | 281.8 | 4.0 | 57 | 116.7 | 4.0 | 57 | 332.3 | 4.2 | 57 | 285.1 | 4.3 | 57 | 213.2 | 4.2 | 57 | 282.6 | 4.1 | 57 | 268.2 | 4.1 | 57 | 265.3 | 4.4 |
| 58 | 283.8 | 4.0 | 58 | 174.9 | 3.9 | 58 | 131.4 | 4.2 | 58 | 246.9 | 4.0 | 58 | 277.6 | | | | | | | | | | |

Pedestal after centermean.

| CHIP 8 | | | CHIP 9 | | | CHIP 10 | | | CHIP 11 | | | CHIP 12 | | | CHIP 13 | | | CHIP 14 | | | CHIP 15 | | |
|--------|-------|------|--------|-------|-----|---------|-------|------|---------|-------|-----|---------|-------|------|---------|-------|-----|---------|-------|-----|---------|-------|------|
| CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD |
| 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 |
| 1 r | 382.9 | 10.1 | 1 r | 310.6 | 9.4 | 1 r | 429.6 | 10.3 | 1 r | 385.4 | 9.6 | 1 r | 253.8 | 11.5 | 1 r | 443.9 | 9.6 | 1 r | 293.7 | 8.6 | 1 r | 286.2 | 10.5 |
| 2 r | 250.1 | 0.7 | 2 r | 249.8 | 0.7 | 2 r | 250.3 | 0.7 | 2 r | 250.1 | 0.6 | 2 r | 250.4 | 0.7 | 2 r | 250.2 | 0.6 | 2 r | 250.5 | 0.7 | 2 r | 249.9 | 0.7 |
| 3 | 249.3 | 4.4 | 3 | 250.5 | 4.3 | 3 | 251.2 | 4.5 | 3 | 250.3 | 5.0 | 3 | 250.1 | 4.8 | 3 | 249.4 | 4.5 | 3 | 252.6 | 4.5 | 3 | 250.7 | 5.0 |
| 4 | 251.8 | 4.3 | 4 | 251.4 | 4.1 | 4 | 249.8 | 4.5 | 4 | 249.8 | 4.6 | 4 | 250.8 | 4.6 | 4 | 251.4 | 4.6 | 4 | 251.0 | 4.3 | 4 | 250.8 | 4.5 |
| 5 | 251.0 | 4.2 | 5 | 251.0 | 4.4 | 5 | 248.9 | 4.5 | 5 | 248.6 | 5.0 | 5 | 249.3 | 4.6 | 5 | 250.6 | 4.1 | 5 | 249.3 | 4.6 | 5 | 251.1 | 4.6 |
| 6 | 250.8 | 4.2 | 6 | 250.0 | 4.2 | 6 | 250.2 | 4.5 | 6 | 251.0 | 4.6 | 6 | 250.0 | 4.5 | 6 | 251.0 | 4.3 | 6 | 250.9 | 4.4 | 6 | 249.0 | 4.4 |
| 7 | 250.2 | 4.2 | 7 | 250.5 | 4.2 | 7 | 248.8 | 4.3 | 7 | 249.1 | 4.8 | 7 | 250.5 | 4.5 | 7 | 249.9 | 4.1 | 7 | 249.3 | 4.4 | 7 | 250.3 | 4.5 |
| 8 | 251.8 | 4.1 | 8 | 248.5 | 4.3 | 8 | 249.3 | 4.3 | 8 | 250.2 | 4.7 | 8 | 251.1 | 4.7 | 8 | 251.4 | 4.2 | 8 | 251.5 | 4.4 | 8 | 251.0 | 4.5 |
| 9 | 250.1 | 4.4 | 9 | 249.3 | 4.3 | 9 | 249.1 | 4.8 | 9 | 250.1 | 4.8 | 9 | 250.0 | 4.6 | 9 | 250.8 | 4.2 | 9 | 249.1 | 4.4 | 9 | 250.3 | 4.4 |
| 10 | 250.9 | 4.1 | 10 | 250.1 | 3.9 | 10 | 250.8 | 4.2 | 10 | 251.0 | 4.5 | 10 | 250.4 | 5.0 | 10 | 249.3 | 4.2 | 10 | 249.9 | 4.2 | 10 | 250.8 | 4.3 |
| 11 | 250.2 | 4.1 | 11 | 250.9 | 4.1 | 11 | 249.6 | 4.3 | 11 | 250.3 | 4.7 | 11 | 250.0 | 4.4 | 11 | 249.4 | 4.3 | 11 | 250.9 | 4.5 | 11 | 250.5 | 4.5 |
| 12 | 251.1 | 4.3 | 12 | 250.2 | 4.1 | 12 | 251.3 | 4.1 | 12 | 249.9 | 4.5 | 12 | 251.8 | 4.3 | 12 | 250.0 | 4.3 | 12 | 248.6 | 4.2 | 12 | 251.3 | 4.3 |
| 13 | 250.0 | 4.0 | 13 | 250.5 | 4.2 | 13 | 249.7 | 4.5 | 13 | 250.2 | 4.3 | 13 | 249.9 | 4.6 | 13 | 251.4 | 4.2 | 13 | 249.3 | 4.5 | 13 | 250.2 | 4.4 |
| 14 | 250.2 | 4.1 | 14 | 249.5 | 4.1 | 14 | 249.6 | 4.2 | 14 | 249.6 | 4.5 | 14 | 249.8 | 4.3 | 14 | 251.1 | 4.1 | 14 | 248.8 | 4.2 | 14 | 249.2 | 4.3 |
| 15 f | 250.3 | 1.9 | 15 f | 250.4 | 1.6 | 15 f | 250.0 | 1.6 | 15 f | 251.0 | 1.6 | 15 f | 250.9 | 1.8 | 15 f | 250.6 | 1.5 | 15 f | 250.0 | 1.8 | 15 f | 250.9 | 1.7 |
| 16 | 250.0 | 4.2 | 16 | 250.2 | 4.3 | 16 | 250.3 | 4.1 | 16 | 250.2 | 4.6 | 16 | 251.6 | 4.5 | 16 | 250.8 | 4.2 | 16 | 250.5 | 4.2 | 16 | 253.1 | 4.4 |
| 17 | 249.3 | 4.1 | 17 | 249.2 | 4.2 | 17 | 249.3 | 4.5 | 17 | 249.3 | 4.5 | 17 | 249.1 | 4.7 | 17 | 251.8 | 4.2 | 17 | 249.2 | 4.2 | 17 | 248.3 | 4.4 |
| 18 | 250.8 | 4.1 | 18 | 251.2 | 4.1 | 18 | 251.4 | 4.2 | 18 | 249.9 | 4.4 | 18 | 249.7 | 4.4 | 18 | 250.8 | 4.1 | 18 | 250.9 | 4.2 | 18 | 251.5 | 4.3 |
| 19 | 251.0 | 4.3 | 19 | 250.1 | 4.1 | 19 | 250.0 | 4.5 | 19 | 250.8 | 4.2 | 19 | 250.5 | 4.3 | 19 | 249.9 | 4.3 | 19 | 250.5 | 4.3 | 19 | 248.4 | 4.3 |
| 20 | 249.7 | 4.2 | 20 | 251.2 | 4.2 | 20 | 249.9 | 4.5 | 20 | 250.7 | 4.5 | 20 | 250.7 | 4.2 | 20 | 251.2 | 4.0 | 20 | 251.2 | 4.2 | 20 | 250.4 | 4.7 |
| 21 | 251.6 | 4.2 | 21 | 249.0 | 4.0 | 21 | 249.6 | 4.1 | 21 | 247.7 | 4.7 | 21 | 249.4 | 4.4 | 21 | 251.0 | 4.2 | 21 | 249.8 | 4.1 | 21 | 249.1 | 4.4 |
| 22 | 250.9 | 4.2 | 22 | 251.3 | 4.4 | 22 | 250.8 | 4.2 | 22 | 249.8 | 4.5 | 22 | 250.1 | 4.4 | 22 | 250.5 | 4.2 | 22 | 251.2 | 4.3 | 22 | 250.2 | 4.4 |
| 23 | 250.4 | 4.4 | 23 | 251.0 | 4.0 | 23 | 249.3 | 4.3 | 23 | 251.4 | 4.3 | 23 | 249.9 | 4.5 | 23 | 250.4 | 4.1 | 23 | 251.7 | 4.3 | 23 | 250.9 | 4.3 |
| 24 | 249.7 | 4.1 | 24 | 250.8 | 4.2 | 24 | 251.2 | 4.5 | 24 | 249.5 | 4.4 | 24 | 251.3 | 4.5 | 24 | 250.6 | 4.2 | 24 | 250.3 | 4.3 | 24 | 250.3 | 4.3 |
| 25 | 251.7 | 4.2 | 25 | 250.0 | 4.4 | 25 | 249.8 | 4.2 | 25 | 250.8 | 4.2 | 25 | 249.2 | 4.5 | 25 | 249.2 | 4.1 | 25 | 250.4 | 4.3 | 25 | 250.8 | 4.4 |
| 26 | 249.0 | 4.2 | 26 | 249.9 | 4.1 | 26 | 250.7 | 4.3 | 26 | 250.4 | 4.5 | 26 | 249.7 | 5.0 | 26 | 250.1 | 4.0 | 26 | 250.1 | 4.2 | 26 | 250.3 | 4.5 |
| 27 | 251.2 | 4.3 | 27 | 250.6 | 4.1 | 27 | 249.7 | 4.2 | 27 | 247.6 | 4.3 | 27 | 250.9 | 4.2 | 27 | 251.1 | 4.0 | 27 | 250.5 | 4.0 | 27 | 251.0 | 4.3 |
| 28 f | 250.6 | 1.6 | 28 f | 250.8 | 1.7 | 28 f | 250.1 | 1.8 | 28 f | 250.4 | 1.6 | 28 f | 250.3 | 1.7 | 28 f | 249.8 | 1.6 | 28 f | 250.0 | 1.8 | 28 f | 251.0 | 1.9 |
| 29 | 251.7 | 4.2 | 29 | 249.9 | 4.2 | 29 | 251.1 | 4.1 | 29 | 250.5 | 4.4 | 29 | 249.8 | 4.2 | 29 | 249.7 | 4.1 | 29 | 250.8 | 4.3 | 29 | 251.1 | 4.5 |
| 30 | 250.5 | 4.1 | 30 | 250.0 | 4.1 | 30 | 250.5 | 4.2 | 30 | 249.1 | 4.4 | 30 | 249.1 | 4.5 | 30 | 250.8 | 3.9 | 30 | 250.1 | 4.3 | 30 | 250.5 | 4.6 |
| 31 | 249.8 | 4.0 | 31 | 250.3 | 4.1 | 31 | 250.4 | 4.3 | 31 | 250.8 | 4.3 | 31 | 250.8 | 4.5 | 31 | 250.3 | 4.1 | 31 | 250.1 | 4.2 | 31 | 249.0 | 4.7 |
| 32 | 250.3 | 4.3 | 32 | 250.7 | 4.2 | 32 | 250.1 | 4.0 | 32 | 250.0 | 4.2 | 32 | 249.7 | 4.2 | 32 | 248.6 | 3.9 | 32 | 251.4 | 4.2 | 32 | 250.9 | 4.4 |
| 33 | 251.4 | 4.1 | 33 | 250.7 | 4.2 | 33 | 248.8 | 4.3 | 33 | 250.6 | 4.4 | 33 | 249.8 | 4.6 | 33 | 250.7 | 4.2 | 33 | 248.2 | 4.1 | 33 | 251.2 | 4.3 |
| 34 | 249.2 | 4.2 | 34 | 249.7 | 4.1 | 34 | 251.3 | 4.1 | 34 | 249.5 | 4.2 | 34 | 250.9 | 4.5 | 34 | 249.2 | 3.9 | 34 | 250.9 | 4.2 | 34 | 248.5 | 4.2 |
| 35 | 249.2 | 4.2 | 35 | 249.1 | 4.2 | 35 | 249.2 | 4.1 | 35 | 250.8 | 4.8 | 35 | 250.9 | 4.3 | 35 | 251.3 | 4.0 | 35 | 248.8 | 4.3 | 35 | 249.8 | 4.5 |
| 36 | 252.7 | 4.0 | 36 | 250.6 | 4.2 | 36 | 250.1 | 4.1 | 36 | 250.6 | 4.2 | 36 | 249.9 | 4.3 | 36 | 249.9 | 4.3 | 36 | 251.7 | 4.2 | 36 | 249.9 | 4.4 |
| 37 | 250.1 | 4.2 | 37 | 251.4 | 4.1 | 37 | 249.3 | 4.3 | 37 | 250.7 | 4.3 | 37 | 251.2 | 4.5 | 37 | 249.9 | 4.0 | 37 | 249.7 | 4.2 | 37 | 250.2 | 4.3 |
| 38 | 249.5 | 4.1 | 38 | 250.3 | 4.1 | 38 | 251.2 | 4.1 | 38 | 249.0 | 4.2 | 38 | 250.2 | 4.3 | 38 | 249.8 | 4.0 | 38 | 250.2 | 4.0 | 38 | 250.1 | 4.3 |
| 39 | 249.4 | 4.6 | 39 | 250.8 | 4.2 | 39 | 250.2 | 4.3 | 39 | 249.8 | 4.5 | 39 | 250.4 | 4.6 | 39 | 249.8 | 4.3 | 39 | 250.6 | 4.4 | 39 | 251.0 | 4.7 |
| 40 | 250.3 | 3.9 | 40 | 250.8 | 4.2 | 40 | 252.0 | 4.4 | 40 | 250.7 | 4.4 | 40 | 250.1 | 4.4 | 40 | 249.7 | 3.9 | 40 | 249.7 | 4.2 | 40 | 251.9 | 4.4 |
| 41 | 250.3 | 4.0 | 41 | 249.3 | 3.8 | 41 | 249.2 | 3.8 | 41 | 249.8 | 4.0 | 41 | 249.5 | 4.2 | 41 | 251.9 | 3.9 | 41 | 251.1 | 3.8 | 41 | 250.5 | 4.0 |
| 42 | 250.2 | 3.9 | 42 | 250.3 | 3.8 | 42 | 250.6 | 4.0 | 42 | 251.1 | 4.0 | 42 | 250.6 | 4.0 | 42 | 250.0 | 3.8 | 42 | 250.1 | 4.3 | 42 | 249.2 | 4.2 |
| 43 | 251.7 | 3.7 | 43 | 250.6 | 4.2 | 43 | 249.5 | 4.0 | 43 | 250.8 | 3.8 | 43 | 250.6 | 3.9 | 43 | 249.6 | 3.8 | 43 | 249.6 | 3.9 | 43 | 251.4 | 4.1 |
| 44 | 250.3 | 4.0 | 44 | 250.6 | 3.8 | 44 | 248.9 | 4.1 | 44 | 249.5 | 3.8 | 44 | 250.0 | 4.1 | 44 | 250.2 | 4.0 | 44 | 251.1 | 4.1 | 44 | 250.7 | 4.3 |
| 45 | 249.2 | 3.9 | 45 | 250.1 | 3.6 | 45 | 251.2 | 4.2 | 45 | 251.3 | 3.8 | 45 | 249.4 | 4.4 | 45 | 250.0 | 3.8 | 45 | 250.0 | 3.8 | 45 | 250.1 | 4.0 |
| 46 | 250.2 | 3.9 | 46 | 249.3 | 3.7 | 46 | 252.4 | 4.0 | 46 | 252.1 | 4.1 | 46 | 251.2 | 4.3 | 46 | 249.2 | 4.1 | 46 | 250.7 | 4.0 | 46 | 249.3 | 4.6 |
| 47 | 250.4 | 3.8 | 47 | 251.3 | 3.8 | 47 | 249.2 | 3.9 | 47 | 250.8 | 4.1 | 47 | 250.7 | 4.1 | 47 | 250.9 | 3.8 | 47 | 251.0 | 3.9 | 47 | 249.3 | 4.0 |
| 48 | 251.0 | 3.7 | 48 | 251.0 | 4.0 | 48 | 249.3 | 4.0 | 48 | 249.9 | 4.0 | 48 | 250.2 | 4.3 | 48 | 249.4 | 3.9 | 48 | 250.9 | 4.2 | 48 | 250.4 | 4.5 |
| 49 | 249.9 | 3.8 | 49 | 251.6 | 3.8 | 49 | 249.7 | 4.0 | 49 | 249.2 | 4.0 | 49 | 250.8 | 4.1 | 49 | 250.8 | 3.7 | 49 | 250.8 | 3.9 | 49 | 250.7 | 4.1 |
| 50 | 250.4 | 4.0 | 50 | 250.7 | 3.8 | 50 | 250.6 | 4.2 | 50 | 250.3 | 4.1 | 50 | 249.5 | 4.0 | 50 | 251.6 | 3.9 | 50 | 250.0 | 3.9 | 50 | 251.3 | 4.4 |
| 51 | 250.5 | 4.0 | 51 | 250.1 | 4.1 | 51 | 249.1 | 4.1 | 51 | 250.2 | 3.8 | 51 | 249.2 | 4.3 | 51 | 250.7 | 3.8 | 51 | 250.0 | 3.8 | 51 | 250.2 | 4.2 |
| 52 | 249.9 | 4.1 | 52 | 252.2 | 4.0 | 52 | 250.5 | 4.0 | 52 | 250.4 | 4.1 | 52 | 249.4 | 4.2 | 52 | 249.5 | 3.9 | 52 | 250.4 | 4.1 | 52 | 250.7 | 4.4 |
| 53 f | 250.3 | 1.5 | 53 f | 250.6 | 1.5 | 53 f | 249.4 | 1.6 | 53 f | 250.2 | 1.5 | 53 f | 250.2 | 1.5 | 53 f | 250.1 | 1.6 | 53 f | 250.9 | 1.5 | 53 f | 250.2 | 1.5 |
| 54 | 251.2 | 3.8 | 54 | 250.8 | 3.8 | 54 | 251.8 | 4.2 | 54 | 250.9 | 4.2 | 54 | 251.1 | 4.1 | 54 | 250.1 | 3.9 | 54 | 249.7 | 4.1 | 54 | 251.4 | 4.0 |
| 55 | 249.9 | 4.3 | 55 | 251.6 | 4.0 | 55 | 251.3 | 3.9 | 55 | 250.0 | 4.2 | 55 | 249.5 | 4.3 | 55 | 249.9 | 3.9 | 55 | 250.8 | 4.1 | 55 | 250.7 | 4.4 |
| 56 | 252.1 | 4.1 | 56 | 250.7 | 3.9 | 56 | 249.0 | 4.1 | 56 | 249.3 | 4.2 | 56 | 251.1 | 4.2 | 56 | 250.7 | 3.8 | 56 | 250.2 | 4.2 | 56 | 250.6 | 4.0 |
| 57 | 251.0 | 3.9 | 57 | 250.4 | 3.9 | 57 | 251.5 | 4.2 | 57 | 251.1 | 4.1 | 57 | 251.3 | 4.1 | 57 | 251.1 | 4.0 | 57 | 250.7 | 4.0 | 57 | 249.3 | 4.3 |
| 58 | 250.1 | 3.9 | 58 | 250.8 | 3.7 | 58 | 250.8 | 4.1 | 58 | 248.2 | | | | | | | | | | | | | |