

Fec test report:

Date: 2020-10-26 15:39:37

Tester name: Boris

Test#1 Monitoring values

Failed

0	FEC label	009	OK
1	FEC DC2438 ID	6c0000024dc35c26	OK
2	FEC_T (to 35°C)	24.344	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.1A to 1.5A)	1.404	OK
5	FEC_Vad (1.9V to 2.0V)	1.330	FAIL

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Failed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 73	FAIL
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 71	FAIL
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 74	FAIL
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 65	FAIL
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 79	FAIL
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 74	FAIL
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 66	FAIL
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 71	FAIL

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdcm(2) Fem(00) FEC_T: 24.344 degC
2	fe 0 moni V 1	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 1 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
7	fe 0 moni I 1	0	0 Tdcm(2) Fem(00) FEC_I: 1.404 A
8	fe 0 moni S 1	0	0 Tdcm(2) Fem(00) FEC_Serial: 6c0000024dc35c26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2088000 (34111488) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdcm(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdcm(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdcm(2) Fem(00) After(10) Reg(3) <- 0x0 0xb0b 0xb0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0xc0c 0xc0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0xd0d 0xd0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdcm(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(15) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdcm(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdcm(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdcm(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdcm(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdcm(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdcm(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdcm(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdcm(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 Tdc(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
46	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
51	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
56	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
61	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
66	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 Tdc(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
78	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
83	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
88	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
93	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
98	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 Tdc(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
110	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V

115	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
120	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
125	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
130	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 TdcM(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
142	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
147	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
152	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
157	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
162	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff0000
168	fe 0 after 12 test_mode 0x1	0	0 TdcM(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	425.6	12.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	349.9	0.7	2 r	317.0	0.7	2 r	305.4	0.7	2 r	311.9	0.7	2 r	286.3	0.7	2 r	316.6	0.7	2 r	295.2	0.7	2 r	301.0	0.7
3	358.3	4.4	3	356.0	4.6	3	157.0	4.6	3	302.9	5.3	3	305.7	4.8	3	260.8	4.3	3	221.9	4.5	3	241.3	4.6
4	245.2	4.3	4	285.8	4.3	4	275.8	4.4	4	257.5	4.5	4	287.8	4.3	4	264.8	4.5	4	227.3	4.4	4	217.0	4.4
5	274.1	4.3	5	228.8	4.3	5	162.4	4.8	5	188.8	5.1	5	324.5	4.4	5	249.9	4.5	5	273.7	4.4	5	226.0	4.9
6	307.9	4.2	6	242.3	4.2	6	184.0	4.2	6	214.1	4.7	6	301.0	4.4	6	231.5	4.5	6	270.9	4.4	6	227.5	4.3
7	324.6	4.4	7	236.0	4.1	7	131.4	4.7	7	239.3	5.0	7	278.2	4.6	7	283.0	4.3	7	217.9	4.5	7	213.7	4.7
8	364.1	4.2	8	310.6	4.1	8	210.6	4.3	8	175.5	4.6	8	264.4	4.4	8	170.5	4.5	8	176.2	4.2	8	303.1	4.2
9	251.9	4.5	9	285.7	4.3	9	130.6	4.9	9	268.6	4.9	9	314.2	4.8	9	172.0	4.5	9	208.8	4.8	9	280.7	4.8
10	339.2	4.1	10	287.2	3.9	10	129.4	4.2	10	191.6	4.6	10	191.2	4.3	10	222.2	4.6	10	193.8	4.7	10	153.7	4.3
11	193.5	4.1	11	240.7	4.5	11	192.6	4.4	11	232.1	4.8	11	252.8	4.7	11	233.3	4.4	11	231.0	4.2	11	308.6	4.7
12	297.8	4.6	12	274.3	4.2	12	168.7	4.3	12	184.6	4.4	12	329.9	4.4	12	202.3	4.3	12	333.1	4.2	12	186.0	4.4
13	206.7	4.3	13	285.6	4.2	13	125.8	4.3	13	249.6	4.8	13	289.4	4.7	13	241.3	4.2	13	209.9	4.2	13	295.4	4.5
14	303.4	4.1	14	203.2	4.4	14	123.4	4.1	14	215.7	4.6	14	284.0	4.5	14	282.9	4.7	14	172.2	4.1	14	321.7	4.2
15 f	232.9	1.7	15 f	111.8	1.7	15 f	130.1	1.7	15 f	285.0	1.7	15 f	299.9	1.7	15 f	245.0	1.6	15 f	251.4	1.7	15 f	236.9	1.7
16	282.5	4.2	16	311.6	3.9	16	182.2	4.2	16	258.9	4.6	16	220.0	4.5	16	209.7	4.5	16	239.6	4.5	16	209.6	4.5
17	221.6	4.2	17	282.8	4.3	17	236.7	4.3	17	320.8	4.5	17	284.1	4.1	17	259.2	4.3	17	279.3	4.2	17	181.2	4.3
18	232.2	4.3	18	284.5	4.1	18	189.3	4.3	18	224.7	4.8	18	267.6	4.4	18	293.0	4.0	18	347.6	4.3	18	157.2	4.7
19	310.8	4.2	19	286.4	4.0	19	227.1	4.2	19	196.5	4.5	19	180.3	4.3	19	202.3	4.2	19	241.8	4.8	19	224.2	4.4
20	265.2	4.2	20	230.1	4.5	20	156.4	4.5	20	249.4	4.8	20	301.8	4.3	20	254.6	4.1	20	208.1	4.4	20	245.0	4.3
21	262.5	4.4	21	242.5	4.2	21	172.6	4.3	21	237.8	4.4	21	208.6	4.2	21	347.9	4.3	21	248.4	4.1	21	173.1	4.7
22	325.8	4.2	22	259.9	4.1	22	220.6	4.5	22	191.4	4.6	22	240.9	4.5	22	265.1	4.3	22	205.1	4.5	22	241.2	4.4
23	338.4	4.3	23	289.8	4.0	23	169.6	4.4	23	210.5	4.2	23	292.9	4.3	23	246.0	4.2	23	196.6	4.3	23	245.2	4.3
24	338.8	4.1	24	285.8	4.1	24	210.1	4.3	24	202.6	4.7	24	157.7	4.3	24	231.9	4.2	24	235.2	4.2	24	242.3	4.2
25	238.0	4.3	25	319.8	4.2	25	134.3	4.0	25	276.6	4.3	25	326.9	4.3	25	284.9	4.2	25	200.0	4.4	25	179.8	4.3
26	314.4	4.2	26	239.0	4.2	26	198.7	4.4	26	217.9	4.6	26	258.1	4.4	26	272.9	4.3	26	285.4	4.3	26	206.7	4.7
27	260.6	4.1	27	232.1	4.0	27	195.9	4.5	27	172.1	4.3	27	298.1	4.2	27	209.1	4.2	27	239.5	4.2	27	210.6	4.4
28 f	275.6	1.7	28 f	204.5	1.7	28 f	202.4	1.8	28 f	228.4	1.8	28 f	253.6	1.6	28 f	256.2	1.7	28 f	282.1	1.8	28 f	217.0	1.8
29	266.5	4.2	29	231.3	3.9	29	208.8	4.3	29	208.8	4.7	29	233.6	4.3	29	247.4	4.1	29	230.8	4.2	29	274.2	4.4
30	270.5	4.1	30	243.6	4.3	30	146.1	4.2	30	241.6	4.5	30	205.2	4.2	30	228.7	4.2	30	279.5	4.3	30	301.5	4.4
31	228.8	4.0	31	315.6	4.1	31	218.5	4.2	31	242.8	4.5	31	311.5	4.4	31	279.1	4.2	31	237.7	4.3	31	378.8	4.6
32	260.9	4.2	32	216.2	4.2	32	244.7	4.2	32	288.8	4.3	32	192.3	4.2	32	257.7	4.0	32	247.3	4.2	32	185.6	4.3
33	278.5	4.1	33	240.2	4.2	33	204.2	4.3	33	273.8	4.5	33	265.8	4.4	33	274.7	4.3	33	165.9	4.3	33	264.9	4.6
34	232.8	3.9	34	259.9	4.0	34	224.9	4.2	34	285.9	4.3	34	294.6	4.5	34	321.5	4.0	34	218.0	4.5	34	216.1	4.2
35	267.1	4.2	35	368.1	4.1	35	200.7	4.4	35	204.8	4.5	35	280.8	4.4	35	314.7	4.2	35	227.6	4.4	35	295.6	4.5
36	305.2	4.2	36	225.3	4.1	36	223.6	4.4	36	267.6	4.5	36	220.2	4.3	36	365.3	4.3	36	192.9	4.4	36	191.2	4.4
37	251.6	4.2	37	229.4	3.9	37	183.4	4.2	37	161.2	4.4	37	281.4	4.1	37	279.1	4.1	37	346.3	4.1	37	239.0	4.6
38	258.1	4.1	38	175.9	3.7	38	227.4	3.9	38	253.6	4.3	38	217.6	4.5	38	284.3	4.1	38	224.9	4.0	38	264.6	4.5
39	291.2	4.4	39	289.4	4.3	39	271.2	4.8	39	209.4	4.8	39	253.9	4.5	39	276.9	4.4	39	220.2	4.4	39	269.5	4.7
40	339.8	4.1	40	144.4	3.9	40	241.8	4.2	40	258.7	4.3	40	206.5	4.1	40	238.4	4.0	40	277.9	4.2	40	266.9	4.5
41	338.8	3.8	41	345.2	3.9	41	301.8	3.9	41	206.1	4.0	41	277.5	4.1	41	282.1	3.9	41	208.6	4.0	41	246.2	4.3
42	250.2	3.9	42	283.4	3.9	42	249.6	4.0	42	194.2	4.1	42	275.7	4.1	42	192.1	4.1	42	212.4	4.3	42	290.4	4.4
43	334.5	3.9	43	311.1	3.8	43	226.2	4.0	43	240.1	4.2	43	316.1	4.0	43	316.1	4.0	43	233.8	4.2	43	315.1	4.1
44	316.2	4.0	44	222.3	3.9	44	297.9	4.2	44	250.5	4.1	44	227.6	4.4	44	264.2	4.0	44	297.6	4.2	44	244.9	4.4
45	297.2	4.0	45	262.7	3.8	45	223.2	3.9	45	192.8	3.8	45	329.8	4.1	45	293.0	4.0	45	286.1	4.1	45	262.5	4.3
46	257.6	3.9	46	185.4	4.3	46	289.1	4.1	46	218.3	4.3	46	265.2	4.1	46	246.7	4.0	46	222.0	4.5	46	181.7	4.3
47	281.0	4.2	47	285.0	3.8	47	281.6	4.0	47	233.4	4.0	47	240.0	3.9	47	275.6	4.3	47	246.2	4.2	47	331.5	4.4
48	236.4	4.2	48	318.9	3.7	48	155.6	4.2	48	239.4	4.1	48	241.1	4.2	48	217.5	4.1	48	207.4	4.1	48	273.1	4.7
49	178.4	3.8	49	349.4	3.7	49	286.2	3.9	49	242.1	4.2	49	248.5	4.0	49	331.8	4.0	49	222.9	4.1	49	259.7	4.3
50	247.8	3.9	50	270.8	3.9	50	280.6	3.9	50	241.8	4.1	50	304.2	4.2	50	316.5	4.0	50	243.2	4.2	50	282.1	4.9
51	196.7	4.0	51	304.4	4.0	51	181.4	4.0	51	195.2	3.9	51	279.4	3.9	51	207.3	3.8	51	327.9	4.7	51	328.9	4.2
52	304.3	3.9	52	271.2	3.8	52	166.1	4.0	52	281.0	4.1	52	262.1	4.3	52	254.4	4.1	52	208.9	4.2	52	231.8	4.5
53 f	262.4	1.5	53 f	320.4	1.5	53 f	186.7	1.7	53 f	138.7	1.5	53 f	258.9	1.6	53 f	206.4	1.6	53 f	251.4	1.7	53 f	246.4	1.6
54	258.6	3.9	54	181.2	3.8	54	193.6	4.3	54	246.4	4.0	54	253.5	4.1	54	237.9	4.0	54	200.1	4.1	54	253.8	4.2
55	325.7	4.1	55	287.2	3.8	55	225.0	4.0	55	230.6	4.2	55	270.6	4.2	55	257.2	4.0	55	108.6	4.0	55	203.6	4.5
56	219.8	4.2	56	254.2	3.7	56	154.8	4.2	56	199.1	4.2	56	260.5	4.2	56	244.8	4.0	56	280.3	4.4	56	190.1	4.4
57	311.9	3.8	57	352.2	4.1	57	163.5	4.3	57	209.5	4.2	57	259.8	4.2	57	258.0	4.0	57	187.1	4.2	57	155.9	4.4
58	281.0	4.0	58	273.5	3.8	58	199.9	3.9	58	204.2	3.9	58	239.0</										

Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	404.6	10.2	1 r	479.9	5.8	1 r	250.2	12.0	1 r	328.6	10.4	1 r	375.1	12.9	1 r	310.9	11.1	1 r	286.2	11.5	1 r	332.5	9.8
2 r	250.2	0.7	2 r	250.5	0.7	2 r	250.9	0.7	2 r	250.1	0.7	2 r	250.8	0.7	2 r	249.9	0.7	2 r	250.8	0.7	2 r	250.5	0.7
3	250.8	4.4	3	250.7	4.3	3	250.0	4.8	3	249.8	5.5	3	248.7	4.9	3	249.3	4.7	3	251.0	4.5	3	251.5	4.5
4	249.6	4.3	4	250.8	4.2	4	250.0	4.3	4	250.4	4.9	4	250.0	4.6	4	251.4	4.4	4	251.7	4.0	4	251.0	4.5
5	250.9	4.8	5	250.2	4.2	5	251.2	4.7	5	251.0	5.6	5	252.6	4.7	5	248.6	4.3	5	249.7	4.7	5	250.8	5.1
6	251.3	4.1	6	250.3	4.2	6	250.6	4.2	6	249.1	5.0	6	250.5	4.4	6	249.7	4.5	6	252.3	4.6	6	251.9	4.6
7	251.5	4.4	7	251.8	4.1	7	251.8	4.6	7	250.1	5.3	7	251.4	4.6	7	250.1	4.4	7	251.2	4.6	7	250.8	4.5
8	249.6	4.0	8	249.8	4.3	8	251.6	4.2	8	250.4	4.6	8	251.5	4.5	8	249.8	4.3	8	252.7	4.4	8	251.6	4.3
9	250.5	4.2	9	249.8	4.2	9	251.0	4.5	9	250.2	4.9	9	252.1	4.8	9	251.2	4.2	9	249.8	4.5	9	250.0	4.5
10	250.6	4.2	10	251.9	4.1	10	251.5	4.6	10	251.2	4.7	10	250.3	4.3	10	249.2	4.4	10	250.8	4.3	10	249.3	4.4
11	250.7	4.4	11	250.6	4.3	11	251.0	4.4	11	250.6	5.0	11	251.2	4.6	11	250.2	4.3	11	249.4	4.4	11	250.6	4.5
12	249.1	4.3	12	252.4	4.0	12	250.0	4.3	12	250.7	4.8	12	249.5	4.5	12	251.3	4.5	12	251.5	4.3	12	252.9	4.3
13	251.8	4.2	13	250.2	4.1	13	251.3	4.2	13	251.2	4.8	13	250.9	4.4	13	251.0	4.3	13	250.4	4.6	13	252.4	4.5
14	250.3	4.2	14	250.9	4.0	14	250.6	4.3	14	250.7	4.7	14	251.5	4.4	14	249.5	4.2	14	251.9	4.2	14	251.2	4.2
15 f	250.7	1.7	15 f	250.2	1.7	15 f	250.4	1.8	15 f	250.8	1.7	15 f	250.5	1.5	15 f	250.8	1.8	15 f	250.7	1.7	15 f	250.7	1.6
16	249.5	4.2	16	249.7	4.1	16	249.8	4.3	16	249.5	4.9	16	250.4	4.6	16	250.6	4.1	16	251.8	4.9	16	250.9	4.6
17	252.2	4.0	17	250.0	4.1	17	249.0	4.2	17	250.3	4.6	17	249.9	4.4	17	250.5	4.1	17	250.4	4.3	17	250.1	4.4
18	250.2	4.2	18	250.0	4.2	18	250.4	4.6	18	250.2	4.8	18	251.6	4.2	18	251.7	4.2	18	250.0	4.2	18	251.1	4.4
19	250.3	4.1	19	251.2	4.1	19	249.8	4.0	19	250.6	4.6	19	252.1	4.6	19	251.3	4.2	19	251.3	4.2	19	250.6	4.5
20	251.2	4.2	20	251.1	4.1	20	251.8	4.1	20	249.7	4.7	20	250.8	4.3	20	249.1	4.0	20	250.9	4.3	20	251.9	4.4
21	251.0	4.2	21	250.6	4.4	21	251.1	4.2	21	250.8	4.4	21	251.1	4.4	21	248.7	4.5	21	251.6	4.2	21	250.0	4.4
22	250.4	4.2	22	249.3	4.0	22	251.2	4.4	22	252.3	4.8	22	250.4	4.5	22	251.1	4.3	22	251.0	4.4	22	251.2	4.6
23	251.7	4.1	23	250.8	4.1	23	249.0	4.2	23	251.2	4.6	23	250.9	4.0	23	250.7	4.0	23	251.2	4.1	23	251.3	4.2
24	250.3	4.2	24	249.7	4.2	24	252.3	4.3	24	249.6	4.6	24	251.0	4.4	24	250.7	4.2	24	250.8	4.0	24	251.8	4.3
25	249.0	4.6	25	251.0	4.0	25	250.7	4.2	25	251.4	4.7	25	251.2	4.2	25	249.2	4.4	25	250.7	4.2	25	250.6	4.6
26	251.3	4.3	26	252.8	4.2	26	250.6	4.2	26	250.6	4.8	26	251.1	4.3	26	250.7	4.2	26	252.4	4.3	26	250.3	4.7
27	250.3	4.3	27	250.6	4.0	27	250.0	4.2	27	250.6	4.5	27	251.1	4.4	27	250.1	4.3	27	250.6	4.2	27	249.4	4.3
28 f	250.4	1.8	28 f	250.2	1.8	28 f	250.7	1.8	28 f	251.7	1.8	28 f	250.3	1.6	28 f	250.2	1.7	28 f	250.3	1.8	28 f	250.8	1.8
29	251.0	4.2	29	250.2	4.0	29	251.1	4.3	29	249.3	4.8	29	249.8	4.3	29	249.9	4.3	29	251.6	4.2	29	250.4	4.4
30	250.3	4.0	30	250.6	4.1	30	250.9	4.4	30	251.0	4.6	30	250.8	4.3	30	250.1	4.1	30	250.0	4.2	30	250.8	4.4
31	250.2	4.2	31	249.4	4.3	31	251.5	4.5	31	249.2	4.8	31	252.3	4.3	31	250.2	4.3	31	249.4	4.4	31	250.6	4.5
32	249.8	4.2	32	248.1	4.1	32	250.3	4.5	32	251.5	4.5	32	251.0	4.2	32	250.5	4.2	32	252.6	4.1	32	250.4	4.4
33	251.5	4.4	33	250.2	4.0	33	251.6	4.5	33	250.3	4.5	33	249.4	4.3	33	251.0	4.2	33	251.0	4.4	33	249.8	4.5
34	250.3	4.0	34	251.3	4.1	34	252.3	4.5	34	249.7	4.2	34	250.3	4.3	34	250.2	3.9	34	248.3	4.1	34	250.7	4.4
35	250.9	4.2	35	250.2	4.2	35	251.4	4.3	35	250.1	4.6	35	249.9	4.5	35	250.3	4.3	35	251.2	4.2	35	249.8	4.4
36	250.5	4.1	36	250.7	3.9	36	250.0	4.2	36	248.3	4.5	36	250.8	4.3	36	252.4	4.1	36	249.6	4.3	36	251.3	4.4
37	251.0	4.5	37	250.3	3.9	37	251.9	4.2	37	250.7	4.8	37	250.5	4.5	37	249.5	4.3	37	250.9	4.2	37	250.6	4.4
38	252.6	4.0	38	250.6	3.8	38	250.6	4.3	38	250.9	4.6	38	251.8	4.0	38	251.3	3.9	38	251.4	4.1	38	249.9	4.3
39	252.3	4.4	39	251.0	4.2	39	251.4	4.5	39	250.5	4.8	39	249.6	4.4	39	250.3	4.4	39	249.2	4.5	39	250.0	4.8
40	251.2	4.0	40	250.0	3.8	40	251.9	4.3	40	250.7	4.3	40	249.8	4.1	40	249.8	4.0	40	250.9	4.2	40	250.5	4.5
41	248.8	3.8	41	250.0	3.8	41	249.1	3.9	41	250.5	3.8	41	250.4	4.0	41	249.5	3.9	41	248.8	4.2	41	250.9	4.1
42	250.1	3.8	42	251.7	3.9	42	249.7	3.9	42	251.6	4.2	42	250.6	4.3	42	248.7	4.2	42	252.2	4.2	42	251.3	4.5
43	251.1	3.8	43	250.4	4.1	43	251.3	4.0	43	250.5	3.9	43	251.6	4.0	43	250.4	4.1	43	249.9	4.0	43	249.9	4.3
44	251.0	4.0	44	249.7	3.9	44	250.4	4.2	44	251.1	4.3	44	251.1	3.9	44	251.7	4.0	44	249.7	4.2	44	250.0	4.7
45	251.7	3.6	45	251.6	3.7	45	250.8	3.9	45	250.9	4.0	45	249.7	4.2	45	252.3	3.8	45	250.0	4.1	45	250.6	4.5
46	250.6	4.0	46	249.9	4.3	46	250.5	4.1	46	249.4	4.3	46	251.6	3.9	46	250.3	4.0	46	250.7	4.0	46	249.7	4.3
47	251.1	3.9	47	251.8	3.6	47	250.3	3.8	47	251.2	3.9	47	251.0	3.9	47	250.5	3.9	47	250.5	4.3	47	250.6	4.4
48	252.6	4.0	48	249.9	3.6	48	250.6	3.9	48	251.6	4.2	48	252.5	4.2	48	250.0	4.1	48	251.3	4.2	48	250.1	4.5
49	251.4	3.8	49	250.1	3.9	49	249.8	3.8	49	251.2	4.1	49	251.2	3.9	49	248.6	4.5	49	250.7	4.0	49	250.8	4.4
50	250.4	3.8	50	251.0	3.8	50	250.7	4.2	50	250.9	4.0	50	251.0	4.2	50	252.1	4.1	50	251.3	4.3	50	250.5	4.6
51	249.4	3.8	51	251.7	3.8	51	250.1	3.9	51	249.2	3.9	51	251.8	4.1	51	251.2	4.0	51	251.0	4.2	51	250.3	4.4
52	251.4	3.9	52	251.2	4.1	52	251.0	4.4	52	252.3	4.2	52	252.6	4.2	52	250.5	4.0	52	251.7	4.1	52	251.8	4.8
53 f	250.4	1.6	53 f	250.6	1.5	53 f	250.3	1.7	53 f	250.0	1.6	53 f	249.6	1.7	53 f	250.6	1.7	53 f	251.1	1.7	53 f	250.9	1.8
54	249.9	3.8	54	250.4	4.0	54	250.2	4.1	54	250.6	4.0	54	250.9	4.1	54	250.4	4.0	54	252.1	4.1	54	251.3	4.2
55	250.8	4.0	55	250.3	4.1	55	250.8	3.9	55	250.2	4.3	55	250.2	4.4	55	249.9	4.1	55	250.8	4.2	55	252.9	4.7
56	251.5	3.9	56	252.9	4.0	56	250.6	3.9	56	251.5	4.0	56	250.8	4.3	56	250.1	4.0	56	250.8	4.0	56	251.0	4.4
57	249.3	4.0	57	248.9	4.2	57	251.4	4.2	57	249.9	4.4	57	249.9	4.3	57	250.1	4.0	57	251.5	4.6	57	249.8	4.5
58	250.8	3.9	58	249.9	3.7	58	250.7	3.9	58	250.5													