

Fec test report:

Date: 2020-10-26 16:05:52

Tester name: Diego

Test#1 Monitoring values

Passed

0	FEC label	012	OK
1	FEC DC2438 ID	bf0000024ddcaa26	OK
2	FEC_T (to 35°C)	23.906	OK
3	FEC_Vdd (3.2V to 3.4V)	3.280	OK
4	FEC_I (1.1A to 1.5A)	1.467	OK
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Failed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean FAILED	STDDEV OK	FAIL

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3061	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3040	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3102	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3005	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3024	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3036	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2876	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdc(2) Fem(00) FEC_T: 23.906 degC
2	fe 0 moni V 1	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.280 V
3	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
7	fe 0 moni I 1	0	0 Tdc(2) Fem(00) FEC_I: 1.467 A
8	fe 0 moni S 1	0	0 Tdc(2) Fem(00) FEC_Serial: bf0000024ddcaa26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12088000 (302546944) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0b0b 0x0b0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0c0c 0x0c0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0d0d 0x0d0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdc(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdc(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdc(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdc(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdc(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdc(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdc(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdc(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 Tdc(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 Tdc(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 Tdc(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
110	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 TdcM(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff0000
168	fe 0 after 12 test_mode 0x1	0	0 TdcM(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	321.8	0.7	2 r	333.4	0.7	2 r	284.5	0.7	2 r	259.9	0.7	2 r	355.7	0.7	2 r	360.8	0.7	2 r	341.2	0.7	2 r	511.0	0.0
3	266.3	4.4	3	301.6	4.8	3	256.5	4.7	3	310.8	5.8	3	351.5	5.0	3	280.0	4.4	3	274.3	4.5	3	446.7	4.6
4	244.8	4.4	4	333.0	4.3	4	264.3	4.5	4	236.3	4.9	4	264.4	4.4	4	270.0	4.2	4	318.2	4.4	4	463.8	4.3
5	191.3	4.3	5	400.3	4.7	5	254.8	4.6	5	196.3	5.3	5	202.0	4.8	5	279.8	4.2	5	280.5	4.3	5	422.2	4.3
6	378.6	4.5	6	261.3	4.2	6	298.4	4.4	6	305.7	4.8	6	259.2	4.4	6	266.7	4.2	6	315.3	4.1	6	429.6	4.1
7	271.6	4.2	7	229.5	4.5	7	360.4	4.6	7	146.7	5.6	7	233.9	4.3	7	281.5	4.1	7	195.6	4.6	7	489.8	4.6
8	334.2	4.5	8	259.7	4.4	8	240.6	4.4	8	127.8	5.3	8	354.5	4.2	8	337.5	4.2	8	347.7	4.1	8	438.2	4.1
9	328.9	4.4	9	262.3	4.5	9	210.5	4.5	9	136.0	5.5	9	259.5	4.5	9	284.1	4.2	9	259.7	4.3	9	433.2	4.4
10	273.5	4.3	10	281.1	4.4	10	315.4	4.4	10	100.3	4.9	10	352.4	4.6	10	306.5	4.2	10	204.9	4.2	10	459.1	4.0
11	261.4	4.4	11	219.9	4.4	11	199.9	4.5	11	241.3	5.1	11	266.1	4.5	11	259.6	4.0	11	257.3	4.4	11	465.2	4.1
12	213.3	4.4	12	240.3	4.1	12	241.5	4.4	12	174.7	4.8	12	348.5	4.3	12	310.7	4.2	12	329.7	4.2	12	432.7	4.1
13	262.7	4.4	13	200.9	4.2	13	243.4	4.6	13	305.7	5.0	13	278.6	4.4	13	362.1	4.2	13	209.7	4.1	13	495.2	4.3
14	337.5	4.2	14	298.8	4.2	14	227.5	4.5	14	305.1	4.8	14	265.5	4.5	14	316.5	4.0	14	238.5	4.2	14	486.1	4.3
15 f	261.3	1.7	15 f	223.5	1.7	15 f	232.1	1.8	15 f	303.2	1.8	15 f	326.0	1.6	15 f	274.4	1.8	15 f	229.9	1.7	15 f	483.3	1.6
16	253.7	4.3	16	290.3	4.2	16	277.5	4.3	16	256.7	5.2	16	244.9	4.3	16	366.1	4.6	16	294.8	4.2	16	420.2	4.2
17	316.4	4.1	17	300.3	4.3	17	247.8	4.2	17	296.9	4.7	17	220.8	4.3	17	258.6	4.1	17	209.6	4.0	17	424.2	4.0
18	257.1	4.2	18	238.4	4.4	18	210.5	4.2	18	252.8	5.2	18	273.1	4.4	18	291.4	4.1	18	290.1	4.0	18	383.3	4.2
19	252.4	4.2	19	296.6	4.0	19	242.1	4.4	19	317.9	4.7	19	304.2	4.2	19	317.6	4.2	19	246.5	4.0	19	437.1	4.0
20	335.7	4.5	20	236.8	4.2	20	222.2	4.3	20	214.2	4.9	20	237.1	4.4	20	357.4	4.3	20	270.4	4.1	20	511.0	0.0
21	345.2	4.2	21	301.4	4.3	21	243.2	4.3	21	251.2	5.2	21	185.6	4.3	21	221.2	4.1	21	196.0	4.2	21	383.7	4.2
22	270.0	4.2	22	195.9	4.5	22	214.2	4.3	22	238.2	5.0	22	259.8	4.5	22	319.7	4.2	22	326.0	4.4	22	429.0	4.3
23	353.8	4.1	23	280.3	4.2	23	313.0	4.4	23	227.8	5.0	23	250.2	4.5	23	352.6	4.1	23	217.5	4.2	23	409.7	4.0
24	195.2	4.3	24	225.0	4.3	24	247.9	4.2	24	210.5	4.7	24	221.1	4.2	24	291.8	4.2	24	350.5	4.0	24	426.4	4.0
25	234.7	4.2	25	218.2	4.1	25	236.3	4.3	25	249.4	4.9	25	299.7	4.2	25	319.2	4.0	25	282.6	4.0	25	503.7	4.0
26	234.0	4.2	26	199.9	4.3	26	273.1	4.5	26	226.9	4.9	26	325.7	4.6	26	264.9	4.1	26	314.5	4.1	26	388.5	4.4
27	247.4	4.2	27	259.0	4.0	27	277.1	4.1	27	214.6	4.6	27	228.1	4.4	27	347.7	4.0	27	198.9	4.1	27	451.9	4.1
28 f	218.5	1.6	28 f	231.5	1.9	28 f	268.9	1.8	28 f	291.4	1.8	28 f	324.3	1.8	28 f	240.6	1.9	28 f	248.6	1.8	28 f	490.5	1.6
29	235.4	4.1	29	262.9	4.3	29	303.8	4.3	29	216.5	4.9	29	284.2	4.2	29	323.8	4.0	29	308.0	4.2	29	403.1	4.2
30	245.8	4.3	30	182.1	4.2	30	256.6	4.2	30	237.6	4.6	30	310.5	4.1	30	351.0	4.0	30	276.9	4.2	30	458.0	4.3
31	342.5	4.3	31	268.1	4.1	31	277.5	4.3	31	212.7	4.8	31	225.8	4.2	31	289.2	4.0	31	313.6	4.2	31	455.6	4.0
32	253.1	4.1	32	168.6	4.2	32	262.2	4.5	32	259.3	4.9	32	301.7	4.3	32	339.1	4.3	32	258.0	4.2	32	508.7	2.9
33	233.0	4.3	33	264.4	4.1	33	270.1	4.4	33	135.7	4.8	33	259.5	4.4	33	308.9	4.0	33	223.9	4.0	33	434.5	4.0
34	265.3	4.2	34	204.2	4.2	34	322.9	4.3	34	282.5	4.9	34	187.3	4.3	34	257.0	4.1	34	309.1	4.0	34	439.2	4.1
35	217.1	4.3	35	227.7	4.2	35	261.3	4.4	35	270.0	4.9	35	279.9	4.2	35	243.1	4.1	35	217.4	4.5	35	421.7	3.9
36	270.9	4.0	36	298.8	4.2	36	262.1	4.4	36	228.2	4.8	36	303.2	4.3	36	285.0	4.2	36	313.2	4.3	36	468.4	4.1
37	262.2	4.5	37	273.9	4.3	37	236.8	4.5	37	261.4	4.9	37	233.9	4.1	37	293.1	4.3	37	227.9	4.1	37	507.7	3.3
38	288.9	4.1	38	269.5	3.9	38	243.1	4.4	38	283.8	4.7	38	171.1	4.2	38	326.0	4.0	38	279.7	4.0	38	486.8	4.1
39	345.1	4.2	39	253.5	4.7	39	207.8	4.6	39	240.3	5.1	39	236.8	4.4	39	314.8	4.4	39	268.4	4.5	39	476.3	4.3
40	309.1	4.0	40	219.9	4.5	40	259.1	4.4	40	193.0	4.5	40	310.5	4.3	40	310.0	4.1	40	331.6	3.9	40	508.2	3.0
41	268.0	3.8	41	288.5	4.0	41	306.7	3.9	41	200.6	4.1	41	207.0	3.8	41	244.5	3.7	41	239.7	3.8	41	496.6	4.1
42	271.5	3.8	42	252.8	4.3	42	298.3	3.9	42	242.2	4.3	42	275.1	4.0	42	310.8	3.8	42	256.3	4.2	42	485.6	4.2
43	223.2	3.8	43	247.2	3.9	43	211.0	4.0	43	160.2	4.2	43	270.8	3.8	43	313.9	3.8	43	307.3	3.9	43	494.6	4.0
44	243.7	3.8	44	221.0	4.1	44	403.8	4.1	44	224.3	4.8	44	233.5	3.9	44	333.1	3.8	44	284.0	4.1	44	439.8	4.5
45	219.1	4.1	45	252.0	4.0	45	223.2	3.9	45	284.2	4.3	45	273.1	4.0	45	312.7	3.7	45	283.8	3.8	45	511.0	0.0
46	316.2	4.0	46	235.7	3.8	46	205.1	4.0	46	293.3	4.5	46	271.7	3.8	46	339.3	3.7	46	357.3	4.0	46	494.2	4.0
47	236.2	3.8	47	269.1	3.8	47	289.1	4.1	47	269.5	4.0	47	310.5	3.8	47	297.2	3.8	47	351.1	3.7	47	428.4	3.8
48	269.3	4.1	48	278.5	4.0	48	176.2	4.1	48	138.7	4.4	48	264.4	3.9	48	278.6	3.9	48	311.9	3.9	48	427.9	4.3
49	228.6	3.7	49	300.4	3.8	49	275.1	4.0	49	207.1	4.3	49	178.1	3.6	49	322.6	3.8	49	355.3	3.8	49	446.6	3.8
50	319.6	3.9	50	295.8	3.9	50	279.8	4.0	50	251.2	4.4	50	307.3	3.9	50	292.6	3.8	50	255.4	4.0	50	464.2	4.3
51	241.7	4.0	51	251.9	4.1	51	224.6	3.9	51	302.3	4.5	51	244.2	4.2	51	276.4	3.7	51	188.7	3.9	51	311.5	3.9
52	274.1	4.0	52	298.7	3.9	52	214.9	4.2	52	221.2	4.4	52	258.5	3.8	52	311.8	4.0	52	333.4	4.0	52	511.0	0.0
53 f	277.5	1.7	53 f	237.8	1.4	53 f	267.6	1.4	53 f	252.1	1.7	53 f	275.0	1.4	53 f	352.0	1.4	53 f	330.2	1.4	53 f	405.0	1.4
54	300.0	3.9	54	251.5	4.0	54	228.8	4.2	54	277.9	4.3	54	318.8	3.7	54	324.3	3.9	54	302.2	3.9	54	443.4	4.0
55	229.2	4.1	55	265.9	3.9	55	301.0	4.0	55	273.3	4.5	55	227.8	3.9	55	336.6	3.9	55	275.2	4.0	55	404.4	4.2
56	274.0	4.0	56	244.8	3.9	56	274.3	4.0	56	214.6	4.1	56	230.5	3.9	56	256.7	3.9	56	206.7	3.8	56	451.6	3.8
57	175.2	4.0	57	233.9	4.0	57	207.2	3.9	57	186.3	4.4	57	297.0	4.0	57	307.6	4.0	57	259.9	3.9	57	478.6	4.2
58	234.4	4.0	58	183.0	4.2	58	328.2	4.2	58	216.0	4.1	58	294.9										

Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	486.9	6.9	1 r	389.5	9.4	1 r	330.0	9.9	1 r	375.2	10.2	1 r	490.7	9.1	1 r	362.5	9.1	1 r	340.7	9.2	1 r	469.7	9.6
2 r	249.5	0.7	2 r	250.7	0.6	2 r	249.7	0.7	2 r	250.2	0.7	2 r	249.9	0.7	2 r	250.2	0.7	2 r	250.3	0.7	2 r	278.7	0.7
3	249.2	4.6	3	248.8	4.5	3	250.2	4.6	3	249.3	5.5	3	251.4	4.5	3	251.9	4.4	3	250.4	4.4	3	250.6	4.3
4	250.4	4.2	4	251.7	4.8	4	251.9	4.4	4	250.6	5.0	4	251.9	4.3	4	249.4	4.2	4	250.2	4.1	4	249.9	4.1
5	250.7	4.4	5	251.7	4.3	5	249.6	4.5	5	249.8	5.3	5	252.2	4.5	5	250.9	4.2	5	249.1	4.5	5	251.4	4.1
6	250.2	4.3	6	250.6	4.2	6	252.8	4.4	6	249.6	4.8	6	251.2	4.5	6	250.5	4.1	6	250.8	4.2	6	248.6	4.0
7	249.9	4.4	7	250.2	4.2	7	250.8	4.5	7	250.1	5.4	7	250.2	4.5	7	250.5	4.2	7	251.4	4.1	7	249.6	4.2
8	250.0	4.2	8	248.9	4.1	8	250.3	4.2	8	250.4	5.2	8	251.6	4.2	8	251.9	4.1	8	250.5	4.2	8	250.2	3.9
9	250.3	4.5	9	250.6	4.3	9	250.7	4.4	9	252.2	5.1	9	248.8	4.7	9	250.4	4.4	9	249.1	4.4	9	250.4	4.2
10	250.1	4.4	10	251.7	4.2	10	251.2	4.3	10	250.7	4.9	10	250.3	4.4	10	250.6	4.5	10	250.7	4.3	10	251.5	4.0
11	252.8	4.4	11	249.9	4.3	11	249.6	4.6	11	251.3	4.9	11	249.7	4.5	11	249.9	4.2	11	249.3	4.3	11	250.3	4.3
12	249.6	4.5	12	250.8	4.2	12	250.8	4.3	12	248.9	4.9	12	250.7	4.5	12	249.5	4.0	12	251.2	4.3	12	250.0	4.0
13	249.7	4.2	13	251.2	4.0	13	250.9	4.3	13	250.8	5.0	13	250.3	4.5	13	249.2	4.1	13	249.7	4.3	13	250.1	4.3
14	251.7	4.5	14	250.4	4.3	14	249.8	4.5	14	249.8	4.6	14	251.1	4.4	14	252.0	4.0	14	250.7	4.1	14	251.0	4.0
15 f	250.3	1.6	15 f	249.9	1.7	15 f	249.8	1.8	15 f	249.8	1.8	15 f	250.7	1.6	15 f	250.4	1.7	15 f	250.4	1.6	15 f	250.7	1.6
16	249.7	4.1	16	252.0	4.2	16	251.7	4.4	16	249.7	5.1	16	249.6	4.3	16	251.3	4.2	16	249.2	4.1	16	249.4	4.0
17	249.6	4.1	17	248.9	4.0	17	250.6	4.2	17	250.5	4.5	17	250.8	4.3	17	250.2	4.0	17	250.5	4.0	17	251.1	3.9
18	252.0	4.5	18	250.3	4.1	18	251.6	4.3	18	251.1	4.7	18	250.7	4.3	18	252.6	4.1	18	250.3	4.4	18	251.0	4.1
19	251.2	4.2	19	249.3	4.3	19	250.7	4.3	19	250.0	4.7	19	250.7	4.3	19	251.3	4.1	19	250.5	3.9	19	250.8	3.9
20	250.4	4.3	20	250.3	4.2	20	250.8	4.4	20	252.3	4.8	20	251.1	4.3	20	252.2	4.4	20	251.0	4.1	20	266.9	4.0
21	251.4	4.3	21	251.3	4.0	21	251.2	4.2	21	251.3	4.8	21	249.7	4.1	21	250.2	4.2	21	250.1	4.1	21	249.9	4.0
22	249.3	4.2	22	249.5	4.2	22	252.5	4.3	22	251.8	4.9	22	249.6	4.4	22	250.7	4.2	22	252.0	4.2	22	249.5	4.0
23	251.4	4.1	23	250.7	4.1	23	249.8	4.5	23	250.0	4.6	23	252.1	4.1	23	250.5	3.9	23	250.4	4.1	23	250.2	4.0
24	250.0	4.2	24	250.8	4.2	24	250.0	4.3	24	250.1	4.6	24	250.8	4.5	24	250.4	4.4	24	251.5	4.1	24	250.6	4.0
25	249.5	4.1	25	252.1	4.1	25	250.4	4.2	25	251.2	5.1	25	250.9	4.3	25	250.6	4.2	25	249.2	4.5	25	250.2	4.0
26	248.1	4.6	26	251.8	4.2	26	251.5	4.3	26	251.2	4.6	26	249.8	4.2	26	250.9	4.1	26	250.2	4.2	26	248.0	4.1
27	252.1	4.2	27	250.2	4.2	27	251.2	4.2	27	252.1	4.5	27	250.7	4.2	27	250.3	4.0	27	251.0	4.1	27	249.9	4.0
28 f	248.6	1.9	28 f	249.8	1.8	28 f	250.4	1.8	28 f	250.6	1.8	28 f	250.6	1.8	28 f	249.9	1.8	28 f	249.9	1.7	28 f	249.5	1.6
29	252.1	4.2	29	250.6	4.0	29	250.1	4.3	29	250.4	4.6	29	249.7	4.3	29	249.8	4.1	29	251.0	4.0	29	250.8	4.1
30	249.7	4.1	30	249.7	4.1	30	249.5	4.2	30	250.0	4.5	30	251.6	4.3	30	250.2	4.2	30	249.2	4.0	30	249.4	4.0
31	250.4	4.2	31	251.3	4.2	31	248.5	4.2	31	251.0	5.0	31	250.5	4.3	31	251.2	4.1	31	250.7	3.9	31	250.4	3.9
32	249.9	4.1	32	250.1	4.0	32	251.3	4.1	32	251.0	4.7	32	250.2	4.6	32	249.5	4.2	32	250.2	4.1	32	254.8	3.9
33	250.6	4.2	33	249.7	4.1	33	251.6	4.5	33	250.0	4.8	33	249.9	4.2	33	249.4	4.1	33	249.6	4.4	33	249.9	4.0
34	249.4	4.0	34	251.8	4.0	34	251.5	4.2	34	249.6	4.5	34	250.1	4.0	34	251.2	3.9	34	250.3	4.1	34	250.8	4.1
35	250.3	4.1	35	251.1	4.2	35	250.1	4.4	35	249.6	4.8	35	249.8	4.1	35	250.2	4.1	35	250.2	4.0	35	250.3	4.1
36	250.1	4.0	36	250.7	4.2	36	250.7	4.2	36	250.8	4.5	36	251.1	4.2	36	250.8	4.1	36	249.2	4.2	36	250.2	4.0
37	250.7	4.1	37	250.1	4.3	37	249.8	4.3	37	250.5	4.5	37	248.2	4.4	37	249.9	4.1	37	250.6	4.1	37	252.4	4.2
38	251.0	4.4	38	249.3	4.0	38	250.9	4.4	38	250.0	4.9	38	249.9	4.3	38	251.1	4.1	38	251.6	4.2	38	249.1	4.2
39	251.0	4.4	39	250.3	4.4	39	249.0	4.5	39	251.4	4.8	39	251.4	4.5	39	251.9	4.0	39	250.6	4.3	39	249.5	4.3
40	249.8	4.1	40	248.9	4.2	40	250.9	4.3	40	250.2	4.7	40	251.2	4.2	40	250.4	4.0	40	250.8	4.3	40	253.5	4.1
41	249.2	4.0	41	251.2	3.9	41	250.2	3.8	41	250.4	4.2	41	250.4	3.9	41	249.3	3.8	41	250.7	3.8	41	249.2	4.0
42	250.0	4.0	42	250.1	4.0	42	250.9	4.2	42	249.7	4.2	42	251.0	4.1	42	250.7	3.8	42	251.9	3.8	42	249.7	4.0
43	249.1	3.9	43	249.3	4.0	43	250.0	3.9	43	251.2	4.0	43	250.7	3.8	43	249.0	3.7	43	250.8	3.7	43	248.2	3.9
44	250.2	4.0	44	251.2	4.1	44	250.5	3.9	44	250.9	4.3	44	249.2	4.0	44	249.9	3.8	44	251.8	3.8	44	248.7	4.0
45	251.2	3.8	45	249.9	4.0	45	249.4	4.0	45	250.9	4.3	45	250.8	4.2	45	250.2	3.9	45	250.9	3.9	45	278.9	3.7
46	249.9	3.9	46	249.9	3.9	46	251.1	4.0	46	250.8	4.3	46	249.7	4.1	46	251.8	3.9	46	251.1	3.8	46	250.8	4.0
47	247.5	3.8	47	251.2	3.7	47	248.8	3.7	47	250.7	4.2	47	249.6	3.9	47	251.4	3.7	47	251.6	3.9	47	249.0	3.8
48	250.5	4.0	48	250.4	3.9	48	249.6	4.1	48	251.2	4.2	48	250.6	3.9	48	249.7	3.8	48	249.3	4.0	48	248.7	4.2
49	248.8	3.9	49	249.6	3.7	49	250.7	3.9	49	251.2	4.2	49	250.1	3.7	49	249.6	3.8	49	250.6	3.9	49	249.2	3.8
50	250.1	3.8	50	250.8	4.0	50	250.8	3.8	50	250.7	4.3	50	251.3	4.0	50	250.5	4.0	50	249.9	4.1	50	249.9	4.0
51	251.3	3.9	51	250.4	3.8	51	250.2	3.9	51	251.2	4.1	51	250.0	3.9	51	250.7	3.6	51	251.2	4.0	51	250.2	3.6
52	250.2	3.8	52	249.5	4.1	52	250.6	4.0	52	250.7	4.3	52	249.8	3.9	52	250.9	3.8	52	249.6	4.0	52	277.8	4.1
53 f	249.4	1.5	53 f	249.7	1.4	53 f	249.9	1.5	53 f	250.8	1.7	53 f	250.5	1.4	53 f	250.2	1.6	53 f	250.2	1.4	53 f	249.7	1.5
54	250.6	3.7	54	251.8	4.1	54	250.2	3.8	54	251.6	4.2	54	249.6	3.7	54	250.5	4.0	54	250.7	4.0	54	250.5	3.9
55	251.2	4.1	55	250.8	3.8	55	251.0	4.1	55	252.1	4.4	55	250.0	3.9	55	250.0	3.7	55	250.7	4.0	55	250.8	4.0
56	248.2	3.8	56	251.1	4.1	56	250.0	4.0	56	250.0	3.9	56	249.8	4.0	56	250.9	3.6	56	249.4	3.6	56	250.5	3.9
57	249.5	4.0	57	249.5	3.9	57	250.2	3.9	57	250.3	4.5	57	252.7	4.0	57	249.1	3.9	57	250.3	4.1	57	251.0	4.2
58	249.3	4.0	58	250.9	4.1	58	251.3	3.9	58	251.1	4.												