

Fec test report:

Date: 2020-10-26 15:43:29

Tester name: Boris

Test#1 Monitoring values

Failed

0	FEC label	009	OK
1	FEC DC2438 ID	6c0000024dc35c26	OK
2	FEC_T (to 35°C)	28.844	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.1A to 1.5A)	1.399	OK
5	FEC_Vad (1.9V to 2.0V)	1.330	FAIL

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Failed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 68	FAIL
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 69	FAIL
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 69	FAIL
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 67	FAIL
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 72	FAIL
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 69	FAIL
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 76	FAIL
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 78	FAIL

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdc(2) Fem(00) FEC_T: 28.844 degC
2	fe 0 moni V 1	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
7	fe 0 moni I 1	0	0 Tdc(2) Fem(00) FEC_I: 1.399 A
8	fe 0 moni S 1	0	0 Tdc(2) Fem(00) FEC_Serial: 6c0000024dc35c26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x2088000 (34111488) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0xb0b 0xb0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0xc0c 0xc0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0xd0d 0xd0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdc(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdc(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdc(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdc(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdc(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdc(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdc(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdc(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 TdcM(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
46	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
51	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
56	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
61	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
66	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 TdcM(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
78	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
83	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
88	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
93	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
98	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 TdcM(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.340 V
110	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V

115	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
120	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
125	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
130	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 TdcM(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
142	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
147	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
152	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
157	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.330 V
162	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff0000
168	fe 0 after 12 test_mode 0x1	0	0 TdcM(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	429.9	11.8	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	351.0	0.7	2 r	320.8	0.6	2 r	307.2	0.7	2 r	313.3	0.7	2 r	287.7	0.7	2 r	318.2	0.7	2 r	295.8	0.7	2 r	302.1	0.7
3	360.1	4.2	3	360.4	4.4	3	158.8	4.7	3	304.5	5.2	3	307.8	4.9	3	262.5	4.6	3	223.4	4.5	3	243.2	4.5
4	245.7	4.3	4	289.3	4.2	4	278.6	4.1	4	260.2	4.5	4	288.7	4.5	4	267.0	4.3	4	229.4	4.3	4	219.4	4.4
5	276.0	4.2	5	233.6	4.3	5	164.5	4.5	5	190.3	5.0	5	326.8	4.8	5	251.9	4.3	5	273.0	4.4	5	226.1	4.5
6	310.3	4.3	6	246.9	4.4	6	185.4	4.3	6	215.2	4.9	6	302.1	4.6	6	232.9	4.4	6	272.8	4.2	6	230.5	4.3
7	326.9	4.1	7	240.2	4.4	7	135.5	4.7	7	241.7	4.9	7	280.7	4.7	7	284.4	4.5	7	219.2	4.8	7	215.3	4.6
8	366.1	4.5	8	315.0	4.2	8	213.0	4.4	8	178.5	4.8	8	266.8	4.5	8	172.8	4.5	8	178.0	4.3	8	305.1	4.5
9	253.6	4.2	9	288.8	4.1	9	134.0	4.3	9	270.0	4.9	9	316.5	4.6	9	175.0	4.5	9	210.2	4.2	9	281.9	4.5
10	340.2	4.3	10	293.0	4.1	10	131.8	4.2	10	193.9	4.6	10	193.5	4.5	10	224.9	4.1	10	195.4	4.2	10	155.6	4.3
11	194.6	4.3	11	244.6	4.2	11	194.6	4.4	11	232.6	4.6	11	257.0	4.8	11	234.8	4.4	11	232.2	4.4	11	310.1	4.5
12	299.2	4.3	12	278.9	4.1	12	171.8	4.1	12	187.4	4.6	12	331.4	4.8	12	204.1	4.4	12	333.9	4.3	12	189.7	4.5
13	209.1	4.6	13	289.4	4.0	13	128.2	4.5	13	252.0	4.9	13	292.1	4.5	13	244.2	4.4	13	212.2	4.4	13	297.3	4.5
14	305.9	4.3	14	207.7	4.1	14	124.7	4.4	14	217.0	4.5	14	287.1	4.4	14	283.5	4.4	14	173.5	4.2	14	322.2	4.4
15 f	235.1	1.7	15 f	215.8	1.8	15 f	131.4	1.7	15 f	287.1	1.8	15 f	301.9	1.6	15 f	247.2	1.7	15 f	252.2	1.7	15 f	238.4	1.7
16	283.4	4.1	16	315.1	4.1	16	184.1	4.2	16	259.9	4.8	16	222.6	4.3	16	211.8	4.1	16	241.4	4.2	16	211.6	4.4
17	226.0	4.1	17	287.3	4.1	17	237.7	4.1	17	323.3	4.5	17	285.6	4.6	17	260.8	4.1	17	280.3	4.2	17	181.8	4.1
18	233.9	4.2	18	289.0	3.9	18	191.2	4.2	18	225.8	4.9	18	271.2	4.4	18	295.7	4.3	18	349.2	4.2	18	159.4	4.3
19	312.9	4.3	19	290.9	4.3	19	228.4	4.6	19	197.3	4.5	19	182.9	4.3	19	203.3	4.4	19	243.1	4.2	19	225.5	4.4
20	267.5	4.3	20	233.9	4.1	20	158.1	4.5	20	250.9	4.6	20	304.5	4.4	20	255.9	4.1	20	209.4	4.3	20	247.9	4.3
21	264.6	4.2	21	246.1	4.2	21	174.9	4.4	21	240.9	4.6	21	212.0	4.4	21	348.6	4.4	21	249.5	4.4	21	173.2	4.5
22	327.8	4.6	22	264.0	4.3	22	224.0	4.1	22	192.7	4.8	22	243.3	4.5	22	267.4	4.4	22	207.0	4.1	22	243.1	4.4
23	339.8	4.3	23	293.9	4.1	23	171.4	4.4	23	213.2	4.3	23	293.8	4.4	23	248.7	4.2	23	197.5	4.1	23	247.8	4.6
24	340.1	4.3	24	289.6	4.2	24	212.4	4.8	24	204.1	4.6	24	160.0	4.3	24	235.2	4.2	24	235.4	4.2	24	244.7	4.2
25	237.5	4.2	25	323.6	4.2	25	136.9	4.2	25	279.0	4.3	25	329.6	4.1	25	288.0	4.3	25	200.2	4.2	25	182.3	4.2
26	316.5	4.2	26	243.5	4.0	26	202.5	4.1	26	218.7	4.2	26	260.6	4.3	26	276.0	4.4	26	287.7	4.6	26	209.4	4.2
27	263.3	4.2	27	235.8	3.9	27	196.3	4.4	27	173.6	4.3	27	300.5	4.5	27	210.2	4.0	27	240.2	4.4	27	210.9	4.3
28 f	277.5	1.6	28 f	208.9	1.7	28 f	204.9	1.8	28 f	230.6	1.7	28 f	255.9	1.8	28 f	258.0	1.7	28 f	282.7	1.7	28 f	218.8	1.8
29	268.2	4.3	29	235.3	3.8	29	211.3	4.5	29	210.0	4.5	29	235.3	4.5	29	249.5	4.4	29	230.9	4.2	29	275.1	4.5
30	272.4	4.3	30	248.5	4.0	30	148.6	4.2	30	240.7	4.4	30	207.1	4.2	30	232.4	4.2	30	281.5	4.1	30	304.0	4.5
31	230.6	4.1	31	320.4	4.0	31	222.0	4.4	31	244.4	4.7	31	313.5	4.3	31	281.1	4.5	31	238.8	4.1	31	379.2	4.3
32	262.0	4.3	32	218.6	4.1	32	246.6	4.2	32	290.9	4.4	32	194.8	4.3	32	261.3	4.2	32	249.9	4.1	32	186.8	4.4
33	281.8	3.9	33	244.3	4.2	33	206.8	4.2	33	276.9	4.5	33	268.3	4.3	33	277.5	4.2	33	167.9	4.3	33	266.6	4.3
34	234.9	4.1	34	265.0	4.2	34	227.8	4.2	34	287.5	4.3	34	297.3	4.3	34	324.0	4.2	34	217.9	4.1	34	216.7	4.3
35	267.3	4.1	35	371.5	4.1	35	204.5	4.2	35	207.2	4.5	35	282.1	4.3	35	316.2	4.5	35	230.4	4.5	35	296.8	4.5
36	305.9	4.0	36	228.4	4.1	36	226.1	4.2	36	268.8	4.3	36	222.4	4.3	36	368.5	4.0	36	193.1	4.0	36	192.4	4.2
37	253.8	4.5	37	233.8	4.0	37	186.9	4.2	37	162.9	4.5	37	284.3	4.4	37	282.8	4.1	37	350.1	4.3	37	240.6	4.5
38	261.0	4.0	38	180.7	4.0	38	230.3	4.0	38	256.6	4.4	38	219.2	4.3	38	286.7	4.3	38	227.8	4.2	38	265.6	4.3
39	295.1	4.4	39	292.9	4.2	39	274.7	4.6	39	210.0	4.7	39	255.1	4.6	39	278.1	4.4	39	219.9	4.5	39	270.1	4.6
40	342.3	4.1	40	148.4	4.0	40	245.0	4.1	40	261.1	4.3	40	207.9	4.4	40	239.8	4.1	40	279.2	4.1	40	268.5	4.7
41	341.6	3.9	41	348.9	3.9	41	303.0	3.6	41	208.5	3.8	41	280.4	4.1	41	283.6	3.9	41	209.2	3.9	41	248.1	4.1
42	251.6	4.0	42	288.6	4.0	42	251.6	3.9	42	197.3	4.0	42	277.5	4.2	42	193.8	3.9	42	214.4	4.0	42	291.4	4.3
43	336.4	3.7	43	315.3	3.9	43	228.8	4.0	43	243.4	3.9	43	318.9	4.0	43	318.4	4.0	43	234.2	4.0	43	315.3	4.2
44	319.5	3.9	44	225.1	3.8	44	300.4	4.0	44	253.7	4.1	44	229.9	4.1	44	266.6	4.0	44	298.2	4.4	44	246.8	4.5
45	301.2	3.8	45	268.0	3.9	45	225.5	4.0	45	195.4	3.9	45	331.6	4.1	45	297.0	3.9	45	286.7	4.1	45	264.3	4.1
46	259.2	3.9	46	188.4	4.0	46	290.1	3.9	46	219.9	4.2	46	267.5	3.9	46	249.9	4.0	46	222.6	4.3	46	183.1	4.4
47	282.8	3.9	47	289.9	3.6	47	282.9	3.9	47	235.9	3.9	47	242.2	4.0	47	277.8	3.8	47	246.0	4.0	47	332.5	4.2
48	239.7	4.0	48	323.0	4.0	48	158.5	4.3	48	240.8	4.1	48	244.5	4.1	48	220.7	4.1	48	208.9	4.1	48	273.3	4.5
49	180.0	4.0	49	352.3	4.0	49	288.4	4.0	49	244.8	4.0	49	250.4	4.2	49	332.9	4.0	49	224.2	4.1	49	258.7	4.1
50	250.9	3.7	50	275.6	4.0	50	282.9	4.1	50	243.7	4.1	50	306.0	4.2	50	319.1	4.1	50	244.3	4.3	50	283.7	4.4
51	197.1	4.0	51	309.0	3.9	51	183.1	4.1	51	195.5	3.9	51	282.1	4.0	51	210.9	3.9	51	329.4	4.1	51	330.4	4.3
52	306.6	3.9	52	276.0	3.9	52	169.1	4.2	52	283.9	4.1	52	265.1	4.2	52	256.1	4.0	52	210.6	4.1	52	233.8	4.3
53 f	264.6	1.6	53 f	324.2	1.6	53 f	188.6	1.7	53 f	140.4	1.6	53 f	259.9	1.6	53 f	208.6	1.7	53 f	252.6	1.7	53 f	247.8	1.6
54	261.7	4.0	54	222.3	4.4	54	195.2	4.3	54	248.4	4.2	54	255.6	3.9	54	241.1	4.0	54	200.0	4.2	54	254.9	4.2
55	327.6	4.0	55	291.3	3.9	55	226.8	4.1	55	233.1	4.1	55	271.9	4.1	55	260.6	4.0	55	109.6	4.3	55	205.4	4.3
56	222.7	3.8	56	259.0	3.9	56	158.3	4.1	56	201.4	3.9	56	263.0	4.3	56	247.3	4.3	56	280.6	4.2	56	192.4	4.5
57	313.8	4.0	57	355.8	3.9	57	166.1	4.2	57	211.8	4.1	57	260.6	4.1	57	260.4	4.0	57	188.8	4.1	57	157.2	4.5
58	282.4	3.9	58	278.1	4.1	58	202.2	3.9	58	206.2	4.1	58	241.0</										

Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	408.9	10.4	1 r	485.1	6.0	1 r	250.1	12.1	1 r	330.5	10.2	1 r	381.6	13.1	1 r	315.6	11.2	1 r	289.0	11.7	1 r	335.5	9.7
2 r	250.2	0.7	2 r	249.9	0.6	2 r	250.3	0.7	2 r	250.4	0.7	2 r	249.9	0.7	2 r	250.3	0.7	2 r	250.1	0.7	2 r	250.3	0.7
3	250.8	4.5	3	250.5	4.5	3	249.4	4.8	3	249.7	5.2	3	249.7	4.9	3	250.4	4.7	3	251.2	4.8	3	251.3	4.7
4	250.0	4.3	4	251.2	4.3	4	248.2	4.4	4	249.5	4.6	4	249.1	4.3	4	250.6	4.4	4	250.6	4.4	4	250.2	4.4
5	250.6	4.3	5	249.4	4.4	5	250.9	4.4	5	251.0	5.2	5	250.4	4.7	5	250.1	4.4	5	251.0	4.7	5	251.1	4.4
6	250.0	4.1	6	249.2	4.3	6	251.2	4.5	6	250.6	4.6	6	250.9	4.6	6	250.3	4.4	6	249.7	4.5	6	249.6	4.5
7	251.0	4.5	7	251.8	4.3	7	249.4	4.5	7	250.2	5.0	7	249.1	4.8	7	251.4	4.6	7	251.2	4.3	7	249.9	4.6
8	249.8	4.2	8	251.1	4.2	8	250.3	4.5	8	249.8	4.3	8	250.1	4.4	8	250.0	4.4	8	251.2	4.4	8	250.3	4.3
9	249.6	4.4	9	250.0	4.2	9	250.6	4.5	9	250.3	5.0	9	250.1	4.6	9	250.3	4.5	9	250.0	4.4	9	249.8	4.7
10	250.2	4.1	10	251.1	4.4	10	250.7	4.2	10	250.9	4.5	10	249.5	4.6	10	249.5	4.2	10	250.8	4.4	10	248.5	4.2
11	251.3	4.3	11	249.4	4.5	11	250.9	4.5	11	250.8	4.7	11	249.1	4.7	11	251.8	4.2	11	249.8	4.3	11	249.4	4.4
12	249.5	4.4	12	250.6	4.1	12	249.4	4.3	12	249.6	4.3	12	250.8	4.4	12	249.9	4.4	12	249.7	4.1	12	248.4	4.3
13	249.8	4.2	13	250.9	4.4	13	249.9	4.4	13	250.6	4.8	13	249.5	4.6	13	250.5	4.4	13	248.2	4.6	13	250.5	4.4
14	250.3	4.0	14	250.4	3.9	14	250.2	4.3	14	251.6	4.4	14	251.4	4.5	14	249.7	4.2	14	250.6	4.3	14	251.1	4.3
15 f	250.5	1.8	15 f	249.2	1.7	15 f	251.1	1.8	15 f	249.9	1.7	15 f	249.7	1.6	15 f	250.8	1.8	15 f	250.4	1.6	15 f	250.7	1.8
16	251.3	4.1	16	250.6	4.2	16	250.5	4.3	16	249.9	4.8	16	248.3	4.5	16	250.8	4.4	16	251.3	4.4	16	249.7	4.4
17	248.7	4.2	17	250.3	4.0	17	249.8	4.3	17	249.1	4.5	17	249.4	4.3	17	249.7	4.4	17	249.7	4.3	17	248.9	4.1
18	249.9	4.2	18	249.7	4.0	18	250.4	4.2	18	251.4	4.6	18	251.2	4.3	18	249.1	4.3	18	250.1	4.3	18	250.2	4.3
19	250.4	4.1	19	249.1	4.2	19	250.3	4.2	19	251.8	4.5	19	249.8	4.3	19	252.4	4.2	19	251.3	4.0	19	248.6	4.3
20	249.9	4.2	20	251.5	4.2	20	250.6	4.3	20	250.0	4.6	20	249.5	4.3	20	250.7	4.4	20	251.3	4.5	20	248.0	4.6
21	249.6	4.1	21	248.9	4.0	21	249.9	4.2	21	248.3	4.4	21	249.2	4.1	21	250.5	4.3	21	250.6	4.2	21	250.2	4.3
22	250.3	4.0	22	250.5	4.5	22	250.1	4.3	22	250.5	4.8	22	249.5	4.6	22	251.1	4.0	22	250.7	4.2	22	249.3	4.3
23	249.7	4.5	23	248.7	4.1	23	251.6	4.4	23	248.4	4.5	23	249.9	4.3	23	250.2	4.1	23	251.8	4.2	23	249.9	4.0
24	251.6	4.4	24	250.5	4.2	24	251.6	4.1	24	249.8	4.5	24	250.1	4.6	24	249.5	4.4	24	250.3	4.3	24	249.5	4.2
25	252.2	4.4	25	250.9	4.1	25	248.8	4.2	25	250.6	4.3	25	249.7	4.1	25	248.3	4.4	25	251.2	4.0	25	248.3	4.4
26	249.2	4.3	26	250.6	4.2	26	249.7	4.7	26	251.5	4.4	26	249.3	4.3	26	249.2	4.3	26	248.7	4.5	26	249.6	4.3
27	250.4	4.1	27	250.1	4.3	27	252.2	4.1	27	250.1	4.3	27	250.4	4.3	27	251.0	4.3	27	250.1	4.7	27	250.7	4.4
28 f	250.9	1.7	28 f	250.5	1.6	28 f	250.5	1.8	28 f	249.7	1.9	28 f	250.4	1.6	28 f	249.9	1.6	28 f	249.8	1.7	28 f	249.7	1.9
29	251.4	4.2	29	250.5	3.9	29	248.8	4.2	29	251.2	4.3	29	250.4	4.4	29	249.1	4.3	29	250.9	4.3	29	249.8	4.4
30	249.7	4.2	30	249.8	4.1	30	249.3	4.0	30	252.2	4.4	30	251.0	4.3	30	250.3	4.2	30	250.3	4.3	30	250.4	4.1
31	250.5	4.0	31	251.6	4.0	31	250.0	4.2	31	249.4	4.6	31	249.8	4.5	31	249.5	4.3	31	249.5	4.0	31	251.0	4.5
32	251.7	4.2	32	250.0	4.0	32	250.2	4.3	32	250.9	4.3	32	249.2	4.3	32	250.7	4.2	32	250.2	4.2	32	249.4	4.4
33	248.7	4.0	33	250.2	4.2	33	249.6	4.4	33	249.4	4.4	33	250.5	4.5	33	250.8	4.2	33	250.9	4.2	33	249.3	4.6
34	251.0	4.2	34	249.8	4.2	34	251.2	4.1	34	249.9	4.3	34	250.5	4.8	34	249.7	4.3	34	251.1	4.3	34	250.8	4.2
35	252.2	4.2	35	251.5	4.2	35	249.2	4.3	35	251.2	4.6	35	250.4	4.6	35	251.7	4.2	35	251.1	4.5	35	250.2	4.5
36	250.3	4.2	36	251.9	4.1	36	250.4	4.2	36	249.7	4.3	36	249.9	4.4	36	249.8	4.3	36	250.2	4.2	36	250.8	4.4
37	250.2	4.1	37	249.3	4.0	37	250.4	4.3	37	251.0	4.4	37	248.6	4.2	37	249.1	4.2	37	247.4	4.2	37	249.3	4.5
38	250.7	3.9	38	248.7	3.9	38	250.3	4.4	38	250.4	4.4	38	251.6	4.2	38	249.7	4.2	38	249.3	4.0	38	249.6	4.3
39	249.0	4.4	39	250.5	4.2	39	249.3	4.6	39	250.7	4.8	39	250.0	4.3	39	251.3	4.5	39	250.5	4.5	39	250.3	4.5
40	250.3	4.2	40	251.2	3.9	40	248.1	4.0	40	250.2	4.3	40	249.5	4.7	40	250.1	4.2	40	250.3	4.1	40	250.1	4.4
41	247.9	4.2	41	249.6	4.1	41	250.5	4.2	41	250.3	4.0	41	249.9	4.0	41	249.8	3.9	41	249.8	4.2	41	248.5	4.7
42	250.1	4.2	42	248.9	3.8	42	249.6	4.1	42	250.1	4.0	42	251.4	4.1	42	248.7	4.0	42	251.1	4.2	42	251.5	4.3
43	249.6	4.0	43	250.3	3.9	43	249.0	3.9	43	249.3	3.7	43	250.6	4.1	43	250.7	4.2	43	250.3	3.7	43	251.7	4.4
44	249.8	3.8	44	250.8	4.1	44	250.8	3.9	44	249.1	4.0	44	250.0	3.9	44	248.9	4.2	44	250.9	4.0	44	249.6	4.1
45	250.2	3.9	45	250.4	3.9	45	250.0	4.3	45	248.7	3.9	45	249.9	4.3	45	250.0	4.0	45	249.6	4.0	45	249.7	4.2
46	251.2	3.9	46	251.0	3.8	46	251.7	3.9	46	249.9	4.0	46	251.6	4.2	46	250.1	4.2	46	250.8	4.0	46	249.6	4.2
47	248.7	4.1	47	250.0	3.8	47	250.6	3.9	47	249.6	4.0	47	250.4	4.0	47	250.7	4.2	47	250.8	4.2	47	250.7	4.2
48	248.4	3.9	48	249.7	3.9	48	251.1	4.0	48	251.2	4.2	48	248.7	4.1	48	248.7	4.2	48	250.2	4.0	48	251.0	4.2
49	250.9	3.9	49	250.1	3.9	49	250.0	3.9	49	249.9	4.0	49	250.9	4.2	49	249.4	4.0	49	251.2	4.1	49	250.9	4.3
50	249.3	4.0	50	250.1	4.0	50	250.7	4.1	50	250.0	4.2	50	249.6	4.2	50	250.7	4.0	50	250.3	4.6	50	249.8	4.7
51	250.4	3.7	51	250.4	3.8	51	250.3	4.0	51	250.6	3.9	51	250.0	4.2	51	249.7	4.0	51	250.3	4.3	51	249.7	4.0
52	248.5	4.0	52	250.0	4.1	52	249.6	4.2	52	249.8	4.6	52	249.4	4.5	52	250.6	4.1	52	250.7	4.2	52	250.7	4.4
53 f	249.6	1.5	53 f	250.7	1.5	53 f	249.8	1.6	53 f	250.4	1.5	53 f	250.7	1.7	53 f	249.5	1.7	53 f	249.7	1.7	53 f	249.5	1.6
54	249.2	4.2	54	251.2	4.1	54	251.6	3.9	54	250.2	4.2	54	249.9	4.3	54	249.3	4.1	54	252.1	4.2	54	250.6	4.3
55	249.2	4.2	55	250.8	4.0	55	249.5	3.9	55	249.6	3.9	55	249.4	4.3	55	248.9	4.0	55	250.5	4.5	55	252.0	4.5
56	249.2	4.0	56	251.0	3.9	56	249.5	3.9	56	249.8	3.9	56	249.9	4.1	56	251.8	4.0	56	250.0	4.0	56	250.1	4.3
57	249.3	4.0	57	249.8	4.2	57	250.5	4.0	57	250.5	4.2	57	249.9	4.2	57	250.7	4.1	57	250.4	4.2	57	249.3	4.5
58	250.4	3.9	58	249.7	4.0	58	250.1	4.0	58	249.7													