

Fec test report:

Date: 2020-10-26 15:48:10

Tester name: Boris

Test#1 Monitoring values

Failed

0	FEC label	011	OK
1	FEC DC2438 ID	630000024da7d926	OK
2	FEC_T (to 35°C)	24.062	OK
3	FEC_Vdd (3.2V to 3.4V)	3.280	OK
4	FEC_I (1.1A to 1.5A)	1.504	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3020	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3010	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3049	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3018	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3032	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3085	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3041	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3049	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
1	fe 0 moni T 1	0	0 Tdc(2) Fem(00) FEC_T: 24.062 degC
2	fe 0 moni V 1	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.280 V
3	fe 0 pulser 1 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 1 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 1	0	0 Tdc(2) Fem(00) FEC_I: 1.504 A
8	fe 0 moni S 1	0	0 Tdc(2) Fem(00) FEC_Serial: 630000024da7d926

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 2	0	0 Tdc(2) Fem(00) Reg(1) <- 0x80000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x2088000 (34111488) FEC_Enable: 2
3	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0909 0x0909 (1 chip verified)
12	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0a0a 0x0a0a (1 chip verified)
13	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0b0b 0x0b0b (1 chip verified)
14	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0c0c 0x0c0c (1 chip verified)
15	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0d0d 0x0d0d (1 chip verified)
16	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0e0e 0x0e0e (1 chip verified)
17	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
18	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
19	fe 0 after 8 read 3	0	0 Tdc(2) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
20	fe 0 after 9 read 3	0	0 Tdc(2) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
21	fe 0 after 10 read 3	0	0 Tdc(2) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
22	fe 0 after 11 read 3	0	0 Tdc(2) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
23	fe 0 after 12 read 3	0	0 Tdc(2) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
24	fe 0 after 13 read 3	0	0 Tdc(2) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
25	fe 0 after 14 read 3	0	0 Tdc(2) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
26	fe 0 after 15 read 3	0	0 Tdc(2) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
27	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 1 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 1 write 0x5 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdcm(2): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdcm(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 TdcM(2) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdf	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfdf0000
72	fe 0 after 9 test_mode 0x1	0	0 TdcM(2) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 TdcM(2) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 1 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 1 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 Tdc(2) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xefff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xefff0000
168	fe 0 after 12 test_mode 0x1	0	0 Tdc(2) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
184	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
189	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdc(2) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdc(2) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdc(2) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdc(2) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 1	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	496.8	9.7	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	458.4	11.2	1 r	511.0	0.0
2 r	393.1	0.7	2 r	318.2	0.7	2 r	372.1	0.7	2 r	365.1	0.7	2 r	356.8	0.7	2 r	311.0	0.7	2 r	285.1	0.7	2 r	320.6	0.7
3	328.2	4.2	3	174.7	4.7	3	378.3	4.6	3	302.3	5.3	3	337.1	4.8	3	378.8	4.7	3	215.3	4.4	3	264.6	4.8
4	310.2	4.1	4	200.4	4.1	4	330.5	4.1	4	274.0	4.5	4	305.8	4.3	4	340.9	4.4	4	295.9	4.4	4	222.1	4.4
5	355.3	4.2	5	191.8	4.2	5	359.9	4.3	5	309.4	5.0	5	314.8	4.4	5	342.7	4.5	5	166.2	4.4	5	277.7	4.6
6	280.3	4.0	6	217.2	4.2	6	330.5	4.2	6	220.2	4.6	6	251.7	4.6	6	307.4	4.3	6	239.8	4.2	6	246.3	4.5
7	274.5	4.1	7	162.9	4.3	7	351.5	4.3	7	300.1	5.2	7	228.6	4.5	7	274.8	4.2	7	253.0	4.4	7	177.0	4.4
8	350.8	4.3	8	165.0	4.1	8	330.7	4.2	8	265.5	4.8	8	322.2	4.3	8	230.4	4.6	8	307.5	4.5	8	230.3	4.5
9	230.2	4.0	9	189.1	4.4	9	364.5	4.2	9	270.5	4.9	9	245.5	4.5	9	337.0	4.2	9	219.4	4.2	9	194.2	4.6
10	275.3	4.1	10	225.6	4.1	10	362.6	4.2	10	251.9	4.7	10	242.6	4.3	10	287.7	4.3	10	204.6	4.5	10	207.9	4.6
11	277.6	4.2	11	182.4	4.1	11	324.9	4.4	11	217.6	4.9	11	259.7	4.3	11	292.9	4.3	11	318.6	4.2	11	256.0	4.5
12	357.6	4.0	12	271.9	4.0	12	441.8	4.1	12	265.4	4.5	12	260.6	4.3	12	358.1	4.2	12	288.4	4.3	12	328.1	4.4
13	292.2	4.3	13	115.3	4.1	13	312.8	4.3	13	242.9	4.7	13	280.6	4.6	13	280.5	4.2	13	294.3	4.3	13	172.2	4.8
14	222.3	4.2	14	200.2	4.1	14	345.2	4.2	14	237.5	4.7	14	277.6	4.5	14	373.3	4.1	14	240.8	4.4	14	169.3	4.5
15 f	325.2	1.7	15 f	209.0	1.6	15 f	359.3	1.6	15 f	255.7	1.7	15 f	191.9	1.6	15 f	302.6	1.6	15 f	183.2	1.7	15 f	271.9	1.6
16	355.8	4.2	16	174.7	4.0	16	327.5	4.3	16	275.8	4.8	16	271.3	4.4	16	205.2	4.2	16	232.6	4.3	16	228.6	4.8
17	254.3	4.0	17	157.1	4.3	17	275.9	4.1	17	268.6	4.4	17	184.2	4.4	17	327.4	4.3	17	264.8	4.0	17	263.5	4.4
18	293.4	4.0	18	175.0	4.2	18	354.9	4.0	18	206.3	4.8	18	283.3	4.3	18	260.7	4.3	18	207.6	4.5	18	178.1	4.6
19	229.0	3.9	19	291.7	4.2	19	359.5	4.3	19	270.3	4.5	19	288.6	4.2	19	252.4	4.3	19	226.7	4.2	19	183.9	4.5
20	340.3	4.4	20	186.7	4.2	20	342.1	4.6	20	295.1	5.0	20	259.4	4.1	20	260.1	4.5	20	345.4	4.2	20	169.3	4.4
21	352.4	4.0	21	196.8	4.2	21	294.1	4.0	21	259.0	4.4	21	179.7	4.4	21	281.9	4.0	21	223.8	4.3	21	290.0	4.4
22	317.7	3.9	22	214.4	4.1	22	277.2	4.1	22	182.4	4.4	22	268.9	4.3	22	279.1	4.4	22	215.9	4.2	22	182.5	4.6
23	292.0	4.1	23	245.5	4.2	23	352.1	4.2	23	263.9	4.4	23	261.4	4.2	23	316.2	4.2	23	110.1	4.2	23	197.6	4.5
24	290.2	4.1	24	203.2	4.2	24	348.1	4.4	24	273.5	4.7	24	264.3	4.2	24	245.8	4.4	24	172.7	4.3	24	311.9	4.5
25	354.6	4.0	25	204.9	4.3	25	334.1	4.0	25	263.5	4.4	25	216.1	4.4	25	191.6	4.2	25	258.3	4.5	25	223.4	4.5
26	339.3	4.0	26	217.6	4.0	26	311.3	4.1	26	287.8	4.5	26	246.4	4.3	26	270.4	4.2	26	225.7	4.5	26	217.1	4.5
27	246.4	3.9	27	166.3	3.9	27	298.5	4.1	27	273.6	4.3	27	252.8	4.2	27	305.4	4.3	27	148.1	4.1	27	276.5	4.3
28 f	295.9	1.7	28 f	191.8	1.6	28 f	352.4	1.7	28 f	313.6	1.7	28 f	280.5	1.7	28 f	211.9	1.7	28 f	198.5	1.8	28 f	129.4	1.8
29	296.4	4.1	29	273.1	4.2	29	321.4	4.3	29	253.5	4.6	29	181.2	4.2	29	335.0	4.4	29	267.3	4.3	29	217.6	4.5
30	310.3	4.0	30	195.7	4.0	30	302.8	4.6	30	351.8	4.8	30	280.5	4.2	30	245.4	4.0	30	341.6	4.2	30	310.2	4.4
31	339.1	4.1	31	209.8	4.4	31	357.4	4.1	31	316.2	4.3	31	323.1	4.2	31	294.8	4.1	31	206.6	4.2	31	267.0	4.6
32	321.4	4.1	32	159.2	4.4	32	343.8	3.9	32	312.5	4.5	32	344.1	4.2	32	293.0	4.2	32	187.3	4.2	32	243.6	4.8
33	270.6	4.0	33	272.9	4.5	33	283.7	4.2	33	228.0	4.5	33	214.1	4.4	33	136.0	4.1	33	175.7	4.2	33	245.7	4.6
34	312.0	3.9	34	249.8	4.0	34	365.5	4.1	34	237.3	4.7	34	264.4	4.2	34	339.4	4.1	34	118.4	4.4	34	272.0	4.8
35	280.1	3.9	35	278.7	4.3	35	293.5	4.1	35	314.3	4.5	35	180.1	4.4	35	325.2	4.2	35	314.8	4.4	35	242.5	5.0
36	311.0	3.9	36	273.0	4.2	36	304.4	4.0	36	278.8	4.4	36	292.4	4.5	36	303.7	4.0	36	259.2	4.2	36	263.6	4.5
37	320.8	4.1	37	204.9	4.2	37	373.6	4.0	37	200.4	4.4	37	356.0	4.3	37	292.3	4.3	37	211.0	4.3	37	285.4	4.5
38	320.0	4.0	38	240.4	4.0	38	232.9	4.0	38	286.9	4.4	38	241.4	4.4	38	171.6	4.1	38	197.5	4.3	38	240.3	4.6
39	302.5	4.1	39	184.1	4.3	39	275.8	4.2	39	268.6	4.8	39	319.0	4.5	39	327.6	4.3	39	166.2	4.5	39	238.9	4.9
40	322.9	4.3	40	203.7	4.1	40	316.5	3.9	40	301.6	4.3	40	316.7	4.1	40	183.5	4.4	40	239.7	4.0	40	255.8	4.4
41	352.1	3.7	41	209.3	3.8	41	314.8	3.8	41	277.9	4.1	41	231.9	4.0	41	316.2	3.9	41	235.7	3.8	41	223.2	4.2
42	366.1	3.9	42	264.0	4.0	42	312.8	3.9	42	246.7	4.0	42	311.1	4.1	42	284.9	4.2	42	232.0	4.3	42	201.8	4.8
43	390.4	3.7	43	266.8	3.8	43	237.5	3.8	43	305.1	4.0	43	290.1	3.9	43	226.2	4.3	43	145.9	4.0	43	219.0	4.6
44	350.0	3.6	44	240.1	3.8	44	295.2	3.7	44	309.1	3.9	44	259.7	3.9	44	193.1	4.2	44	169.9	4.0	44	244.4	4.4
45	284.2	3.8	45	187.9	3.9	45	323.9	3.8	45	256.4	3.9	45	265.9	3.9	45	302.8	3.8	45	236.2	4.0	45	256.3	4.4
46	340.0	3.7	46	208.4	4.1	46	297.6	3.9	46	302.8	4.0	46	229.2	3.9	46	256.4	4.0	46	265.2	4.4	46	291.4	4.8
47	227.8	3.7	47	235.4	3.8	47	312.3	3.6	47	286.8	4.0	47	272.8	3.8	47	202.5	3.9	47	238.3	4.0	47	269.3	4.6
48	232.2	4.0	48	275.5	3.9	48	317.2	3.8	48	299.2	4.1	48	274.1	4.0	48	242.9	4.0	48	204.7	3.9	48	236.7	4.6
49	373.7	4.0	49	189.1	3.9	49	317.1	3.8	49	211.8	4.0	49	271.1	3.9	49	248.6	3.9	49	232.7	4.0	49	276.1	4.3
50	361.5	3.9	50	216.8	3.9	50	365.4	3.8	50	267.9	4.1	50	270.3	3.8	50	309.0	4.1	50	304.9	4.0	50	256.4	4.8
51	386.7	3.6	51	189.8	3.9	51	368.7	3.7	51	258.1	4.2	51	225.5	3.9	51	326.2	3.9	51	300.9	3.8	51	271.6	4.7
52	257.7	3.8	52	245.1	4.0	52	290.7	3.7	52	269.4	3.9	52	238.0	3.9	52	166.7	4.1	52	170.7	4.1	52	352.9	4.6
53 f	304.0	1.4	53 f	203.8	1.4	53 f	318.8	1.4	53 f	333.7	1.5	53 f	218.5	1.5	53 f	355.5	1.6	53 f	226.4	1.6	53 f	242.4	1.6
54	293.7	3.8	54	139.7	4.0	54	342.9	3.9	54	278.5	3.7	54	262.4	3.8	54	249.2	4.0	54	233.6	4.2	54	171.8	4.2
55	317.1	3.8	55	247.2	3.8	55	351.1	4.1	55	210.0	4.1	55	235.3	4.0	55	263.2	3.9	55	127.3	4.2	55	274.3	4.6
56	334.0	3.6	56	208.8	4.1	56	386.3	3.9	56	301.7	4.0	56	326.6	3.8	56	268.1	4.0	56	311.9	4.1	56	205.2	4.4
57	345.6	3.9	57	267.6	4.2	57	379.2	4.1	57	270.9	4.0	57	164.9	4.5	57	240.2	4.1	57	210.8	4.1	57	283.2	4.5
58	299.5	3.8	58	175.2	4.0	58	353.4	3.9	58	259.2	3.9	58	254.2</										

Pedestal after centermean.

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	511.0	0.0	1 r	251.1	11.0	1 r	458.4	9.9	1 r	495.1	5.9	1 r	462.2	8.5	1 r	451.1	10.5	1 r	251.4	11.0	1 r	313.3	11.5
2 r	249.8	0.7	2 r	250.4	0.7	2 r	250.2	0.7	2 r	250.3	0.7	2 r	249.9	0.7	2 r	250.4	0.7	2 r	250.2	0.7	2 r	249.9	0.7
3	249.1	4.2	3	249.8	4.6	3	250.3	4.8	3	250.2	5.3	3	250.2	5.2	3	249.8	4.5	3	251.0	4.7	3	250.4	4.7
4	249.9	4.1	4	250.9	4.3	4	249.6	4.2	4	250.8	4.7	4	250.2	4.4	4	250.3	4.2	4	251.6	4.2	4	250.6	4.6
5	248.6	4.4	5	248.7	4.5	5	248.5	4.3	5	250.9	5.2	5	250.6	4.3	5	249.6	4.5	5	251.6	4.5	5	249.8	4.5
6	249.9	4.1	6	248.7	4.6	6	250.8	4.2	6	250.2	4.6	6	248.7	4.3	6	251.1	4.3	6	249.3	4.2	6	251.2	4.5
7	249.8	4.2	7	249.8	4.3	7	250.8	4.5	7	249.9	5.3	7	250.6	4.6	7	248.8	4.5	7	248.8	4.3	7	250.6	4.5
8	248.6	4.0	8	250.2	4.4	8	250.4	4.1	8	250.4	4.8	8	249.5	4.4	8	250.3	4.2	8	250.4	4.4	8	250.5	4.2
9	250.4	4.6	9	248.7	4.2	9	250.7	4.5	9	249.9	5.1	9	249.8	4.5	9	250.2	4.1	9	252.1	4.3	9	250.1	4.6
10	249.6	4.1	10	249.5	4.2	10	250.9	4.3	10	249.6	4.6	10	249.4	4.4	10	249.3	4.3	10	250.7	4.1	10	250.7	4.6
11	248.5	4.2	11	250.7	4.2	11	249.8	4.4	11	249.5	4.8	11	249.3	4.6	11	249.1	4.1	11	249.2	4.3	11	250.2	4.7
12	249.8	3.9	12	248.6	4.4	12	250.1	4.2	12	250.7	4.6	12	248.8	4.2	12	252.2	4.2	12	250.4	4.3	12	249.3	4.3
13	249.3	4.0	13	250.7	4.4	13	248.9	4.2	13	250.5	4.7	13	249.4	4.5	13	250.7	4.3	13	250.9	4.2	13	249.1	4.6
14	250.0	4.1	14	249.6	4.2	14	251.0	4.4	14	250.1	4.5	14	249.1	4.7	14	249.7	4.0	14	251.1	4.1	14	250.7	4.3
15 f	249.6	1.6	15 f	250.3	1.7	15 f	250.1	1.6	15 f	249.3	1.5	15 f	250.5	1.6	15 f	250.0	1.5	15 f	249.8	1.7	15 f	249.9	1.7
16	248.4	4.1	16	249.4	4.0	16	249.2	4.5	16	250.0	4.9	16	251.5	4.4	16	250.0	4.3	16	250.2	4.3	16	250.1	4.5
17	249.1	4.2	17	250.7	4.2	17	248.4	4.0	17	248.2	4.4	17	251.7	4.3	17	250.2	4.3	17	250.7	4.2	17	249.8	4.4
18	250.8	4.0	18	250.0	4.1	18	249.0	4.3	18	251.3	4.9	18	251.1	4.5	18	248.9	4.5	18	249.4	4.7	18	250.7	4.5
19	250.0	4.0	19	249.2	4.2	19	250.6	4.2	19	249.9	4.5	19	249.9	4.2	19	250.4	4.2	19	248.3	4.2	19	249.8	4.4
20	250.6	4.1	20	249.6	4.3	20	249.0	4.3	20	250.8	4.5	20	249.5	4.3	20	250.6	4.3	20	250.8	4.2	20	249.9	4.4
21	249.8	4.0	21	249.8	4.2	21	248.8	4.1	21	250.7	4.4	21	249.3	4.3	21	249.1	4.1	21	249.5	4.2	21	250.0	4.4
22	250.2	4.1	22	250.8	4.3	22	251.7	4.2	22	250.4	4.8	22	249.2	4.5	22	250.7	4.5	22	250.2	4.4	22	250.2	4.5
23	250.5	4.0	23	248.9	4.3	23	250.8	4.2	23	251.3	4.4	23	249.9	4.2	23	250.7	4.2	23	249.4	4.4	23	249.5	4.5
24	249.9	4.3	24	249.9	4.2	24	250.1	4.2	24	251.4	4.8	24	251.0	4.3	24	249.6	4.4	24	249.5	4.6	24	250.3	5.0
25	250.2	4.2	25	250.1	4.1	25	250.1	4.1	25	251.4	4.7	25	247.8	4.5	25	249.8	4.1	25	250.8	4.1	25	250.5	4.3
26	249.6	4.2	26	250.5	4.2	26	250.9	4.2	26	252.0	4.8	26	249.6	4.5	26	250.4	4.0	26	249.7	4.3	26	250.7	4.6
27	249.7	3.9	27	250.6	4.1	27	249.4	4.2	27	250.7	4.2	27	250.8	4.1	27	251.1	4.4	27	249.8	4.3	27	248.9	4.5
28 f	250.4	1.7	28 f	248.5	1.7	28 f	250.5	1.7	28 f	249.5	1.7	28 f	249.2	1.7	28 f	250.4	1.7	28 f	249.1	1.8	28 f	250.9	1.8
29	251.6	4.2	29	250.0	4.3	29	250.7	4.0	29	248.7	4.8	29	250.8	4.4	29	250.3	4.0	29	250.2	4.4	29	250.8	4.7
30	250.5	4.0	30	251.8	4.0	30	250.4	4.2	30	251.0	4.4	30	249.8	4.9	30	251.0	4.2	30	248.2	4.1	30	250.9	4.6
31	249.6	3.9	31	250.1	4.3	31	249.6	4.1	31	249.8	4.4	31	249.8	4.2	31	250.2	4.2	31	249.3	4.3	31	248.9	4.4
32	249.8	3.8	32	249.7	4.1	32	250.2	4.3	32	250.6	4.5	32	250.1	4.3	32	249.9	4.1	32	250.5	4.4	32	249.9	4.8
33	250.0	4.1	33	249.9	4.1	33	250.4	4.0	33	249.9	4.4	33	250.6	4.3	33	249.9	4.4	33	250.9	4.2	33	250.0	4.7
34	249.8	4.2	34	250.5	4.2	34	251.5	4.0	34	249.9	4.5	34	250.6	4.2	34	249.5	4.0	34	249.6	4.3	34	249.2	4.5
35	249.1	4.0	35	247.7	4.4	35	251.0	4.1	35	251.7	4.5	35	250.7	4.2	35	250.7	4.4	35	250.7	4.4	35	249.4	4.5
36	248.8	3.9	36	249.7	4.0	36	248.6	4.1	36	249.1	4.3	36	250.8	4.5	36	250.4	4.1	36	249.3	4.0	36	250.3	4.7
37	248.5	4.2	37	250.6	4.0	37	249.5	4.0	37	250.0	4.6	37	250.0	4.2	37	251.3	4.3	37	250.4	4.2	37	249.1	4.5
38	249.0	4.1	38	250.8	4.3	38	250.4	3.9	38	250.6	4.3	38	251.3	4.4	38	250.6	4.0	38	252.1	4.2	38	250.4	4.7
39	248.4	4.1	39	250.3	4.3	39	250.4	4.3	39	248.9	4.7	39	250.5	4.6	39	250.0	4.5	39	249.7	4.2	39	249.3	4.8
40	249.8	3.9	40	248.4	4.0	40	250.7	4.5	40	249.8	4.3	40	250.7	4.2	40	249.8	4.1	40	250.5	4.2	40	250.4	4.5
41	249.1	3.7	41	249.4	3.9	41	250.1	3.9	41	249.8	4.0	41	250.5	3.8	41	251.4	3.9	41	250.1	4.0	41	250.1	4.3
42	249.2	3.9	42	250.1	4.0	42	249.7	3.9	42	249.9	4.0	42	249.1	4.0	42	248.8	4.1	42	249.2	4.1	42	250.0	4.6
43	250.5	3.6	43	249.4	3.8	43	248.7	3.7	43	249.1	4.0	43	249.8	4.0	43	250.1	3.8	43	250.1	3.8	43	250.7	4.4
44	249.2	3.7	44	250.1	3.8	44	250.9	3.9	44	249.8	4.2	44	249.7	4.1	44	249.5	4.0	44	250.1	4.0	44	250.1	4.5
45	250.5	3.8	45	250.4	3.8	45	249.9	3.9	45	251.0	3.8	45	250.0	3.8	45	250.7	3.8	45	249.7	4.1	45	249.4	4.4
46	249.9	3.9	46	249.2	3.8	46	250.0	3.9	46	249.8	4.0	46	249.5	3.8	46	249.9	4.3	46	250.1	4.0	46	250.8	4.5
47	250.9	3.8	47	251.4	4.0	47	252.3	3.8	47	250.1	3.7	47	250.8	4.0	47	247.6	4.0	47	249.2	4.1	47	250.8	4.3
48	250.0	3.7	48	248.2	3.9	48	250.9	3.9	48	251.1	4.6	48	250.8	4.0	48	251.4	4.0	48	250.1	4.0	48	249.6	4.5
49	249.0	3.6	49	250.6	3.6	49	250.8	3.8	49	248.1	3.8	49	249.5	4.0	49	249.8	3.7	49	250.1	4.0	49	250.7	4.4
50	249.8	3.9	50	250.6	3.8	50	250.1	4.0	50	249.8	4.1	50	250.0	3.8	50	249.0	3.9	50	249.7	4.1	50	250.7	4.3
51	250.2	3.9	51	249.2	4.0	51	248.9	3.7	51	250.5	4.0	51	250.6	3.9	51	250.9	4.1	51	250.3	4.0	51	248.8	4.6
52	249.5	3.9	52	251.6	4.1	52	249.9	3.8	52	250.2	4.3	52	249.9	3.8	52	251.1	4.1	52	250.7	4.2	52	251.1	4.8
53 f	250.1	1.4	53 f	250.1	1.5	53 f	249.8	1.5	53 f	250.3	1.4	53 f	249.9	1.5	53 f	250.0	1.5	53 f	250.1	1.5	53 f	251.1	1.5
54	249.0	3.9	54	249.2	4.0	54	250.1	3.7	54	248.2	4.0	54	251.5	4.0	54	248.6	3.9	54	250.0	4.2	54	249.9	4.4
55	250.3	3.8	55	250.7	4.1	55	251.1	3.9	55	250.8	4.1	55	250.4	4.1	55	250.7	4.0	55	249.4	4.3	55	251.0	4.6
56	249.1	4.0	56	249.7	3.9	56	250.0	3.8	56	248.8	4.0	56	249.0	4.0	56	250.9	4.0	56	248.3	3.9	56	250.6	4.3
57	249.2	4.4	57	248.6	4.1	57	250.7	3.8	57	250.4	4.1	57	250.0	3.9	57	250.4	4.2	57	250.6	4.2	57	251.2	4.5
58	248.1	3.9	58	249.2	4.0	58	250.8	3.8	58	251.0													