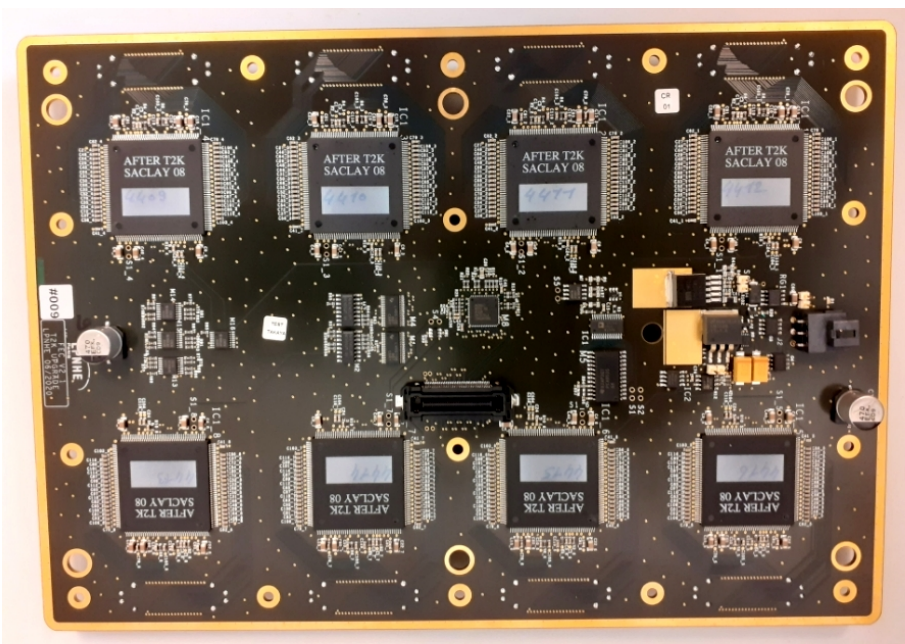
FRONT END CARD - PHASE II

DESIGN



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Thanks to Xavier de la Broïse / CEA-Irfu
for his preliminary work

Specifications.

Functions.

The Front-End Card (FEC) performs three mains functions (see figure 1) : the digital conversion of the 576 analog signals coming from the resistive Micromegas detector, the calibration of this conversion function, and the monitoring of the board.

The monitoring consists in measuring some voltages, the supply current and the temperature of the board, and in reading the board identification serial number.

The calibration of the conversion function consists in generating a voltage step signal through an in series capacitance to simulate an analog input signal. The amplitude of this step is well known and is controllable.

The digital conversion of the 576 analog signals is performed through several stages. As the Phase-II resistive Micromegas detector is self-protected against sparks, there is no need of specific protection on the 576 inputs of the FEC. So the first stages are the shaping, the analogical storage and the multiplexing of the signals (576 → 8). These steps are performed by the "After" ASIC (see document "ASIC After datasheet", P. Baron and E. Delagnes). At last, the analog signals are converted into digital values by the 8 channel ADC and finally sent to the FEM board through 8 LVDS outputs.

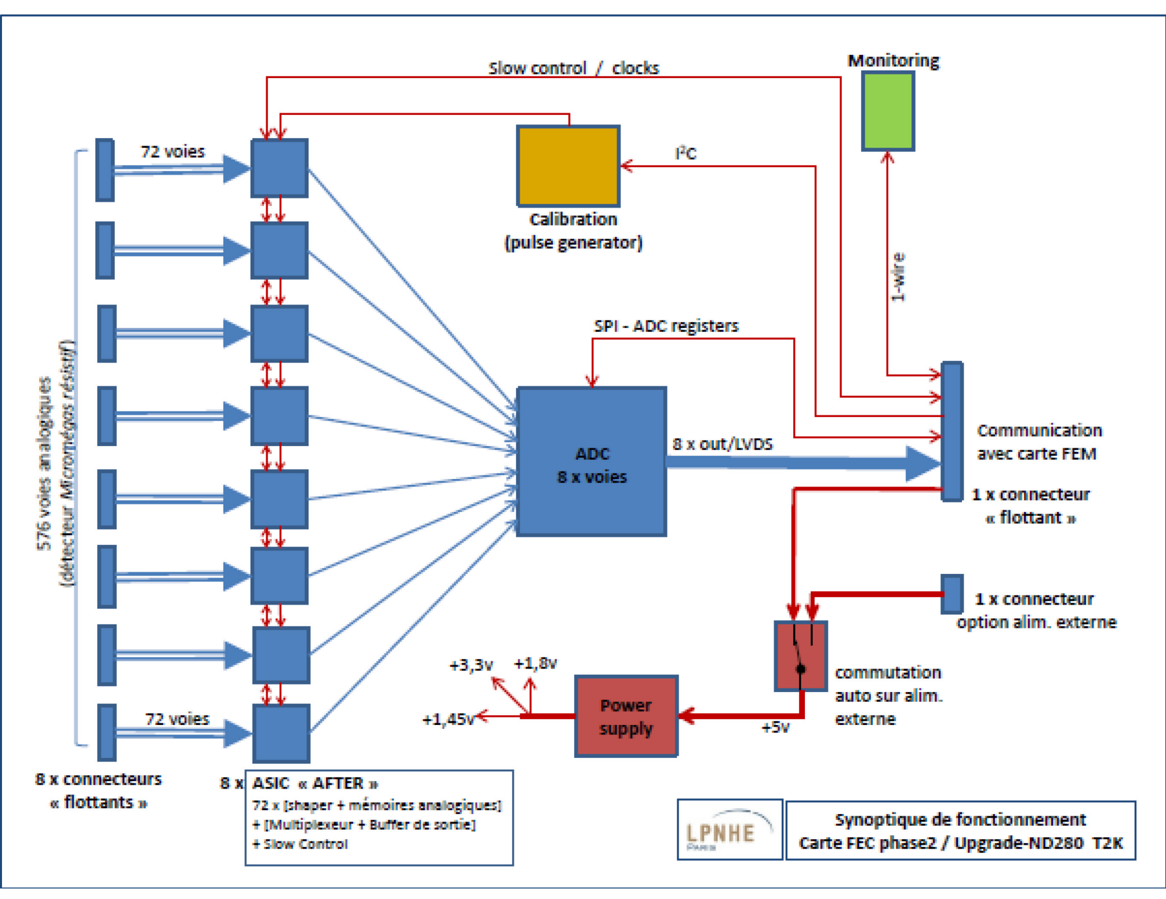


Figure 1: Schematic diagram of the FEC board main functions

Requirements.

The global performances required for the 576 analogic channels are the same as those required for the “After” ASIC. Refer to its documentation ("ASIC After datasheet") for relevant details. The main specifications are remained below.

Parameter	Value
Number of channels	72
Number of Time bins	511
MIP charge	12fC to 60fC
MIP/noise	100
Dynamic range	10 MIPS on 12bits
Dynamic range (output)	2 V
I.N.L	1% range 0-3 MIPS; 5% range 3-10 MIPS
Gain	Adjustable (4 values)
Sampling frequency	1MHz to 50MHz
Shaping Time	100ns to 2µs
Read out frequency	20 to 25MHz
Polarity of detector signal	Negative (anode of Micromegas TPC end-cap) or Positive (Cathode).
Calibration	Selection 1/72
Test	one internal test capacitor per channel

Figure 2 : List of the After chip requirements

However, the FEC board should fulfil in addition specific requirements, listed below.

First requirement concerns the routing of the 576 analog signals from the input connectors : the crosstalk should be of course minimized, as well as the capacitance between the lines and the ground layers in order to minimize the noise added to the input signals, due to the use of a charge amplifier as input stage.

The precision of the calibration signal is also an important requirement. A square signal charging a capacitance is used. Its rising time is not critical, because it has no sensible influence on the charge measurement. It only should be clearly lower than the shaping time of the shaping stage (it to say, at less, 100 ns). At the opposite, the precision of the measurement is directly correlated to the precision of the calibration signal amplitude. This one should be better than ±2 %.

Finally, the last requirement concerns the design of the printed circuit board and the implantation of components. They should avoid noise perturbations between the analog and the digital parts of the board.

Environmental conditions.

The FEC boards will be connected directly on the back of the resistive Micromegas detectors. So they will be located between the TPC itself and the second well, in a stuffy atmosphere (CO_2 in light overpressure) at 22 °C ±5 °C. The boards should not warm up excessively, nor warm their environment or the gas in the TPC chamber (convection moves can be prejudicial). So these boards should be cooled : a chilling system composed of cooling shieldings and liquid circuit should be used for this purpose.

These boards will be located in areas that will be rarely and not easily accessible, so that the maintenance during the whole experience life will be difficult. So the quality of manufacturing of these boards should be strictly controlled.

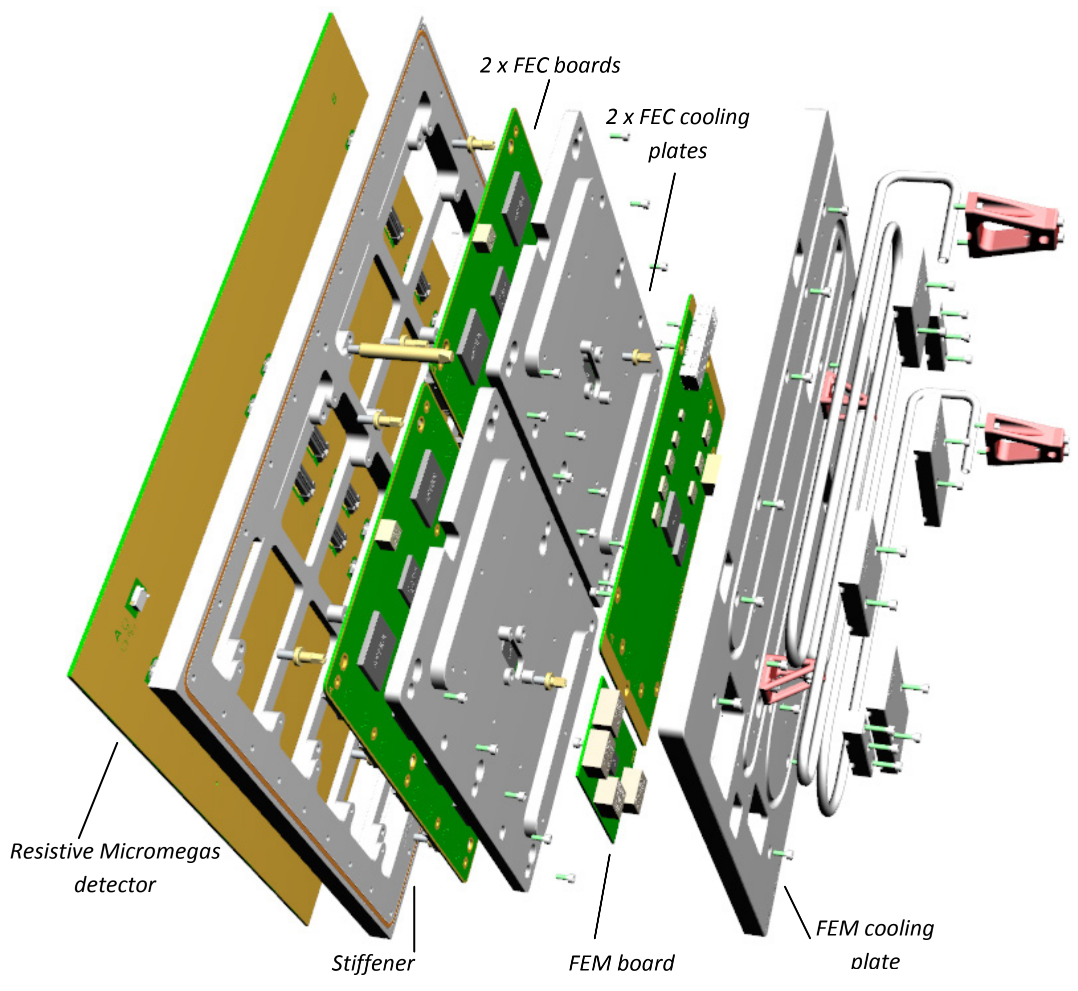


Figure 3 : Preliminary drawing for the assembly of a detection module : 1 resistive Micromegas detector, 1 stiffener, 2 FEC boards, 1 FEM board, their shielding/cooling plates.

Printed circuit board.

All the components of the board are RoHS compliant. So the board can be cabled, and will be cabled, following a RoHS/Lead free process.

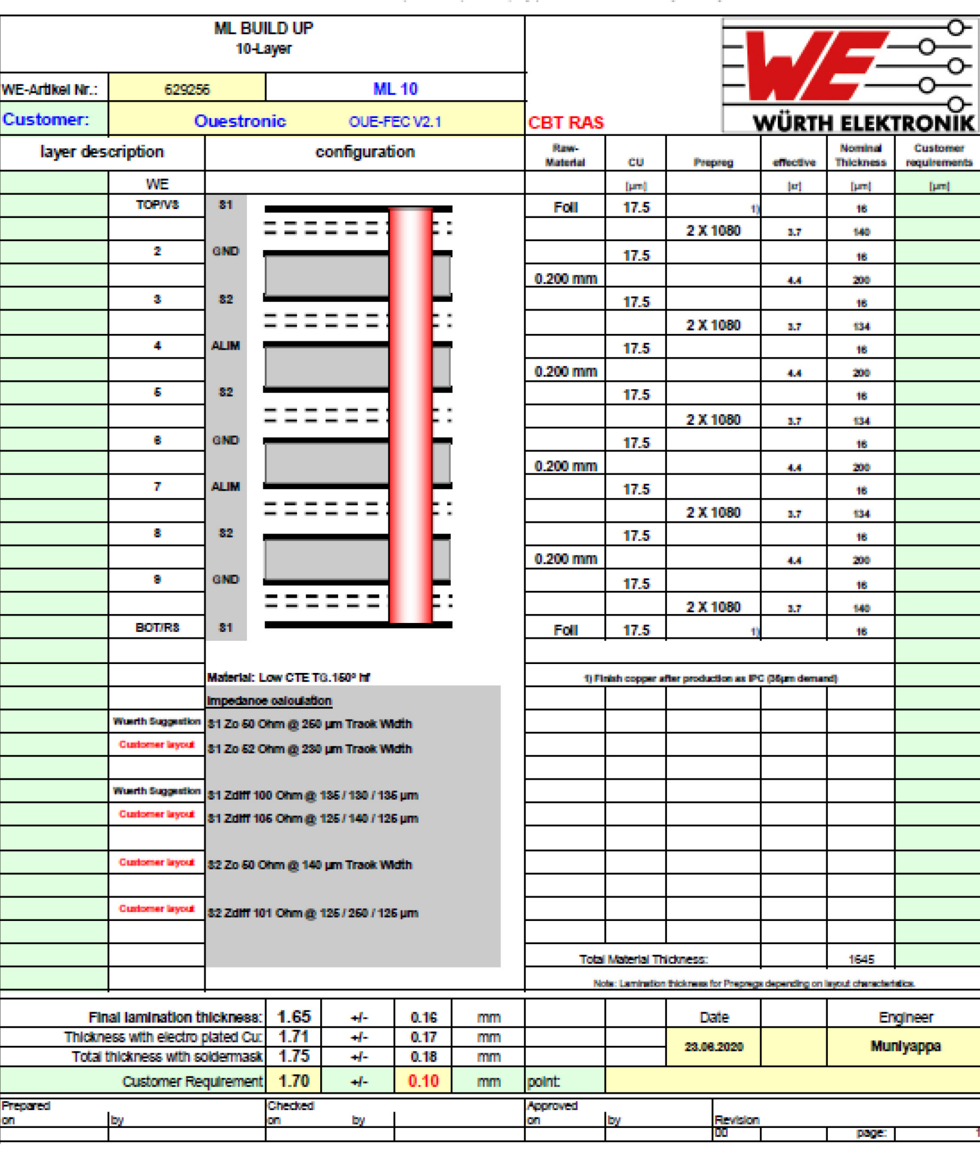
Dimensions.

Dimensions of the board are : 259 mm x 182 mm x 1,7 mm.
Two side by side boards support the surface of one resistive Micromegas detector (see figure 3.).

Lines configuration.

The PCB is planned to be in FR4 HTg-150-HF (HF : halogen free). The routing of the lines needs 10 layers. The package of the integrated circuits and connectors used, the density of the lines, lead to a class 6 printed circuit board.

Stacking up of layers.



ML BUILD UP
10-Layer

WE-Artikel Nr.:	629256	ML 10
Customer:	Ouestronic	OUE-FEC V2.1

CBT RAS

WÜRTH ELEKTRONIK

layer description (WE)	configuration	Raw-Material	CU [µm]	Prepreg	effective [εr]	Nominal Thickness [µm]	Customer requirements [µm]
TOP/V8	S1	Foil	17.5	1)		16	
				2 X 1080	3.7	140	
2	GND		17.5			16	
		0.200 mm			4.4	200	
3	S2		17.5			16	
				2 X 1080	3.7	134	
4	ALIM		17.5			16	
		0.200 mm			4.4	200	
5	S2		17.5			16	
				2 X 1080	3.7	134	
6	GND		17.5			16	
		0.200 mm			4.4	200	
7	ALIM		17.5			16	
				2 X 1080	3.7	134	
8	S2		17.5			16	
		0.200 mm			4.4	200	
9	GND		17.5			16	
				2 X 1080	3.7	140	
BOT/R8	S1	Foil	17.5	1)		16	

Material: Low CTE TG.150° hf

1) Finish copper after production as IPC (35µm demand)

Impedance calculation

Wuerth Suggestion	S1 Zo 50 Ohm @ 250 µm Track Width
Customer layout	S1 Zo 52 Ohm @ 230 µm Track Width
Wuerth Suggestion	S1 Zdiff 100 Ohm @ 135 / 130 / 135 µm
Customer layout	S1 Zdiff 105 Ohm @ 125 / 140 / 125 µm
Customer layout	S2 Zo 50 Ohm @ 140 µm Track Width
Customer layout	S2 Zdiff 101 Ohm @ 125 / 250 / 125 µm

Total Material Thickness: 1645

Note: Lamination thickness for Prepregs depending on layout characteristics.

Final lamination thickness:	1.65	+/-	0.16	mm
Thickness with electro plated Cu:	1.71	+/-	0.17	mm
Total thickness with soldermask	1.75	+/-	0.18	mm
Customer Requirement	1.70	+/-	0.10	mm

point:

Date	Engineer
23.06.2020	Muniyappa

Prepared on	by	Checked on	by	Approved on	by	Revision	page:
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Figure 19 : Layer stacking-up proposed by the PCB manufacturer