| Fec test report: |
|---|
| Date: 2020_10_19-11-58-59 |
| Tester name: |

## Test#1 Monitoring values — Passed

| | | | |
|---|---|---|---|
| 0 | FEC label | cit_micro | OK |
| 1 | FEC DC2438 ID | 3c0000024da1b926 | OK |
| 2 | FEC_T (to 35°C) | 23.281 | OK |
| 3 | FEC_Vdd (3.2V to 3.4V) | 3.270 | OK |
| 4 | FEC_I (1.2A to 1.5A) | 1.426 | OK |
| 5 | FEC_Vad (1.9V to 2.0V) | 1.950 | OK |

## Test#2 Slow control registers: — Passed

## Test#3 Pedestal run: — Passed

| | | | | |
|---|---|---|---|---|
| 0 | After chip #0 | Mean OK | STDDEV OK | OK |
| 1 | After chip #1 | Mean OK | STDDEV OK | OK |
| 2 | After chip #2 | Mean OK | STDDEV OK | OK |
| 3 | After chip #3 | Mean OK | STDDEV OK | OK |
| 4 | After chip #4 | Mean OK | STDDEV OK | OK |
| 5 | After chip #5 | Mean OK | STDDEV OK | OK |
| 6 | After chip #6 | Mean OK | STDDEV OK | OK |
| 7 | After chip #7 | Mean OK | STDDEV OK | OK |

## Test#4 AD9637 test patterns — Passed

| | | | | |
|---|---|---|---|---|
| 0 | ADC channel #0 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 1 | ADC channel #1 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 2 | ADC channel #2 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 3 | ADC channel #3 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |
| 4 | ADC channel #4 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 5 | ADC channel #5 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 6 | ADC channel #6 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 7 | ADC channel #7 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |

## Test#5 Pulser run — Passed

| | | | | |
|---|---|---|---|---|
| 0 | After chip #0 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 3067 | OK |
| 1 | After chip #1 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 3080 | OK |
| 2 | After chip #2 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 3130 | OK |
| 3 | After chip #3 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 3127 | OK |
| 4 | After chip #4 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 3122 | OK |
| 5 | After chip #5 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 2981 | OK |
| 6 | After chip #6 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 3112 | OK |
| 7 | After chip #7 | DAC: 483 G(120) ADC(2850 to 3150) | ADC AMPL: 3066 | OK |

## FEC test final result: — Passed

Monitoring test

| NO | Command | Error | Response |
|---|---|---|---|
| 0 | fe fec_enable 1 | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x40000 |
| 1 | fe 0 moni T 0 | 0 | 0 Tdcm(2) Fem(00) FEC_T: 23.281 degC |
| 2 | fe 0 moni V 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V |
| 3 | fe 0 pulser 0 model T2K2 | 0 | 0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 4 | fe 0 pulser 0 base 0x3FFF | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 5 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 6 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 7 | fe 0 moni I 0 | 0 | 0 Tdcm(2) Fem(00) FEC_I: 1.426 A |
| 8 | fe 0 moni S 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Serial: 3c0000024da1b926 |

Slow control registers test

| NO | Command | Error | Response |
|---|---|---|---|
| 0 | fe 0 mode after | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe fec_enable 1 | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x40000 |
| 2 | fe fec_enable | 0 | 0 Tdcm(2) Fem(00) Reg(1) = 0x2048080 (33849472) FEC_Enable: 1 |
| 3 | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 4 | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 5 | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 6 | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 7 | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 8 | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 9 | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 10 | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 11 | fe 0 after 0 wrchk 3 0x0 0x0101 0x0101 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified) |
| 12 | fe 0 after 1 wrchk 3 0x0 0x0202 0x0202 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified) |
| 13 | fe 0 after 2 wrchk 3 0x0 0x0303 0x0303 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified) |
| 14 | fe 0 after 3 wrchk 3 0x0 0x0404 0x0404 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified) |
| 15 | fe 0 after 4 wrchk 3 0x0 0x0505 0x0505 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified) |
| 16 | fe 0 after 5 wrchk 3 0x0 0x0606 0x0606 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified) |
| 17 | fe 0 after 6 wrchk 3 0x0 0x0707 0x0707 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified) |
| 18 | fe 0 after 7 wrchk 3 0x0 0x0808 0x0808 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified) |
| 19 | fe 0 after 0 read 3 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101 |
| 20 | fe 0 after 1 read 3 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202 |
| 21 | fe 0 after 2 read 3 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303 |
| 22 | fe 0 after 3 read 3 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404 |
| 23 | fe 0 after 4 read 3 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505 |
| 24 | fe 0 after 5 read 3 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606 |
| 25 | fe 0 after 6 read 3 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707 |
| 26 | fe 0 after 7 read 3 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808 |
| 27 | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 28 | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 29 | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 30 | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 31 | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 32 | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 33 | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 34 | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |

ADC pattern test

| NO | Command | Error | Response |
|---|---|---|---|
| 0 | fe 0 mode after | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe 0 test_mode | 0 | 0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0 |
| 2 | be 0 state eb | 0 | 0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current_ |
| 3 | be 0 state tg | 0 | 0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG ) |
| 4 | be 0 state pm | 0 | 0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE ) |
| 5 | fe 0 state | 0 | 0 Tdcm(2) Fem(00) State = 0x3 ( Aligned SCA_Write ) |
| 6 | daq 0xFFFFFF F | 0 | 0 Tdcm(2): daq paused |
| 7 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 8 | fe 0 emit_empty_ch 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 10 | fe 0 keep_rst 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 11 | fe 0 skip_rst 2 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x40000 |
| 12 | fe adc 0 model AD9637 | 0 | 0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637) |
| 13 | fe adc 0 write 0x14 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0) |
| 14 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 15 | fe adc 0 write 0x5 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1) |
| 16 | fe adc 0 write 0xD 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 17 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 18 | fe adc 0 write 0x5 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2) |
| 19 | fe adc 0 write 0xD 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 20 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |

| | | | |
|---|---|---|---|
| 21 | fe adc 0 write 0x5 0x04 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4) |
| 22 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 23 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 24 | fe adc 0 write 0x5 0x08 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8) |
| 25 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 26 | fe adc 0 write 0x4 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1) |
| 27 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 28 | fe adc 0 write 0xD 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 29 | fe adc 0 write 0x4 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2) |
| 30 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 31 | fe adc 0 write 0xD 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 32 | fe adc 0 write 0x4 0x04 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4) |
| 33 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 34 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 35 | fe adc 0 write 0x4 0x08 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8) |
| 36 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 37 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 38 | fe 0 subtract_ped 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 39 | fe 0 zero_suppress 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 40 | fe 0 zs_pre_post 4 8 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0xc4 |
| 41 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdcm(2) Reg(0) <- 0x0 |
| 42 | be 0 eb check_ev_nb 1 | 0 | 0 Tdcm(2) Reg(0) <- 0x800000 |
| 43 | be 0 eb check_ev_ts 1 | 0 | 0 Tdcm(2) Reg(0) <- 0x1000000 |
| 44 | be 0 eb ts_tolerance 0 | 0 | 0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 45 | be 0 event_limit 0x0 | 0 | 0 Tdcm(2) Reg(6) <- 0x0 |
| 46 | be 0 trig_rate 0 50 | 0 | 0 Tdcm(2) Reg(6) <- 0x32 |
| 47 | be 0 restart | 0 | 0 Tdcm(2) Reg(5) <- restart done |
| 48 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 49 | be 0 trig_ena 1 | 0 | 0 Tdcm(2) Reg(6) <- 0x1000 |
| 50 | be 0 trig_ena 0 | 0 | 0 Tdcm(2) Reg(6) <- 0x0 |
| 51 | be 0 state eb | 0 | 0 Tdcm(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Curren |
| 52 | be 0 state tg | 0 | 0 Tdcm(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS ) |
| 53 | be 0 state pm | 0 | 0 Tdcm(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE ) |
| 54 | fe 0 state | 0 | 0 Tdcm(2) Fem(00) State = 0x11 ( Aligned Dev_Ready ) |
| 55 | fe adc 0 write 0x4 0x0F | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15) |
| 56 | fe adc 0 write 0x5 0x0F | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15) |
| 57 | fe adc 0 write 0xD 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0) |

| Pulser test | | | |
|---|---|---|---|
| NO | Command | Error | Response |
| 0 | daq 0xFFFFFF F | 0 | 0 Tdcm(2): daq paused |
| 1 | fe 0 after 0:7 wrchk 3  0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 2 | fe 0 after 0:7 wrchk 4  0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 3 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 4 | fe 0 emit_empty_ch 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 5 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 6 | fe 0 keep_rst 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 7 | fe 0 skip_rst 2 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x40000 |
| 8 | fe 0 test_enable 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 test_mode 1 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x400 |
| 10 | fe 0 tdata A 0x1FF | 0 | 0 Tdcm(2) Fem(00) TestData: linear ramp from 0 to 510 |
| 11 | fe 0 test_zbt 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 12 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 13 | fe 0 asic_mask | 0 | 0 Tdcm(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0 |
| 14 | fe 0 pulser 0 enable 0 | 0 | 0 Tdcm(2) Fem(00) Reg(3) <- 0x0 |
| 15 | fe 0 pulser 0 ft_enable 0 | 0 | 0 Tdcm(2) Fem(00) Reg(3) <- 0x0 |
| 16 | fe 0 pulser 0 model T2K2 | 0 | 0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 17 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 18 | fe 0 pulser 0 ampl 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3fff |
| 19 | fe 0 pulser 0 delay 3000 | 0 | 0 Tdcm(2) Fem(00) Reg(3) <- 0xbb8 |
| 20 | fe pulser load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 21 | fe 0 pulser 0 enable 1 | 0 | 0 Tdcm(2) Fem(00) Reg(3) <- 0x10000 |
| 22 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdcm(2) Reg(0) <- 0x0 |
| 23 | be 0 eb check_ev_nb 1 | 0 | 0 Tdcm(2) Reg(0) <- 0x800000 |
| 24 | be 0 eb check_ev_ts 1 | 0 | 0 Tdcm(2) Reg(0) <- 0x1000000 |
| 25 | be 0 eb ts_tolerance 0 | 0 | 0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 26 | be 0 event_limit 0x0 | 0 | 0 Tdcm(2) Reg(6) <- 0x0 |
| 27 | be 0 trig_rate 0 50 | 0 | 0 Tdcm(2) Reg(6) <- 0x32 |
| 28 | be 0 trig_delay 0 0 | 0 | 0 Tdcm(2) Reg(8) <- 0x0 |
| 29 | be 0 trig_delay 1 0 | 0 | 0 Tdcm(2) Reg(8) <- 0x0 |
| 30 | be 0 trig_delay 2 0 | 0 | 0 Tdcm(2) Reg(9) <- 0x0 |
| 31 | be 0 trig_delay 3 0 | 0 | 0 Tdcm(2) Reg(9) <- 0x0 |
| 32 | be 0 ss_trig_delay 0x4 | 0 | 0 Tdcm(2) Reg(14) <- 0x4 |
| 33 | be 0 ss_trig_ena 1 | 0 | 0 Tdcm(2) Reg(6) <- 0x10000 |
| 34 | be 0 restart | 0 | 0 Tdcm(2) Reg(5) <- restart done |
| 35 | be 0 restart | 0 | 0 Tdcm(2) Reg(5) <- restart done |
| 36 | be 0 isobus 0x0C | 0 | 0 Tdcm(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP  auto-clear) |

| | | | |
|---|---|---|---|
| 37 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 38 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 39 | fe 0 asic_mask 0xfffe | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000 |
| 40 | fe 0 after 0 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration |
| 41 | fe 0 after 0 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 42 | fe 0 after 0 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 43 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 44 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 45 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 46 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 47 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 48 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 49 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 50 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 51 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 52 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 53 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 54 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 55 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 56 | fe 0 asic_mask 0xfffd | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000 |
| 57 | fe 0 after 1 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration |
| 58 | fe 0 after 1 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 59 | fe 0 after 1 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 60 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 61 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 62 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 63 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 64 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 65 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 66 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 67 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 68 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 69 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 70 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 71 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 72 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 73 | fe 0 asic_mask 0xfffb | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000 |
| 74 | fe 0 after 2 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration |
| 75 | fe 0 after 2 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 76 | fe 0 after 2 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 77 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 78 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 79 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 80 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 81 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 82 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 83 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 84 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 85 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 86 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 87 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 88 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 89 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 90 | fe 0 asic_mask 0xfff7 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xfff70000 |
| 91 | fe 0 after 3 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration |
| 92 | fe 0 after 3 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 93 | fe 0 after 3 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 94 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 95 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 96 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 97 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 98 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 99 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 100 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 101 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 102 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 103 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 104 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 105 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 106 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 107 | fe 0 asic_mask 0xffef | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000 |
| 108 | fe 0 after 4 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration |
| 109 | fe 0 after 4 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 110 | fe 0 after 4 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 111 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 112 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 113 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 114 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |

| | | | |
|---|---|---|---|
| 115 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 116 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 117 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 118 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 119 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 120 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 121 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 122 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 123 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 124 | fe 0 asic_mask 0xffdf | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xffdf0000 |
| 125 | fe 0 after 5 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration |
| 126 | fe 0 after 5 wrchk 3  0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 127 | fe 0 after 5 wrchk 4  0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 128 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 129 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 130 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 131 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 132 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 133 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 134 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 135 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 136 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 137 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 138 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 139 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 140 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 141 | fe 0 asic_mask 0xffbf | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xffbf0000 |
| 142 | fe 0 after 6 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration |
| 143 | fe 0 after 6 wrchk 3  0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 144 | fe 0 after 6 wrchk 4  0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 145 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 146 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 147 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 148 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 149 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 150 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 151 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 152 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V |
| 153 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 154 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 155 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 156 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 157 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 158 | fe 0 asic_mask 0xff7f | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xff7f0000 |
| 159 | fe 0 after 7 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration |
| 160 | fe 0 after 7 wrchk 3  0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 161 | fe 0 after 7 wrchk 4  0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 162 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 163 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 164 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 165 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 166 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 167 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 168 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 169 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 170 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 171 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START  auto-clear) |
| 172 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 173 | be 0 trig_ena 0 | 0 | 0 Tdcm(2) Reg(6) <- 0x0 |

# Pedestal data before centermean

| CHIP 0 | | | CHIP 1 | | | CHIP 2 | | | CHIP 3 | | | CHIP 4 | | | CHIP 5 | | | CHIP 6 | | | CHIP 7 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD |
| 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 |
| 1 r | 469.2 | 10.8 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 499.1 | 7.5 | 1 r | 511.0 | 0.0 | 1 r | 510.9 | 0.3 | 1 r | 395.2 | 12.1 | 1 r | 511.0 | 0.0 |
| 2 r | 267.5 | 0.7 | 2 r | 314.9 | 0.7 | 2 r | 326.1 | 0.6 | 2 r | 305.9 | 0.7 | 2 r | 331.3 | 0.7 | 2 r | 354.4 | 0.7 | 2 r | 283.1 | 0.7 | 2 r | 298.1 | 0.7 |
| 3 | 185.5 | 4.6 | 3 | 299.6 | 4.3 | 3 | 302.3 | 4.3 | 3 | 162.0 | 4.4 | 3 | 261.6 | 4.6 | 3 | 315.5 | 4.5 | 3 | 185.6 | 4.1 | 3 | 386.5 | 4.4 |
| 4 | 217.3 | 4.4 | 4 | 243.2 | 4.3 | 4 | 261.3 | 4.2 | 4 | 162.9 | 4.5 | 4 | 258.6 | 4.7 | 4 | 334.9 | 4.0 | 4 | 246.0 | 4.3 | 4 | 244.4 | 4.4 |
| 5 | 221.5 | 4.2 | 5 | 247.2 | 4.2 | 5 | 254.9 | 4.3 | 5 | 127.3 | 4.4 | 5 | 229.5 | 4.3 | 5 | 338.3 | 4.5 | 5 | 200.8 | 4.3 | 5 | 319.8 | 4.3 |
| 6 | 228.7 | 4.1 | 6 | 279.9 | 4.1 | 6 | 248.6 | 4.3 | 6 | 200.2 | 4.4 | 6 | 211.7 | 4.3 | 6 | 375.2 | 4.3 | 6 | 185.0 | 4.2 | 6 | 310.8 | 4.5 |
| 7 | 304.5 | 4.2 | 7 | 313.2 | 4.0 | 7 | 187.9 | 4.3 | 7 | 286.6 | 4.4 | 7 | 240.5 | 4.2 | 7 | 266.8 | 4.2 | 7 | 164.5 | 4.4 | 7 | 321.4 | 4.2 |
| 8 | 293.4 | 4.3 | 8 | 215.7 | 4.1 | 8 | 150.7 | 4.2 | 8 | 229.4 | 4.2 | 8 | 271.1 | 4.2 | 8 | 266.9 | 4.3 | 8 | 250.3 | 4.4 | 8 | 230.8 | 4.3 |
| 9 | 289.1 | 4.2 | 9 | 261.8 | 4.4 | 9 | 201.8 | 4.0 | 9 | 217.9 | 4.2 | 9 | 266.4 | 4.3 | 9 | 313.6 | 4.2 | 9 | 208.1 | 4.2 | 9 | 296.3 | 4.1 |
| 10 | 216.0 | 4.2 | 10 | 255.4 | 4.4 | 10 | 163.9 | 4.1 | 10 | 114.6 | 4.2 | 10 | 267.1 | 4.3 | 10 | 359.9 | 4.1 | 10 | 217.8 | 4.4 | 10 | 241.1 | 4.5 |
| 11 | 194.4 | 4.5 | 11 | 246.8 | 3.8 | 11 | 188.8 | 4.3 | 11 | 192.8 | 4.3 | 11 | 168.2 | 4.1 | 11 | 294.8 | 4.2 | 11 | 268.5 | 4.3 | 11 | 338.3 | 4.0 |
| 12 | 157.2 | 4.2 | 12 | 239.6 | 4.0 | 12 | 254.3 | 4.2 | 12 | 234.0 | 4.3 | 12 | 268.2 | 4.4 | 12 | 312.6 | 4.5 | 12 | 245.7 | 4.1 | 12 | 280.1 | 4.5 |
| 13 | 243.5 | 4.4 | 13 | 213.0 | 4.2 | 13 | 196.2 | 4.3 | 13 | 278.8 | 4.6 | 13 | 303.5 | 4.2 | 13 | 288.1 | 4.1 | 13 | 127.2 | 4.5 | 13 | 170.0 | 4.0 |
| 14 | 258.7 | 4.2 | 14 | 253.6 | 4.3 | 14 | 249.3 | 4.2 | 14 | 218.8 | 4.2 | 14 | 364.0 | 4.2 | 14 | 336.8 | 4.0 | 14 | 161.7 | 4.2 | 14 | 257.1 | 4.4 |
| 15 f | 218.4 | 1.6 | 15 f | 258.6 | 1.6 | 15 f | 260.2 | 1.7 | 15 f | 167.0 | 1.8 | 15 f | 252.9 | 1.5 | 15 f | 247.7 | 1.8 | 15 f | 133.9 | 1.8 | 15 f | 309.3 | 1.6 |
| 16 | 251.6 | 4.3 | 16 | 229.4 | 4.0 | 16 | 231.0 | 4.0 | 16 | 163.5 | 4.1 | 16 | 267.3 | 4.1 | 16 | 293.7 | 4.1 | 16 | 186.8 | 4.3 | 16 | 334.0 | 4.2 |
| 17 | 191.3 | 4.1 | 17 | 271.4 | 4.3 | 17 | 228.9 | 4.2 | 17 | 268.1 | 4.0 | 17 | 266.5 | 4.4 | 17 | 270.1 | 4.1 | 17 | 131.7 | 4.2 | 17 | 219.9 | 4.3 |
| 18 | 286.8 | 4.3 | 18 | 276.5 | 4.3 | 18 | 284.2 | 3.9 | 18 | 181.4 | 4.1 | 18 | 235.9 | 4.2 | 18 | 319.5 | 4.0 | 18 | 232.1 | 4.4 | 18 | 306.8 | 4.3 |
| 19 | 221.0 | 4.1 | 19 | 213.2 | 4.1 | 19 | 231.3 | 4.0 | 19 | 229.1 | 4.3 | 19 | 294.6 | 4.3 | 19 | 352.1 | 4.0 | 19 | 187.7 | 4.3 | 19 | 211.1 | 4.3 |
| 20 | 184.6 | 4.4 | 20 | 217.1 | 4.0 | 20 | 199.8 | 4.3 | 20 | 211.0 | 4.4 | 20 | 306.2 | 4.1 | 20 | 316.8 | 4.3 | 20 | 169.0 | 4.3 | 20 | 298.0 | 4.1 |
| 21 | 202.3 | 4.4 | 21 | 238.0 | 3.9 | 21 | 163.9 | 4.2 | 21 | 266.8 | 4.3 | 21 | 256.0 | 4.1 | 21 | 317.6 | 3.9 | 21 | 141.9 | 4.3 | 21 | 305.0 | 4.4 |
| 22 | 211.3 | 4.2 | 22 | 247.2 | 4.0 | 22 | 255.8 | 3.9 | 22 | 236.2 | 4.2 | 22 | 252.3 | 3.9 | 22 | 294.3 | 4.2 | 22 | 186.6 | 4.2 | 22 | 283.2 | 4.2 |
| 23 | 261.7 | 4.2 | 23 | 247.1 | 4.1 | 23 | 326.6 | 4.1 | 23 | 132.5 | 4.0 | 23 | 198.1 | 4.2 | 23 | 281.2 | 4.1 | 23 | 223.4 | 4.5 | 23 | 229.8 | 4.2 |
| 24 | 202.3 | 4.3 | 24 | 296.8 | 4.0 | 24 | 222.6 | 4.1 | 24 | 198.8 | 4.0 | 24 | 310.8 | 4.0 | 24 | 298.0 | 4.1 | 24 | 192.9 | 4.0 | 24 | 226.9 | 4.3 |
| 25 | 167.3 | 4.2 | 25 | 270.3 | 4.3 | 25 | 170.4 | 4.1 | 25 | 244.5 | 4.1 | 25 | 317.9 | 4.3 | 25 | 253.9 | 4.3 | 25 | 152.0 | 4.4 | 25 | 287.0 | 4.1 |
| 26 | 195.7 | 4.1 | 26 | 222.8 | 4.2 | 26 | 242.4 | 4.2 | 26 | 211.1 | 4.0 | 26 | 283.6 | 4.2 | 26 | 377.3 | 4.1 | 26 | 268.7 | 4.2 | 26 | 313.9 | 4.3 |
| 27 | 234.0 | 4.2 | 27 | 270.2 | 4.0 | 27 | 274.1 | 4.0 | 27 | 256.1 | 4.1 | 27 | 360.3 | 4.4 | 27 | 244.6 | 4.2 | 27 | 212.1 | 4.2 | 27 | 283.4 | 4.4 |
| 28 f | 197.5 | 1.6 | 28 f | 251.7 | 1.6 | 28 f | 239.2 | 1.7 | 28 f | 217.3 | 1.9 | 28 f | 243.0 | 1.6 | 28 f | 250.6 | 1.9 | 28 f | 135.4 | 1.8 | 28 f | 277.6 | 1.7 |
| 29 | 212.8 | 4.2 | 29 | 249.2 | 4.2 | 29 | 281.1 | 4.0 | 29 | 267.6 | 4.0 | 29 | 263.5 | 4.2 | 29 | 248.9 | 4.4 | 29 | 217.4 | 4.2 | 29 | 268.0 | 4.2 |
| 30 | 255.2 | 4.1 | 30 | 279.1 | 4.1 | 30 | 273.5 | 3.9 | 30 | 195.5 | 4.0 | 30 | 288.1 | 4.6 | 30 | 282.9 | 4.2 | 30 | 257.2 | 4.2 | 30 | 326.0 | 4.1 |
| 31 | 122.1 | 4.2 | 31 | 299.1 | 4.3 | 31 | 306.7 | 4.1 | 31 | 289.3 | 4.0 | 31 | 241.3 | 4.1 | 31 | 291.2 | 4.1 | 31 | 190.7 | 4.3 | 31 | 323.6 | 4.2 |
| 32 | 274.1 | 4.4 | 32 | 225.8 | 4.1 | 32 | 247.9 | 4.0 | 32 | 213.5 | 4.5 | 32 | 305.9 | 4.1 | 32 | 322.9 | 4.3 | 32 | 191.3 | 4.3 | 32 | 291.4 | 4.2 |
| 33 | 144.3 | 4.0 | 33 | 297.2 | 4.2 | 33 | 269.3 | 4.0 | 33 | 190.0 | 4.1 | 33 | 257.7 | 4.1 | 33 | 298.0 | 4.3 | 33 | 175.4 | 4.2 | 33 | 247.6 | 4.2 |
| 34 | 236.9 | 4.0 | 34 | 274.6 | 4.0 | 34 | 337.9 | 4.0 | 34 | 259.8 | 4.1 | 34 | 288.4 | 4.4 | 34 | 285.8 | 4.1 | 34 | 159.6 | 4.4 | 34 | 256.1 | 4.3 |
| 35 | 209.5 | 4.1 | 35 | 241.8 | 4.0 | 35 | 174.3 | 4.2 | 35 | 260.1 | 4.3 | 35 | 198.4 | 4.2 | 35 | 289.5 | 4.3 | 35 | 280.3 | 4.1 | 35 | 309.3 | 4.5 |
| 36 | 308.7 | 4.1 | 36 | 228.6 | 4.1 | 36 | 194.2 | 4.0 | 36 | 286.5 | 4.1 | 36 | 290.1 | 4.6 | 36 | 305.1 | 4.1 | 36 | 315.9 | 4.2 | 36 | 268.6 | 4.1 |
| 37 | 241.9 | 4.2 | 37 | 222.3 | 4.3 | 37 | 254.3 | 4.1 | 37 | 158.8 | 4.2 | 37 | 303.1 | 4.3 | 37 | 315.5 | 3.9 | 37 | 225.9 | 4.3 | 37 | 295.1 | 4.1 |
| 38 | 185.2 | 4.1 | 38 | 300.4 | 4.1 | 38 | 230.1 | 3.9 | 38 | 163.7 | 4.1 | 38 | 243.7 | 4.4 | 38 | 238.3 | 4.1 | 38 | 261.0 | 4.3 | 38 | 299.3 | 4.3 |
| 39 | 260.9 | 4.1 | 39 | 265.9 | 4.3 | 39 | 251.1 | 4.3 | 39 | 204.6 | 4.3 | 39 | 255.9 | 4.6 | 39 | 352.7 | 4.3 | 39 | 235.4 | 4.4 | 39 | 348.5 | 4.3 |
| 40 | 241.3 | 4.2 | 40 | 252.4 | 4.0 | 40 | 234.4 | 4.0 | 40 | 173.5 | 4.1 | 40 | 269.4 | 4.3 | 40 | 293.6 | 4.3 | 40 | 195.2 | 4.2 | 40 | 287.3 | 4.3 |
| 41 | 190.7 | 3.9 | 41 | 323.0 | 3.9 | 41 | 237.2 | 4.0 | 41 | 252.2 | 3.9 | 41 | 256.7 | 3.9 | 41 | 259.0 | 3.9 | 41 | 201.3 | 4.0 | 41 | 343.4 | 4.1 |
| 42 | 165.6 | 4.0 | 42 | 218.2 | 3.8 | 42 | 189.8 | 4.0 | 42 | 240.4 | 4.0 | 42 | 315.3 | 4.2 | 42 | 317.0 | 3.9 | 42 | 150.2 | 3.9 | 42 | 244.5 | 4.1 |
| 43 | 215.3 | 4.1 | 43 | 220.6 | 3.9 | 43 | 259.2 | 3.9 | 43 | 206.4 | 3.7 | 43 | 292.6 | 4.5 | 43 | 359.4 | 3.8 | 43 | 209.2 | 4.2 | 43 | 276.4 | 4.1 |
| 44 | 276.5 | 4.0 | 44 | 278.4 | 3.9 | 44 | 222.9 | 4.1 | 44 | 299.6 | 3.9 | 44 | 265.9 | 4.2 | 44 | 195.6 | 3.8 | 44 | 233.1 | 3.9 | 44 | 255.6 | 4.1 |
| 45 | 182.0 | 4.1 | 45 | 238.8 | 3.7 | 45 | 231.6 | 3.9 | 45 | 289.9 | 3.8 | 45 | 220.9 | 3.8 | 45 | 281.2 | 3.9 | 45 | 261.4 | 4.0 | 45 | 278.7 | 4.1 |
| 46 | 158.8 | 3.9 | 46 | 263.5 | 3.9 | 46 | 246.4 | 3.7 | 46 | 253.8 | 3.9 | 46 | 263.7 | 4.0 | 46 | 298.8 | 3.9 | 46 | 207.2 | 3.9 | 46 | 306.4 | 4.2 |
| 47 | 336.8 | 4.0 | 47 | 207.3 | 4.0 | 47 | 240.9 | 4.0 | 47 | 286.3 | 3.8 | 47 | 274.1 | 4.0 | 47 | 310.2 | 4.0 | 47 | 240.5 | 3.8 | 47 | 273.8 | 4.1 |
| 48 | 208.3 | 3.9 | 48 | 236.7 | 3.8 | 48 | 246.7 | 3.9 | 48 | 254.8 | 3.8 | 48 | 262.3 | 4.2 | 48 | 308.0 | 4.0 | 48 | 203.6 | 4.2 | 48 | 317.8 | 4.1 |
| 49 | 309.0 | 4.0 | 49 | 246.7 | 4.0 | 49 | 267.8 | 3.8 | 49 | 153.7 | 3.8 | 49 | 243.2 | 4.3 | 49 | 233.4 | 4.0 | 49 | 248.1 | 4.1 | 49 | 323.0 | 4.1 |
| 50 | 246.3 | 4.0 | 50 | 249.9 | 4.0 | 50 | 180.6 | 3.9 | 50 | 184.3 | 3.9 | 50 | 208.1 | 3.9 | 50 | 406.6 | 4.2 | 50 | 219.1 | 4.2 | 50 | 330.0 | 4.0 |
| 51 | 243.5 | 4.1 | 51 | 242.7 | 3.8 | 51 | 256.6 | 4.1 | 51 | 195.7 | 4.0 | 51 | 282.5 | 4.0 | 51 | 288.8 | 3.9 | 51 | 253.9 | 4.3 | 51 | 372.8 | 4.0 |
| 52 | 202.1 | 4.1 | 52 | 226.2 | 3.8 | 52 | 175.8 | 4.0 | 52 | 160.4 | 3.9 | 52 | 238.3 | 3.9 | 52 | 344.3 | 4.2 | 52 | 224.2 | 4.0 | 52 | 363.5 | 4.2 |
| 53 f | 233.4 | 1.9 | 53 f | 230.3 | 1.7 | 53 f | 204.9 | 1.6 | 53 f | 191.4 | 1.5 | 53 f | 184.1 | 1.6 | 53 f | 367.6 | 1.6 | 53 f | 269.4 | 1.6 | 53 f | 354.5 | 1.7 |
| 54 | 180.5 | 4.0 | 54 | 236.2 | 3.9 | 54 | 216.6 | 3.8 | 54 | 201.8 | 3.9 | 54 | 272.5 | 4.1 | 54 | 284.7 | 3.9 | 54 | 197.9 | 4.0 | 54 | 228.2 | 4.1 |
| 55 | 198.4 | 4.0 | 55 | 260.1 | 3.8 | 55 | 253.9 | 3.9 | 55 | 245.8 | 3.9 | 55 | 228.2 | 4.2 | 55 | 320.4 | 4.1 | 55 | 234.0 | 4.5 | 55 | 251.6 | 4.0 |
| 56 | 238.1 | 3.9 | 56 | 254.9 | 4.0 | 56 | 257.4 | 4.0 | 56 | 193.6 | 3.7 | 56 | 247.5 | 3.9 | 56 | 289.8 | 3.9 | 56 | 187.7 | 4.0 | 56 | 298.9 | 4.1 |
| 57 | 195.0 | 4.1 | 57 | 262.8 | 4.2 | 57 | 322.4 | 4.0 | 57 | 274.1 | 3.9 | 57 | 265.1 | 4.1 | 57 | 315.6 | 3.9 | 57 | 239.0 | 4.1 | 57 | 318.1 | 4.2 |
| 58 | 263.6 | 4.1 | 58 | 215.5 | 3.9 | 58 | 219.1 | 4.2 | 58 | 190.7 | 4.0 | 58 | 211.3 | 4.2 | 58 | 381.8 | 3.9 | 58 | 232.7 | 4.0 | 58 | 298.8 | 4.0 |
| 59 | 225.1 | 4.1 | 59 | 229.8 | 4.1 | 59 | 250.8 | 3.9 | 59 | 172.2 | 3.8 | 59 | 218.7 | 4.0 | 59 | 257.4 | 3.8 | 59 | 205.4 | 4.2 | 59 | 282.1 | 4.1 |
| 60 | 217.8 | 4.0 | 60 | 263.3 | 3.8 | 60 | 199.9 | 3.8 | 60 | 183.5 | 4.2 | 60 | 281.9 | 3.8 | 60 | 348.3 | 3.9 | 60 | 199.4 | 4.1 | 60 | 311.3 | 4.0 |
| 61 | 218.2 | 4.1 | 61 | 302.1 | 4.0 | 61 | 197.9 | 4.1 | 61 | 247.9 | 4.0 | 61 | 286.1 | 4.0 | 61 | 307.9 | 3.7 | 61 | 123.5 | 4.0 | 61 | 322.0 | 4.2 |
| 62 | 269.5 | 4.3 | 62 | 317.4 | 4.0 | 62 | 257.3 | 4.0 | 62 | 210.5 | 3.7 | 62 | 324.9 | 4.2 | 62 | 266.9 | 3.8 | 62 | 141.5 | 4.0 | 62 | 239.4 | 4.2 |
| 63 | 193.7 | 4.0 | 63 | 162.1 | 3.9 | 63 | 237.8 | 3.9 | 63 | 213.7 | 4.2 | 63 | 224.1 | 4.1 | 63 | 290.1 | 3.7 | 63 | 151.9 | 4.1 | 63 | 345.7 | 4.1 |
| 64 | 185.7 | 4.1 | 64 | 251.5 | 3.8 | 64 | 182.4 | 4.0 | 64 | 175.8 | 4.0 | 64 | 245.3 | 4.0 | 64 | 348.0 | 3.9 | 64 | 293.1 | 4.2 | 64 | 382.9 | 4.4 |
| 65 | 175.7 | 4.2 | 65 | 378.6 | 3.8 | 65 | 224.7 | 3.8 | 65 | 153.2 | 3.9 | 65 | 219.0 | 4.0 | 65 | 266.6 | 4.0 | 65 | 136.6 | 4.2 | 65 | 284.1 | 4.0 |
| 66 f | 286.5 | 1.7 | 66 f | 311.2 | 1.6 | 66 f | 206.5 | 1.6 | 66 f | 215.9 | 1.6 | 66 f | 197.2 | 1.6 | 66 f | 343.9 | 1.6 | 66 f | 256.9 | 1.6 | 66 f | 258.4 | 1.6 |
| 67 | 188.4 | 4.0 | 67 | 251.2 | 4.0 | 67 | 133.0 | 4.0 | 67 | 221.7 | 4.0 | 67 | 341.0 | 3.9 | 67 | 260.0 | 3.8 | 67 | 212.4 | 4.1 | 67 | 335.5 | 4.7 |
| 68 | 257.7 | 4.2 | 68 | 219.3 | 4.1 | 68 | 227.7 | 3.8 | 68 | 180.4 | 3.9 | 68 | 264.1 | 4.1 | 68 | 297.8 | 3.9 | 68 | 169.7 | 4.0 | 68 | 333.7 | 4.0 |
| 69 | 280.0 | 4.2 | 69 | 297.4 | 4.1 | 69 | 158.8 | 3.8 | 69 | 148.6 | 4.0 | 69 | 227.1 | 3.9 | 69 | 367.5 | 4.2 | 69 | 154.9 | 4.0 | 69 | 276.6 | 4.1 |
| 70 | 181.7 | 4.1 | 70 | 238.8 | 4.0 | 70 | 276.5 | 3.9 | 70 | 325.3 | 4.0 | 70 | 313.0 | 4.0 | 70 | 273.6 | 3.8 | 70 | 167.8 | 4.1 | 70 | 212.7 | 4.4 |
| 71 | 248.5 | 4.1 | 71 | 237.3 | 4.0 | 71 | 259.7 | 3.8 | 71 | 190.1 | 4.0 | 71 | 266.7 | 4.2 | 71 | 348.5 | 4.1 | 71 | 122.9 | 4.2 | 71 | 280.0 | 4.1 |
| 72 | 238.4 | 4.3 | 72 | 354.1 | 4.2 | 72 | 227.7 | 3.9 | 72 | 283.5 | 3.9 | 72 | 289.8 | 4.2 | 72 | 299.6 | 4.0 | 72 | 207.1 | 4.5 | 72 | 288.6 | 4.0 |
| 73 | 265.9 | 4.2 | 73 | 236.5 | 4.2 | 73 | 187.9 | 3.9 | 73 | 277.2 | 3.9 | 73 | 265.9 | 4.2 | 73 | 330.6 | 3.9 | 73 | 286.8 | 3.9 | 73 | 325.4 | 4.2 |
| 74 | 168.1 | 4.2 | 74 | 252.3 | 4.0 | 74 | 167.4 | 3.9 | 74 | 190.1 | 3.9 | 74 | 295.8 | 3.9 | 74 | 307.3 | 3.8 | 74 | 142.4 | 4.1 | 74 | 267.5 | 4.0 |
| 75 | 155.5 | 4.3 | 75 | 271.2 | 4.1 | 75 | 254.2 | 4.0 | 75 | 221.0 | 4.0 | 75 | 227.9 | 4.1 | 75 | 331.9 | 4.0 | 75 | 194.9 | 4.0 | 75 | 273.6 | 4.2 |
| 76 | 278.3 | 4.2 | 76 | 270.4 | 4.0 | 76 | 188.8 | 4.1 | 76 | 228.3 | 3.9 | 76 | 265.7 | 4.1 | 76 | 294.3 | 3.9 | 76 | 220.9 | 4.1 | 76 | 239.3 | 4.1 |
| 77 | 285.8 | 3.9 | 77 | 213.3 | 4.2 | 77 | 286.0 | 4.0 | 77 | 194.9 | 4.1 | 77 | 251.6 | 4.0 | 77 | 250.9 | 4.3 | 77 | 167.3 | 3.9 | 77 | 269.4 | 4.0 |
| 78 | 273.6 | 4.2 | 78 | 237.8 | 3.9 | 78 | 230.7 | 4.2 | 78 | 188.8 | 3.9 | 78 | 278.3 | 4.0 | 78 | 292.2 | 4.0 | 78 | 171.9 | 4.2 | 78 | 254.3 | 4.1 |

Pedestal after centermean.

| CHIP 0 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 251.5 | 10.7 |
| 2 r | 250.8 | 0.7 |
| 3 | 251.8 | 4.2 |
| 4 | 250.3 | 4.3 |
| 5 | 250.4 | 4.2 |
| 6 | 250.6 | 4.3 |
| 7 | 249.3 | 4.2 |
| 8 | 250.2 | 4.2 |
| 9 | 250.7 | 4.3 |
| 10 | 249.0 | 4.3 |
| 11 | 250.1 | 4.3 |
| 12 | 251.3 | 4.2 |
| 13 | 251.0 | 4.2 |
| 14 | 251.0 | 4.0 |
| 15 f | 250.8 | 1.9 |
| 16 | 251.0 | 3.9 |
| 17 | 248.9 | 4.3 |
| 18 | 249.8 | 4.1 |
| 19 | 250.6 | 4.0 |
| 20 | 250.8 | 4.2 |
| 21 | 251.2 | 4.2 |
| 22 | 250.6 | 4.1 |
| 23 | 249.6 | 4.2 |
| 24 | 250.7 | 4.3 |
| 25 | 250.6 | 4.1 |
| 26 | 250.7 | 4.1 |
| 27 | 250.8 | 4.1 |
| 28 f | 249.8 | 1.7 |
| 29 | 249.6 | 4.3 |
| 30 | 250.6 | 4.0 |
| 31 | 249.4 | 4.2 |
| 32 | 249.7 | 4.2 |
| 33 | 250.6 | 4.0 |
| 34 | 248.7 | 4.6 |
| 35 | 250.9 | 4.3 |
| 36 | 250.1 | 4.0 |
| 37 | 249.8 | 4.3 |
| 38 | 249.9 | 4.1 |
| 39 | 250.8 | 4.4 |
| 40 | 250.7 | 4.0 |
| 41 | 251.2 | 3.9 |
| 42 | 249.4 | 4.2 |
| 43 | 250.9 | 3.9 |
| 44 | 250.2 | 3.8 |
| 45 | 249.2 | 4.0 |
| 46 | 249.9 | 4.1 |
| 47 | 249.6 | 3.9 |
| 48 | 252.1 | 4.0 |
| 49 | 250.0 | 4.1 |
| 50 | 250.4 | 3.9 |
| 51 | 249.1 | 4.1 |
| 52 | 251.8 | 4.0 |
| 53 f | 250.7 | 1.8 |
| 54 | 249.8 | 3.9 |
| 55 | 250.2 | 4.1 |
| 56 | 250.7 | 4.1 |
| 57 | 250.5 | 4.0 |
| 58 | 250.2 | 4.1 |
| 59 | 249.4 | 4.1 |
| 60 | 249.1 | 4.1 |
| 61 | 251.0 | 4.2 |
| 62 | 251.3 | 4.0 |
| 63 | 251.3 | 4.1 |
| 64 | 250.3 | 3.9 |
| 65 | 249.1 | 4.2 |
| 66 f | 249.5 | 1.7 |
| 67 | 251.2 | 4.1 |
| 68 | 250.3 | 4.0 |
| 69 | 251.0 | 4.2 |
| 70 | 250.4 | 4.0 |
| 71 | 251.2 | 4.0 |
| 72 | 251.3 | 4.0 |
| 73 | 250.6 | 4.0 |
| 74 | 250.7 | 4.1 |
| 75 | 251.1 | 4.2 |
| 76 | 251.3 | 4.3 |
| 77 | 249.7 | 4.3 |
| 78 | 249.7 | 4.0 |

| CHIP 1 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 405.2 | 9.2 |
| 2 r | 249.8 | 0.7 |
| 3 | 250.2 | 4.3 |
| 4 | 249.6 | 4.3 |
| 5 | 249.6 | 4.1 |
| 6 | 250.4 | 4.2 |
| 7 | 249.5 | 4.1 |
| 8 | 249.6 | 4.0 |
| 9 | 249.1 | 4.1 |
| 10 | 250.5 | 4.2 |
| 11 | 251.0 | 4.2 |
| 12 | 250.0 | 4.3 |
| 13 | 250.8 | 4.2 |
| 14 | 250.4 | 4.1 |
| 15 f | 249.6 | 1.7 |
| 16 | 250.8 | 4.0 |
| 17 | 251.1 | 4.0 |
| 18 | 250.2 | 4.0 |
| 19 | 249.4 | 4.1 |
| 20 | 249.8 | 4.0 |
| 21 | 250.1 | 4.0 |
| 22 | 251.0 | 4.0 |
| 23 | 249.2 | 4.5 |
| 24 | 251.1 | 3.9 |
| 25 | 251.9 | 4.1 |
| 26 | 248.8 | 3.9 |
| 27 | 251.0 | 4.1 |
| 28 f | 249.8 | 1.7 |
| 29 | 251.4 | 4.0 |
| 30 | 250.9 | 4.0 |
| 31 | 249.7 | 4.1 |
| 32 | 249.7 | 4.0 |
| 33 | 251.6 | 4.1 |
| 34 | 252.1 | 4.1 |
| 35 | 249.8 | 3.9 |
| 36 | 250.3 | 4.4 |
| 37 | 250.7 | 4.0 |
| 38 | 249.7 | 4.1 |
| 39 | 250.3 | 4.2 |
| 40 | 250.9 | 3.8 |
| 41 | 249.6 | 3.8 |
| 42 | 251.8 | 3.8 |
| 43 | 248.9 | 4.0 |
| 44 | 252.0 | 3.6 |
| 45 | 249.9 | 3.8 |
| 46 | 250.0 | 3.9 |
| 47 | 250.8 | 4.0 |
| 48 | 249.7 | 4.0 |
| 49 | 249.8 | 4.0 |
| 50 | 250.6 | 3.9 |
| 51 | 247.4 | 4.0 |
| 52 | 249.5 | 4.0 |
| 53 f | 250.1 | 1.7 |
| 54 | 249.8 | 4.0 |
| 55 | 250.3 | 3.9 |
| 56 | 250.1 | 4.1 |
| 57 | 249.9 | 4.0 |
| 58 | 248.2 | 4.0 |
| 59 | 250.2 | 4.1 |
| 60 | 252.5 | 4.0 |
| 61 | 249.9 | 4.0 |
| 62 | 251.7 | 4.1 |
| 63 | 250.5 | 4.0 |
| 64 | 249.4 | 4.0 |
| 65 | 250.2 | 4.1 |
| 66 f | 250.2 | 1.7 |
| 67 | 250.3 | 3.9 |
| 68 | 249.8 | 4.0 |
| 69 | 251.6 | 4.0 |
| 70 | 250.1 | 4.2 |
| 71 | 249.1 | 4.2 |
| 72 | 250.6 | 3.9 |
| 73 | 250.8 | 4.1 |
| 74 | 250.5 | 3.8 |
| 75 | 251.6 | 3.8 |
| 76 | 251.3 | 3.9 |
| 77 | 251.0 | 4.0 |
| 78 | 248.9 | 4.3 |

| CHIP 2 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 438.5 | 8.8 |
| 2 r | 250.2 | 0.6 |
| 3 | 250.2 | 4.4 |
| 4 | 251.5 | 4.1 |
| 5 | 249.4 | 4.1 |
| 6 | 250.9 | 4.2 |
| 7 | 249.4 | 4.0 |
| 8 | 249.1 | 4.3 |
| 9 | 251.8 | 4.4 |
| 10 | 249.0 | 4.4 |
| 11 | 249.8 | 4.4 |
| 12 | 248.5 | 4.1 |
| 13 | 250.0 | 4.0 |
| 14 | 250.3 | 4.0 |
| 15 f | 250.4 | 1.6 |
| 16 | 249.2 | 4.1 |
| 17 | 251.8 | 4.1 |
| 18 | 250.4 | 3.9 |
| 19 | 250.9 | 4.1 |
| 20 | 249.5 | 4.0 |
| 21 | 251.6 | 4.1 |
| 22 | 249.2 | 4.0 |
| 23 | 250.7 | 4.2 |
| 24 | 249.1 | 4.1 |
| 25 | 250.1 | 4.2 |
| 26 | 250.3 | 4.4 |
| 27 | 249.9 | 3.8 |
| 28 f | 250.3 | 1.6 |
| 29 | 249.9 | 4.0 |
| 30 | 251.0 | 4.0 |
| 31 | 250.2 | 4.1 |
| 32 | 249.8 | 4.0 |
| 33 | 249.7 | 4.1 |
| 34 | 249.8 | 4.0 |
| 35 | 248.8 | 4.1 |
| 36 | 250.5 | 3.9 |
| 37 | 250.6 | 4.0 |
| 38 | 249.7 | 4.3 |
| 39 | 250.6 | 4.1 |
| 40 | 251.6 | 3.9 |
| 41 | 250.7 | 3.9 |
| 42 | 249.8 | 3.9 |
| 43 | 251.1 | 4.0 |
| 44 | 249.3 | 3.9 |
| 45 | 249.7 | 4.3 |
| 46 | 248.9 | 3.7 |
| 47 | 250.0 | 3.8 |
| 48 | 249.9 | 3.9 |
| 49 | 250.5 | 3.8 |
| 50 | 250.8 | 3.8 |
| 51 | 250.1 | 4.0 |
| 52 | 251.2 | 3.9 |
| 53 f | 250.3 | 1.6 |
| 54 | 248.8 | 3.8 |
| 55 | 249.8 | 3.7 |
| 56 | 249.7 | 4.2 |
| 57 | 249.5 | 4.0 |
| 58 | 249.4 | 3.8 |
| 59 | 250.2 | 3.9 |
| 60 | 250.2 | 3.8 |
| 61 | 250.7 | 3.9 |
| 62 | 249.5 | 3.8 |
| 63 | 250.1 | 3.9 |
| 64 | 251.1 | 4.1 |
| 65 | 251.0 | 3.9 |
| 66 f | 249.3 | 1.6 |
| 67 | 249.9 | 3.9 |
| 68 | 251.6 | 4.0 |
| 69 | 250.1 | 3.8 |
| 70 | 251.8 | 4.0 |
| 71 | 250.6 | 4.0 |
| 72 | 250.5 | 4.0 |
| 73 | 251.0 | 4.3 |
| 74 | 251.5 | 4.0 |
| 75 | 249.8 | 3.9 |
| 76 | 249.5 | 4.0 |
| 77 | 248.7 | 4.1 |
| 78 | 249.3 | 3.9 |

| CHIP 3 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 250.6 | 8.7 |
| 2 r | 250.0 | 0.7 |
| 3 | 249.5 | 4.6 |
| 4 | 250.0 | 4.4 |
| 5 | 249.2 | 4.2 |
| 6 | 250.3 | 4.1 |
| 7 | 249.6 | 4.4 |
| 8 | 251.0 | 4.1 |
| 9 | 249.9 | 4.4 |
| 10 | 251.1 | 4.3 |
| 11 | 248.8 | 4.2 |
| 12 | 251.3 | 4.2 |
| 13 | 250.5 | 4.0 |
| 14 | 248.6 | 4.1 |
| 15 f | 249.6 | 1.9 |
| 16 | 250.7 | 4.0 |
| 17 | 249.8 | 4.0 |
| 18 | 249.8 | 4.3 |
| 19 | 250.4 | 4.2 |
| 20 | 249.7 | 4.2 |
| 21 | 250.2 | 4.0 |
| 22 | 250.3 | 4.3 |
| 23 | 250.8 | 4.5 |
| 24 | 248.8 | 4.1 |
| 25 | 249.7 | 4.2 |
| 26 | 251.0 | 4.1 |
| 27 | 250.4 | 4.0 |
| 28 f | 251.0 | 1.8 |
| 29 | 249.5 | 4.2 |
| 30 | 251.3 | 4.1 |
| 31 | 250.6 | 4.1 |
| 32 | 248.5 | 4.2 |
| 33 | 249.2 | 4.2 |
| 34 | 249.5 | 4.0 |
| 35 | 251.3 | 4.2 |
| 36 | 248.9 | 4.2 |
| 37 | 249.4 | 4.0 |
| 38 | 250.4 | 4.2 |
| 39 | 249.8 | 4.3 |
| 40 | 249.2 | 4.1 |
| 41 | 249.9 | 4.0 |
| 42 | 251.4 | 3.8 |
| 43 | 250.5 | 3.9 |
| 44 | 248.3 | 3.8 |
| 45 | 249.5 | 3.7 |
| 46 | 250.5 | 4.0 |
| 47 | 251.3 | 3.8 |
| 48 | 249.8 | 4.0 |
| 49 | 249.6 | 3.9 |
| 50 | 249.7 | 4.0 |
| 51 | 251.2 | 4.0 |
| 52 | 250.2 | 3.7 |
| 53 f | 250.8 | 1.7 |
| 54 | 250.2 | 3.9 |
| 55 | 249.6 | 3.9 |
| 56 | 250.9 | 4.1 |
| 57 | 249.3 | 4.0 |
| 58 | 250.3 | 4.0 |
| 59 | 249.8 | 4.0 |
| 60 | 249.3 | 3.8 |
| 61 | 250.6 | 4.2 |
| 62 | 249.3 | 3.7 |
| 63 | 249.9 | 4.0 |
| 64 | 250.7 | 3.9 |
| 65 | 249.8 | 4.0 |
| 66 f | 249.6 | 1.6 |
| 67 | 249.7 | 3.9 |
| 68 | 251.0 | 4.0 |
| 69 | 249.2 | 3.8 |
| 70 | 251.5 | 3.9 |
| 71 | 250.9 | 4.0 |
| 72 | 250.2 | 4.0 |
| 73 | 248.4 | 4.1 |
| 74 | 250.6 | 4.0 |
| 75 | 250.4 | 3.9 |
| 76 | 252.6 | 4.0 |
| 77 | 250.1 | 4.3 |
| 78 | 249.9 | 3.9 |

| CHIP 4 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 364.5 | 9.1 |
| 2 r | 250.6 | 0.7 |
| 3 | 248.8 | 4.4 |
| 4 | 249.6 | 4.3 |
| 5 | 250.4 | 4.4 |
| 6 | 249.1 | 4.4 |
| 7 | 251.1 | 4.3 |
| 8 | 252.3 | 4.2 |
| 9 | 250.7 | 4.4 |
| 10 | 250.4 | 4.2 |
| 11 | 250.4 | 4.2 |
| 12 | 250.0 | 4.1 |
| 13 | 251.8 | 4.1 |
| 14 | 251.9 | 4.1 |
| 15 f | 249.7 | 1.5 |
| 16 | 250.4 | 4.0 |
| 17 | 249.7 | 4.1 |
| 18 | 250.7 | 4.3 |
| 19 | 251.7 | 4.0 |
| 20 | 251.2 | 4.4 |
| 21 | 248.9 | 4.1 |
| 22 | 250.8 | 4.0 |
| 23 | 250.2 | 4.3 |
| 24 | 248.8 | 4.0 |
| 25 | 252.1 | 4.1 |
| 26 | 248.5 | 3.8 |
| 27 | 251.3 | 4.4 |
| 28 f | 249.8 | 1.6 |
| 29 | 249.4 | 4.5 |
| 30 | 250.5 | 4.1 |
| 31 | 252.1 | 4.1 |
| 32 | 250.6 | 4.0 |
| 33 | 248.7 | 4.1 |
| 34 | 250.0 | 4.2 |
| 35 | 250.4 | 4.2 |
| 36 | 250.9 | 4.3 |
| 37 | 252.1 | 4.0 |
| 38 | 248.5 | 4.2 |
| 39 | 250.5 | 4.5 |
| 40 | 249.9 | 4.0 |
| 41 | 249.6 | 3.9 |
| 42 | 249.6 | 3.8 |
| 43 | 251.3 | 3.9 |
| 44 | 250.8 | 4.2 |
| 45 | 250.7 | 3.9 |
| 46 | 251.4 | 4.0 |
| 47 | 250.1 | 3.9 |
| 48 | 251.5 | 3.9 |
| 49 | 252.7 | 4.0 |
| 50 | 250.9 | 3.9 |
| 51 | 251.2 | 4.0 |
| 52 | 250.7 | 3.9 |
| 53 f | 250.7 | 1.7 |
| 54 | 250.3 | 4.0 |
| 55 | 249.9 | 4.0 |
| 56 | 249.7 | 4.0 |
| 57 | 250.4 | 4.1 |
| 58 | 250.0 | 4.0 |
| 59 | 250.6 | 3.9 |
| 60 | 249.8 | 4.0 |
| 61 | 250.4 | 3.8 |
| 62 | 249.1 | 4.3 |
| 63 | 249.8 | 4.0 |
| 64 | 249.8 | 4.1 |
| 65 | 250.7 | 3.8 |
| 66 f | 250.6 | 1.7 |
| 67 | 249.2 | 4.0 |
| 68 | 249.3 | 4.0 |
| 69 | 250.8 | 4.2 |
| 70 | 249.8 | 3.8 |
| 71 | 248.6 | 4.3 |
| 72 | 250.2 | 4.1 |
| 73 | 248.7 | 4.2 |
| 74 | 249.1 | 4.2 |
| 75 | 250.1 | 4.3 |
| 76 | 248.2 | 4.2 |
| 77 | 250.7 | 3.9 |
| 78 | 249.8 | 4.1 |

| CHIP 5 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 276.8 | 12.0 |
| 2 r | 250.5 | 0.7 |
| 3 | 251.0 | 4.3 |
| 4 | 251.2 | 4.3 |
| 5 | 249.1 | 4.1 |
| 6 | 250.0 | 4.2 |
| 7 | 249.8 | 4.2 |
| 8 | 250.5 | 4.0 |
| 9 | 248.8 | 4.1 |
| 10 | 250.9 | 4.0 |
| 11 | 249.4 | 4.2 |
| 12 | 248.3 | 4.4 |
| 13 | 249.9 | 4.0 |
| 14 | 249.7 | 4.1 |
| 15 f | 249.4 | 1.8 |
| 16 | 249.7 | 4.0 |
| 17 | 251.1 | 4.0 |
| 18 | 248.2 | 4.3 |
| 19 | 250.8 | 4.2 |
| 20 | 250.3 | 4.2 |
| 21 | 250.2 | 4.2 |
| 22 | 250.4 | 3.9 |
| 23 | 250.6 | 4.1 |
| 24 | 250.5 | 4.1 |
| 25 | 249.1 | 4.2 |
| 26 | 250.4 | 4.4 |
| 27 | 248.8 | 4.1 |
| 28 f | 249.6 | 1.9 |
| 29 | 250.4 | 4.0 |
| 30 | 250.9 | 4.1 |
| 31 | 250.3 | 3.9 |
| 32 | 249.8 | 4.1 |
| 33 | 250.4 | 4.2 |
| 34 | 249.8 | 4.1 |
| 35 | 250.5 | 4.0 |
| 36 | 250.7 | 4.2 |
| 37 | 249.6 | 4.1 |
| 38 | 250.5 | 3.9 |
| 39 | 250.9 | 4.3 |
| 40 | 249.8 | 4.1 |
| 41 | 249.8 | 3.9 |
| 42 | 249.2 | 3.8 |
| 43 | 251.1 | 4.0 |
| 44 | 250.7 | 3.9 |
| 45 | 250.2 | 3.8 |
| 46 | 249.5 | 4.0 |
| 47 | 249.7 | 3.9 |
| 48 | 249.8 | 3.9 |
| 49 | 251.8 | 4.1 |
| 50 | 248.4 | 3.9 |
| 51 | 249.7 | 4.0 |
| 52 | 250.4 | 3.9 |
| 53 f | 250.3 | 1.7 |
| 54 | 248.7 | 3.9 |
| 55 | 250.5 | 3.8 |
| 56 | 249.1 | 3.9 |
| 57 | 248.7 | 3.8 |
| 58 | 249.4 | 3.8 |
| 59 | 250.6 | 3.9 |
| 60 | 250.2 | 3.9 |
| 61 | 249.7 | 3.8 |
| 62 | 250.3 | 3.9 |
| 63 | 250.8 | 4.0 |
| 64 | 251.8 | 3.8 |
| 65 | 249.4 | 3.8 |
| 66 f | 250.5 | 1.5 |
| 67 | 250.7 | 4.0 |
| 68 | 249.7 | 3.8 |
| 69 | 250.4 | 3.8 |
| 70 | 250.8 | 3.9 |
| 71 | 250.4 | 4.0 |
| 72 | 250.9 | 3.8 |
| 73 | 249.9 | 3.8 |
| 74 | 250.8 | 3.8 |
| 75 | 250.1 | 3.9 |
| 76 | 249.4 | 4.0 |
| 77 | 249.1 | 4.0 |
| 78 | 250.6 | 4.0 |

| CHIP 6 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 251.0 | 12.1 |
| 2 r | 250.5 | 0.7 |
| 3 | 249.9 | 4.6 |
| 4 | 250.2 | 4.3 |
| 5 | 251.5 | 4.4 |
| 6 | 250.3 | 4.3 |
| 7 | 250.9 | 4.5 |
| 8 | 249.6 | 4.1 |
| 9 | 250.8 | 4.0 |
| 10 | 248.1 | 4.4 |
| 11 | 249.8 | 4.3 |
| 12 | 250.8 | 4.2 |
| 13 | 251.0 | 4.3 |
| 14 | 249.9 | 4.4 |
| 15 f | 249.9 | 1.7 |
| 16 | 250.1 | 4.1 |
| 17 | 249.1 | 4.3 |
| 18 | 251.1 | 4.1 |
| 19 | 250.9 | 4.3 |
| 20 | 251.3 | 4.3 |
| 21 | 249.6 | 4.4 |
| 22 | 250.9 | 4.4 |
| 23 | 251.5 | 4.2 |
| 24 | 249.2 | 4.3 |
| 25 | 251.9 | 4.3 |
| 26 | 250.4 | 4.1 |
| 27 | 249.9 | 4.2 |
| 28 f | 251.0 | 1.8 |
| 29 | 249.7 | 4.2 |
| 30 | 251.1 | 4.2 |
| 31 | 250.5 | 4.1 |
| 32 | 249.6 | 4.2 |
| 33 | 251.4 | 4.3 |
| 34 | 249.3 | 4.3 |
| 35 | 251.0 | 4.2 |
| 36 | 249.7 | 4.2 |
| 37 | 248.3 | 4.5 |
| 38 | 250.5 | 4.2 |
| 39 | 252.8 | 4.5 |
| 40 | 250.1 | 4.1 |
| 41 | 251.2 | 4.2 |
| 42 | 251.4 | 4.0 |
| 43 | 250.4 | 4.0 |
| 44 | 248.8 | 4.2 |
| 45 | 251.0 | 4.2 |
| 46 | 249.8 | 4.0 |
| 47 | 250.5 | 4.0 |
| 48 | 251.1 | 4.0 |
| 49 | 251.6 | 4.0 |
| 50 | 250.3 | 4.1 |
| 51 | 251.2 | 4.0 |
| 52 | 249.0 | 4.2 |
| 53 f | 251.4 | 1.6 |
| 54 | 249.2 | 4.0 |
| 55 | 250.2 | 4.4 |
| 56 | 252.1 | 4.0 |
| 57 | 250.5 | 4.0 |
| 58 | 249.2 | 4.3 |
| 59 | 250.0 | 4.1 |
| 60 | 250.1 | 4.0 |
| 61 | 249.2 | 4.1 |
| 62 | 250.7 | 3.9 |
| 63 | 251.1 | 4.1 |
| 64 | 251.6 | 4.1 |
| 65 | 248.7 | 4.0 |
| 66 f | 251.0 | 1.6 |
| 67 | 251.6 | 4.1 |
| 68 | 250.5 | 4.2 |
| 69 | 250.7 | 4.1 |
| 70 | 249.2 | 4.2 |
| 71 | 251.7 | 4.1 |
| 72 | 249.6 | 4.2 |
| 73 | 250.0 | 4.1 |
| 74 | 251.9 | 4.1 |
| 75 | 249.1 | 4.1 |
| 76 | 249.7 | 4.6 |
| 77 | 252.1 | 4.2 |
| 78 | 249.6 | 4.2 |

| CHIP 7 | | |
|---|---|---|
| CH | M | STD |
| 0 r | 250.0 | 0.0 |
| 1 r | 421.1 | 13.9 |
| 2 r | 250.4 | 0.7 |
| 3 | 250.7 | 4.2 |
| 4 | 249.4 | 4.5 |
| 5 | 248.8 | 4.3 |
| 6 | 249.8 | 4.2 |
| 7 | 250.9 | 4.2 |
| 8 | 249.9 | 4.4 |
| 9 | 250.8 | 4.2 |
| 10 | 250.7 | 4.3 |
| 11 | 250.8 | 4.1 |
| 12 | 252.3 | 4.2 |
| 13 | 250.8 | 4.2 |
| 14 | 250.4 | 4.4 |
| 15 f | 250.7 | 1.7 |
| 16 | 251.1 | 4.3 |
| 17 | 251.6 | 4.4 |
| 18 | 250.3 | 4.2 |
| 19 | 251.4 | 4.3 |
| 20 | 250.2 | 4.1 |
| 21 | 249.9 | 4.4 |
| 22 | 251.5 | 4.0 |
| 23 | 250.9 | 4.2 |
| 24 | 249.7 | 4.1 |
| 25 | 250.3 | 4.2 |
| 26 | 250.8 | 4.1 |
| 27 | 251.6 | 4.3 |
| 28 f | 250.4 | 1.8 |
| 29 | 250.2 | 4.0 |
| 30 | 251.2 | 4.3 |
| 31 | 249.6 | 4.1 |
| 32 | 251.9 | 4.3 |
| 33 | 249.4 | 4.4 |
| 34 | 249.8 | 4.4 |
| 35 | 250.9 | 4.2 |
| 36 | 250.6 | 4.3 |
| 37 | 251.4 | 4.1 |
| 38 | 249.3 | 4.2 |
| 39 | 248.7 | 4.3 |
| 40 | 250.0 | 4.1 |
| 41 | 251.1 | 4.0 |
| 42 | 250.9 | 4.0 |
| 43 | 250.3 | 4.3 |
| 44 | 249.1 | 4.1 |
| 45 | 249.6 | 4.0 |
| 46 | 250.1 | 3.9 |
| 47 | 249.4 | 3.8 |
| 48 | 250.4 | 4.2 |
| 49 | 249.9 | 4.3 |
| 50 | 251.1 | 4.2 |
| 51 | 248.0 | 3.9 |
| 52 | 250.5 | 4.1 |
| 53 f | 250.4 | 1.8 |
| 54 | 251.1 | 4.0 |
| 55 | 251.6 | 4.0 |
| 56 | 250.5 | 4.3 |
| 57 | 250.5 | 4.0 |
| 58 | 251.1 | 4.0 |
| 59 | 251.8 | 4.2 |
| 60 | 250.7 | 4.3 |
| 61 | 250.4 | 4.1 |
| 62 | 249.5 | 4.0 |
| 63 | 250.7 | 4.0 |
| 64 | 249.1 | 4.1 |
| 65 | 251.4 | 4.0 |
| 66 f | 250.5 | 1.6 |
| 67 | 249.1 | 4.0 |
| 68 | 249.9 | 4.0 |
| 69 | 250.3 | 3.9 |
| 70 | 250.7 | 4.1 |
| 71 | 251.0 | 4.0 |
| 72 | 249.9 | 4.3 |
| 73 | 250.3 | 4.0 |
| 74 | 248.0 | 4.0 |
| 75 | 251.2 | 4.2 |
| 76 | 249.4 | 4.0 |
| 77 | 250.9 | 4.1 |
| 78 | 250.2 | 4.4 |