Centre de Physique des Particules de Marseille

ATLAS LAR CALORIMETER UPGRADES

Phase 1 Control and Monitoring and Phase 2 AIDAQ Project

November 23, 2020

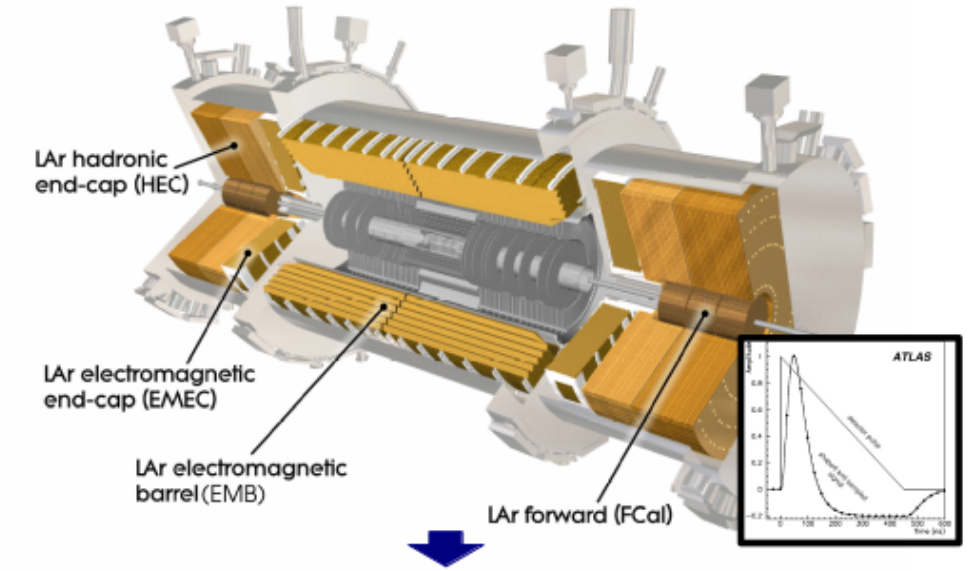
Etienne FORTIN

Overview

ATLAS LAr

Pb(Cu,W)/LAr sampling calorimeter

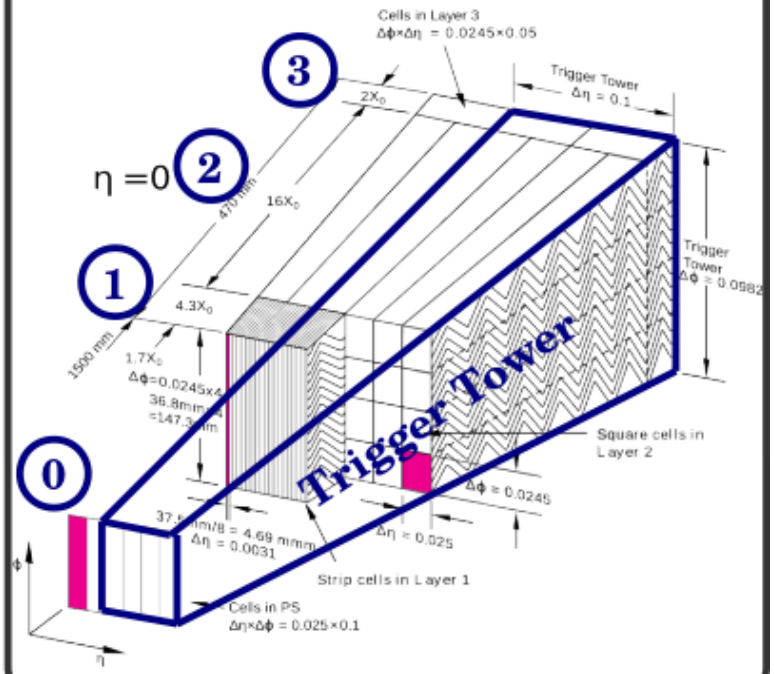
- ~180k cells → only for main readout (100 kHz max)



γ, e±, jets, MET from ionisation pulse

Run 1 & 2 : Trigger Tower (TT) (6k)

- Cell clusters in (η,φ) for trigger

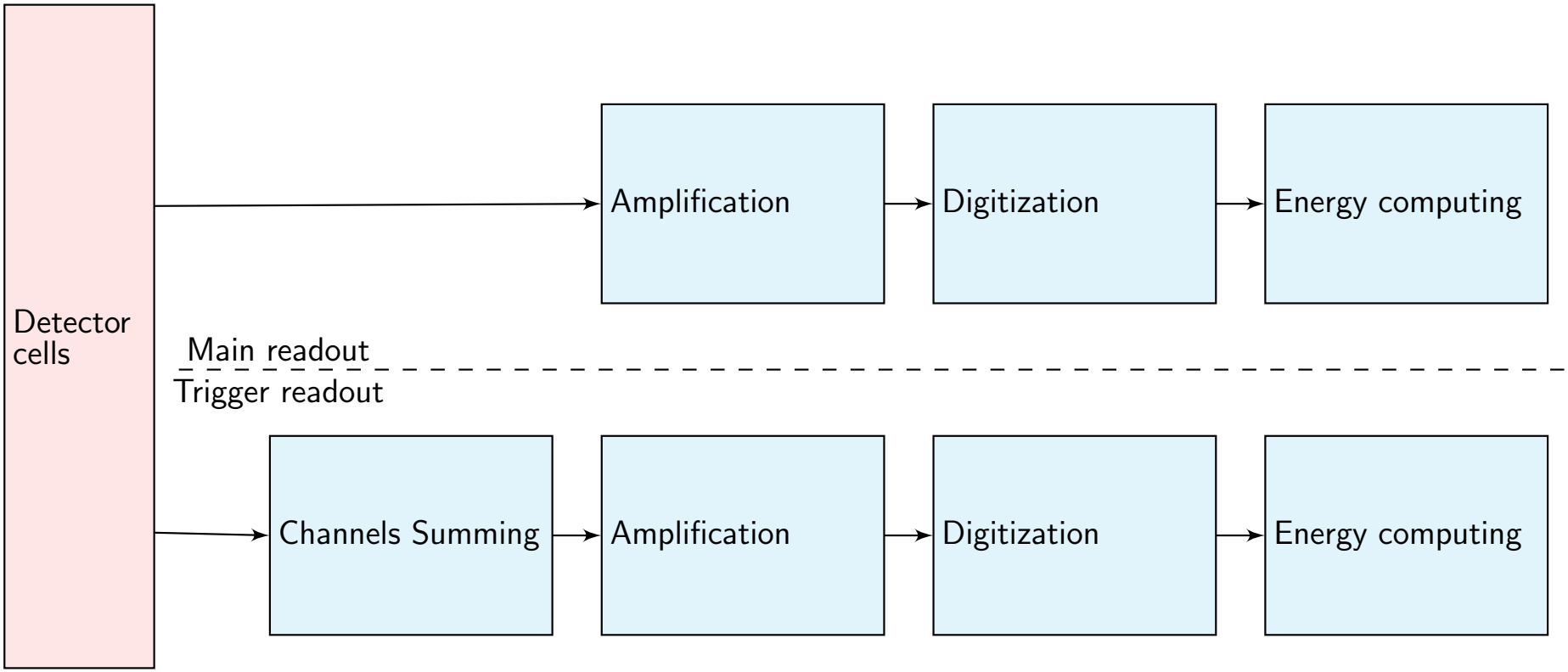


- Is integrated in the ATLAS Detector Control System (DCS)
- The Run Control Application configured it for data taking

LHC-HL Plan

- Phase 1 (now): Trigger Readout upgrade
- Phase 2: Main readout upgrade

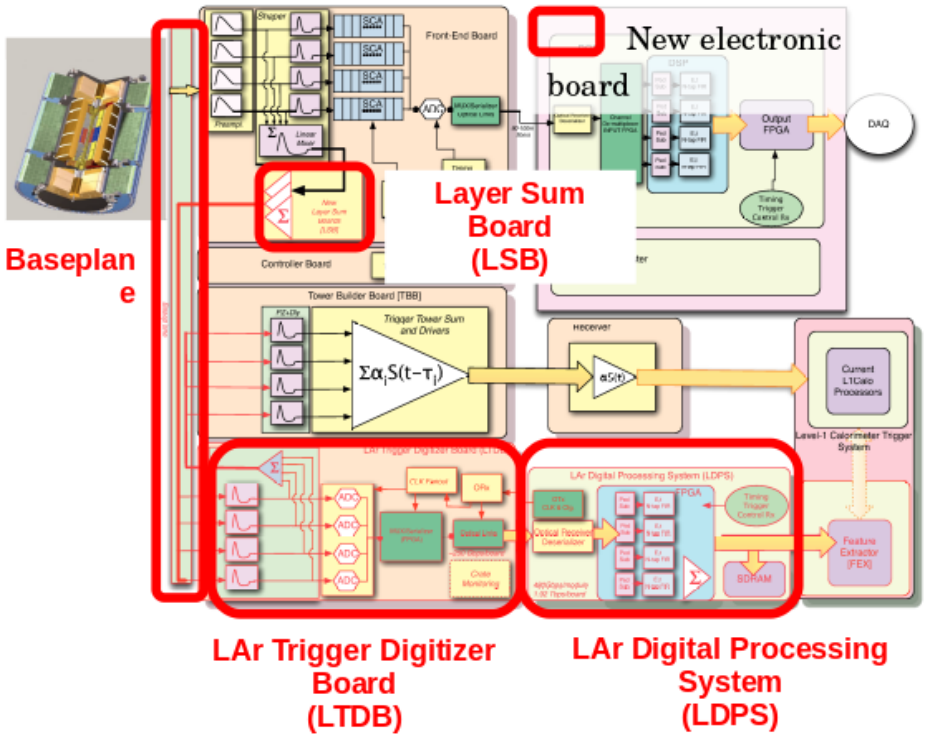
Readout


Detector cells
Amplification
Digitization
Energy computing
Main readout
Trigger readout
Channels Summing
Amplification
Digitization
Energy computing

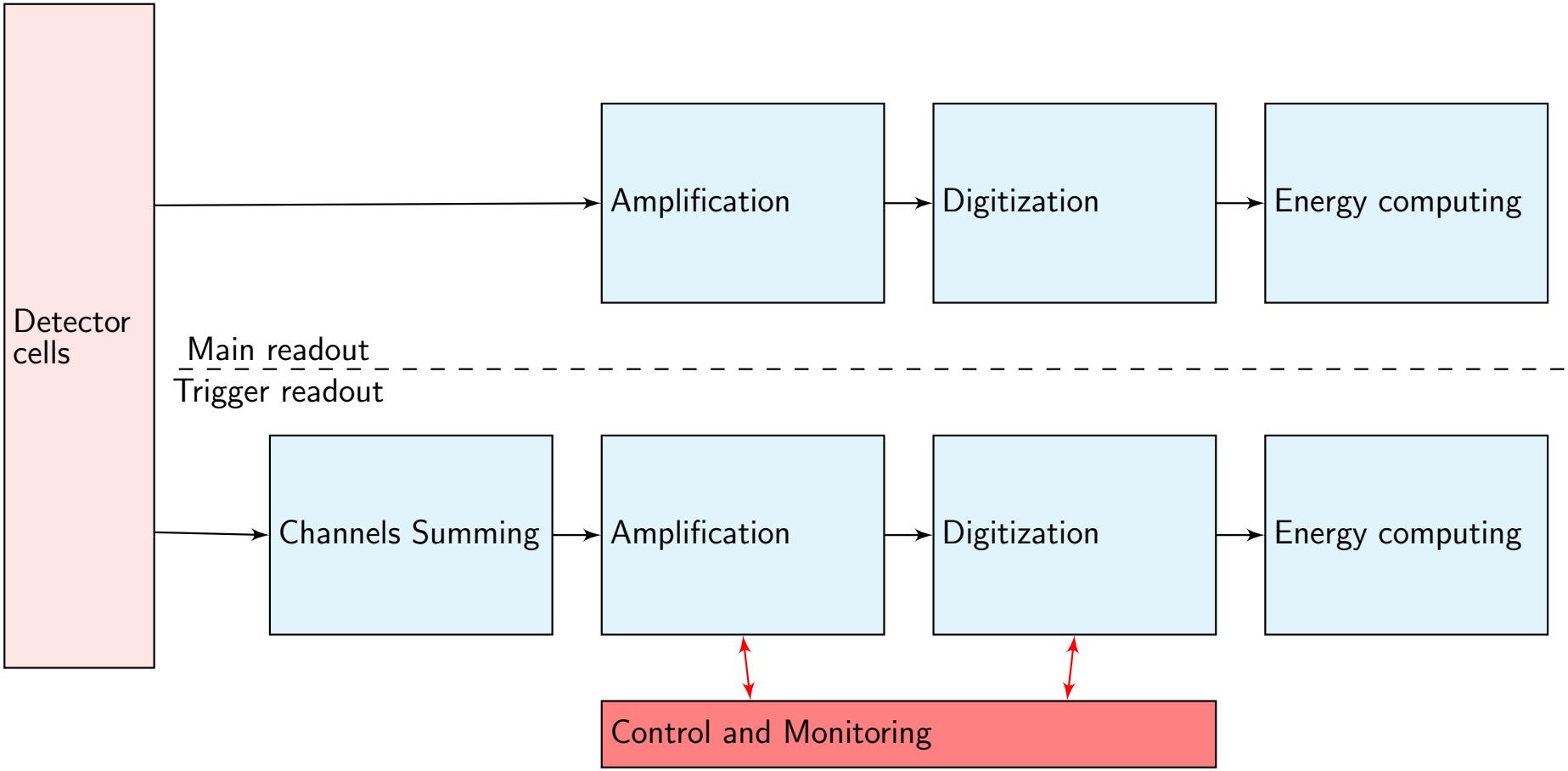
Phase 1 Trigger upgrade

LTDB:

- Digitizes Super Cell Signals at 40 MHz, 12b precision
- Send ADC to LDPS
- 320 Channels per board
- Send old layer sums to legacy trigger system (backup)
- Increased granularity



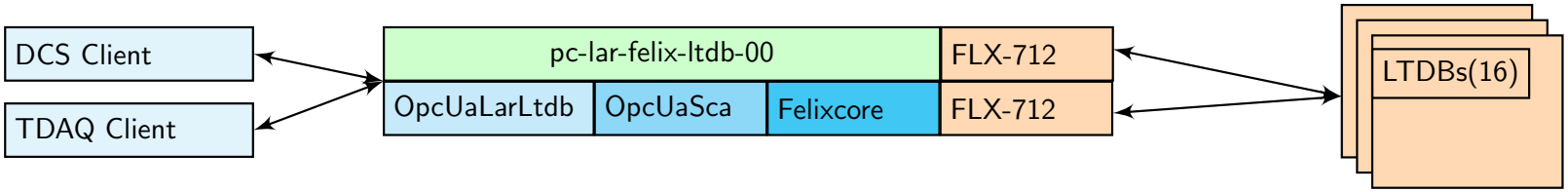
Ltdb Control and monitoring



Have a fast and reliable control and monitoring ?

- about 120 boards
- containing about 135 components who may need a specific configuration
- Some components have hardware issue and need a different configuration process
- about 400k Registers in total
- Some components need a calibration
- The control is done through a GBT SCA asic providing several I2C bus, GPIO and monitoring Adc

LTDB control: Choosen setup



Felix-712:

- Switch that handle 40 slow control links
- GBT protocol (Rad-Hard optical links) (CERN

Felixcore:

- Server to control the felix

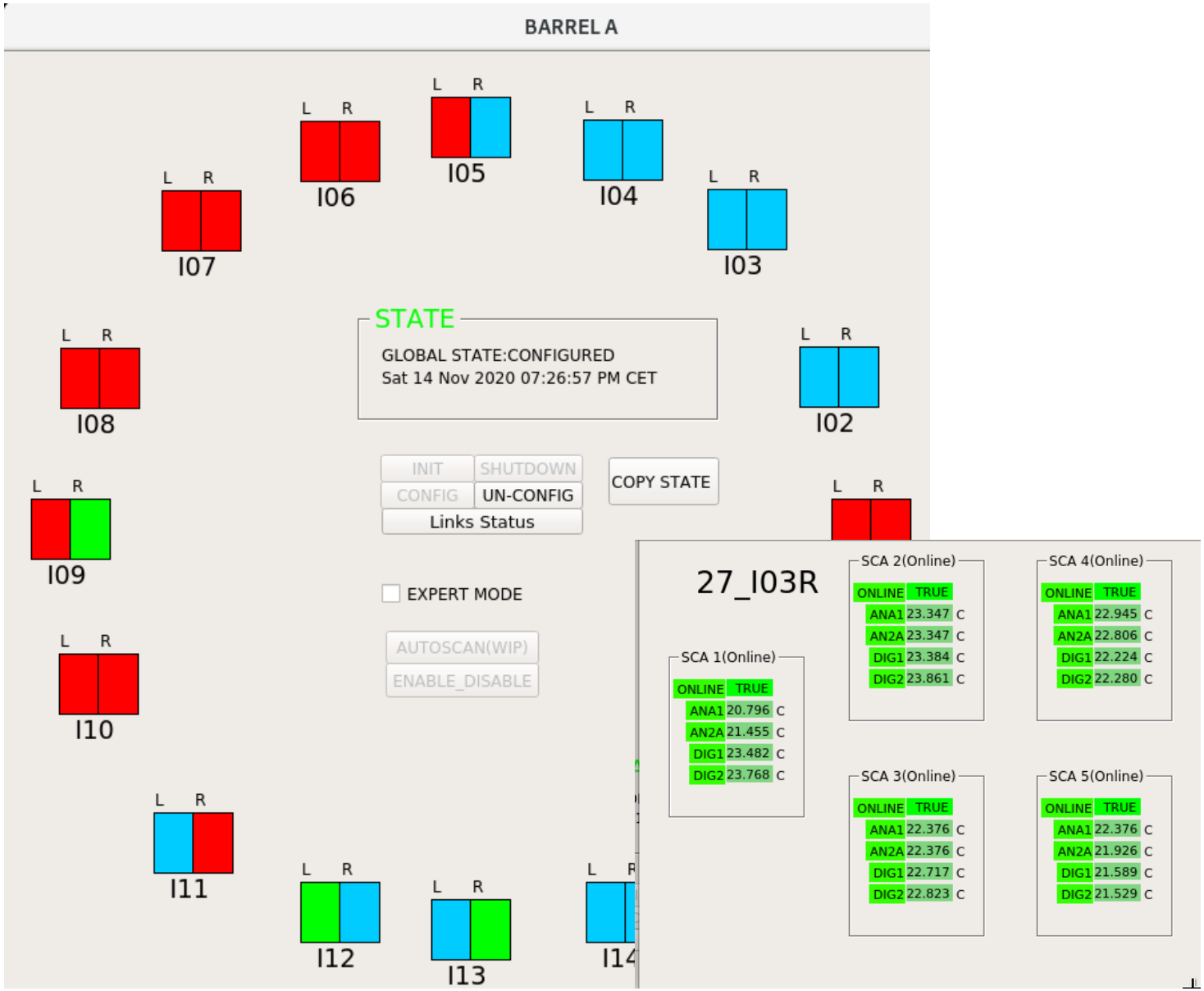
OpcUaScaServer:

- Server to provide abstraction over the Felix
- Provide function at GBT-SCA level
- For example I2CSlave.write, Gpio.read

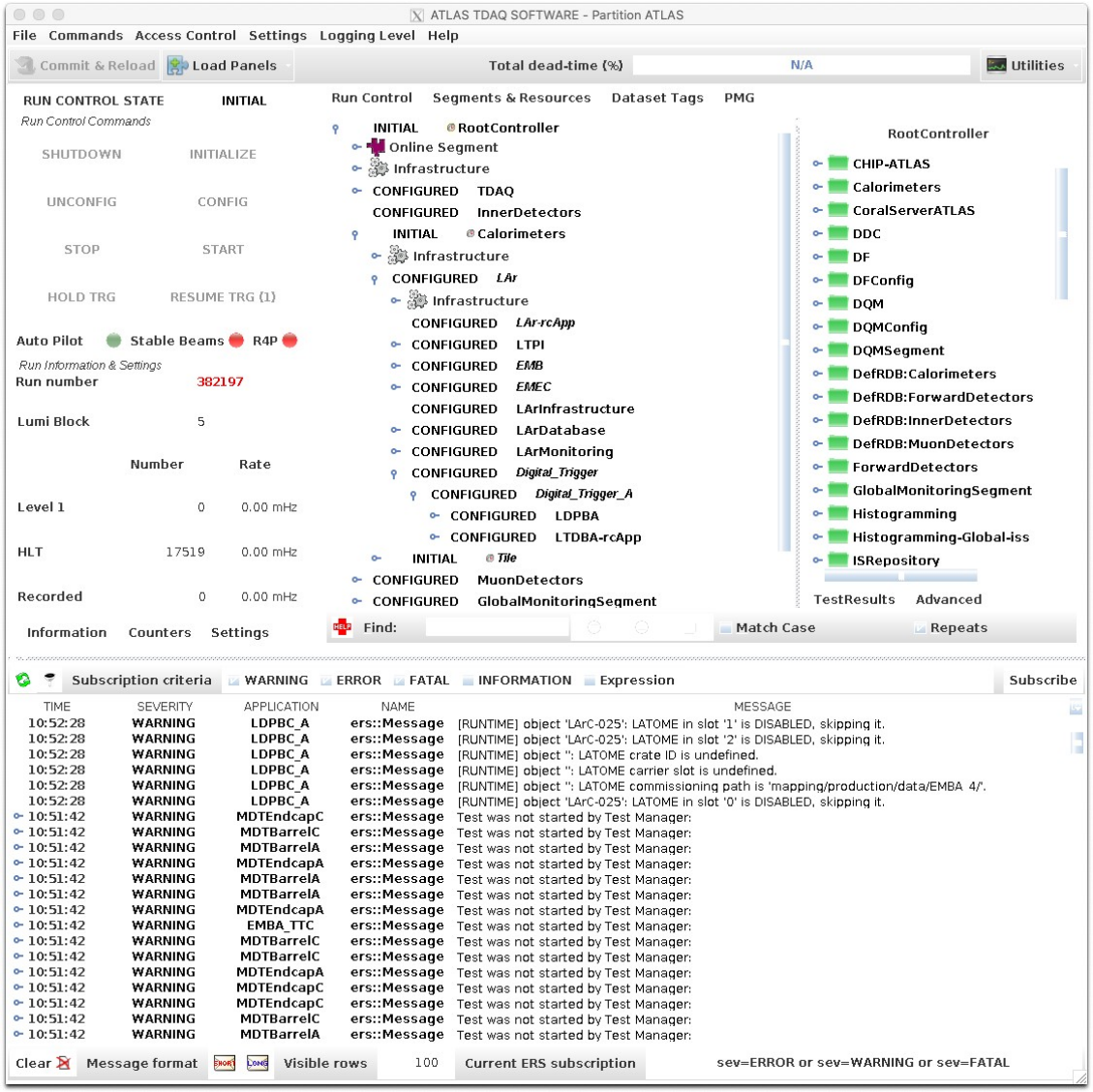
OpcUaLarLtdb

- Develloped at CPPM
- Server which provide to TDAQ (Run Control) or DCS high level functions to control the LTDB and monitoring values.
- For example one function per TDAQ transition (Init,Configure)
- Can handle several hardware errors with retries or dedicated functions
- Multi-threaded, a configuration take 9s now
- Is able to read BE boards (LDPS) for calibrations
- One C++ class per component

My DCS Client

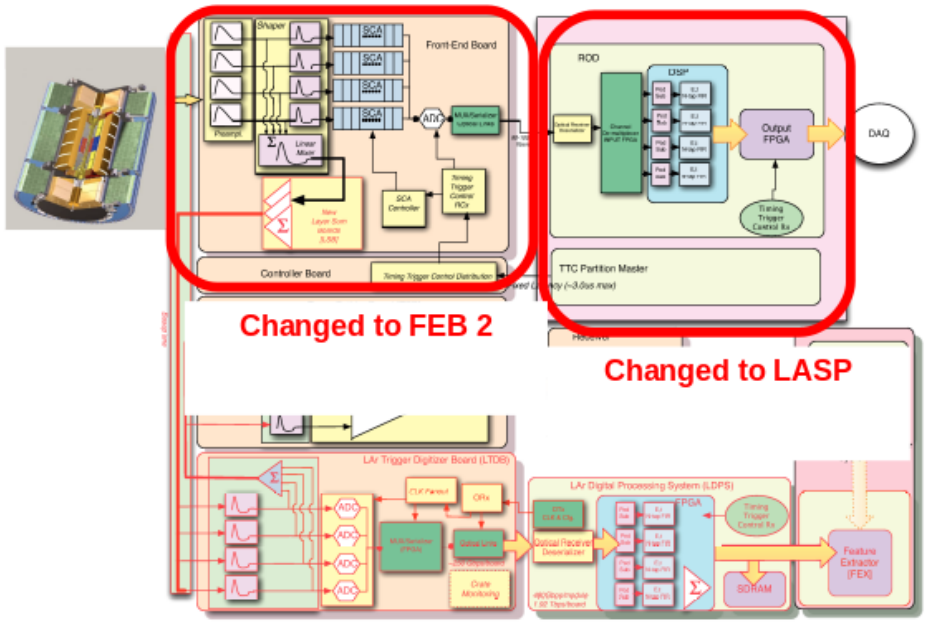


TDAQ Client(Included in ATLAS partition)

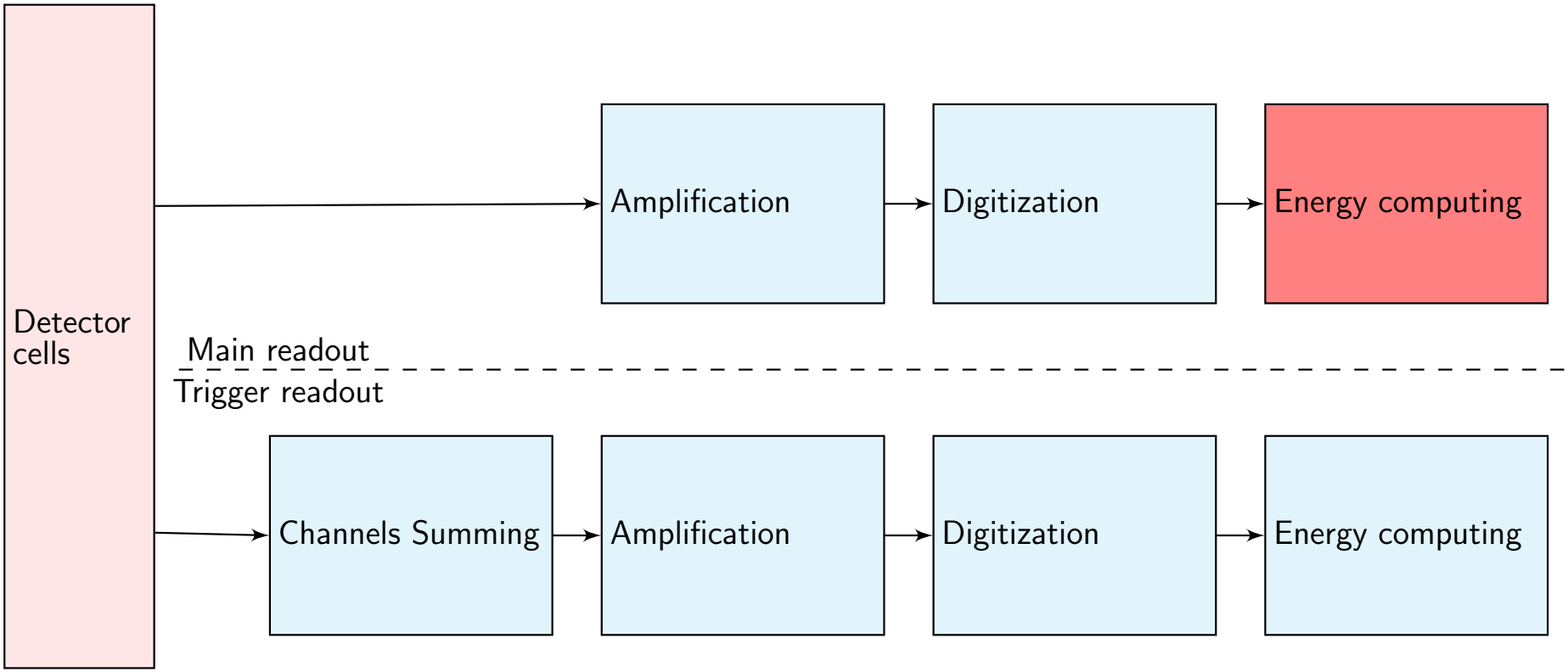


Phase 2 upgrade: AIDAQ

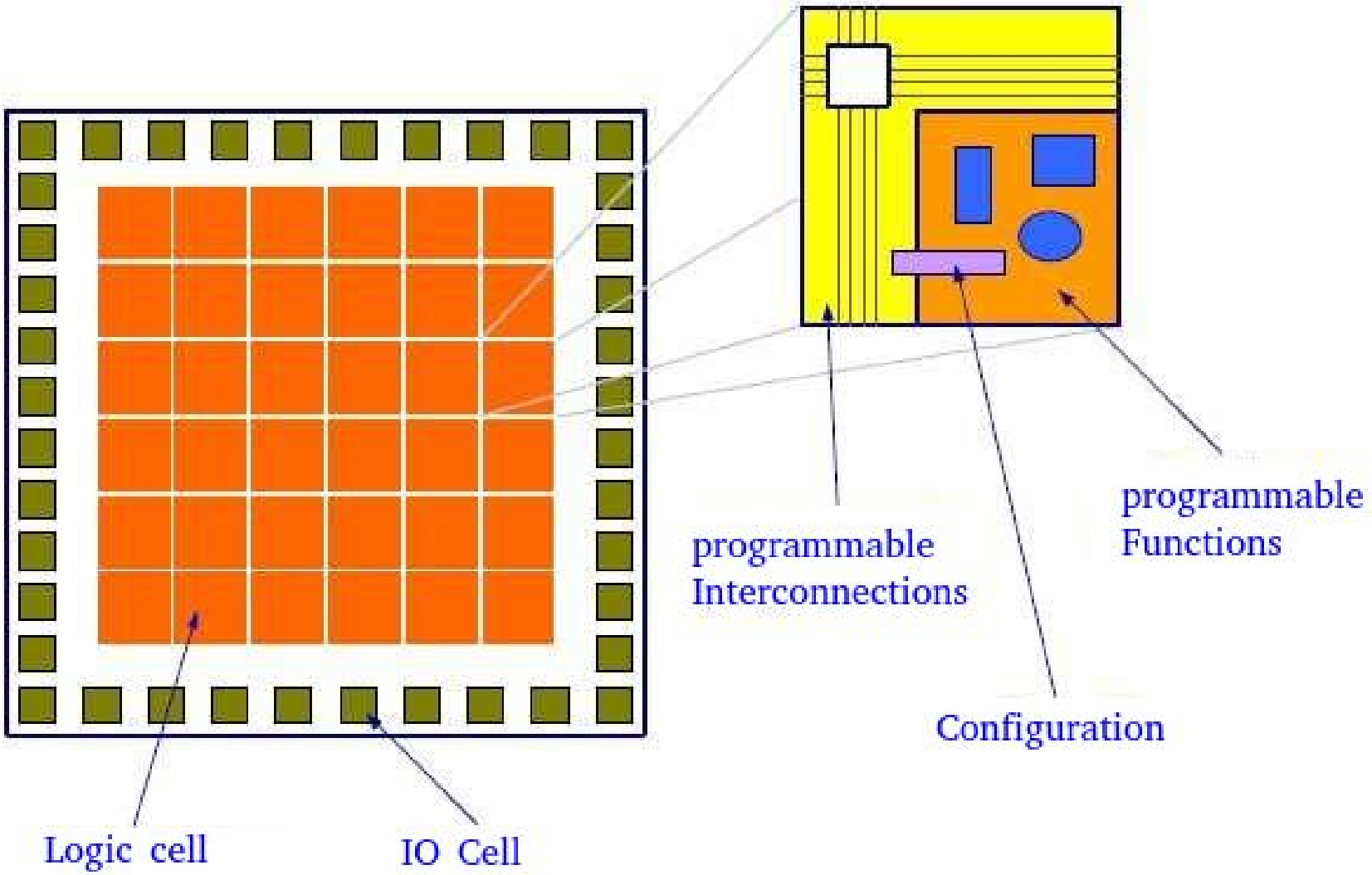
- We want to devellop a neural network to compute energies coming from the ADC of the liquid Argon Calorimeter of ATLAS.
- To increase the performance with the Hi-Lumi pile up.
- Implemented in the new readout board, the LASP
- 2 Stratix 10 FPGAs.



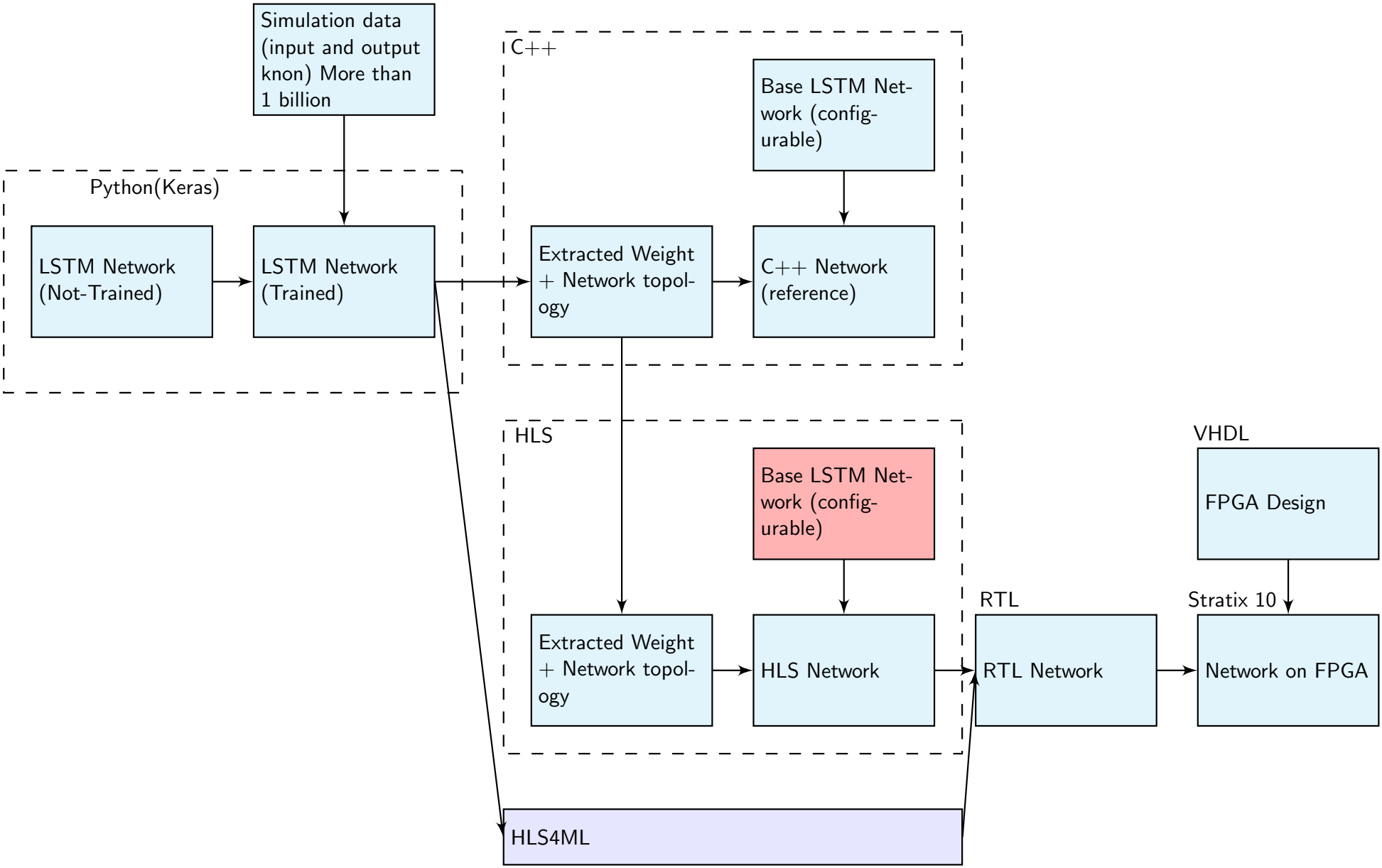
Phase 2 upgrade: AIDAQ



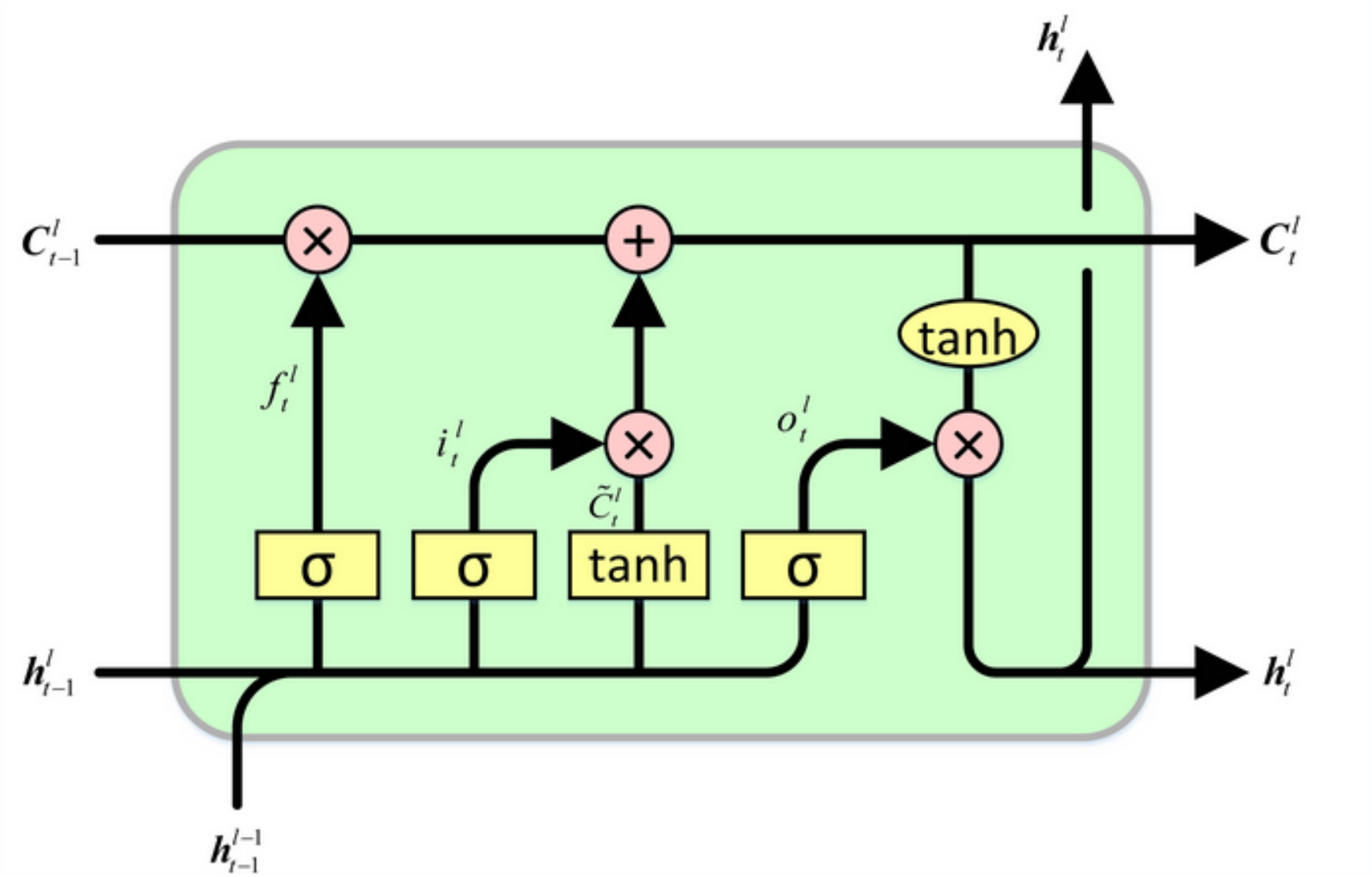
FPGA


programmable
Interconnections
programmable
Functions
Configuration
Logic cell
IO Cell

Phase 2 upgrade: AIDAQ

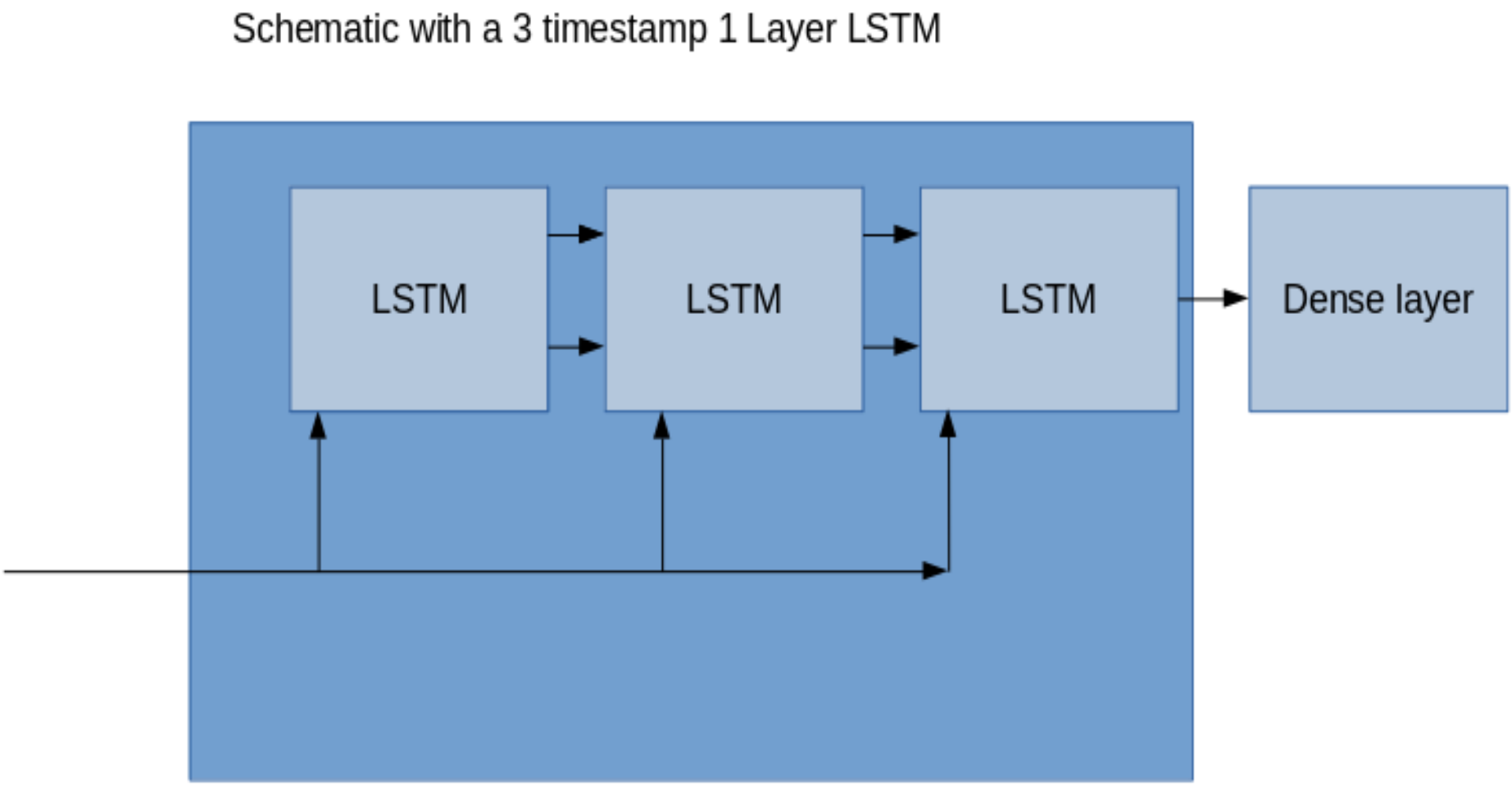


LSTM cell

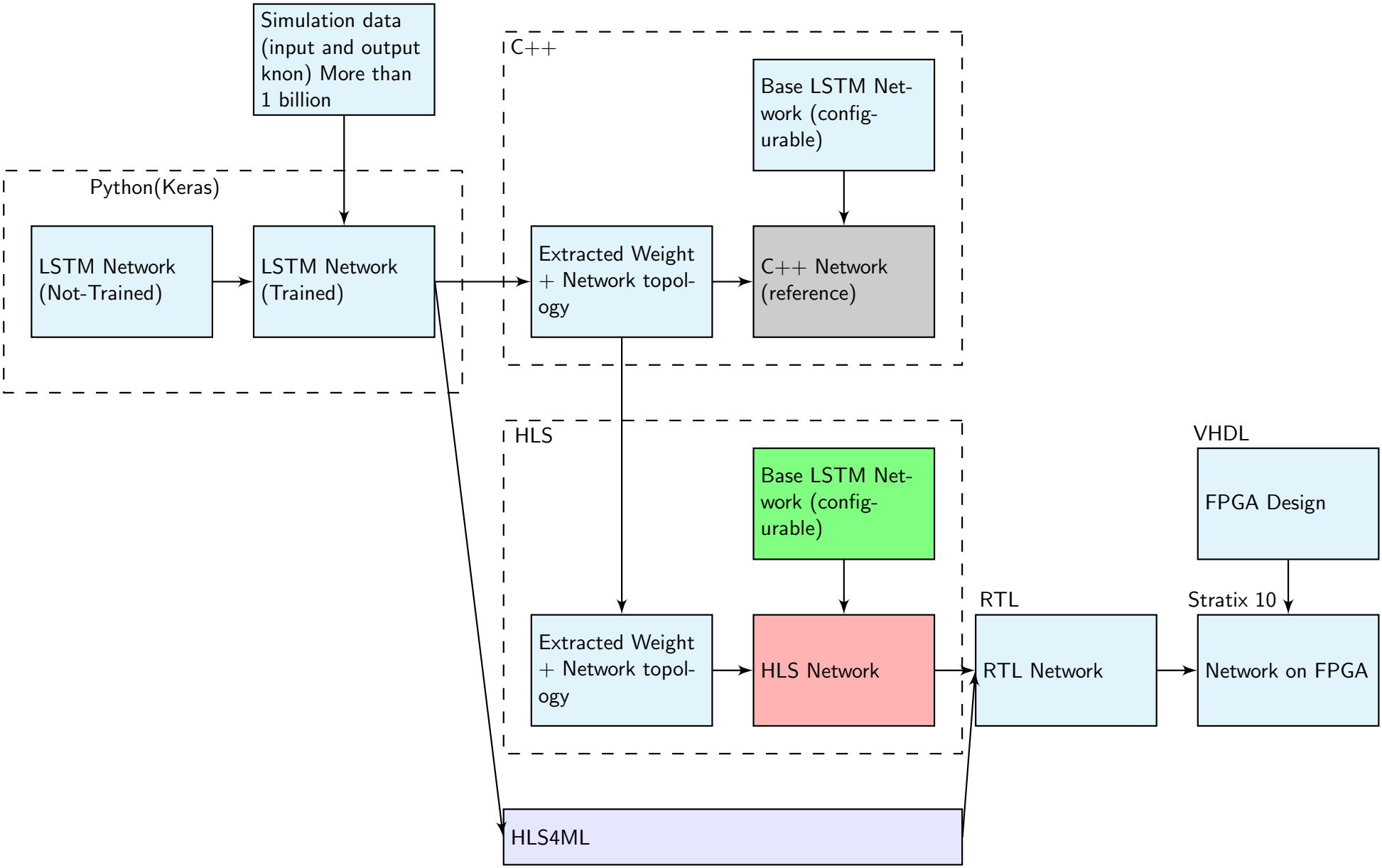

h_t^l
C_{t-1}^l
C_t^l
tanh
f_t^l
i_t^l
o_t^l
$\tilde{C}_t^l$
σ
σ
tanh
σ
h_{t-1}^l
h_t^l
h_{t-1}^{l-1}

Implementation

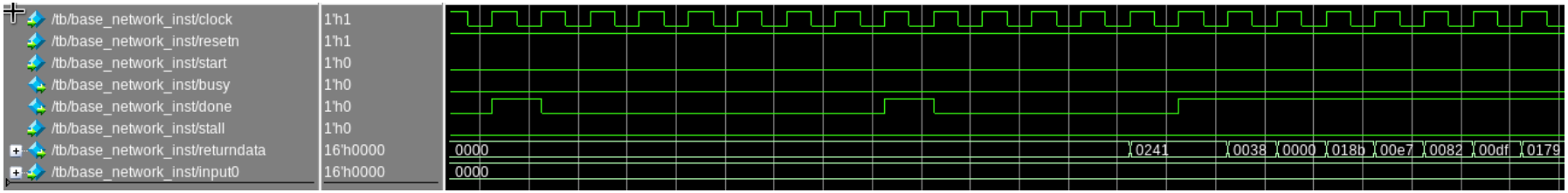
I made a Design fully unrolled to decrease IIx



Phase 2 upgrade: AIDAQ



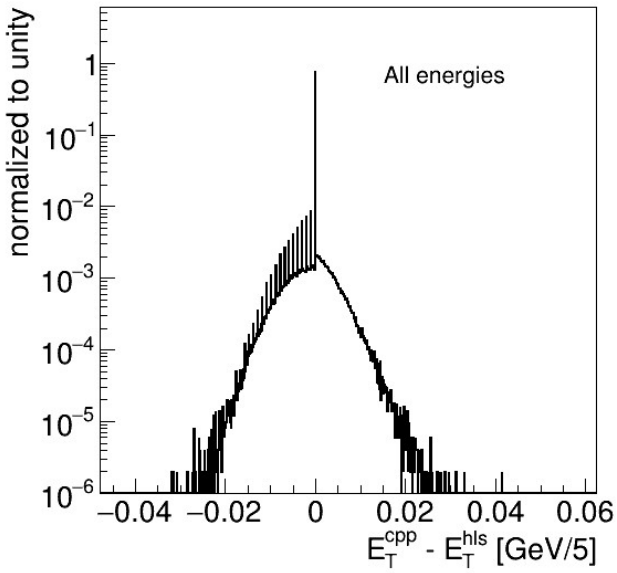
Result (modelsim)



- Test with 10 inputs ->Correct number of output
- outputs are correct
- First 2 value with un-fixed latency
- But after these 2 , fix latency and II at 1 !

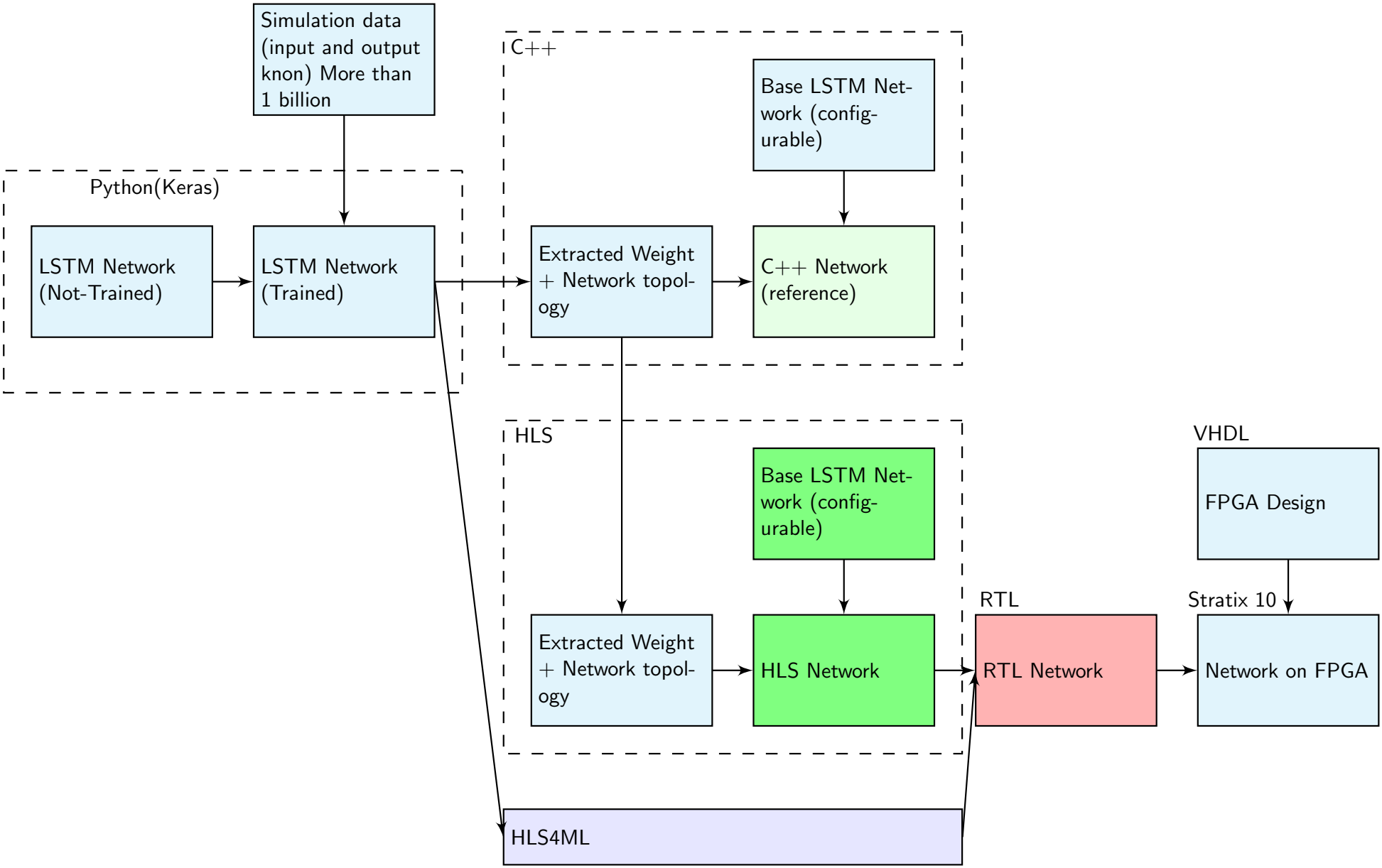
Result

On simulation for 2 billions inputs we compared the output of the "HLS lstm" and the one from our C++ reference.



The differences in output come only from the Look Up table used by nnet::activations. With "real" mathematic it match perfectly

Phase 2 upgrade: AIDAQ



Targeted Device and configuration Used

- Stratix10, 1SG280HU2F50E2VG
- Quartus 20.2 (Migration to 20.3 is ongoing)
- Internal vector size 4
- 10 timestamps
- 10 inputs
- ac_fixed <16,6,true >type

Clock and latency

Clock Frequency Summary

	Quartus Fitter: Clock Frequency (MHz)	Compile Target Frequency (MHz)	Compile Estimated Frequency (MHz)
Clock 1x	TBD(?)	480	480

Verification Statistics

	Invocations	Latency (min,max,avg)	II (min,max,avg)	Details
Spacer	Invocations	Latency (min,max,avg)	II (min,max,avg)	Details
base_network	10	522,534,532.3	1,1,1	Click for details
Explicit component invocations	0	n/a,n/a,n/a	n/a,n/a,n/a	Click for details
Enqueued component invocations	10	522,534,532.3	1,1,1	Click for details

Ressource usage

	ALUTs	FFs	RAMs	MLABs	DSPs	Details
System	62803 (3%)	76796 (2%)	207 (2%)	98 (0%)	186 (3%)	
base_network	62803 (3%)	76796 (2%)	207 (2%)	98 (0%)	186 (3%)	1 compute unit.
Component call	0	0	0	0	0	16b wide with ...
Component return	0	0	0	0	0	16b wide with ...
Variable: - 'inputs' (lstm_cell.cpp:107)	72	288	0	0	0	Register\n9 re...
base_network.B1.start	62731 (3%)	76508 (2%)	207 (2%)	98 (0%)	186 (3%)	

Conclusion

- Devellopment is on-going
- First working lstm is done
- More work to be done to be able to include it in HLS4ML
- Take too much ressources for our use
- Can be reduce with multiplexing.

Questions

Questions ?

RoadMap

We want to devellop a LSTM network for ATLAS and also include LSTM on quartus HLS4ML. For these we need to acheive different steps

- Understand HLS for quartus, LSTMs networks ,HLS4ML : Acheived
- Devellop a LSTM in HLS specific to our application : Acheived
- Use HLS4ML librairies : For now only activation function use it (nnet_activation.h)
- Implement it in FPGA (Stratix 10) : Work in progress
- Move to a fully configurable LSTM with parameters : Work in progress
- Include in HLS4ML : To be done