MICROCHANNEL COOLING

Prospectives FCC
22 juine 2020

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE
CPPM

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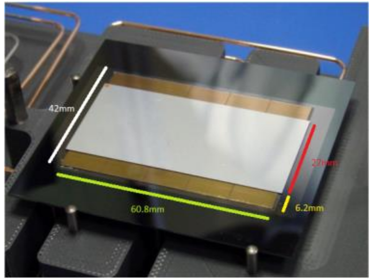
OUTLINE

- ❖ Thermal management problematic for pixel sensor
- ❖ Cooling with Si microchannel
- ❖ Silicon microchannel cooling applications
- ❖ Aida 2020 ongoing developments
- ❖ Silicon microchanel cooling optimization @IN2P3

THERMAL MANAGEMENT PROBLEMATIC FOR PIXEL SENSOR

Future pixel sensors will require more and more cooling



NA62 – GTK sensor

Active elctronic consumption

LHCb : 0.5 W/cm²

LHCb upgrade I (2021) or ITK : ~2 W/cm²

LHCb upgrade II (2034) : ~ 3 - 5 W/cm² (estimation)

Thermal management issues

- Lifespan > 10 years - Availability and reliability : 7/7
- High magnetic field – High radiation

- Material must be minimal
- Sensor T<<0°C
- Coolant T cannot be lowered at will : low TFM

Micro/nano technologies progress

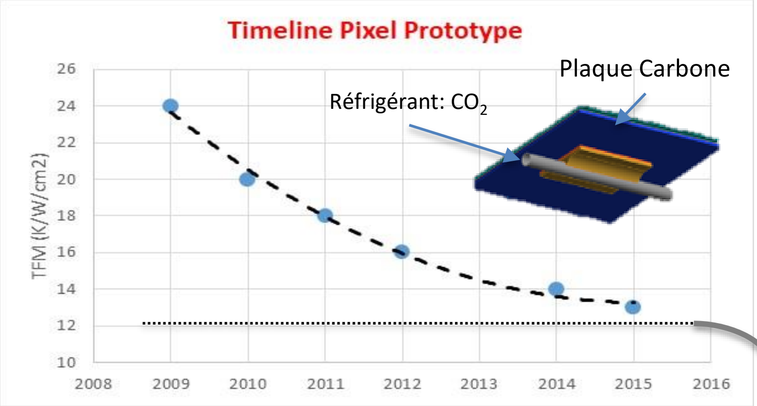
Etching size reduction

Consumption reduction

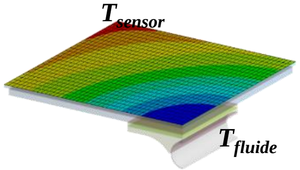
Current Trend

Densification
Time resolved pixel

Consumption increase



TFM for Conductive cooling



$$TFM = \frac{(T_{sensor} - T_{fluide})}{Surface\ power\ density}$$

P= 2W/cm² & T_{fluide} = -35 °C

→ T_{sensor} > - 9°C

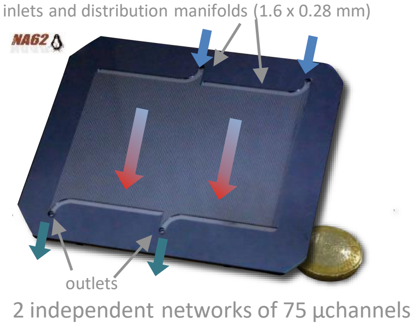
E. Anderssen et al., Advanced Materials and Tools Research, Forum on Tracking Detector Mechanics 2015 (Amsterdam, NL): https://indico.cern.ch/event/363327/contribution/34

COOLING WITH SI MICROCHANNEL

μ-fluidics (microchannel) device as **heat exchanger** for thermal management of heat source

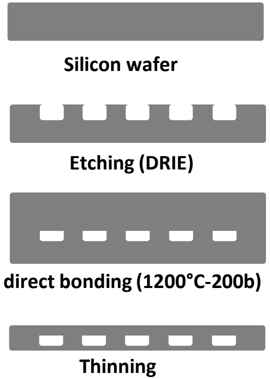
Equivalent Diameter < 1 mm

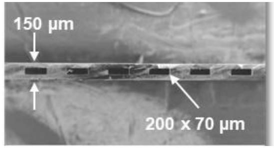
Single or dual (boiling) phase flow

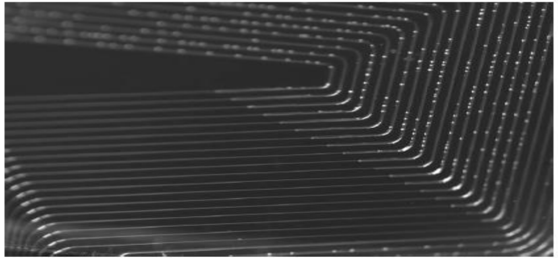


Microchannel on NA62-GTK

Microchannel etched on Si wafer





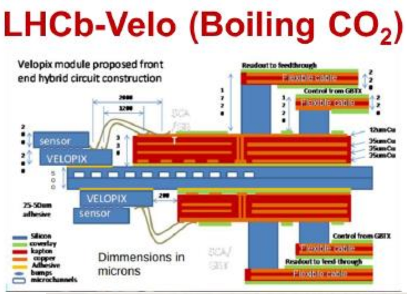


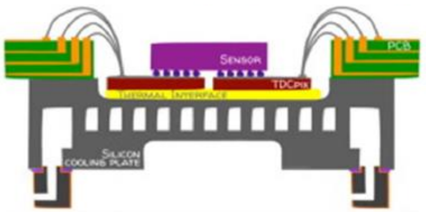
- Locally distributed cooling
- Large thermal exchange surface
- Minimal path of thermal resistances
- Low X_0
- Temperature Homogeneity
- Radiation hard
- Compatible with "HEP fluids"
- No CTE mismatch with Si

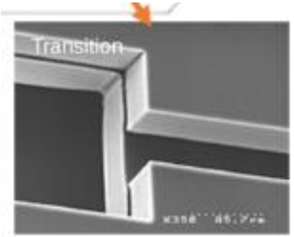
Minimizing TFM (locally distributed cooling, large thermal exchange surface, minimal path of thermal resistances)

Typically TFM for Si cold plate circulating boiling CO_2 is lower than 3 $K.cm^2/W$

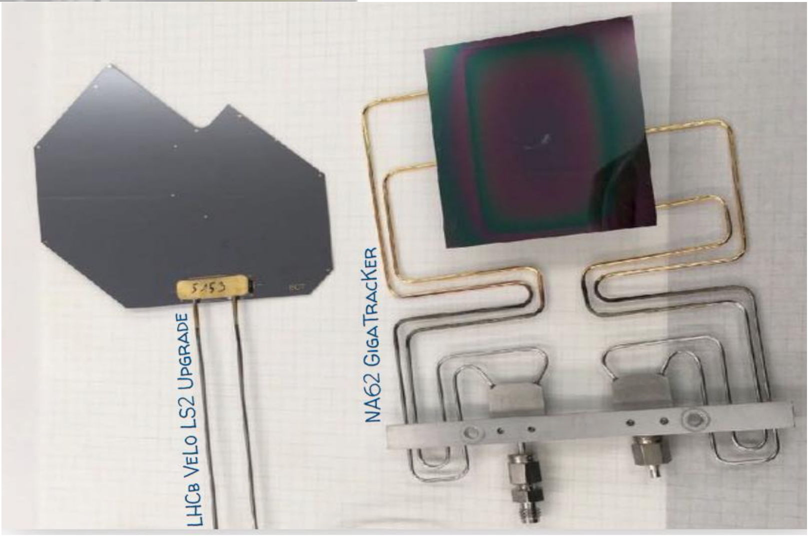
SI MICROCHANNEL COOLING APPLICATIONS





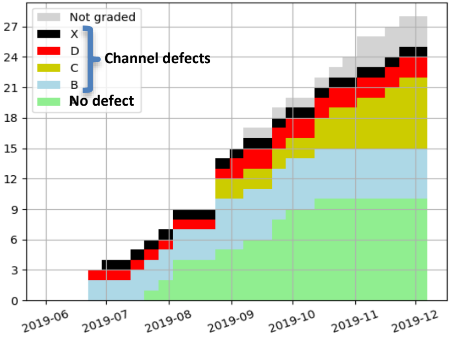


Chanel restriction (LHCb-Velo)



Advantage

- Low TFM (~$3 Kcm^2/W$)
- Minimum material budget: very thin coldplate (250-500µm)
- No CTE mismatch with Si sensor
- Channel failure has little impact on cooling



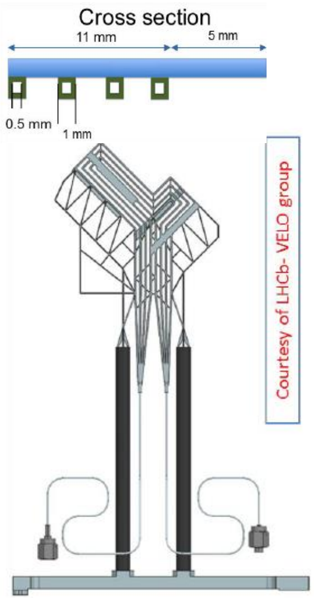
Silicon microchannel production on LHCb

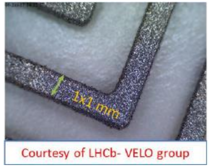
Drawback:

- Expensive process (>120 steps)
- Size limitation
- Few competent subcontactors
- Direct bonding difficult
- Bad prod. Output
- Simulation not enough predictive

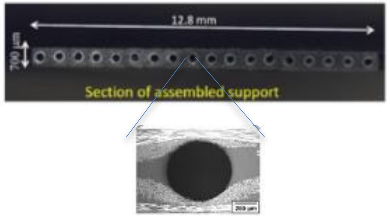
AIDA 2020 ONGOING DEVELOPMENT

Alternative process

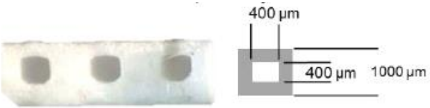




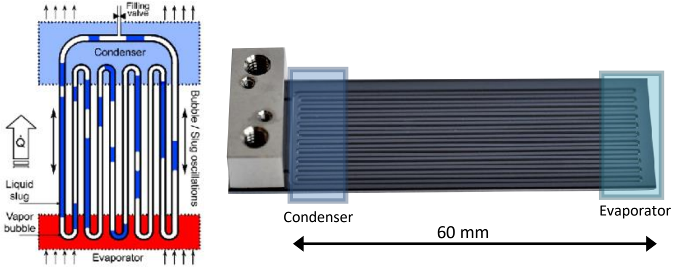
Ti 3D printing
- Low mass
- Cheap
- Easy to integrate



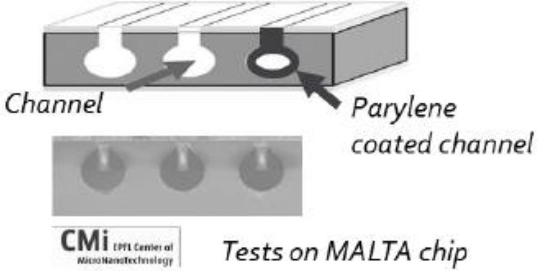
Carbon microvascular
- Ultralight
- Can be very long



Céramic 3D printing
- Lighter than metal
- Flexibility
- CTE compatible



Micro oscillating heat pipe: « caloduc »
- No pump
- Self-contained and self-actuated.
- Eliminate connectors



Microchannel back to sensor
- CMOS Compatible
- Silicon advantage
- No bonding

SILICON MICROCHANEL COOLING OPTIMIZATION @IN2P3

Objectives

- Cost reduction
- Design optimization

→ Kaizen approach instead of technological breakthrough

- Process optimization
  - *Laser etching & cutting*
  - *Direct bonding replaced by anodic bonding coated glass*
- Optimization of the connections
  - *Anodic bonding*
  - *Serialization of cooling plates*

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Inexpensive, flexible and fast process

- Design optimization
  - *Predictive Simulation*
  - *Caraterisation : heat engineering*

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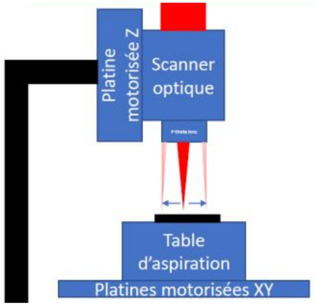
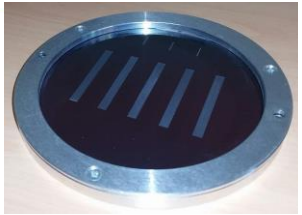
TFM optimization
Material optimization
Fast design

SILICON MICROCHANEL COOLING OPTIMIZATION @CPPM

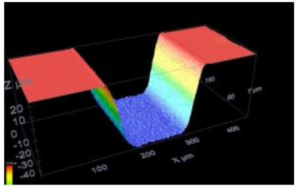
Process optimization :

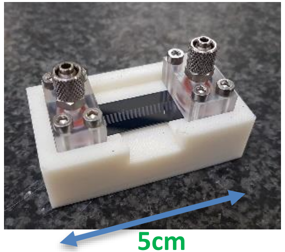
- Laser etching



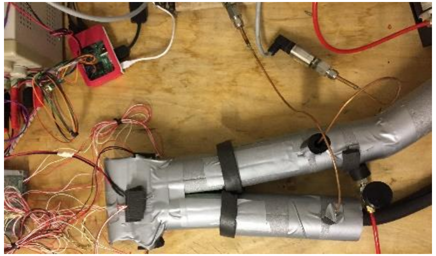


Low cost for a prototype (<1k€)
Fast prototyping and optimization
Adapted to SiC
Complementary to chemical etching



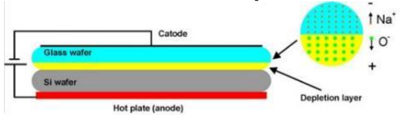


5cm



Tests in progress

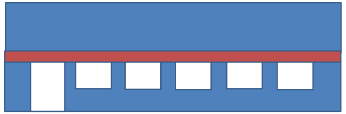
- Anodic bonding Si wafer coated (electron beam) with 5μm of glass



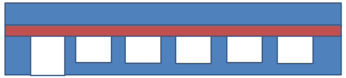
Glass deposition

Thin layer of glass (5μm)

Etching (DRIE)



Anodic Bonding



Thining

4 inch wafer with a thickness of 500 μm

Low cost (<1k€)
Fast production
Mature technology
Bonding can be done at home
Possibility to do complex structure

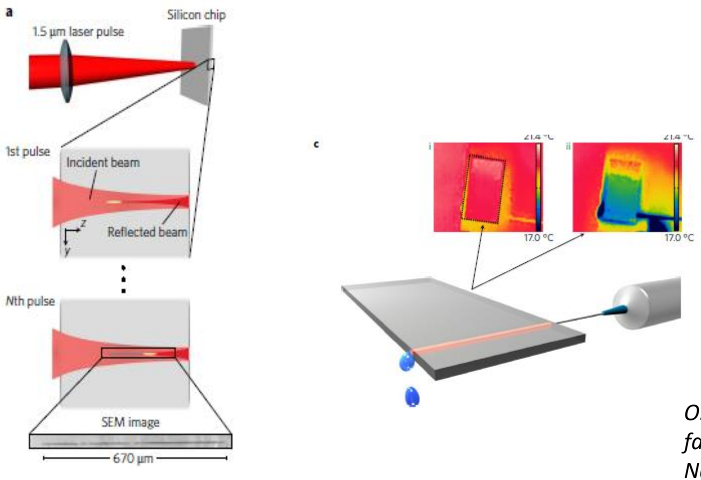
Pressure tests 06/2020

SILICON MICROCHANEL COOLING OPTIMIZATION @CPPM

Process optimization possibilties:

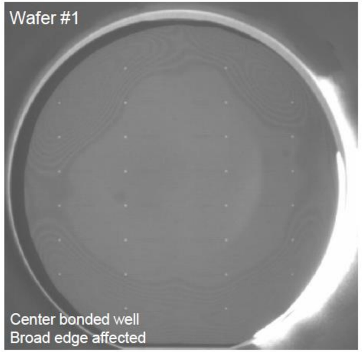
- Anodic bonding of connector on cooling plate → **Cost & time saving**
- Anodic bonding of sensor/electronic on cooling plate → **Time & material saving**
- In chip 3D etching

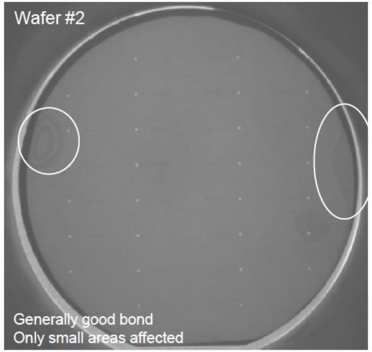
Thesis in co-tutuelle?

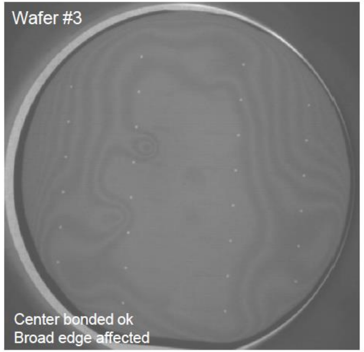


O. Tokel & Al - In-chip microstructures and photonic devices fabricated by nonlinear laser lithography deep inside silicon Nat. Photon. VOL 11 | OCTOBER 2017 | 639–645 |

ANODIC BONDING RESULT @CPPM







Anodic bonding @ FEMTO_ST: bonding default

Wafer 5 after thining

Cooperation with FEMTO_ST to investigate bonding pb?

CONCLUSIONS

- **Strong interest in microchannel cooling for tracker detectors :**
  - NA62 GTK wishes to use microchannels by anodic bonding in 2021.
  - R&D for LHCb-upgrade II vertex detector - Contribution to framework TDR in 2021 ?
  - FCC, BELLE, AIDA++ …
- **We can play a major role in the development of microchannel if we intensify our efforts**
- **Complementary skills on :**
  - LAPP: simulation, tests
  - CPPM: process
  - LPNHE: connectors, tests
- **Industrial transfer potential (computers, biology, space, microreactors, etc.)**