RD53A Module Testing Document

v0.2

Abstract

This document describes quality control (QC) testing procedures of fully assembled RD53A triplet and quad modules, with focus on electrical lab testing and test setups.

Prepared by	*Checked by*	*Approved by*
Lingxin Meng		

Distribution List

History of Changes

Rev. No.	*Date*	*Pages*	*Description of changes*
Draft	5th November 2019	All	Draft on CDS
0.1	17 February 2020	All	Moved to LaTeX
0.2	8 April 2020	All	Handling, storage and shipping, production flow, WB protection, thermal cycling, SLDO procedure, add equipment (PSU, DAQ PC, monitoring, interlock)

Contents

1 Introduction

The document describes quality control (QC) test during pixel module production. A list of tests are given at each stage and a brief description of what to look for specific to that stage. The detailed procedure of recurring tests is in Section 5. Additional tests for quality assurance (QA) and design verification (DV) are given in Section 6 and Section 7, respectively.

2 Related Documents

- Technical Specification for ITk Pixel Modules (AT2-IP-ES-0009) [1]
- Technical Specification and Acceptance Criteria for the Bump Bonding of the ITk pixel modules (AT2-IP-EP-0003) [2]
- Technical Specification and Acceptance Criteria for 3D Sensors for the ATLAS Pixel Tracker Upgrade (AT2-IP-EP-0002) [3]
- Technical Specification and Acceptance Criteria for the Planar Pixel Sensors for the ITK project (AT2-IP-EP-0006) [4]
- RD53A Manual (CERN-RD53-PUB-17-001) [5]
- Assembly docment (AT2-XX-XX-XXXX) [6]
- Parylene coating procedure (AT2-XX-XX-XXXX) [7]
- Shipping requirements (AT2-XX-XX-XXXX)

3 Conventions

FE or chip: frontend ASIC

Bare (pixel) module: flip-chipped sensor-FE-assembly

Module PCB or flex, hybrid: flexible or rigid PCB; populated or loaded with electrical components but no bare module

(Dressed) Module: assembly of bare module and populated flex with electrical connections

Cell: thermal pyrolytic graphite (TPG) tile with aluminium graphite socket in Outer Barrel

Loaded module: dressed module glued on local support

3.1 Temperature Definition

Reference to [3], temperatures to be verified with local support.

Temperature throughout this document refers to what is measured on the module negative temperature coefficient (NTC), according to the QC section of the Module Specs ([1]). However, as the temperature varies largely depending on the chip activity, this temperature is limited to the condition in which the chip is powered and successfully configured (e.g. after a digital scan), with the sensor on the operational bias voltage. The temperature stability at this condition should be within $\pm 1\,^{\circ}\mathrm{C}$.

It's nearly impossible to define testing temperatures that are comparable with the temperatures later in the loading stage due to different methods and areas of cooling, margins in assembly, large temperature gradient across the module and position of the NTC on the module PCB. On local support level, the modules are going to be tested at one high temperature, one low temperature (operation temperature) and maybe an intermediate one.

The low temperature is given by the operation temperature with CO2 at $-40\,^{\circ}\mathrm{C}$ and a detector cooling target at $-35\,^{\circ}\mathrm{C}$ [8]. Simulations [9] have shown an average of $-17\,^{\circ}\mathrm{C}$ on planar and $-27\,^{\circ}\mathrm{C}$ on 3D sensors. Taking into account some temperature gradient between the silicon and NTC, assuming similar to [10], this would give us a testing temperature of

- $-15\,^{\circ}\mathrm{C}$ for planar and
- $-25\,^{\circ}\mathrm{C}$ for 3D.

The high temperature for measurements on local support is defined by the temperature of the CO2 which should be above the dew point of the air in the lab, say $15\,^{\circ}\mathrm{C}$. The testing temperature then can be estimated to

- $30\,^{\circ}\mathrm{C}$ for planar and
- $20\,^{\circ}\mathrm{C}$ for 3D.

One intermediate temperature can be added for planar, which would be $20\,^{\circ}\mathrm{C}$, since measurement in the sensor specification documents [3, 4] are given at this temperature. This would correspond to a CO2 temperature at about $0\,^{\circ}\mathrm{C}$.

However, to test the power-on behaviour of the FE at the operation temperature of the CO2, test setups should be able to cool down to $-35\,^{\circ}\mathrm{C}$, measured on the module NTC.

For the overview, here is a summary table of the testing temperatures. In case of the SLDO test, the temperature refers exceptionally to unpowered modules.

	SLDO (°C)	Low Temp. (°C)	Interm. Temp. (°C)	High Temp. (°C)
Planar	−35	−15	20	30
3D	−35	−25	-	20

Table 1: Table of suggested testing temperatures.

4 Production and Assembly Flow

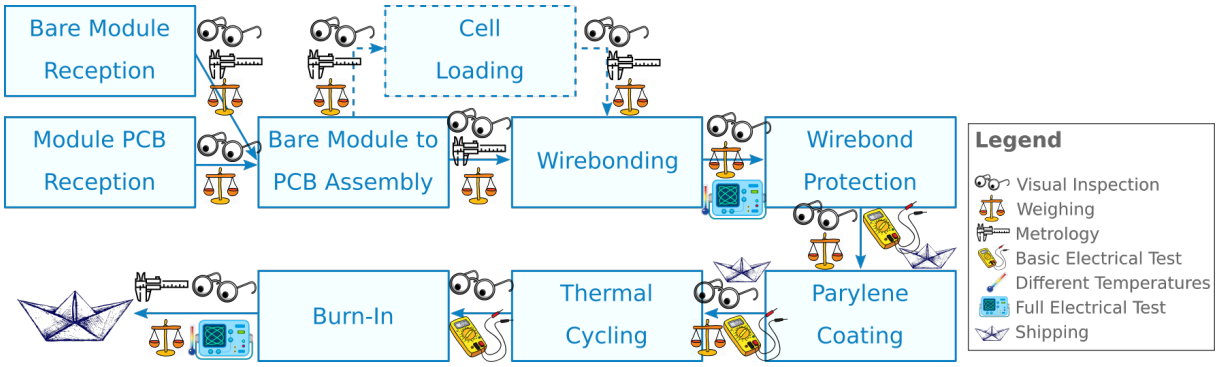

Figure 1: Production flow.

The module production flow, including tests along it is shown in the schematic above. It starts with the reception of bare modules and loaded module printed circuit boards (PCBs). Both should have passed QC in their previous stage. Until after wirebonding, no electrical testing can be done (except for the bare single modules for triplets). Therefore, it is important to perform a full electrical characterisation right after wirebonding at low and high temperatures, to ensure the wirebond quality and the correct I_{ref} setting. A second full electrical characterisation at different temperatures is performed at the end of module production, before the shipment to the loading sites. Between other steps, basic electrical tests shall be performed to check that the module is still functional.

4.1 Module Handling

([1] 1.17) The front-end chip (FE) chip is an electrostatic sensitive device and must be handled properly to avoid damage from electrostatic discharge (ESD). The international standard IEC 60747-1, chapter IX must be followed. The working environment, including tools, materials and containers for handling and transport of modules should provide for ESD protection (refer to IEC 61340-5-1 and IEC 61340-5-2). All operators dealing with the items must be grounded to same potential as the equipment with at least the use of grounding wrist straps. To avoid damage from particulates bare modules, module PCBs and assembled modules must always be handled in a clean room environment with a particle count corresponding to at least class 10000 (ISO 7), or better, using properly

designed tools and materials to prevent touching with bare hands and applying excessive pressure. Use of special tweezers or ESD dedicated vacuum pick up tools for picking up the parts are required. If modules are to be transported between cleanrooms, a suitable carrier should be used, and the container should remain closed during transportation. The container should be externally cleaned on re-entering the cleanroom.

add transport specs

4.2 Reception of Bare Components, Assembly and Wirebonding

Reception tests of bare module (including bare module IV) and bare module PCB, assembly procedure, wirebonding and all tests involved, are covered by the assembly QC in [6].

Wirebonding should follow the schematic given in [6] and [?]. During wirebonding, all wirebonds for the I_{ref} should be set initially according to the wirebonding schematic in [?]. According to on the wafer probing data, corresponding wirebonds should then be pulled to acquire the best value to 4 µA. Systematics on behaviour in cold environment have to be collected with SCC modules.

exact procedure here or in assembly doc?

At this stage, the first full electrical test has to be performed with all routed lanes (4/FE for triplets and 3/FE for quads) and with maximum readout speed (640 Mbit/s or 1.28 Gbit/s), which includes tests at warm and cold temperatures. The cold test is especially important to test for SLDO start-up behaviour. In addition, I_{ref} should be measured cold. If necessary, any wirebonds can be corrected at this stage.

4.3 Attach to Module Carrier

After wirebonding, the module will be placed on a module carrier for testing and further processes, according to instructions given in [11].

procedure and orientation

4.3.1 Attachment of the Data Pigtail

Attach the data pigtail into the Molex connector according to [12] page 11–17 or use the appropriate tooling (under development) [13].

4.3.2 Attachment of the Power Pigtail

TBD

4.4 Wirebond Protection

Reference to wirebond protection document [14]

4.5 Parylene Coating

4.5.1 Masking for Parylene Coating

Due to the complex and fragile components of the pixel module, the masking for Parylene coating will need to be done by ourselves before sending to the coating vendor. The full procedure of masking and unmasking is described in the masking document in [7].

4.5.2 Package for Shipment

Follow Section 4.8.

4.5.3 Reception Test on Testing Sites

Upon returning of the Parylene coated modules to the testing sites, the package should be visually inspected immediately. The content should be unpacked within a week and a reception test should be performed.

4.5.4 QC

Visual Inspection: Should be performed before and after removing of the masking to check the uniformity and if the removal process damaged anything. After removing the masking, check the electrical contacts for any possible coating material.

Weighing: After removing the masking, weigh the module to determin the amount of Parylene coated.

Basic electrical testing: Do a basic electrical test to ensure that all electrical contacts are fully functional. This is the last electrical testing before thermal cycling, therefore it's necessary here to check for disconnected bumps (scan included in basic electrical tests), maybe source scan necessary.

4.6 Thermal Cycling

Estimated duration: 10 h

According to [15] our modules would face about 100 temperature cycles down to $-45\,^{\circ}\mathrm{C}$ and in worst case 1 cycle down to $-55\,^{\circ}\mathrm{C}$. Therefore the thermal cycling procedure is adapted as below.

4.6.1 Procedure

In order to easily achieve the necessary low temperature, the module shall not be powered during this test. Each module has to go through

- 10 cycles from −45 °C to +40 °C
- and 1 cycle from −55 °C to +60 °C.

Ramp rate shall not be faster than 15 °C/minute [16], humidity low enough that the dew point $T_{\mathrm{DP}} \leq T_{\mathrm{module}} - 10\,^{\circ}\mathrm{C}$.

4.6.2 QC

Visual Inspection to look for any condensation, corrosion, cracks or delamination on any material. Basic electrical tests (includes bump bonds check, scan or source)

Pass criteria ([1] 11.20): max bump bond failures increase of <0.01% (75 pix/RD53A chip) . Sensor current change by <10% to previous (before thermal cycling under the same condition).

4.7 Burn-In

Duration: 48 h

4.7.1 Procedure

Stability test to be conducted cold, should be done with operational FE running noise scan continuously. The previous testing time spent per module may be taken into account in the 48 h.

4.7.2 Requirements

Interlock, remote control of equipment, remote monitoring of environment, define environment: temperature, humidity, interlock requirements, interlock procedure

4.7.3 QC

Visual Inspection: last visual verification, corrosion of electrical contacts, dirt, scratches

Metrology as final sign-off that module is within the envelope, planarity of the whole module, alignment of bare module on flex

Final Full Electrical Test that can be integrated into the burn-in process at its end.

4.7.4 Pass Criteria

Sensor current stability in time better than 20% (48 h burn-in). All component specs within tolerances described above Fully functional

Module dimensions within the envelope and specifications. From [1] 11.14, 11.15.

Metrology: Planarity ±12.5 µm at room temperature

4.8 Packaging and Shipping

From [1] 8: The modules will be loaded into transport boxes for shipment. Shipment takes place between assembly and test, test and Parylene coating, and test and local support loading institutes. The requirements for the module transport boxes are the combination of the ASTM D4169-DC18 and MIL-STD-2073-1E (standard practice for military packaging) and MIL-STD-3010 (test procedures for packing materials). The standards cover the tests to qualify the shipping boxes and the reference ??? (PSD) to apply to simulate the transport load. The designer should apply the PSD to the part to confirm acceptance.

Acceptance criteria are:

- Maximum stress level must be less than 1/10 of the yield.
- Minimum clearances must be respected while the excitation is active.
- Experimental data should be obtained using mechanical and active components.

4.8.0.1 Packaging Preliminary!

The module should be packed in its carrier frame with top and bottom covers in an antistatic bag containing moisture absorbers (Silica gel, e.g. small 2 g pack) and an non-reversible humidity indicator. The moisture absorber and humidity indicator have to be fixed (taped) onto the module carrier to prevent any movement during transport. The bag should be flushed with dry air or vacuum sealed.

The bagged modules are placed into a well padded shipping box (e.g. Pelicases). A temperature logger (e.g. Mini Temperature Datalogger) should be placed inside the shipping box in a representative position, while an impact/shock logger (e.g. Extech VB300 Vibration Data Logger) should be placed on the outside of the shipping packaging.

4.9 Storage

([1] 1.17) At all times, bare modules, module PCBs and assembled modules should be stored in clean containers in a controlled inert (dry air or nitrogen) environment, with temperature: 18 °C to 24 °C, RH between 0% and 30%, and particle count corresponding to ISO Class 7.

Modules can be stored in membrane boxes or in custom-made module handling and shipping tools. After the module is coated with Parylene and mounted into a custom-made test box the module can be stored in an environment with a particle count corresponding to ISO Class 9.

5 QC Tests

Section 5.1, section 5.2 and section 5.3 should be covered by the assembly QC in [6].

Reception tests have to be performed immediately to check for damage, especially occured during the transport process. The minimum requirement are visual inspections of the packaging and of the components, which have to be performed within a week of receiving the components.

5.1 Visual Inspection of Packaging

Immediate inspection of the packaging for any anomalies and damage, which have to be documented with photographs and commented/uploaded onto the database (shipping category). After carefully opening the package: evaluation of any data logger (temperature, humidity, impact/shock), check for anti-static packaging, padding, moisture absorber. Check the packaging of each (batch of?) bare module for the proper closure, fixation of the module inside. Document the state.

5.2 Visual Inspection

Average duration:

Visual inspection should be done at the beginning and end of each stage, i.e. assembly, loading into module carrier, wirebonding, wirebond protection, coating, cell loading, thermal cycling and burn-in. This should be done in two steps:

- Computer-aided comparison with the image of the previous stage, requires a high-resolution (defined in equipment) camera that captures the whole module. For a better comparability, the picture of each module has to be taken from the same angle with the same lighting conditions. Therefore, an identical alignment is needed. The comparison can be done using e.g. OpenCV with a custom software script. Potential damage/anomalies should be highlighted and commented. Each usable picture will be uploaded into the database for later comparison.

- Detailed microscope inspection by humans at different lighting and angles. Problematic sections of the module should be photographed with high resolution. Look for details that are not obvious, e.g. loose wirebonds, corrosions, excess encapsulant. Sometimes other means might be needed, e.g. use dry air to check loose wirebonds or to blow away debris. Any anomalies should be documented and marked. All pictures should be uploaded onto the database for later comparison.

5.2.1 Procedure

See assembly QC document [6]

5.3 Metrology

5.4 Full Electrical Tests

Estimated duration: 2 h (without source scan)

All tests are done with the FE powered in SLDO mode (constant current) if not otherwise specified. The tests should be repeated at temperatures defined in Section 3.1. in order to compare the values obtained later in measurements on local support. All tests with planar modules have to be done using the same config for the dedicated temperature (linFE cold: VDDD at 1.3 V and LDAC at 185) while for 3D modules the config still has TBD.

The sensors are reverse biased, the bias voltages and leakage currents given in this document are absolute values. If not otherwise specified, the default bias voltage is the minimum bias voltage required to fully deplete a sensor type, which are 10 V for 3D, 50 V for 100 µm planar and 90 V for 150 µm planar.

5.4.1 Sensor IV

To check for sensor damages and changes in response to the bias voltage, sensor IV is measured. The breakdown is defined when $\mathrm{dI/dV} > 5\,\mu\mathrm{A/\,V}$ in [17].

5.4.1.1 Test Environment The test shall be conducted in a light-tight environment with a relative humidity of <50% ([3, 4]). The dew point should never exceed $T - 10\,^{\circ}\mathrm{C}$. The FE shall not be powered during this test.

5.4.1.2 3D single sensors of 150 µm thickness A 3D triplet module consists of three single bare modules on one module PCB. The module PCB and the common test adapter allow to power each of the single modules separately with high voltage (HV) and low voltage (LV). For a better comparison with IV curves taken before assembly, IV curve of the triplet module should be taken for each single sensor separately.

Typical values at sensor level The typical depletion voltage V_{depl} of n-in-p 3D sensors is smaller than 10 V. The breakdown voltage, defined as the "leakage current increase by a factor of 5 over 1 V" [3], should be higher than 30 V. The values at 20 °C are summarised in the table below.

Item	Typical Value
Full depletion voltage (V_{depl})	< 10 V
Breakdown voltage	> 30 V
Leakage current	$< 2.5\,\mu A/cm^2$ at 30 V
Leakage current slope	$\frac{I(V_{depl}+10\,V)}{I(V_{depl}+9\,V)} < 2$

Table 2: Typical values for 3D sensor IV at 20 °C.

Procedure The leakage current should be measured from 0 to 50 V or breakdown in steps of 1 V with a 10 s delay at each step, and a compliance of 100 µA.

Pass Criteria ([1] 1.22:) The maximum sensor leakage current increase compared to that measured at sensor reception (before flip-chipping) should not be greater than a factor of 2, and with an absolute of less than 5.0 $\mu A/cm^2$, measured at 30 V. The maximum reduction in the breakdown voltage compared to that measured at sensor reception (before flip-chipping) should not exceed 10 V. The absolute breakdown should still be greater than 30 V.

5.4.1.3 Planar sensors of 100 µm and 150 µm thickness

There are triplet modules consisting of single planar bare modules on the coupled rings of the Inner System, the procedure is the same as for the 3D triplets as described above, but the typical values are as following.

Typical values at sensor level The typical depletion voltage V_{depl} of n-in-p planar sensors is smaller than 50 V for 100 µm thin sensors and 90 V for 150 µm thin sensors. The breakdown voltage, defined as "leakage current increase by more than 20% over a voltage step of 5 V" [4], is higher than V_{depl}+70 V, i.e. 120 V for 100 µm and 160 V for 150 µm. The values at 20 °C are summarised in the table below.

Item	Typical Value
Full depletion voltage (V_{depl})	$5\,V < V_{depl} < 50\,V$ (100 µm) $12\,V < V_{depl} < 90\,V$ (150 µm)
Breakdown voltage	> 120 V (100 µm) > 160 V (150 µm)
Leakage current	$<= 0.75\,\mu A/cm^2$ at V_{depl} + 50 V

Table 3: Typical values for planar sensor IV at 20 °C.

Procedure The leakage current should be measured from 0 to 200 V or breakdown in steps of 5 V with 10 s delay between steps, and a compliance of 100 µA.

Pass Criteria ([1] 1.22:) The maximum sensor leakage current increase compared to that measured at sensor reception should not be greater than a factor of 2, thus with an absolute of less than 1.5 $\mu A/cm^2$ measured at V_{depl}+50 V. The maximum reduction in the breakdown voltage compared to that measured at sensor reception should not exceed 50 V. The absolute breakdown should still be greater than V_{depl}+70 V.

5.4.2 SLDO qualification

This is independent from HV. This test should be done first at the high temperature to verify that the bandgaps are functional in general, and then at −35 °C to check how they behave at the low temperature.

5.4.2.1 Procedure

- Set a voltage limit on V_{in} at 1.9 V, please account for power loss in LV cables. Power up the chip at the high temperature by applying 1.1 A/FE (3.3 A for a triplet and 4.4 A for a quad) and measure V_{in}, then measure the VI curve by ramping down the LV PSU at 0.1 A current steps.

Repeat the procedure at −35 °C and measure V_{in}. If the bandgaps start (see pass criteria), repeat this 5 times to eliminate randomness while making sure that the temperature measured on the module NTC has time to recover to −35 °C. If SLDO fails to start at −35 °C, try to increase the temperature in 15 °C steps until the bandgaps start, measure V_{in}.

5.4.2.2 Pass criteria Bandgaps shall start at 1.1 A/FE and V_{in} shall be at nominal value: 1.4 V<= V_{in} <= 1.8 V.

Temperature (°C)	Grade
-35	1
$-35 < T \leq -20$	2
$-20 < T \leq -5$	3
$-5 < T \leq 10$	4
$10 < T$	5

Table 4

All FEs should start within a current window of 0.3 A for the whole module at all test temperatures.

5.4.3 Chip Configuration

First, check writing and reading of global and pixel registers. Then checkout the default configuration for the module under test (should have the following values from wafer probing), check and verify the chip against wafer probing data and the nominal values:

- I_{ref} set to 4 µA (not sure if possible with RD53A module PCB)
- Vref_ADC set to 0.9 V
- VDDA/VDDD set to 1.2 V
- VCAL_MED at 500, compare with wafer probing data
- VCAL_HIGH at 3500, compare with wafer probing data

5.4.3.1 Pass Criteria Everything configurable at high and low temperatures.

Comparison against wafer probing: If the values from wafer probing are within nominal, the reference currents and voltages measured at high temperature shall be within 20% variation of that measured at wafer probing. If not, then the chip should be tuned to the nominal values and the discrepancy noted in the database.

Temperature stability: The difference between the measured reference current and voltages generated by it, i.e. Vref_ADC, VCAL, measured at high and low temperatures, shall agree within 2%. VDDA and VDDD be within 5% [18].

5.4.4 Pixel Failure Test (Tuning)

Tuning is needed for bad pixel analysis. The procedure to be executed with applied HV (30 V for 3D and V_{depl}+50 V for planar, as per [1, 3, 4]). Compare threshold tuning at different temperatures to check for stability over temperature.

5.4.4.1 Procedure Duration: 1 h

Full tuning

- Digital scan
- Analog scan
- Threshold scan before tuning: for comparison of untuned threshold (dispersion) at default setting (chip specific) with trimmed voltages from 4.4.3. Chip Configuration
- Global thres tuning (target 1 ke, linFE tune to 2 ke and retune to 1 ke)
- Pixel tuning (target 1 ke, linFE tune to 2 ke and retune to 1 ke)
- Tot tuning (10 ke@7 ToT)
- Retune pixel, fine tune pixel

- Final threshold scan: gives tunability of pixels, comparison of threshold (dispersion) and noise level ToT scan (@ 10 ke)
- Noise occupancy scan: record number and map of noisy pixels
- Stuck pixel scan
- Crosstalk scan

Minimum threshold tuning (numbers TBC) (to test the injection circuit, since the relation between noise and min thres should be constant, e.g. if noise changes but min thres remains, something wrong in the injection circuit)

- Duplicate the config from the full tuning
- Minimum threshold tuning

5.4.4.2 Pixel Failure Categories (= Pixel Level Cuts [19])

Failure Name	Scan Type	Criteria
Digital Dead	Digital Scan	Occupancy<1% of injections
Digital Bad	Digital Scan	Occupancy<98% or>102% of injections
Merged Bump	Analog Scan	Occupancy<98% or>102% of injections
Crosstalk Scan	High crosstalk Analog Scan	Analog Dead Occupancy<1% of injections
Analog Bad	Analog Scan	Occupancy<98% or>102% of injections
Tuning Failed	Threshold Scan	s-curve fit failed
Tuning Bad	Threshold Scan ToT Scan	$\|ThresholdPixel - ThresholdDistributionMean\| > 5\sigma$ ToT response is 0 or 15 BCs
High ENC	Threshold Scan	$\|NoisePixel - NoiseDistributionMean\| > 3\sigma$
Noisy	Noise Scan	Occupancy> 10^{-6} hits per BC
Disconnected Bump	Disc Bump Scan Source Scan	TBD Occupancy<1% of mean Occupancy
High Crosstalk	Crosstalk Scan (inj to one neighbour)	50x50: Occ>0 with 25 ke injection (sync) 50x50: Occ>0 with 40 ke injection (lin+diff) 25x100: paired: Occ>0 with 2500 e injection (sync) 25x100: paired: Occ>0 with 2500 e injection (lin+diff) 25x100: unpaired: Occ>0 with 15 ke injection (sync) 25x100: unpaired: Occ>0 with 20 ke injection (lin+diff)

Table 5

5.4.5 Bump Bond Quality

5.4.5.1 Procedure

Bare module level and before thermal cycling: x-ray inspection?

- Disconnected bump scan: record number and map of disconnected bumps
- (Source scan with >50hits/pixel, duration estimate example TBD according to source: record number and map of disconnected bumps)

5.4.5.2 Time estimation

Extrapolated from source measurements

- 3.7 GBq Am (LBL) on a single module at 20 kHz with trigger multiplier 16: took 10 h to get ∼34 hits/pixel
  → ∼60 h for a quad for 50 hits/pixel
- 21 MBq Sr90 (CERN) on a single module at 100 kHz with trigger multiplier 16: took 10 minutes to get ∼17 hits/per pixel
  → ∼2 h(or 10 h at 20 kHz) for a quad for 50 hits/pixel

Calculated

- Amptek Mini-X2 X-Ray Tube with Ag anode [20] (cost ∼7k)
- Flux at 30 cm: 1e6/second/mm^2
- Efficiency in silicon (300 µm): ∼5%
- Hit rate on a quad: ∼80 MHz
- With 10 kHz trigger rate and trigger multiplier 16: 100 s needed for 50 hits/pixel, can be improved by decreasing the distance to >5 cm (still quite good uniformity, theoretically)
- BUT x-ray has to penetrate the module PCB

5.4.5.3 Pass Criteria As defined in [1] 1.24 and 1.25 for digital and analog operation, respectively Digital: not worse than wafer probing, however allow up to 5 more dead pixels/chip Analog: noise and min threshold within 10% compared with wafer probing.

Max bond failures <300 per FE (< 0.4% for RD53A), max cluster size 50.

5.4.6 Module Selection

A categorised grading system is under development.

5.5 Basic Electrical Tests

In order to verify if the module is fully functional after each stage, it is sufficient to perform a subset of the full electrical tests at high temperature. Apart from the sensor IV, where the FE should not be powered, the FE shall be powered in SLDO mode for tests that involve DAQ.

- Sensor IV (FE off)
- Register test

- Digital scan
- Analog scan
- Threshold scan
- ToT scan
- Disconnected bumps

6 QA Tests (Preliminary)

6.1 Assembly

To verify the assembly procedure, sensor IV is taken at bare module level and compared with sensor IV taken after assembly and wirebonding. According to [3, 4], the test are conducted in a light-tight environment with a relative humidity of <50% at 20 °C.

For other assembly QA tests refer to [6].

6.2 Parylene Coating

Batch-wise:

For each coating batch a reference material should be coated, so that after the procedure the thickness of the Parylene can be measured with a micrometer with a precision of $\pm 1\,\mu$m. Also have to check for uniformity.

6.3 Electrical Tests

6.3.1 SLDO

Measure V_{in} at each FE by measuring the voltage drop across Rext as a function of the total input current. The current of each FE can be calculated as $I_{\text{in}} = V_{\text{in}} R_{\text{eff}}$, where $slope = R_{\text{eff}} = R_{\text{ext}} k$. Has to rely on the Rext value and the current mirror k measured during wafer probing. Then obtain V_{offs} and $VDD = V_{\text{ref}}/2$ via MUX (probe pad or ADC). Then add 20% in current headroom.

Pass: All FE in one module fully operational within 20% headroom (expert test) at all test temperatures.

6.3.2 Chip Configuration

Wafer probing is not temperature controlled, but the cleanroom is at a controlled room temperature of 20 C. Due to the large thermic volume (thick wafer on an aluminium chuck) on a the chip temperature should be close to 20 C too.

Measure the values at the MUX output and compare to ADC read to verify the ADC calibration.

Cold tests needed:

Find $I_{REF} = 4\,\mu A$. Calibrate ADC LSB at VREF_ADC $= 0.9\,V$. Measure the voltages from Section 5.4.3 at the analog MUX output and compare to ADC read.

During QA find out if and how much these chip values change during the stages, build statistics

7 DV Tests (Preliminary)

7.1 Thermal Cycling

7.1.0.1 Destructive Tests

- For ∼10 modules in total in ITk: Thermal cycling from $-55\,°C$ to $60\,°C$, do basic electrical tests after every 5 cycles, until module not working or disconnected bumps >50%.
- For ∼5 modules in total in ITk: Shock test with dipping in liquid nitrogen, do basic electrical tests after each dip, until module not working or disconnected bumps >50%.

If done, what is the share between the countries/clusters?

8 Test System

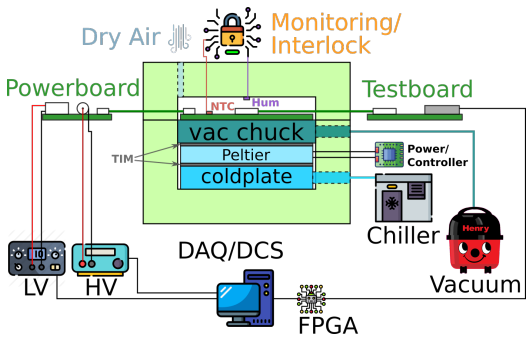

Figure 2: Diagram of an electrical test setup.

For electrical tests, the schematic of a test setup in a laboratory is shown in Fig. 2. The central box is the common development of a cooling unit [21] that is compatible with the common module carrier [11] for one triplet or quad module. The volume within

the foam shells is flushed with dry air. The module, in a carrier, sits on top of a stack consisting of a vacuum chuck, Peltier element and a cold plate. The layers are connected to an external vacuum pump, a control and power element, and a chiller, respectively. The thermal interface between the layers in the stack is ensured by the use of thermal interface material (TIM) sheets.

The test [22, 23] and power adapter boards are connected over flat pigtails to the module on the one side, and to the readout PC or power supply units, respectively, on the other side.

8.1 Scale

Precision down to 0.1 mg.

8.2 Visual Inspection

Preliminary!

- Digital camera with at least 16 Mpix (image of the full module, 1000 pix/cm or 2540 dpi for 4000×4000 pix = 16 Mpix/16 cm^2)
- E.g. Canon EOS R, or Canon EOS M6 Mark II
- Lens: EF 100 mm f/2.8 L Macro IS USM
- Lens adapter
- Tripod or stand for camera
- Remote trigger
- Lightbox or stand for consistent lighting conditions

- Digital microscope with a reslution down to 1 µm (image of module details)
- Capable of recording images
- E.g. Keyence, MicroVu, SmartScope

8.3 PSU

Power supply requirements adapted from [24].

8.3.1 Low Voltage

A LV power supply unit (PSU) is needed to provide the FE chips a constant current to operate in SLDO mode. Each RD53A chip requires 1.1 A, thus results in 3.3 A for a triplet and 4.4 A for a quad, at a voltage of up to 1.9 V. Due to observations of the dependance of the SLDO switch-on behaviour [25], a fast ramp-up time of the PSU is

recommended. Table 6 contains the PSU requirements. Table 10 gives a list of common low voltage power supplies that can be used for RD53A modules, if they are already available in various labs. Planning for ITkPixV1 and a much larger number of modules being tested during production, if new PSUs have to be acquired, it is recommended to use the Rohde&Schwarz HMP4040 (4 individually floating channels).

Delivered voltage	2 V
Delivered current	8 A
Constant current mode	yes
Set voltage precision	0.01 V
Set current precision	1 mA
Set voltage limit	yes
Set current limit	
Measured voltage precision/resolution	0.01 V
Measured current precision/resolution	1 mA
Ramp-up speed	<10 ms (∼800–900 A/s)
Ripple for f<=20 MHz	<20 mVpp
Ripple for f>20 MHz	<1 mVpp
Remote control interface	GPIB/RS232/Ethernet/USB
Multi-channel ground	individual floating

Table 6: LV PSU requirements.

8.3.2 High Voltage

A HV PSU is needed to provide the sensor its bias voltage. Table 7 shows the requirements. Again, available common lab supplies, like Keithley 2410, can be used for RD53A. If a new HV PSU is has to be purchased, which will also be used for production, CAEN DT1415 (8 individually floating channels) suffices all the criteria below.

8.4 DAQ Computer

A data acquisition (DAQ) PC is needed for reading out a module, controlling and monitoring the detector control system (DCS) system. The hardware components of a DAQ computer that has been tested and working is listed in Table 8. The readout software relies on CERN CentOS 7 as an operating system (OS).

8.5 Vacuum Pump

Preliminary!

<100 mbar per vacuum chuck of the common cooling unit.

E.g. KNF Neuberger - N816.1.2KN.18

Output voltage	0–200 V
Output current	0–1 mA
Constant voltage mode	yes
Set voltage precision	0.1 V
Set current precision	5 nA
Set voltage limit	yes
Set current limit	0.1–10 µA
Measured voltage precision/resolution	0.1 V
Measured current precision/resolution	5 nA
DC regulation at load	0.2 V
Programmable ramp	1–50 V/s
Over(under)-voltage trip reaction time	10–1000 ms
Over-current trip reaction time	10 ms
Ripple for f<=20 MHz	<20 mVpp
Ripple for f>20 MHz	<1 mVpp
Emergency ramp-down	100–400 V/s
Multi-channel ground	individual floating
Remote control interface	GPIB/RS232/Ethernet/USB
(Off-mode, if used for SP chain)	low-ohmic <10 Ω (planar) or high ohmic (3D)

Table 7: HV PSU requirements.

Item	Description	(CHF)
CPU	Intel Core i5-8400 2.8 GHz 6-Core Processor	200
CPU cooler	Noctua NH-L9x65 33.84 CFM CPU Cooler	50
Mainboard	Asus PRIME Z370-A II ATX LGA1151	150
Memory	Corsair Vengeance LPX 32 (2x16) GB DDR4-3200	160
Storage	Samsung 970 Evo 500 GB M.2-2280 NVMe SSD	100
Case	Corsair 100R ATX Mid Tower Case	70
Power Supply	Corsair TXM Gold 550 W 80+ Semi-modular ATX	100

Table 8: Exemplary components for a DAQ PC and their estimated prices.

8.6 Cooling

The estimated heat dissipation per RD53A quad module is about 10 W. For testing a module using the common cooling unit that deploys a double-stack Peltier element, the cooling power required per testing unit is estimated to be ∼100 W with a chiller that is capable of provide a temperature of lower than −10 °C.

8.6.1 Peltier Power and Control

For powering and controlling the Peltier element, an efficient way is to use a PSU per Peltier embed the control in software. (under development [26])

8.6.2 Chiller

Requirement for the chiller is the ability to provide ∼100 W cooling power per module at −10 °C.

8.7 Monitoring and Interlock

Monitoring and interlock are interdependent and therefore placed in the same section. Monitoring and a software interlock that shuts down (sub)systems in a controlled way can be implemented in the same unit, while a fail-safe hardware interlock has to be used in addition.

- Environment-related: module overheating, condensation
- Equipment-related: Loss of monitoring
- Power-related: power supply failure, power cut

8.7.1 Monitoring, DCS and Software Interlock

Monitoring has to be done on the test system and the test environment. Monitoring data have logged throughout the course of testing a module and for every module individually. The DCS and monitoring data have to be sampled with an appropriate frequency to reflect changes.

add tables for IV, VI, tuning, thermal cycling, burn-in

The system monitoring includes the voltage and current meausrement of the PSUs powering the sensor and the chip. The specifications thereof can be found in Section 8.3.

Environmental monitoring can be easily done using an Arduino or similar. Each cooling unit should have its own temperature and humidity or dew point measurement. The temperature monitoring must include the NTC on the module PCB and at least an additional temperature sensor for the volume of the cooling unit.

The software interlock can be implemented on the DAQ PC or on an external microcontroller. It should contain an automated error-handling sequence to execute the actions listed below. To prevent the system from undergoing a hard shutdown, the threshold are set more strict than for the hardware interlock.

make a table out of this

- Environment-related:
  - Module overheating
    - Ramp down HV, switch off LV
  - High humidity
    - Switch off cooling

- Loss of monitoring
  - Controlled shutdown of the affected unit
  - Controlled shutdown of the whole system
- Power-related
  - Power supply failure
    - Decouple the affected module
    - Shutdown power supply
  - Power-cut
    - Use a uninterruptable power supply (UPS) as a buffer and controlledly shut down the whole system
    - Make sure the testing system remains off when the power is back on
    - Manual restart required
- Alarm-system: email, text message

8.7.2 Hardware Interlock

The hardware interlock should sit between the UPS and the system to cut off power if the software interlock fails.

Failure mode	Min.	Max.	Action
Module Temperature T_{module}	-	$> +40\,^{\circ}\text{C}$	Switch off HV and LV
Module Temperature T_{module}	$< -55\,^{\circ}\text{C}$	-	Switch off cooling
Dew Point T_{DP}	-	$\geq T_{\text{module}}$	Switch off cooling
Open testbox			Switch off system
Loss of monitoring			Switch off system

Table 9: Hardware interlock.

A PSU

Brand		Rohde&Schwarz (Hameg)	
Model		HMP4040	
No. of channels		4	
Channel			
Delivered voltage	2 V	32 V	
Delivered current	8 A	10 A	
Constant current mode	yes	yes	
Set voltage precision	0.01 V	$<0.05\% + 5\,\mathrm{mV}$	
Set current precision	1 mA	$<0.1\% + 5\,\mathrm{mA}$	
Set voltage limit	yes	yes	
Set current limit	yes	yes	
Measured voltage resolution	0.01 V	1 mV	
Measured voltage precision	0.01 V	$<0.05\% + 5\,\mathrm{mV}$	
Measured current resolution	1 mA	$<1\,\mathrm{A}$: 0.2 mA; $\geq 1\,\mathrm{A}$: 1 mA	
Measured current precision	1 mA	$0.1\% + 2\,\mathrm{mA}$	
Ramp-up speed	$<10\,\mathrm{ms}$ ($\geq 800\,\mathrm{A/s}$)	$<5\,\mathrm{ms}$ ($>2\,\mathrm{kA/s}$)	
Ripple for f$\leq$=20 MHz	<20 mVpp	<1.5 mV rms, <1 mA rms	
Ripple for f$>$20 MHz	<1 mVpp		
Remote control interface	GPIB/RS232/Ethernet/USB		
Multi-channel ground	individual floating	individual floating	
Price estimate (CHF)		1800	
Price/module (CHF)		455	
Can be used for		RD53A, ITkPixV1	

Table 10: LV PSU models.

List of Acronyms

DAQ data acquisition

DCS detector control system

DV design verification

ESD electrostatic discharge

FE front-end chip

NTC negative temperature coefficient

PCB printed circuit board

PSD ???

PSU power supply unit

QA quality assurance

QC quality control

TPG thermal pyrolytic graphite

TIM thermal interface material

References

[1] Technical Specification for ITk Pixel Modules. Technical report, CERN, Geneva, Dec 2019. https://edms.cern.ch/document/2019657/1.

[2] Technical Specification and Acceptance Criteria for the Bump Bonding of the ITk pixel modules. Technical report, CERN, Geneva, Dec 2019. https://edms.cern.ch/document/1817526/1.

[3] Technical Specification and Acceptance Criteria for 3D Sensors for the ATLAS Pixel Tracker Upgrade. Technical Report ATL-COM-UPGRADE-2017-001, CERN, Geneva, Dec 2019. https://edms.cern.ch/document/1817524/1.

[4] Technical Specification and Acceptance Criteria for the Planar Pixel Sensors for the ITK project. Technical Report ATL-COM-UPGRADE-2017-002, CERN, Geneva, Dec 2019. ://edms.cern.ch/document/1817538/1.

[5] Maurice Garcia-Sciveres. The RD53A Integrated Circuit. Technical Report CERN-RD53-PUB-17-001, CERN, Geneva, Oct 2017. ://cds.cern.ch/record/2287593.

[6] Assembly QC. Technical Report xxx, CERN, Geneva, 2020. blank.

[7] Masking Procedure for Parylene Coating. Technical Report xxx, CERN, Geneva, 2020. blank.

[8] Eric Anderssen. QA/QC Temperature. https://indico.cern.ch/event/857601/contributions/3635777.

[9] Diego Alvarez Feito. Local Supports Thermal FEA: Summary of Initial Results. https://indico.cern.ch/event/728934/contributions/3562202.

[10] Master Thesis: Characterization of the joined ATLAS and CMS RD53A Pixel Chip. Feb 2019. https://cds.cern.ch/record/2658031.

[11] Module Carrier. https://twiki.cern.ch/twiki/bin/view/Atlas/ItkPixCoolingUnit.

[12] Product Specification for 0.3mm PITCH FPC CONNECTOR. https://www.molex.com/pdm_docs/ps/PS-502598-002-001.pdf.

[13] Introduction - ITk Common Hybrid Meeting, 27 March, 2020. https://indico.cern.ch/event/903207/contributions/3801310.

[14] Wirebond Protection Document. Technical Report xxx, CERN, Geneva, 2020. blank.

[15] Danilo Giugni. General approach for Thermal Mechanics QA&QC. https://indico.cern.ch/event/860761/contributions/3661710.

[16] Temperature Cycling. Jedec 22-a104e, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, October 2014.

[17] IBL Module Electrical Tests. Technical report, CERN, Geneva, Dec 2019. https://edms.cern.ch/document/1221585/1.

[18] Elodie Resseguie. Update on SLDO Calibration. https://indico.physics.lbl.gov/indico/event/1035/contributions/4478.

[19] ATLAS Pixel IBL: Stave Quality Assurance. Technical Report ATL-INDET-PUB-2014-006, CERN, Geneva, Sep 2014. https://cds.cern.ch/record/1754509.

[20] Mini-X2 X-Ray Tube System for XRF. https://www.amptek.com/products/x-ray-sources/mini-x2-ray-tube.

[21] Module Cooling Unit . https://twiki.cern.ch/twiki/bin/view/Atlas/ItkPixCoolingUnit.

[22] RD53A Triplet Test Adapter. https://gitlab.cern.ch/itk-pixel-hybrid/rd53a_triplet_testboard_japan.

[23] RD53A Quad Test Adapter. https://gitlab.cern.ch/itk-pixel-hybrid/rd53a_testboard_japan.

[24] Requirements for the Power Supply System of the ATLAS ITk Pixel Detector. Technical report, CERN, Geneva, Dec 2019. https://edms.cern.ch/document/2192745/2.

[25] Vasilije Perovic et al. Results with RD53A prototype modules at ETHZ. https://indico.cern.ch/event/829670/contributions/3473445.

[26] Peltier Cooling for Test Modules. https://gitlab.cern.ch/berkeleylab/labremote-apps/peltier-cooling.