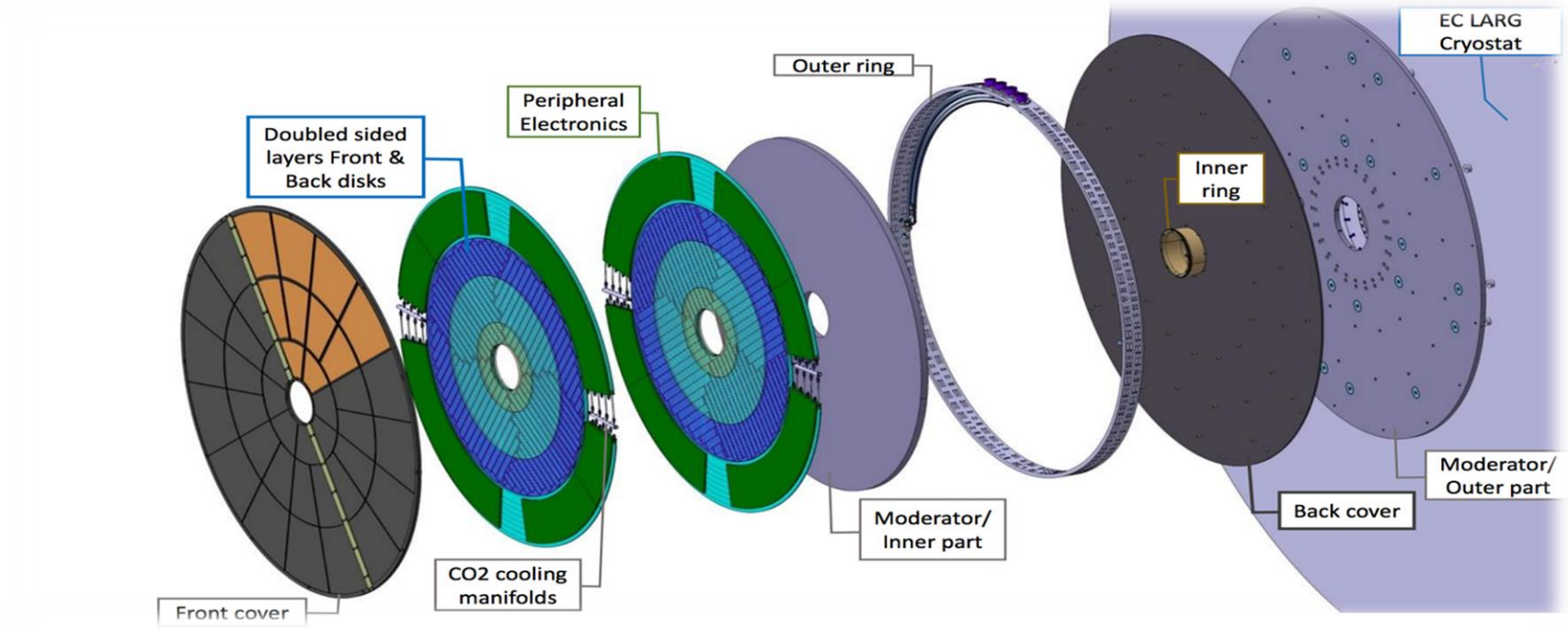
ATLAS Timing Detector Electronics



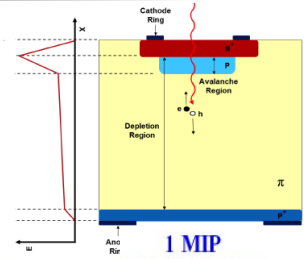
Nathalie Seguin-Moreau on behalf of ATLAS HGTD

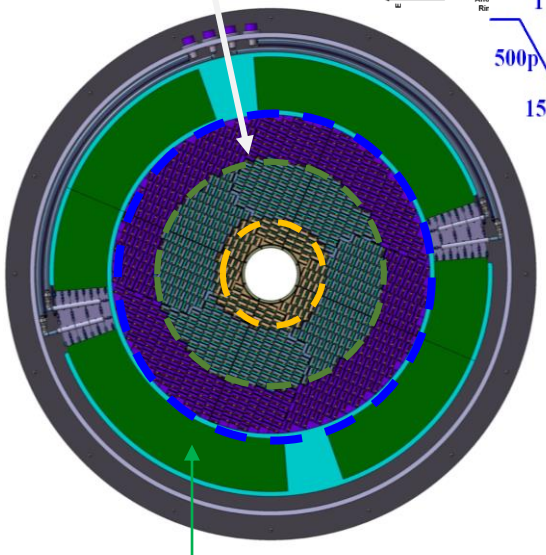
ACES 2020, 27 May 2020

ATLAS HGTD

ATLAS High Granularity Timing Detector in HL-LHC

LGAD sensors
1.3 x 1.3 mm^2
Thickness = 50 µm



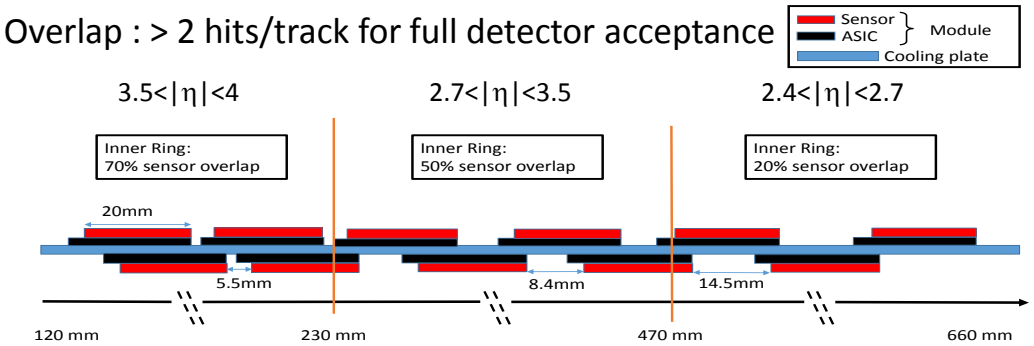


Peripheral Electronics Boards (PEB)

Active area: LGAD sensor (450 PADs of 1.3 x1.3 mm2) bump-bonded onto **2 ASICs (225 channels/ASIC)**
- **Inner ring** : 12 cm< R< 23 cm (3.5 < η < 4.0) replaced each 1000 fb^{-1}
- **Middle ring** : 23 cm< R< 47 cm (2.7 < η < 3.5) replaced at 2000 fb^{-1}
- **Outer ring** : 47 cm< R< 64 cm (2.4 < η < 2.7) never replaced

Rings replacement allows to keep:
- 2.5x10^{15} n_{eq}/cm^2 max (w/SF=1.5) and TID 2 MGy max (w/SF=2.25)
- Charge in irradiated sensor > 4fC

Overlap : > 2 hits/track for full detector acceptance

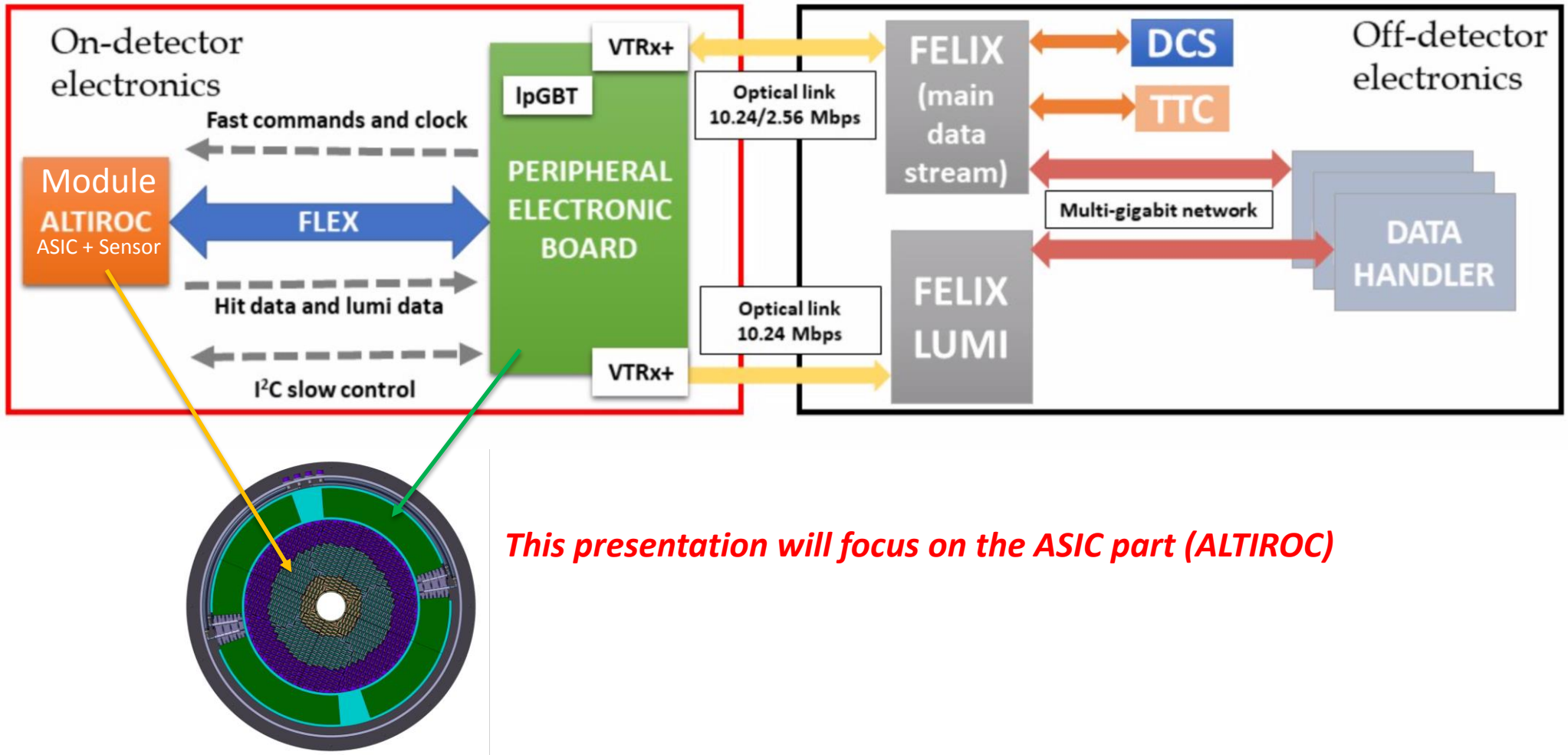


REQUIREMENTS of HGTD DETECTOR

- **Time measurement** for minimum ionizing particle with a **resolution between 30 ps to 50 ps per track over the detector's lifetime**
- **Luminosity measurement**: sum of the hits for each Bunch Crossing

HGTD Electronics: Module – Flex – PEB - DAQ

Data transmission path for hit data, luminosity data, clocks, fast commands, DCS/Slow Controls



This presentation will focus on the ASIC part (ALTIROC)

Requirements for the ASIC

Key requirement: Time resolution per track, combining multiple hits, is 30 ps at the start of lifetime to 50 ps after 4000 fb-1 => Time resolution /hit must be < 35 ps at start and 70 ps at the end of lifetime.

Maximum jitter (σ_{elec})	**25 ps at 10 fC at the start of the HL-LHC and 70 ps for 4 fC at the end**
TDC contribution	**< 10 ps**
Time walk contribution	**< 10 ps**
Clock contribution	**< 15 ps**

TDC conversion time	**< 25 ns**

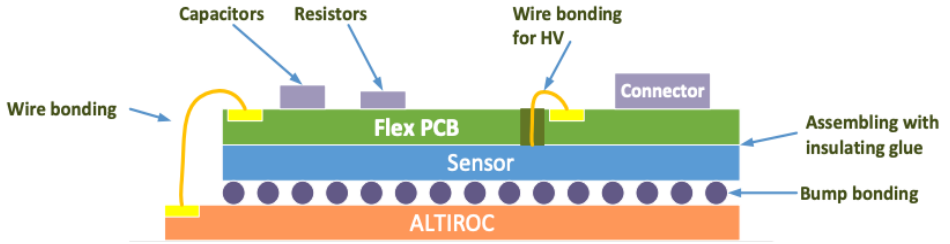
Clock phase adjustment	100 ps

Main contributors to time resolution

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$

with $\sigma_{elec}^2 = \sigma_{Time\ walk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2$

PAD size	1.3 x 1.3 mm^2 x 50 µm => **Cdet = 4 pF**
ASIC size and channels /ASIC	2x2 cm^2 15x15=225 channels/ASIC
Single PAD noise (ENC)	**< 3000 e- or 0.5 fC**
Minimum threshold	**2 fC**
Dynamic range	**4 fC** to 50 fC



TID Tolerance	**2 MGy** (inner modules replaced after each 1000 fb^{-1} , middle ring after 2000 fb^{-1})
Full chip SEU probability	< 5 % / hour

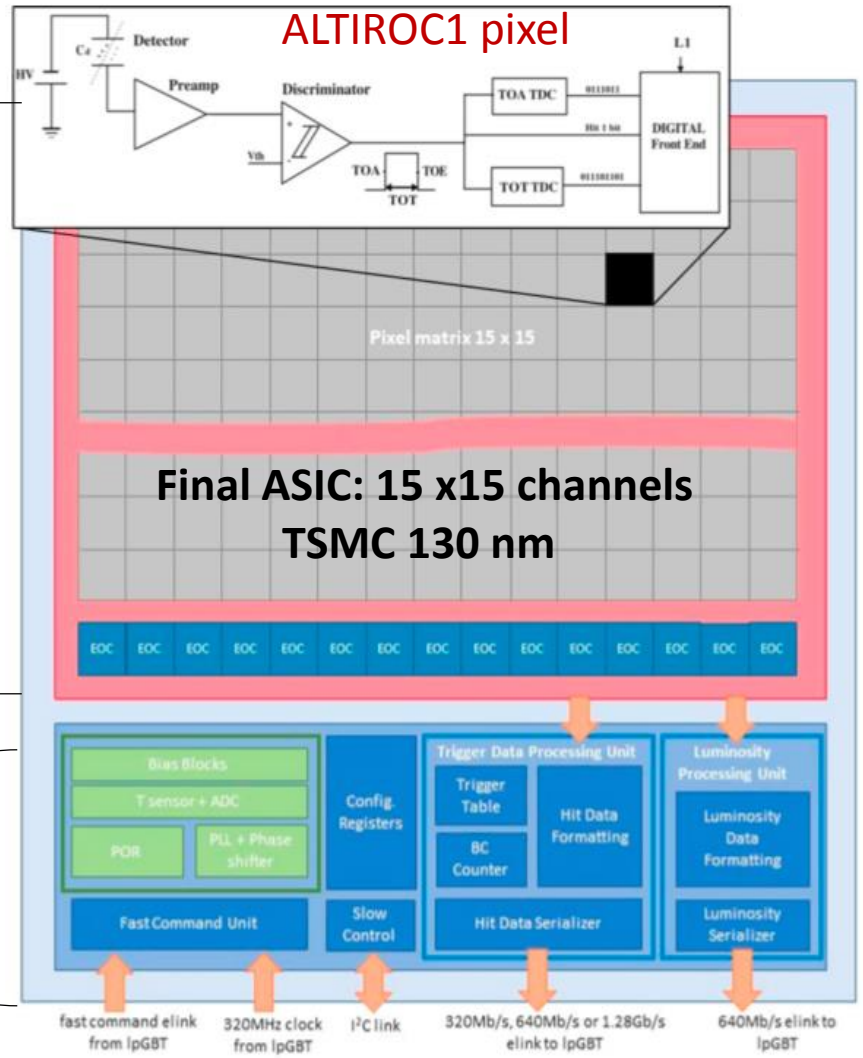
ASIC designed in CMOS 130 nm

Trigger rate (latency)	1 MHz L0 (10 µs) or 0,8 MHz L1 (35 µs)

e-link driver bandwidth	320 Mbit/s, 640 Mbit/s and 1,28 Gbit/s

Voltage and Power dissipation per ASIC	1.2V and 300 mW cm^{-2} => 1.2 W/ASIC (225 ch) or **4.4 mW/channel** and 200 mW for the common part

Front end electronics-ASIC: ALTIROC, analog part



Analog blocks Tested with Altiroc 0/1

Digital blocks Under design

- Main challenge = small jitter (low noise/capacitance) down to 4 fC

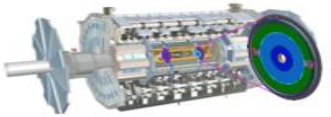
⇒ **Analog FE performance crucial**

$$\sigma_{elec} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

C_d: sensor cap (~4 pF)
t_d: LGAD drift time, 600 ps
Q_{in}: MIP charge (10 fC at start, 4 fC at end)
e_n: noise spectral density of input trans.

⇒ **ALTIROC1 prototypes** (5x5 ch), which integrate

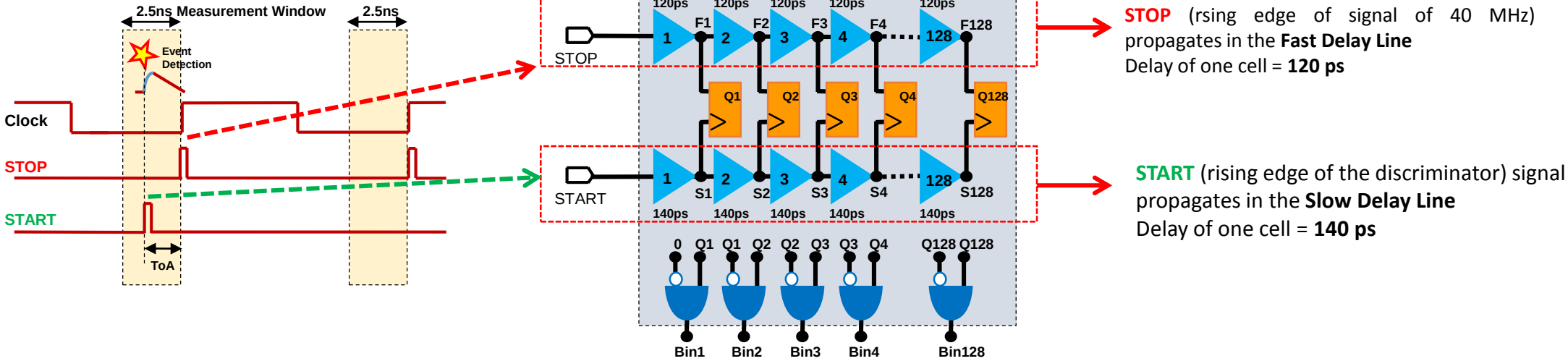
- A voltage **preamplifier** followed by a **discriminator**:
  - Time walk correction made with a Time over Threshold (TOT) architecture
- **Two TDC** (Time to Digital Converter) to provide digital **Hit data** =Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
  - TOA TDC: bin of 20 ps (7 bits), range of 2.5 ns, to be centered on the bunch crossing
  - TOT TDC: bin of 40 ps (9 bits), range of 20 ns
- One local memory (**SRAM**):
  - 17 bits of the time measurement (Hit data) stored until L0/L1 trigger (~ 1 MHz), trigger latency = 10 µs in Altiroc1, will be 35 µs in full size ASIC (Altiroc2)
- *Altiroc1 also integrates a phase shifter as a standalone clock*



TOA TDC Architecture (Simplified): Vernier Delay Line

TOA TDC
- Resolution: 20 ps
- Range: 2.5 ns
- 7 bits

TDC Power consumption 0.4 mA *1.2 V = 0,5 mW @ 10% occupancy



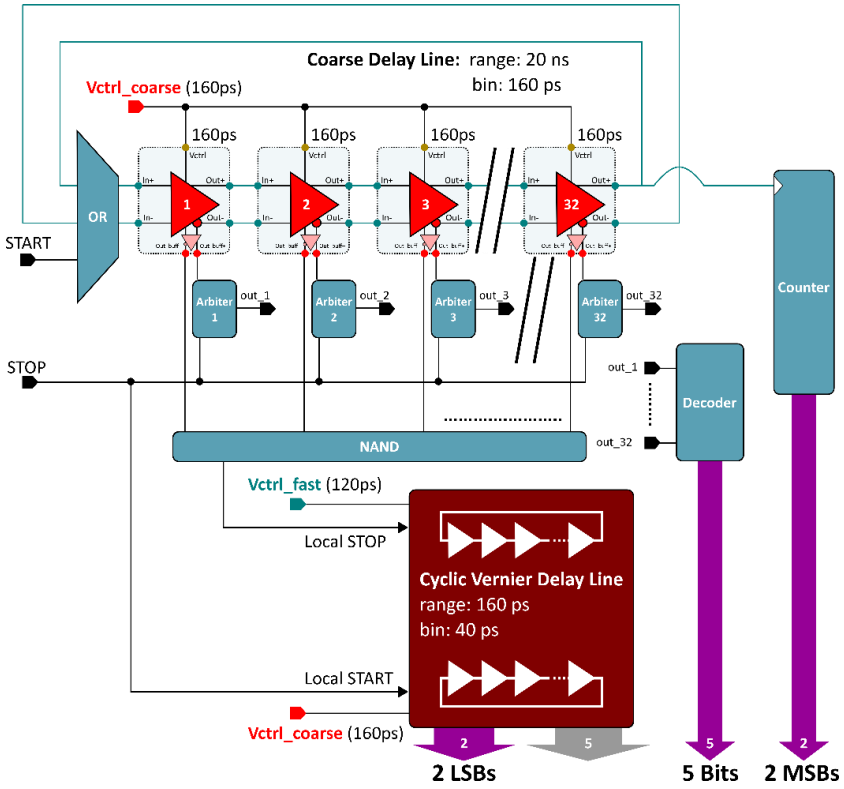
STOP (rsing edge of signal of 40 MHz) propagates in the **Fast Delay Line**
Delay of one cell = **120 ps**

START (rising edge of the discriminator) signal propagates in the **Slow Delay Line**
Delay of one cell = **140 ps**

Differential shunt capacitor voltage-controlled delay cells

- START pulse comes first and initializes the TDC operation. STOP pulse follows the START with a delay that represents the time interval to be digitalized.
- At each tap of the Delay Line, STOP signal catches up to the START signal by the difference of the propagation delays of cells in Slow and Fast branches: i.e. 140ps – 120ps = 20ps (LSB).
- The number of cells necessary for STOP signal to surpass the START signal represents the result of TDC conversion
- Cycling configuration used in order to reduce the total number of Delay Cells.
- TDC range is equal to 128 * 20 ps = 2.56 ns

TDC for TOT measurement



TOT TDC (Altiroc1)

Coarse delay line (LSB_coarse= 160 ps) +
Cyclic Vernier line (LSB_fine= 40 ps)

- LSB = **40 ps**
- Range: **20 ns**, 9 bits

TDC Power consumption:
0.4 mA * 1.2 V = 0.5 mW @ 10% ocupancy

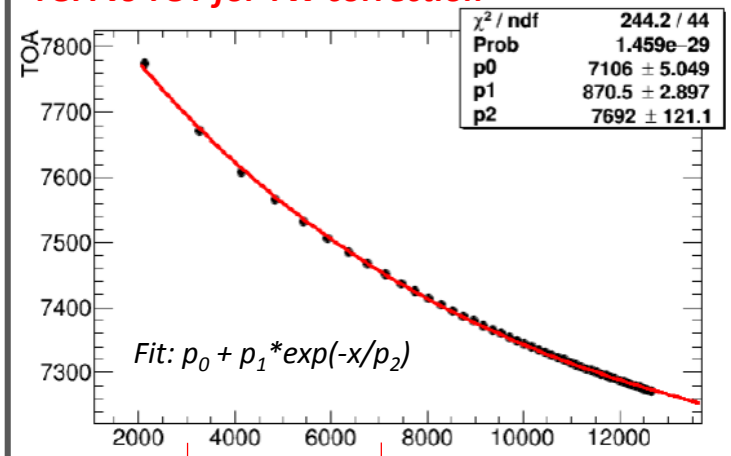
TW correction within ± 5 ps for small charges

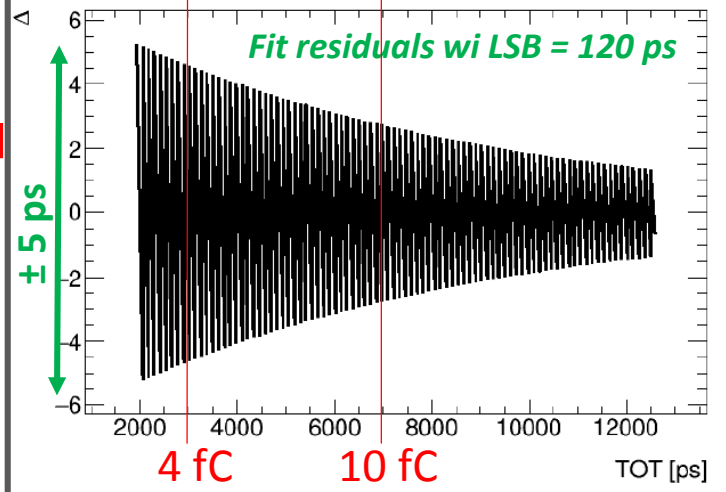
⇒ NEW TOT TDC in Altiroc2

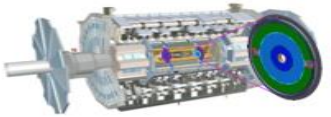
- Coarse part only, fine part removed
- LSB coarse= 120 ps

Simulation using LGAD signal

TOA vs TOT for TW correction

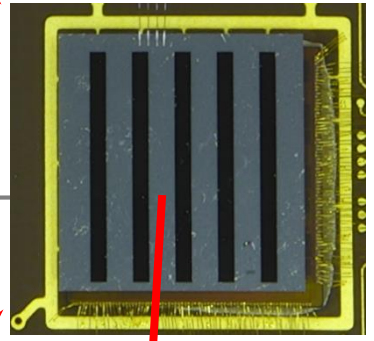






ATLAS HGTD

TESTBENCH

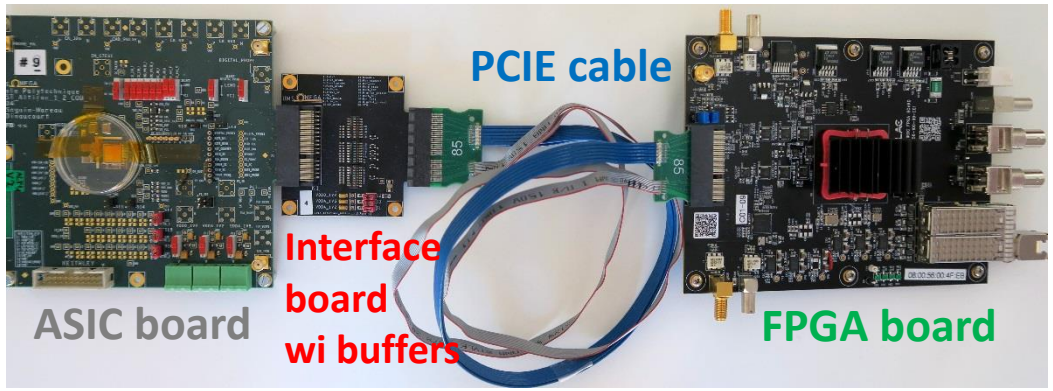


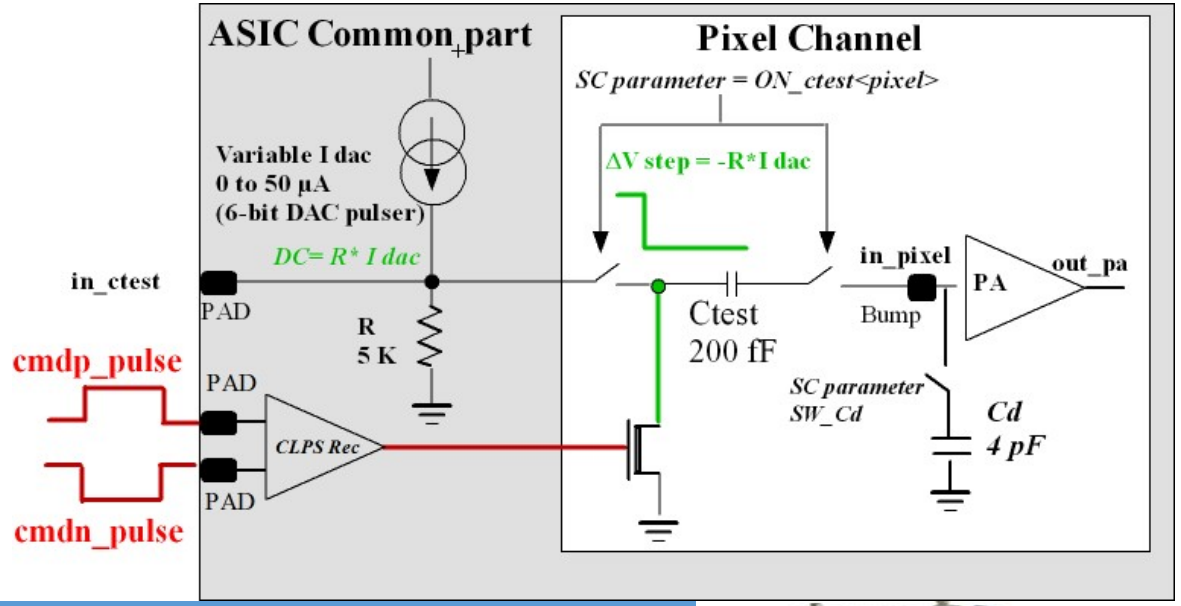
- **ALTIROC1_V1, ALTIROC1_V2**: testbench measurements (ASIC alone or with sensor), irradiation tests, testbeam

- **Setup:** ASIC board (ASIC alone or bump bonded onto sensor) + FPGA board

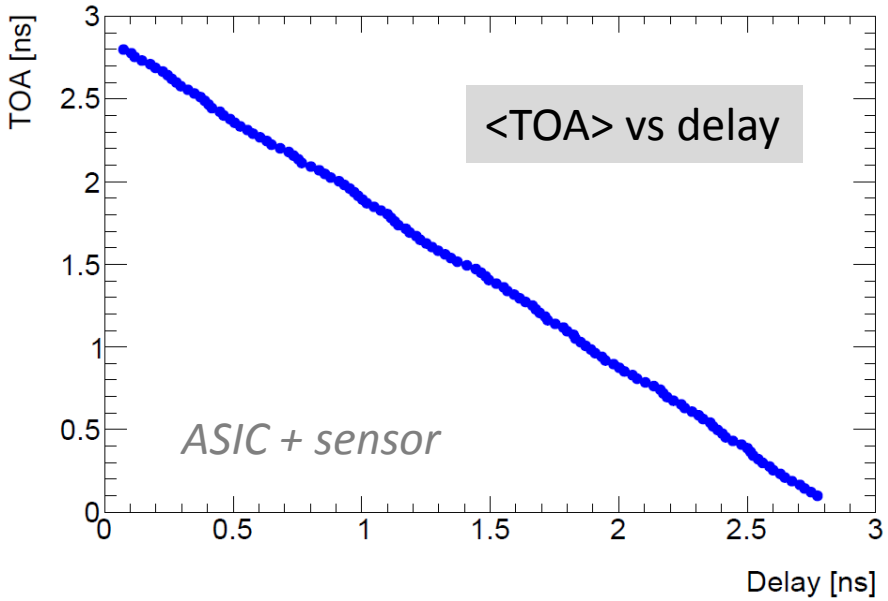
- Charge injection (0 up to 50 fC) using **ASIC internal calibration pulser** controlled by **cmd_pulse** input, generated by the FPGA, synchronous to 40 MHz clock
- ASIC alone: Cd=4 pF can be set by SC to mimic sensor capacitor
- **External trigger,** width and delay tunable by 10 ps steps **:** used to characterize the TOA and TOT TDC alone

- **Tests at system level**: need to add **interface board to filter FPGA signals (3 MHz noise DC DC converters)** => Vth could be set < 2fC

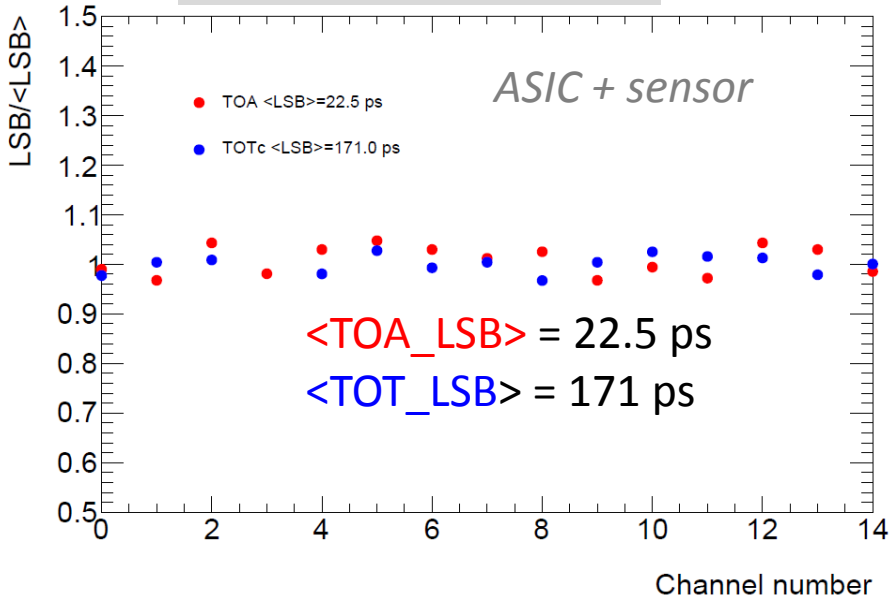


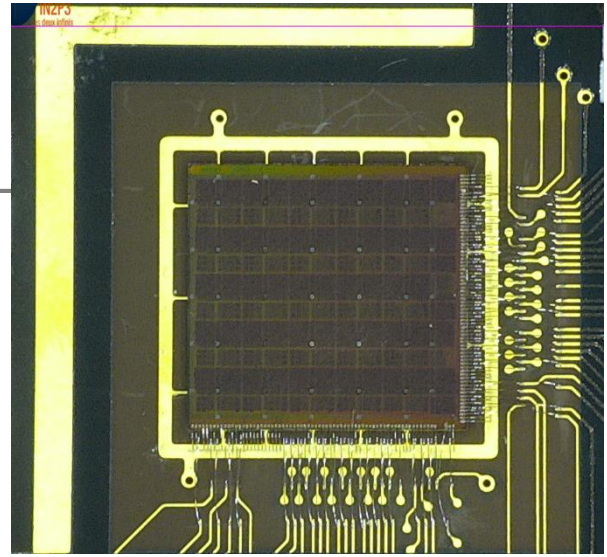


ALTIROC1_V2- TDC performance



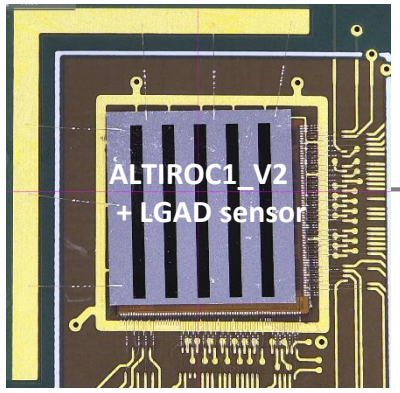
LSB /<LSB> vs channel





ALTIROC1_V2
(5 × 5 channels)

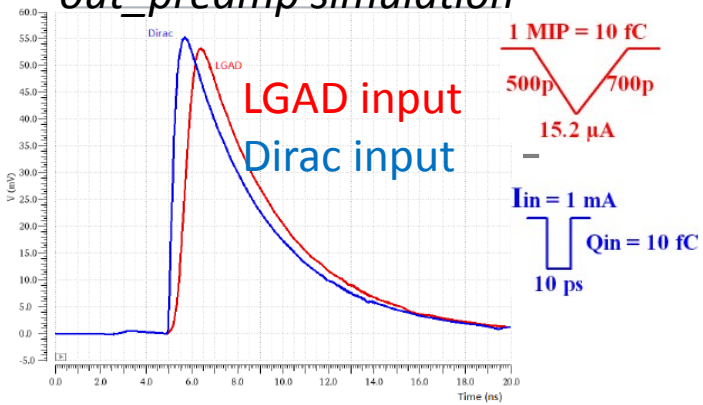
- <TOA> vs delay: Small discontinuities due to LSB bin size (can be calibrated with Random Programmable Generator)
- TOA_LSB and TOT_LSB can be adjusted to 20 ps and 160 ps per channel using Slow Control parameters

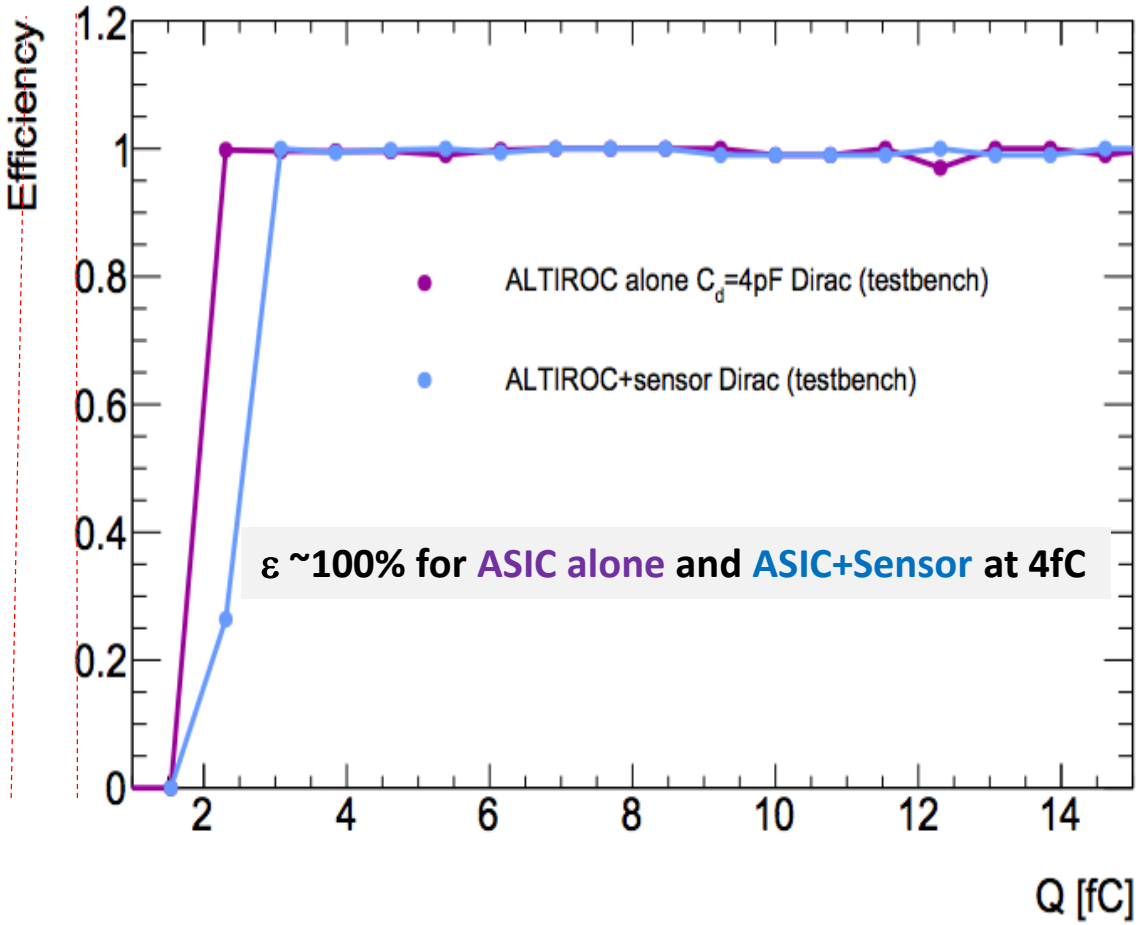


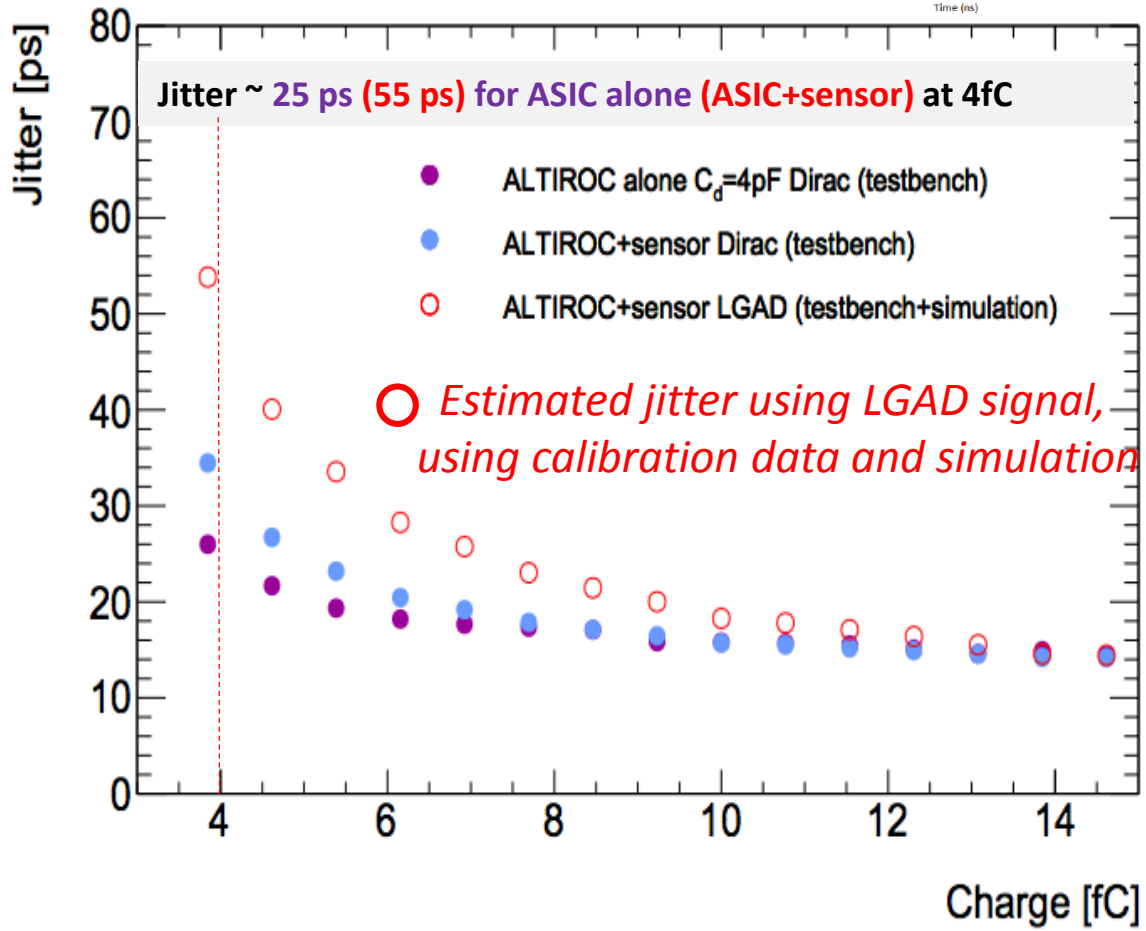
ALTIROC1_V2- Analog performance at system level

System level = ASIC bump-bonded onto a 5x5 LGAD sensor (1.3 mm x 1.3 mm x 50 µm)

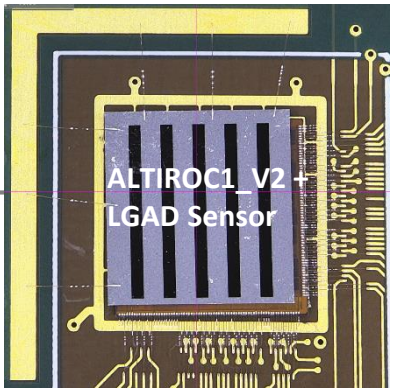
out_preamp simulation

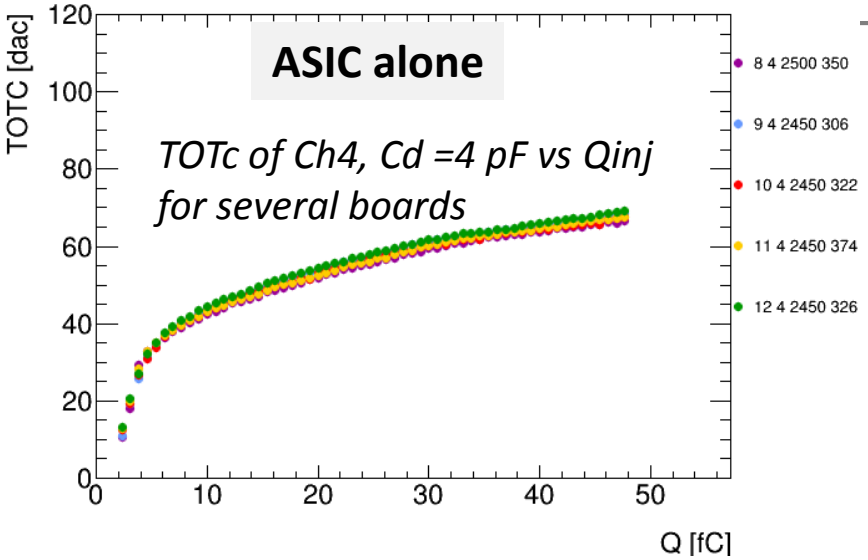


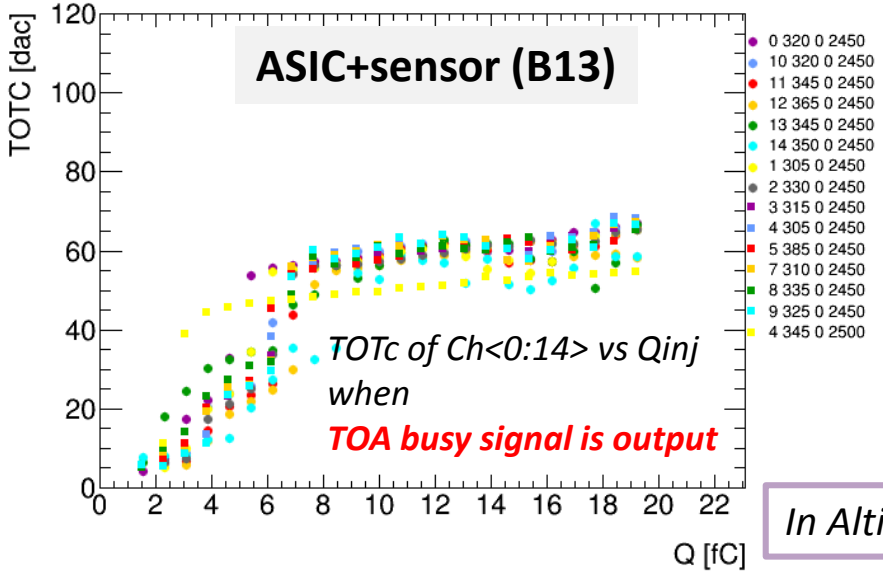




ALTIROC1_V2- Analog performance at system level

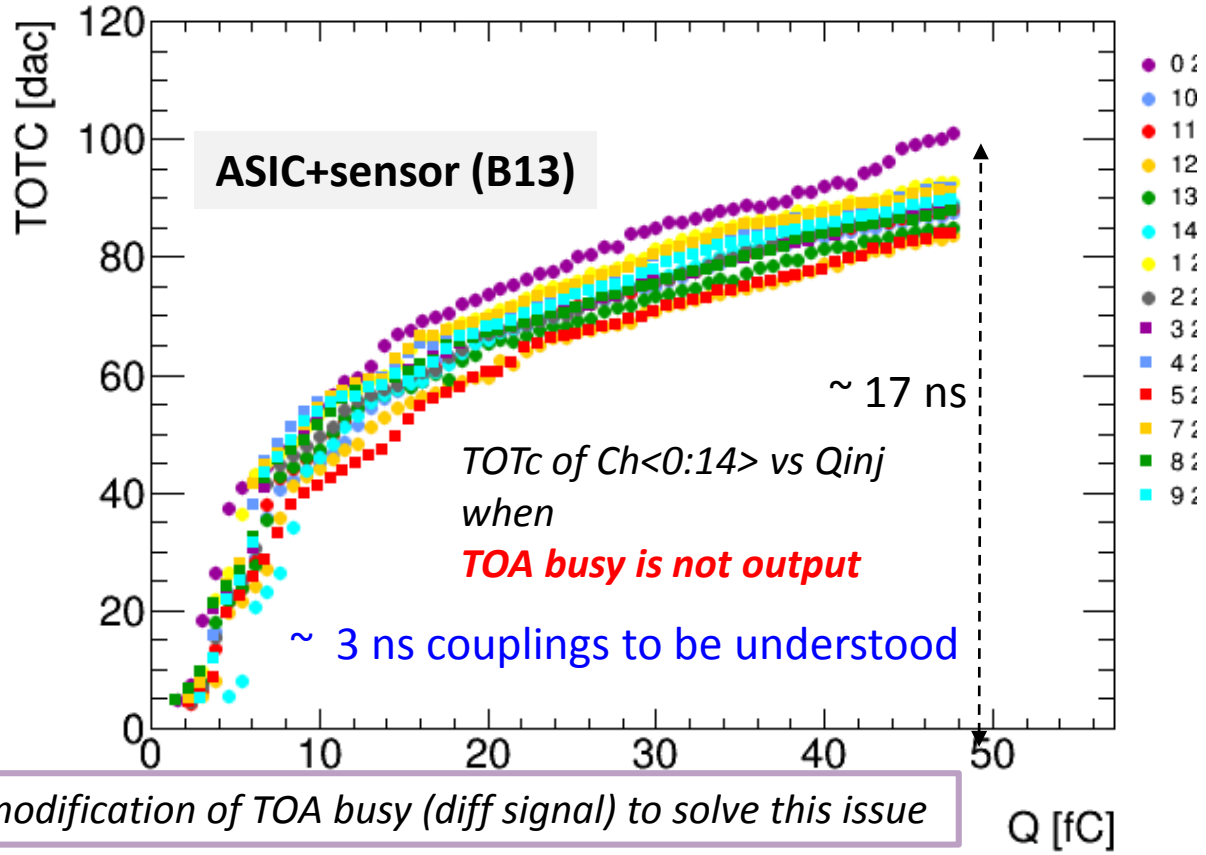






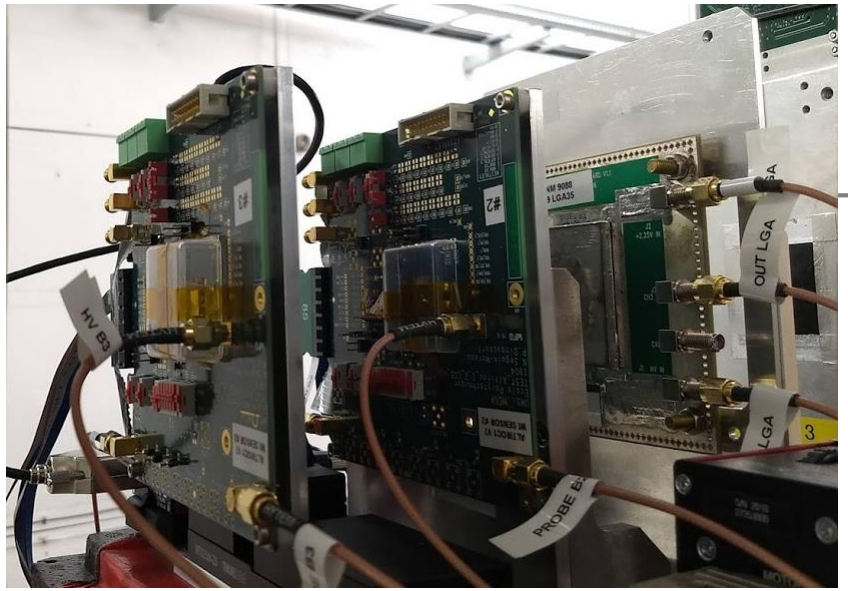
<TOTc_LSB> ~ 170 ps

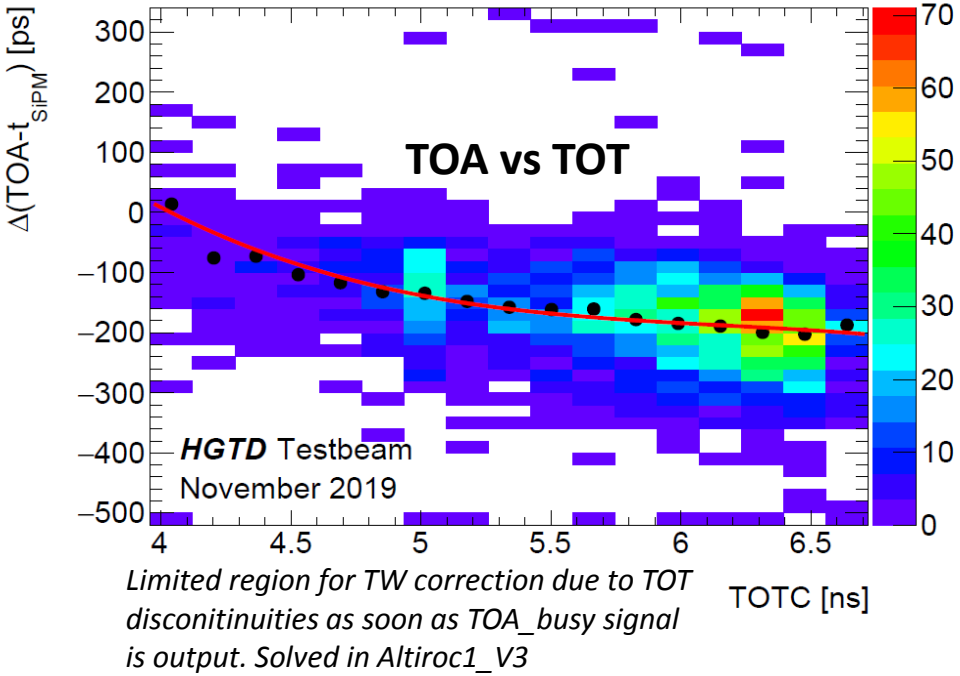
TOA_busy signal: necessary in testbeam (synchronization)



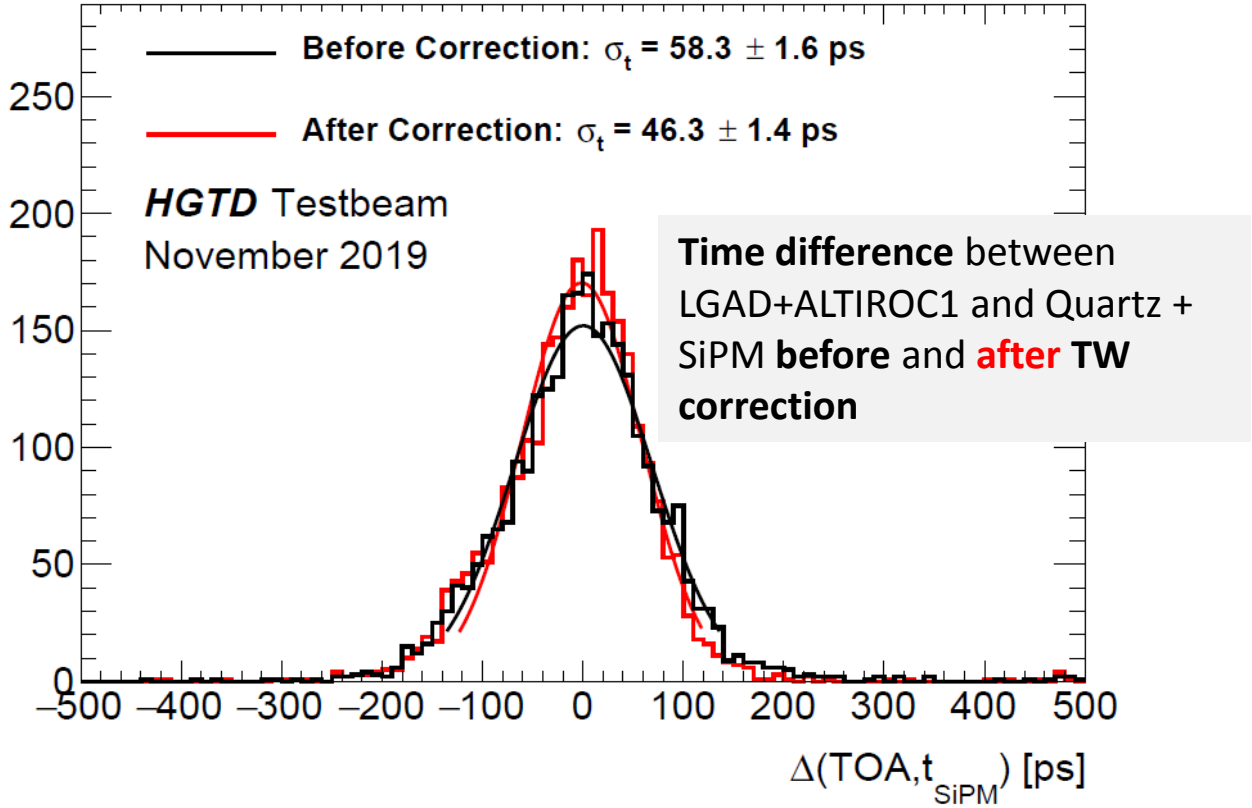
In Altiroc1_V3: modification of TOA busy (diff signal) to solve this issue

TEST BEAM measurements with Altiroc1_V2





Limited region for TW correction due to TOT disconitinuities as soon as TOA_busy signal is output. Solved in Altiroc1_V3



Time difference between LGAD+ALTIROC1 and Quartz + SiPM **before** and **after TW correction**

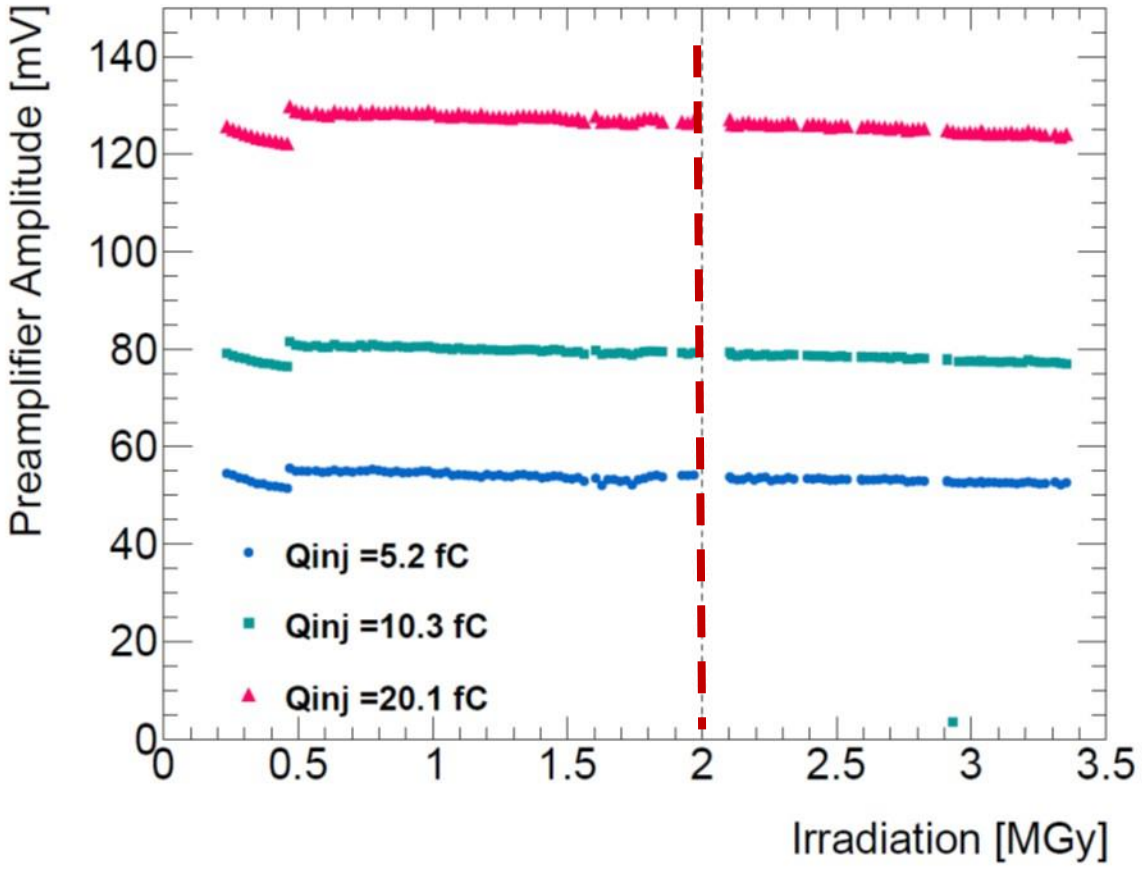
Time resolution= 46 ps => electronics jitter 39 ps after substracting Landau fluctuations (25 ps) $\sigma^2_{hit} = \sigma^2_{Landau} + \sigma^2_{clock} + \sigma^2_{elec}$

New interface boards designed after this TB => jitter should be reduced by 35 % and so electronic jitter contribution should be 26 ps in testbeam (36 ps for time resolution)

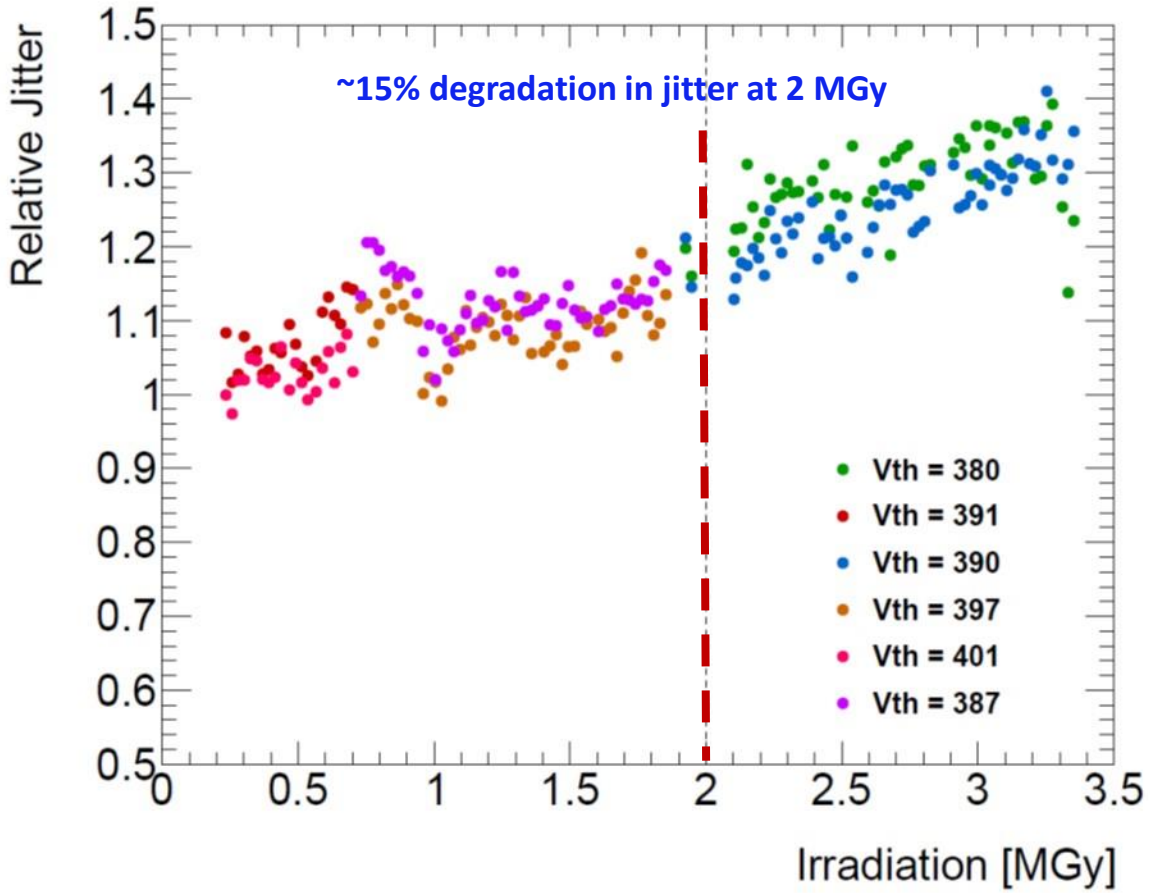
Irradiations tests with Altiroc1_V1 (June 28- July 8, 2019)

CERN facility, TID up to 340 Mrad, requirement: 200 Mrad max

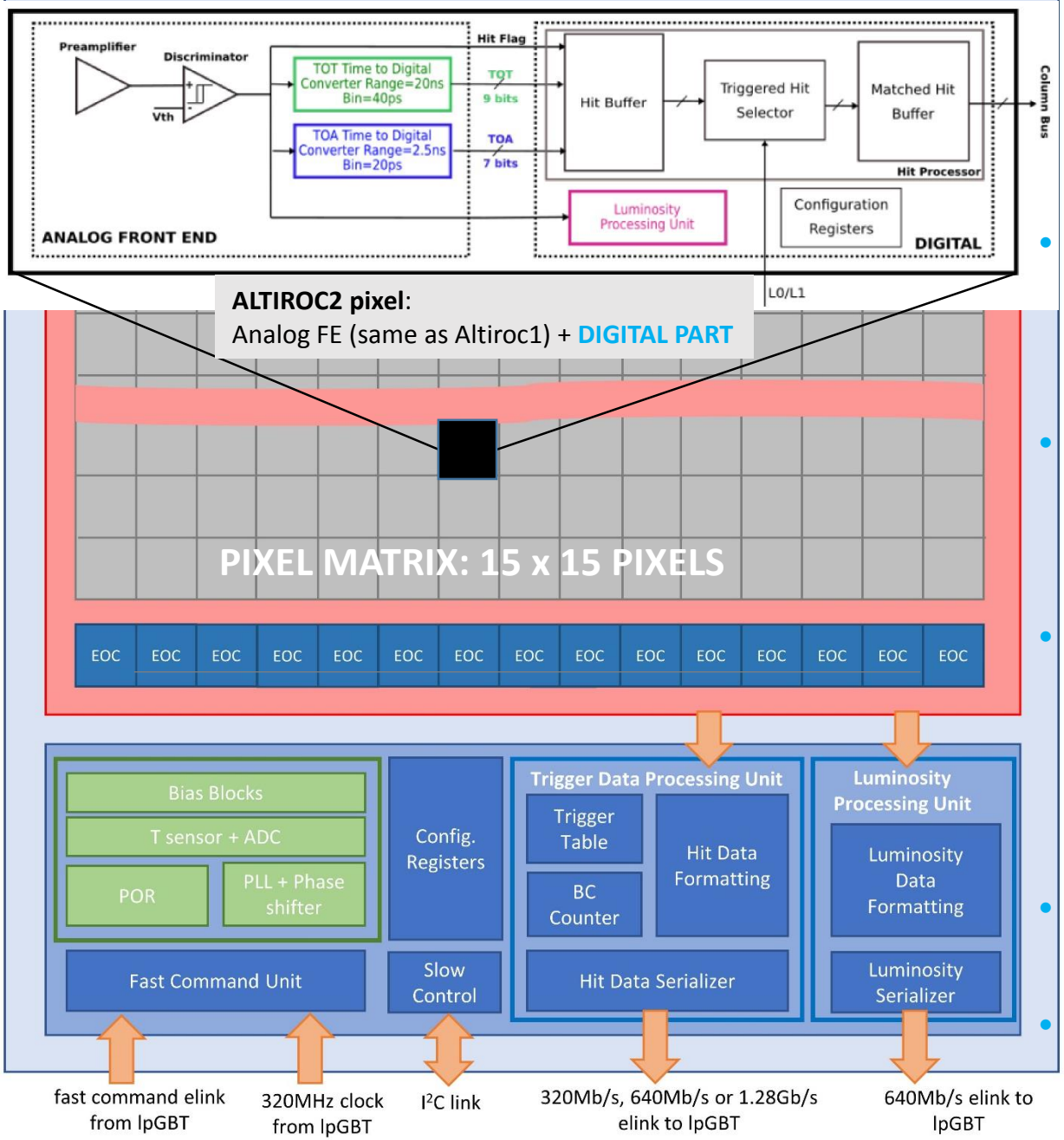
Preamp amplitude for various input charges



Jitter measurement on scope (not measured with TDC)



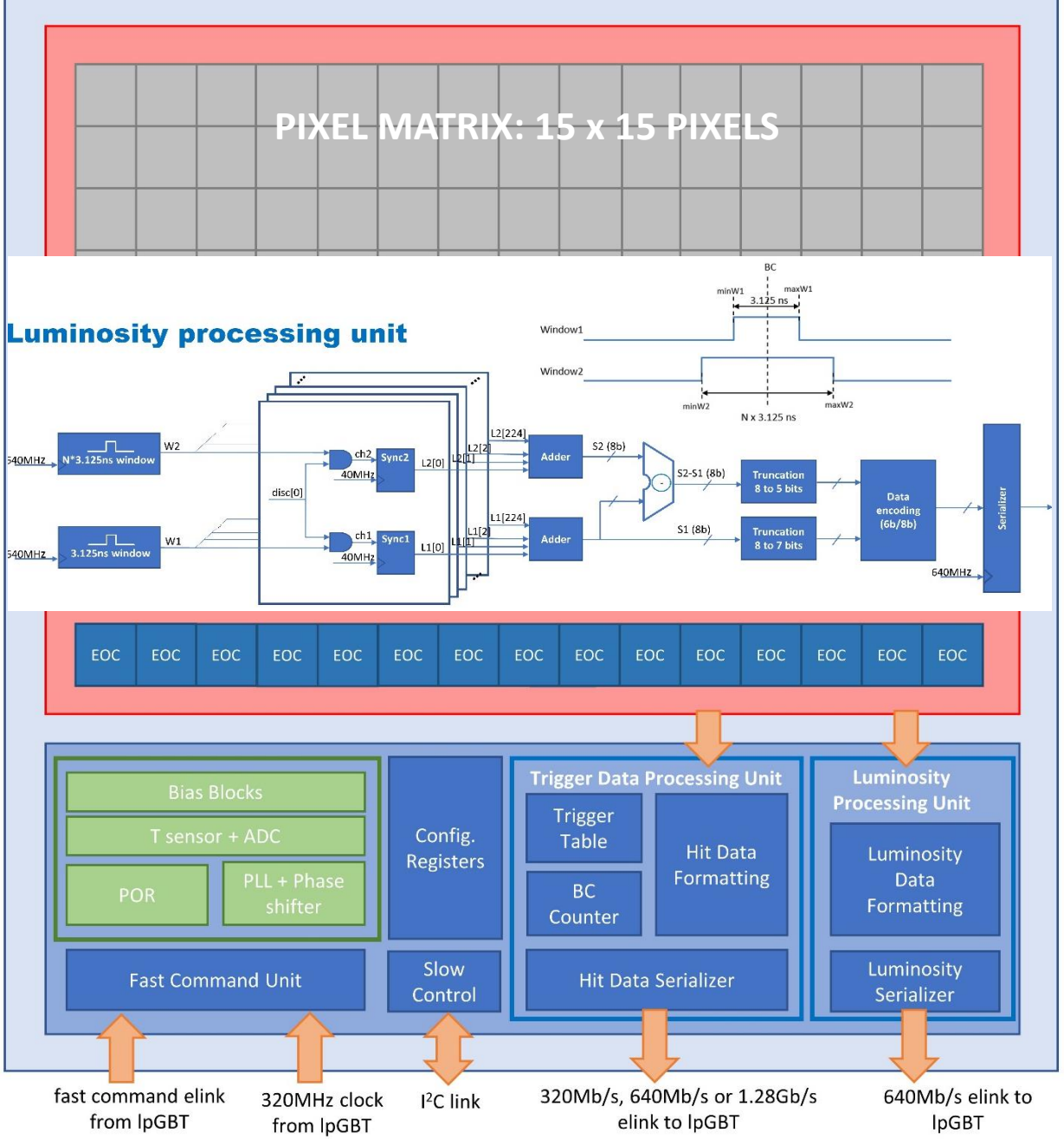
ALTIROC2 (225 ch): Pixel digital part



- **Hit buffer**: SRAM 1536 x 19 bits
  - Circular buffer to store timing data for each BC, until a trigger arrives
  - Data= Hit and TOT and TOA bits, only in case of hit to save power
  - Control unit to handle R/W pointers
- **Trigger Hit Selector** =
  - Each received trigger associated to a trigger tag
  - If data stored in Hit buffer related to received trigger, TOA/TOT data + trig tag stored into Matched Hit Buffer
- **Matched Hit Buffer**: 32 positions FIFO
  - Control Unit: looks for data related to a trigger event when requested by the End Of Column
  - Matched flag handled through a priority OR chain. Pixel at the top of the column with highest priority
  - Synchronous readout at 40 MHz
- **Luminosity process unit**
  - checks if hits are within 2 programmable windows
- **I2C configuration registers**

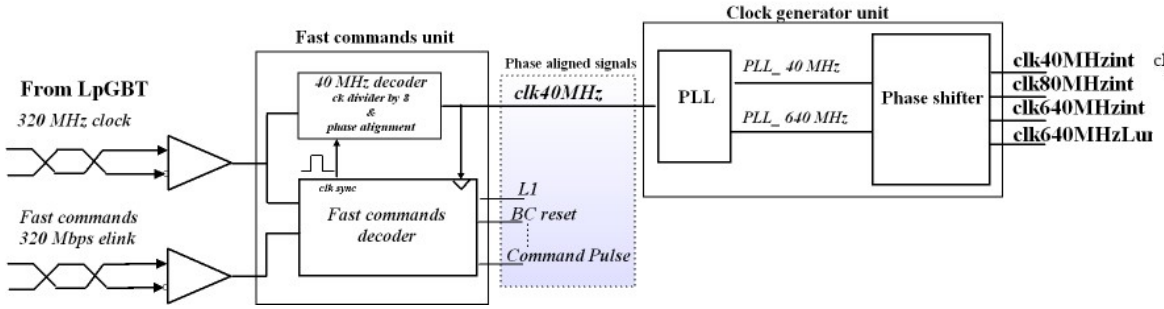
All these digital blocks are integrated in Altipix prototype, first tests in July 2020

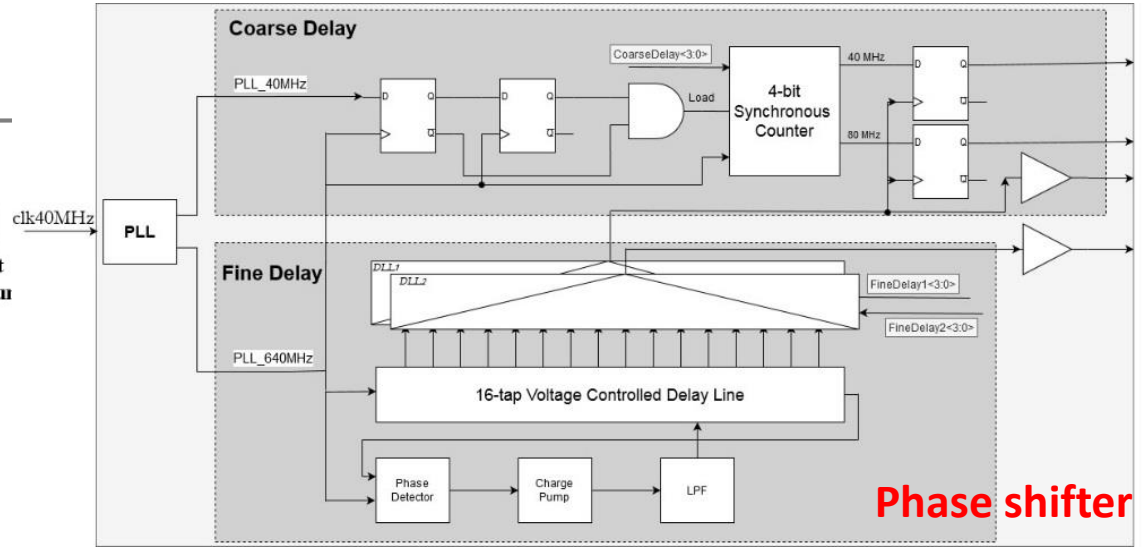
ALTIROC2 (225 ch): Periphery



- **End Of Column:**
  - readout of columns + data transfer to trigger data and luminosity data processing units
- **Luminosity process unit**:
  - Calculates the Nb of hits/BC within 2 time windows generated by window generator unit in the EoC. W1: around the BC, 3.125ns, W2: N*3.125 ns
  - S1 (sum of hits in W1), S2 (sum of hits in W2)
  - S2-S1 (7 bits) and S1 (5bits) = 12 bits lumi data + 4 bits (BCID) serialized and transmitted at 40 MHz
- **320 Mbit/s fast commands decoder**:
  - 8 bits commands @25 ns: IDLE,GBRST, BCR,L0/ L1 trigger, CAL, TriggerID, SetTrigID
  - 40 MHz ck extracted from Fast Commands
- **Trigger Processing unit:**
  - Reads time data from pixel matrix
  - Packs data into frames before serializing them
- **Hit data transmission**
  - Average data to be transmitted depends on radial position: 320 Mb/s, 640 Mb/s, 1.28 Gb/s
- **Slow Control:**
  - I2C link, 1024 * 8-bit registers (Triplication + auto correction)

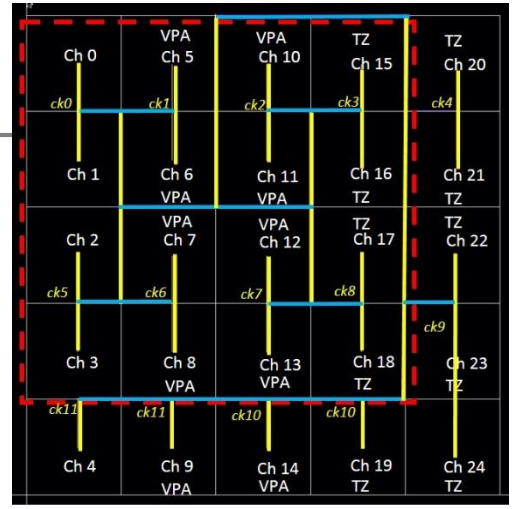
ALTIROC2: Clock distribution





- **40 MHz clock**
  - TOA TDC and most of the digital blocks, including the I2C and configuration registers
- **80 MHz clock**
  - to read out the timing data from the pixel matrix and to pack them into frames in the Trigger Data Processing Unit
- **Two 640 MHz clocks**
  - one to serialize the data (clk640MHzInt)
  - one clock to generate the time windows for the luminosity measurement (clk640MHzLumInt)
- **Phase shifter:**
  - Step 97 ps, range 25 ns. Ck phase alignment + to center the 2.5 ns measurement time window of the TOA TDC on the Bunch Crossing
- **5 ck trees**
  - 40 MHz ck, 80 MHz clock, Lumi windows (W1 and W2), calibration pulse command (= cmd_pulse in Altiroc1)

ALTIROC: Ck trees

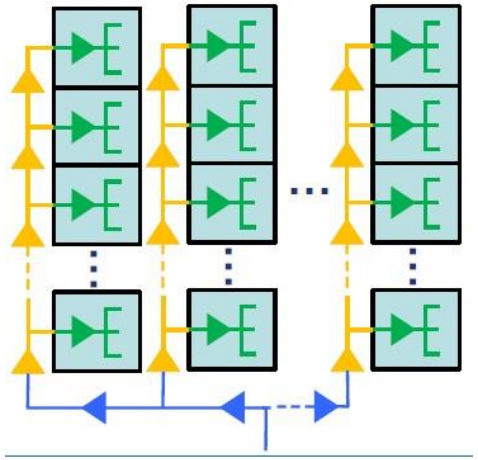


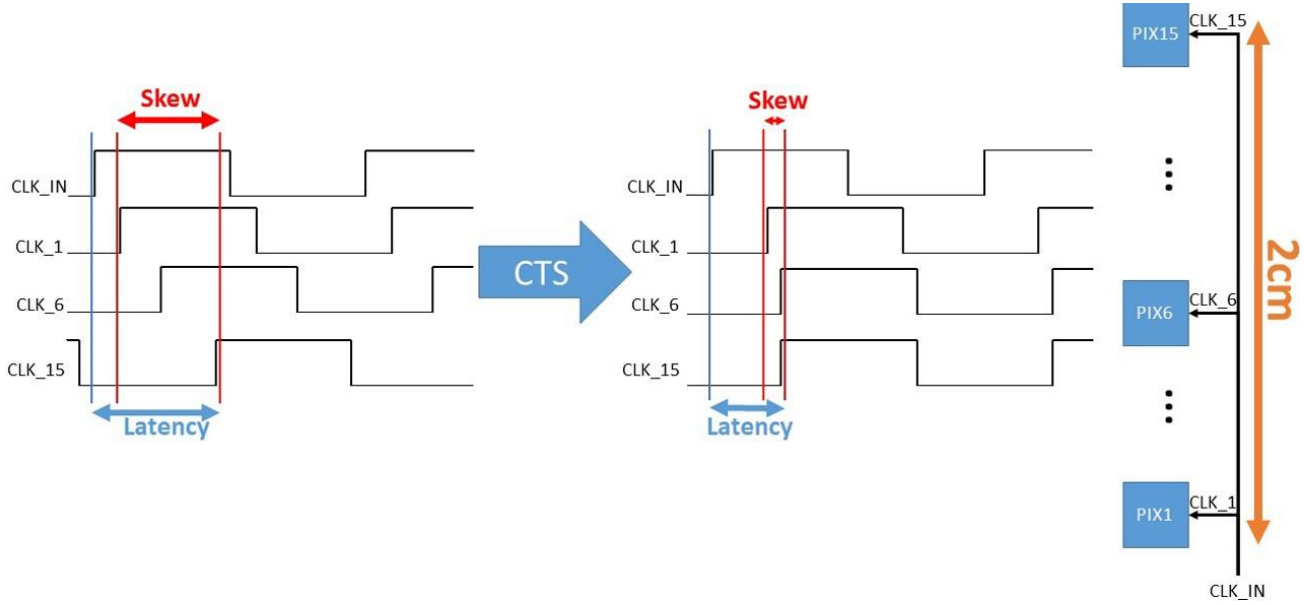
ALTIROC1 ck tree (well distributed on 16 channels)

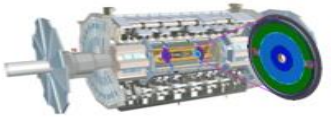
- 40 MHz and cmd_pulse, ck trees done manually
- Uniformity: 18 ps rms
- Average power (ck40 MHz) = 0.6 mW with 16 channels => 10 mW per ck tree for 225 channels

ALTIROC2 ck trees

- 5 ck trees
- Digital On Top vs Analog On Top?
- Skew (< 100 ps) vs power vs radiation hardness





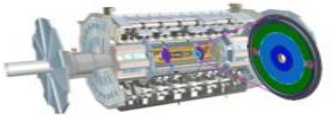


ATLAS HGTD

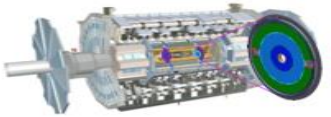
SUMMARY & CONCLUSIONS

- Good analog performance demonstrated with ALTIROC1 prototypes
  - Very useful to understand system issues with sensor
  - Jitter (ASIC+sensor) < 35 ps at 4 fC with calibration pulse
  - Vth (ASIC+sensor) can be set at 2 fC
  - Testbeam expected before the end of this year with new interface board and with Altiroc1_V3 prototype (expected this summer) where TOT issues solved

- Design of first full size ASIC (ALTIROC2) is on going , submission November 2020
  - Mix of Digital On Top (DOT) and Analog On Top (AOT), compromise between power dissipation, timing verifications, analog performance
  - Analog performance crucial , floor plan (power distribution, grounding) done AoT
  - Tests @system level will be done



BACK UP SLIDES

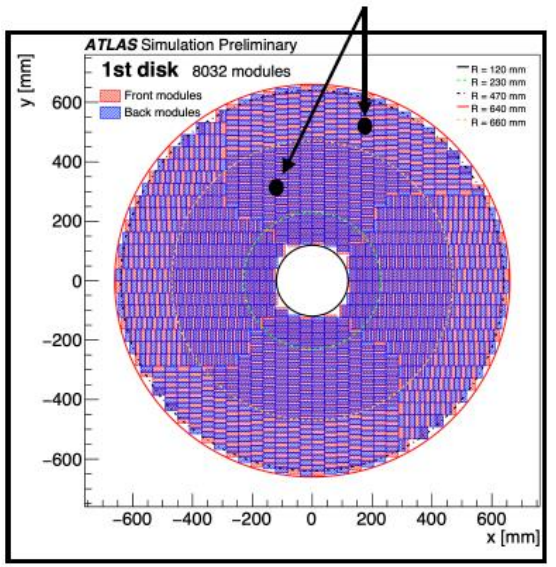


t0 (TOA) Calibration

Goal: measure the same hit time (t_hit) for tracks from the same interaction

⇒ Need to correct various effects :

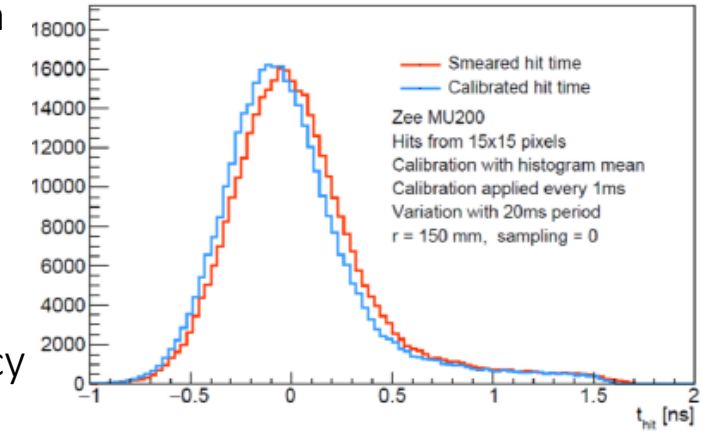
t_hit= TOA_t0 = t0_static_ASIC + t0_static_online + t0_dynamic_offline



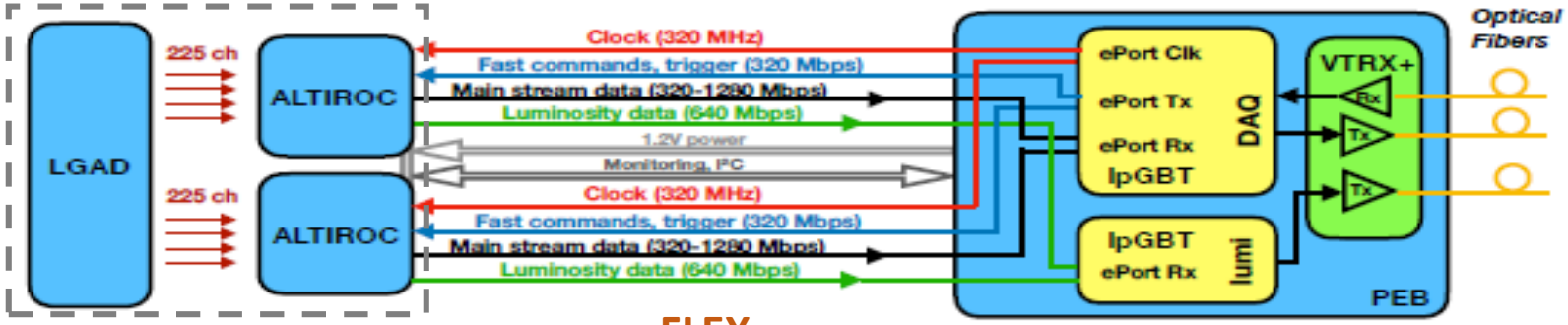
- t0 dispersion inside one ASIC: t0_static_ASIC
  - Due to ck skew between channels, static dispersion. Offline correction using ASIC internal calibration pulser to have **t0_static_ASIC** better than 5 ps

- t0 dispersion between ASICs: **t0_static_online** and **t0_dynamic_offline**
  - Due to TOF (η, ϕ, flex cable length), static dispersion. Online correction using each ASIC phase shifter to adjust the TOA window and so to get **t0_static_online** within ~ 100 ps.

  - Due to dynamic variations (drift of 40 MHz clock-RF, temperature …). Offline correction using minimum bias physics events to re-adjust each ASIC t0 and so to have **t0_dynamic_offline** within the needed accuracy of 10 ps (average of hits done over different integration windows)



HGTD module: Flex module and tails



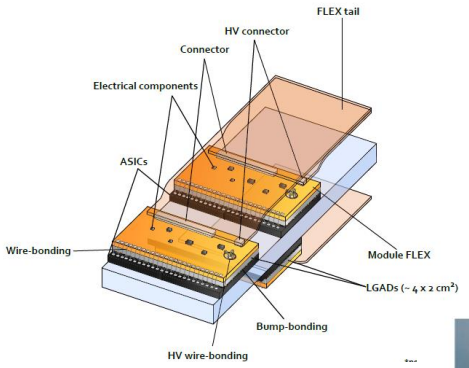
HGTD module

FLEX

Peripheral electronics
PEB

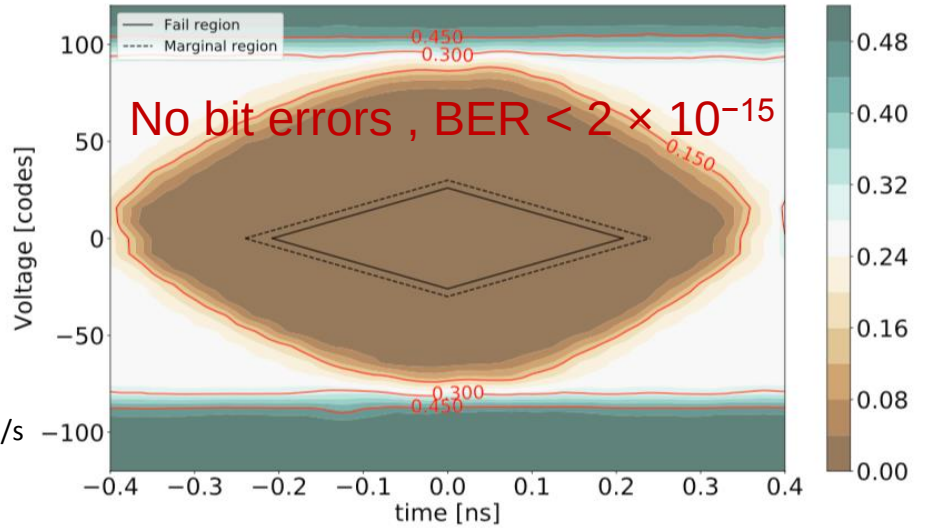
Tolerance in length	1 mm
Tolerance in width	100 µm
Flex tail maximum thickness	220 µm
Module flex maximum thickness	500 µm
Insulation resistance of HV line	10 GΩ
Maximum resistance of power planes	2.7 mΩ cm^{-1}
Maximum resistance of ground planes	0.7 mΩ cm^{-1}
Impedance of single lines	50 Ω–65 Ω
Impedance of differential lines	90 Ω–120 Ω
Maximum allowed BER	10^{-12}
Radiation tolerance	2 MGy
Neutron fluence	2.5x10^{15}neq/cm^2

LGAD sensor (450 PADs of 1.3 x1.3 mm2)
bump-bonded onto
2 ASICs (225 channels/ASIC)

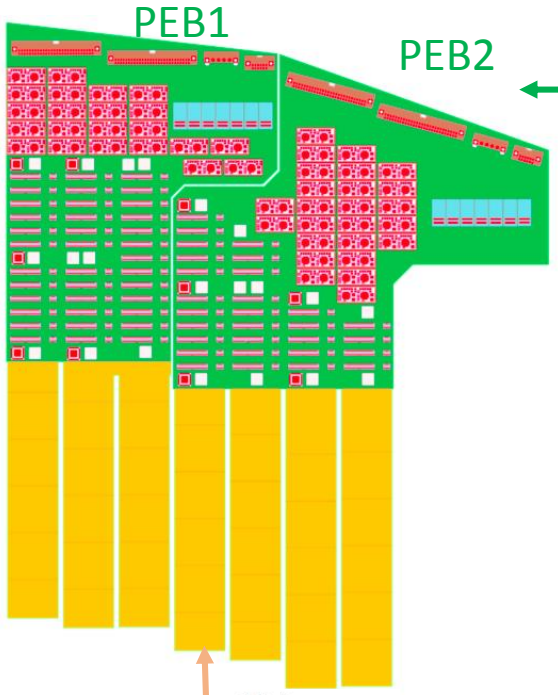


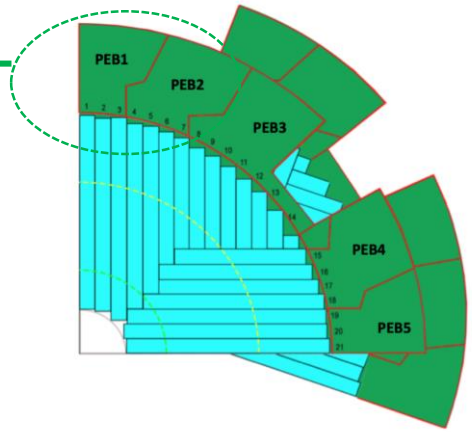
- **FLEX** will connect the signals from each bare module to the peripheral electronics board
- Baseline: 2 pieces, module flex and tail (up to 69 cm)
- Flex prototypes (still in a single piece) within the specifications

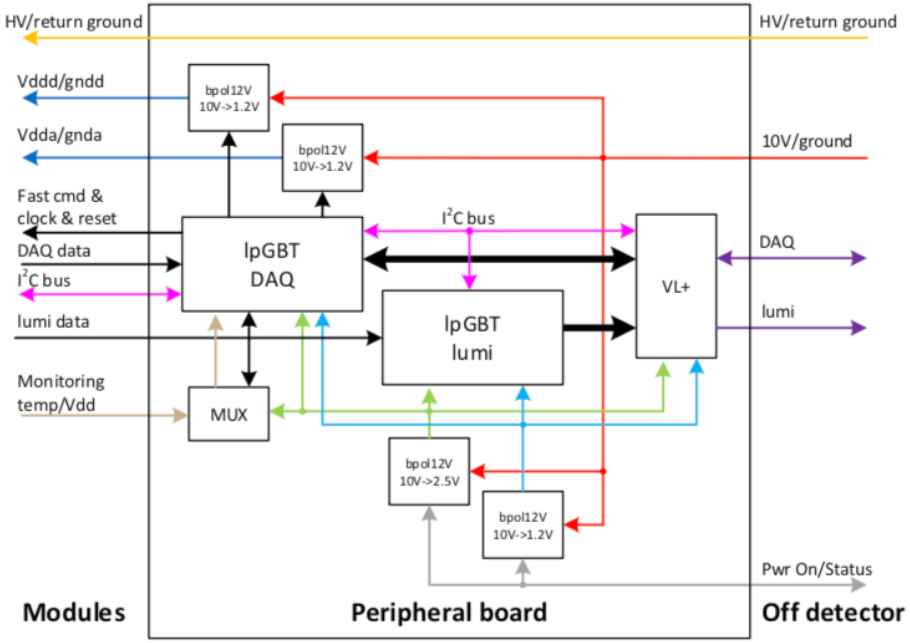
HV=1KV
1.25 Gbit/s

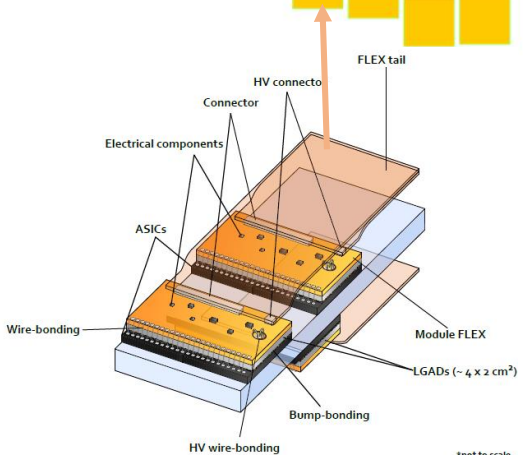


Peripheral Electronics Boards (PEB)









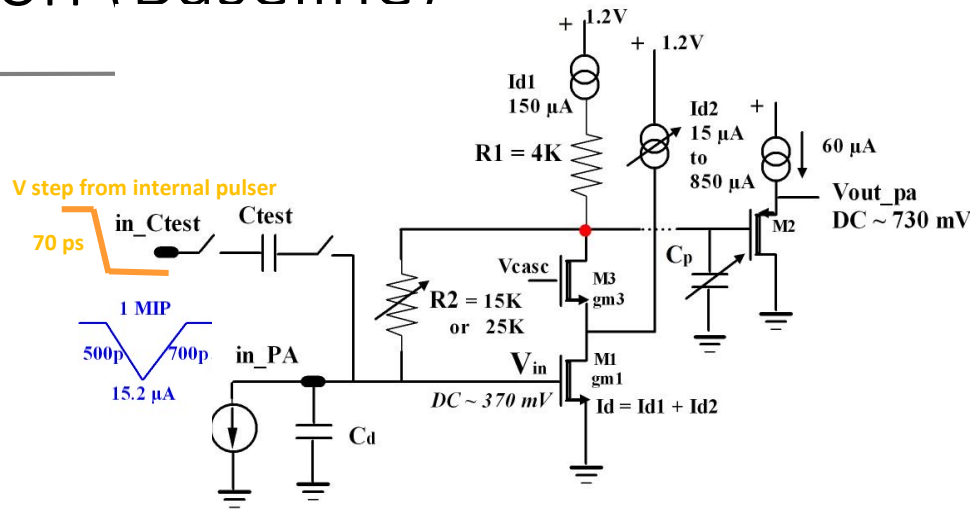
- **Data transfer** between modules ←→ DAQ/luminosity/DCS systems
- Distributes **HV** to sensors and **DC voltages** to ASICs (through DC-DC regulators)
- Use mostly components developed by CERN for the LHC upgrades: **lpGBTs, VTRx optical receiver and transmitter, bPOL12V converter**.
- Main challenge is the **high component density** (short flex tails of 6 outer modules integrated in PEB PCB to avoid connectors)
- Design ongoing, first prototype expected by end 2020

ALTIROC Preamp: Voltage configuration (Baseline)

- Id tuneable: Id (M1) = Id_1 (150 µA) + Id_2 (tuneable up to 850 µA)
- BW tuneable with Cp: **1 GHz** down to 200 MHz
- R2=25K: for DC bias, Rin ~ 1.6 KΩ, Fall time= 2.2 RinCd
- Sensor leakage current: absorbed by R2

$$V_{out\_pa} = G_{pa}\, Vin = G_{pa}\frac{Q_{IN}}{C_d} \sim \alpha\, I_d \frac{Q_{IN}}{C_d}$$

G_{pa} ~ gm_1 x R_1 and gm_1 ~ 20 * (Id_1 + Id_2)

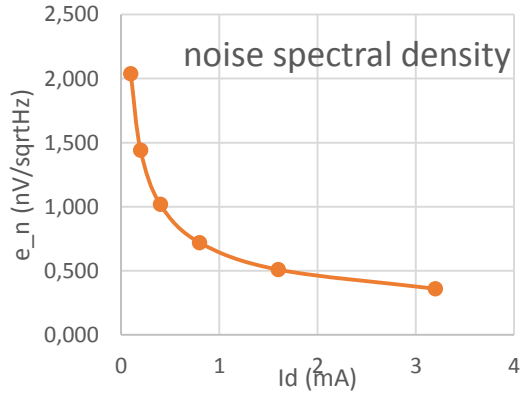


- Noise independant of Cd, depends of **√BW** and of **$1/\sqrt{I_d}$**

$$N = G.e_n\sqrt{\frac{\pi}{2}BW} = G.e_n\sqrt{\frac{\pi}{2}\frac{0.35}{t_{10-90\_PA}}} = \frac{G.e_n}{\sqrt{2t_{10-90\_PA}}}$$

with en given by: $$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$

$$\sigma_t^{\,J} = \frac{e_n C_d}{Q_{in}}\sqrt{t_d}$$



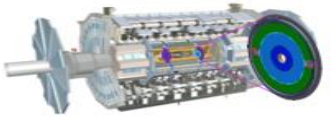
$$\frac{dV}{dt} == \frac{G.Q_{in}}{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}$$

- Signal rise time is the convolution of signal duration td and amplifier risetime $t_{10\text{-}90\_PA}$

Cooling system: requirements

HGTD Component	Power consumption	Total [kW]
Sensor	30 to 100 mW cm^{-2}	2.0–6.4 (*)
ASIC	< 300 mW cm^{-2}	17.6–19.2(**)
Flex cable	6.8 mW cm^{-1}	2.0
Total in active region		**21.6–27.6**
HGTD vessel heaters	100 W m^{-2}	1.3
Pre-heaters (Perip. electr.)		8.8
Ambient pick-up		2.5
Total power dissipation		**34.2–40.2**

- - 35 ^{o}C using CO2 evaporative cooling (as ITK)
- Main dissipation from ASIC and irradiated sensors
- Total power dissipation = 40 KW

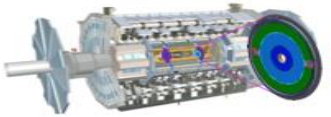


HGTD Electronics: requirements and parameters

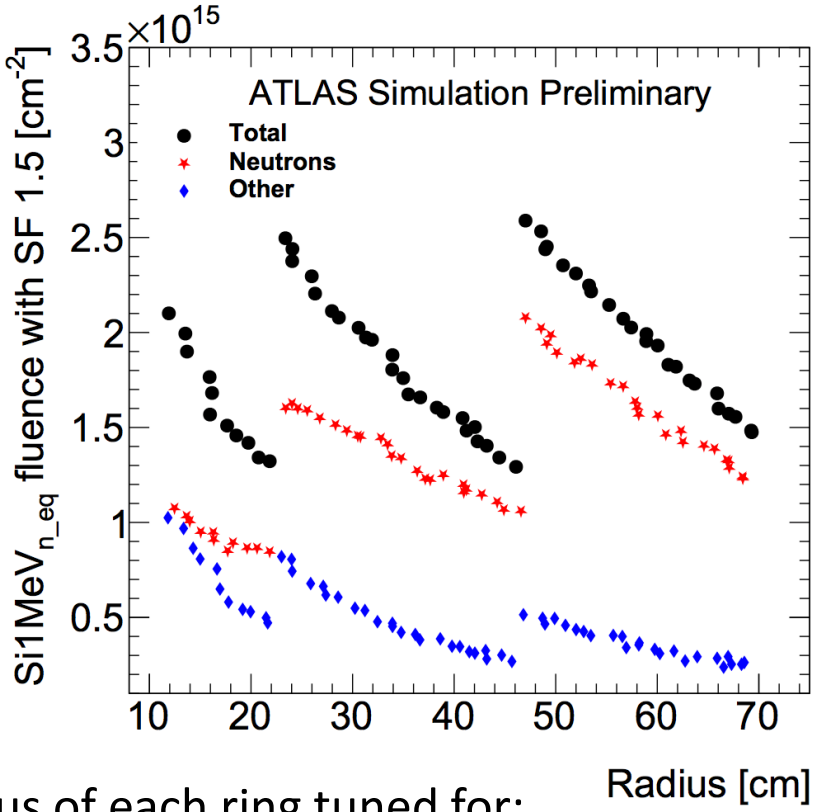
Pad size	$1.3 \times 1.3\,\mathrm{mm}^2$
Voltage	1.2 V
Power dissipation per area (per ASIC)	$300\,\mathrm{mW\,cm^{-2}}$ (Total: 1.2 W)
e-link driver bandwidth	$320\,\mathrm{Mbit\,s^{-1}}$, $640\,\mathrm{Mbit\,s^{-1}}$, or $1.28\,\mathrm{Gbit\,s^{-1}}$
Temperature range	−40 °C to 40 °C
TID tolerance (w/ SF =2.25)	2.0 MGy
Full Chip SEU Upset probability	< 5%/hour

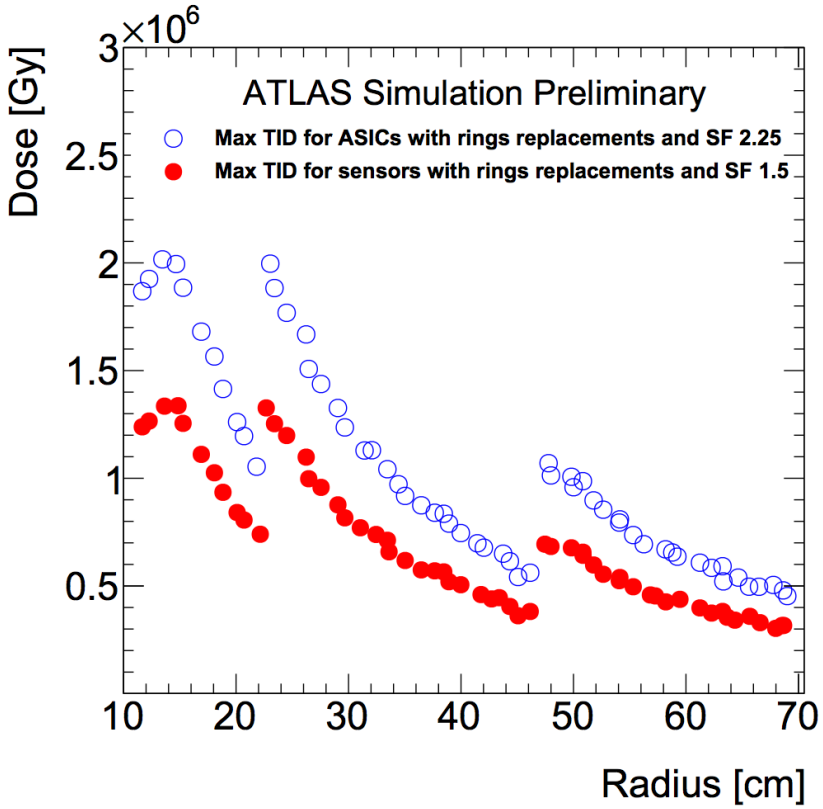
$$\sigma^2_{hit} = \sigma^2_{Landau} + \sigma^2_{clock} + \sigma^2_{elec}$$
with $\sigma^2_{elec} = \sigma^2_{Time\ walk} + \sigma^2_{jitter} + \sigma^2_{TDC}$

Maximum leakage current	5 µA
Single pad noise (ENC)	< 3000 e^- = 0.5 fC
Cross-talk	< 5%
Threshold dispersion after tuning	< 10%
Maximum jitter	25 ps at 10 fC 70 ps at 4 fC
TDC contribution	< 10 ps
Time walk contribution	< 10 ps
Minimum threshold	2 fC
Dynamic range	4 fC–50 fC
TDC conversion time	< 25 ns
Trigger rate	1 MHz L0 or 0.8 MHz L1
Trigger latency	10 µs L0 or 35 µs L1
Clock phase adjustment	100 ps



Radiation levels in HGTD at 4000 fb-1 (Fluka with ITK 3.1 layout Oct 2020)





Radius of each ring tuned for:

- 2.5x10^{15}n$_{eq}$/cm2 max. for sensors (including SF = 1.5)
- 2 MGy max for ASIC (with SF =1.5x1.5= 2.25)
- Ring radii will be optimized before construction to account for possible future changes of the materials in ITk