DE LA RECHERCHE À L'INDUSTRIE

cea

READOUT ELECTRONICS FOR T2K-II HA-TPC: ELEMENT DENOMINATION, DAQ OPTIONS, DATA FORMAT

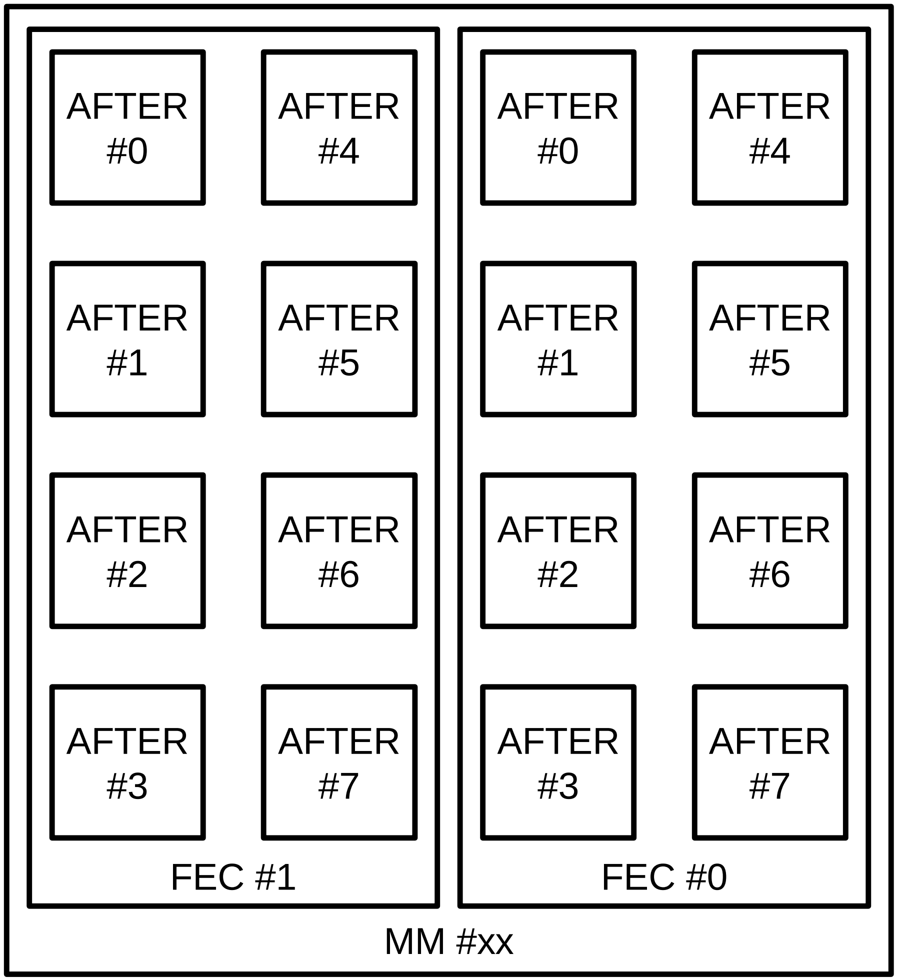
D. Calvet,
CEA Paris-Saclay

Saclay, 27 April 2020

www.cea.fr

Irfu

LOGICAL MAPPING OF ERAM FRONT-END ELECTRONICS

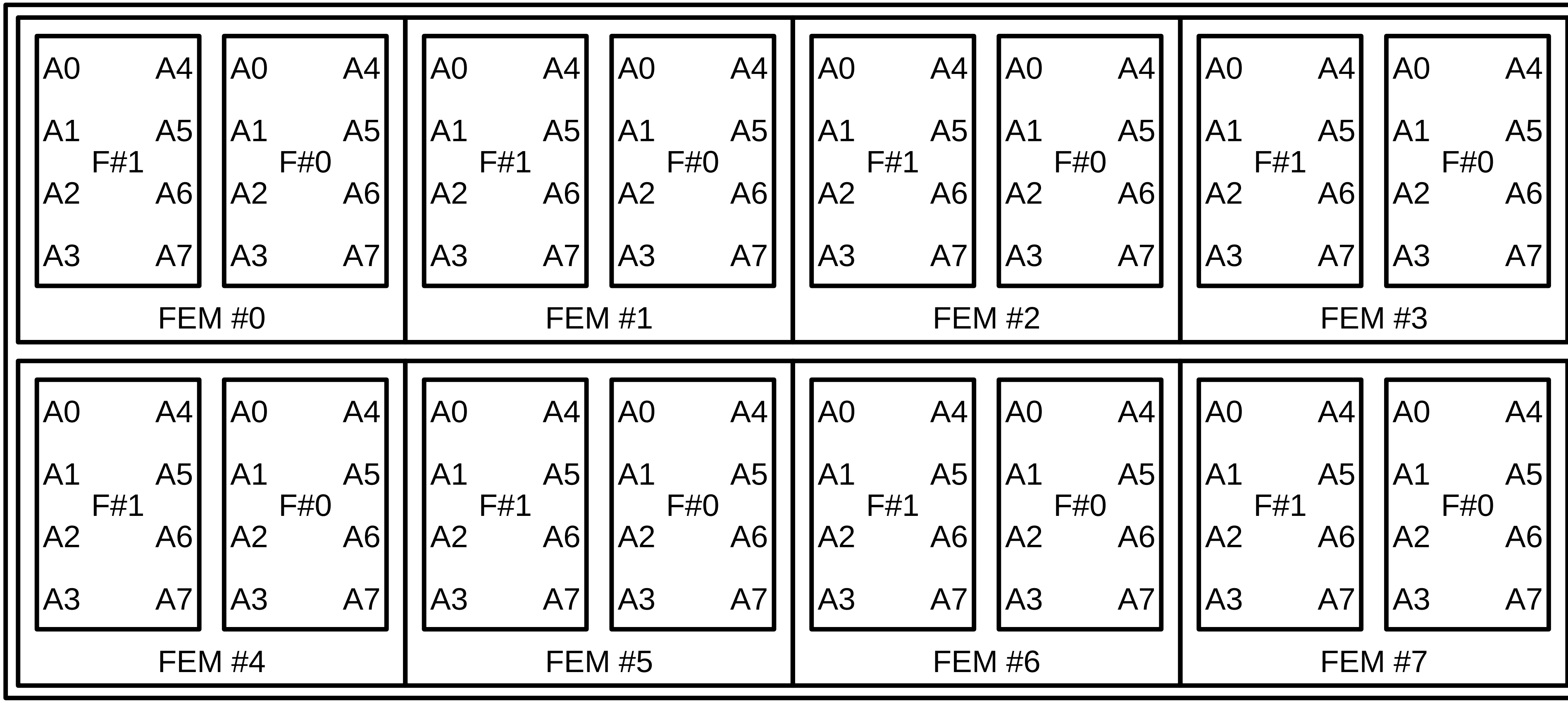


View from the outside of the HA-TPC

Remarks

- Each AFTER maps to an area of 9x8 pads
- AFTER channels are referred by a DAQ Channel number in [0;78]. Only 72 values correspond to physical channels
- Conversion from DAQ Channel to pad {X,Y} simply requires a loop-up table determined by:
  - ERAM layout
  - FEC layout
  - AFTER chip pinout and internal logic in the silicon
  - FEM layout and FPGA firmware
- Note that FEC #1 is left of FEC #0 in the currently foreseen layout

HA-TPC FRONT END-PLATE MAPPING TO FEMS



Beam upstream

Upper or lower HA-TPC; Front End-plate

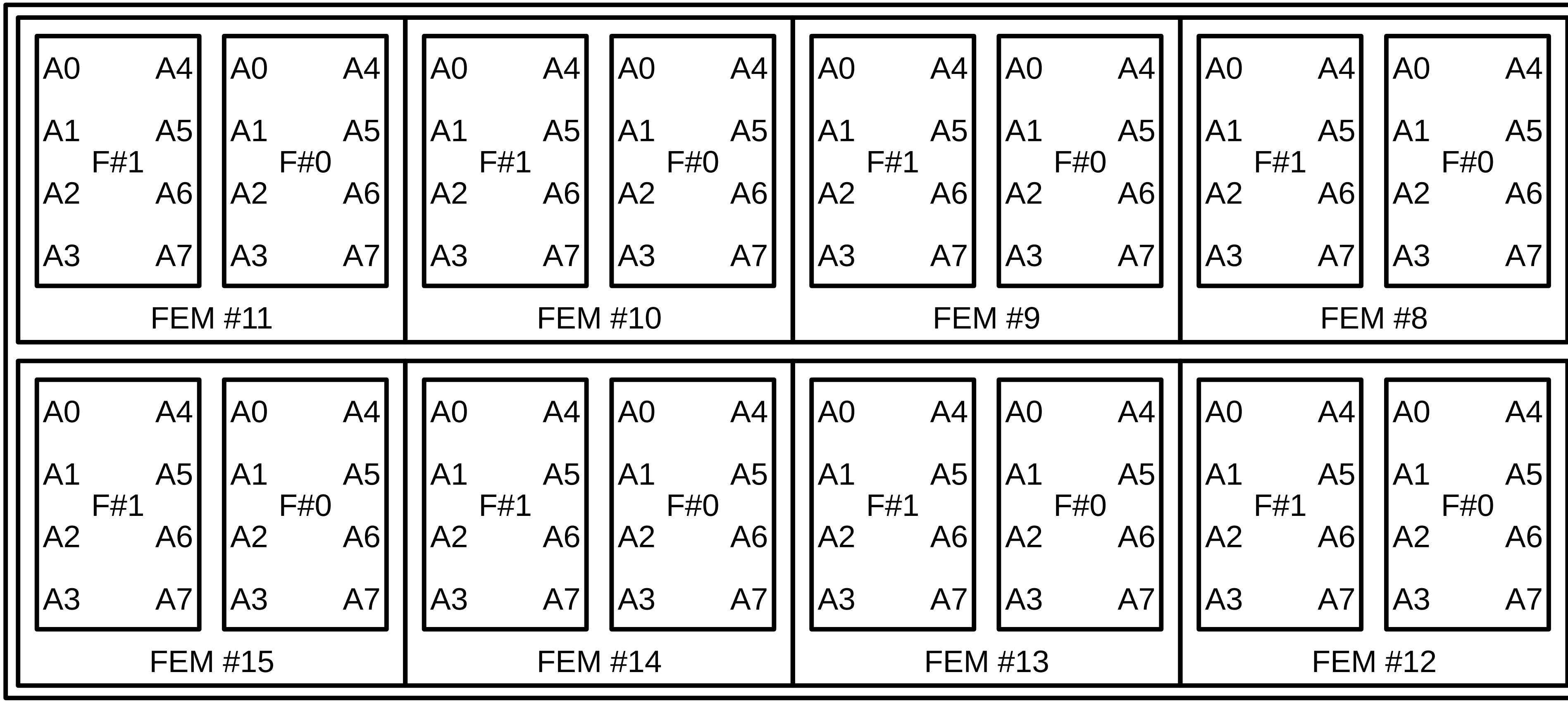
View from the outside of the HA-TPC

Beam downstream

Remarks

- FEM numbering used by DAQ determined by optical fiber connections to physical ports of TDCM

HA-TPC REAR END-PLATE MAPPING TO FEMS



Beam downstream

Upper or lower HA-TPC; Rear End-plate

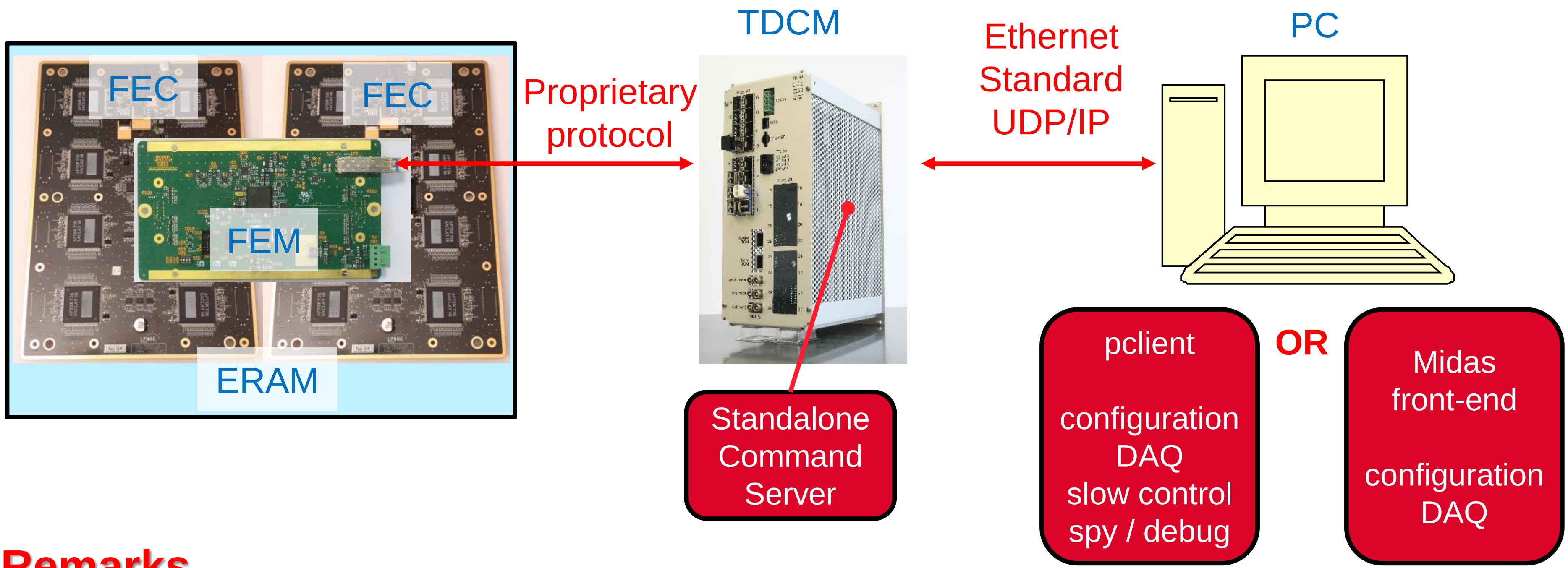
View from the outside of the HA-TPC

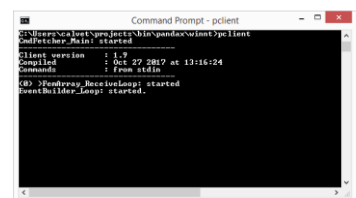
Beam upstream

Remarks

- FEM numbering used by DAQ determined by optical fiber connections to physical ports of TDCM

DAQ MODEL DESY TEST BEAM 2020 – MINIMAL AND NOMINAL SCHEMES





Web Interface

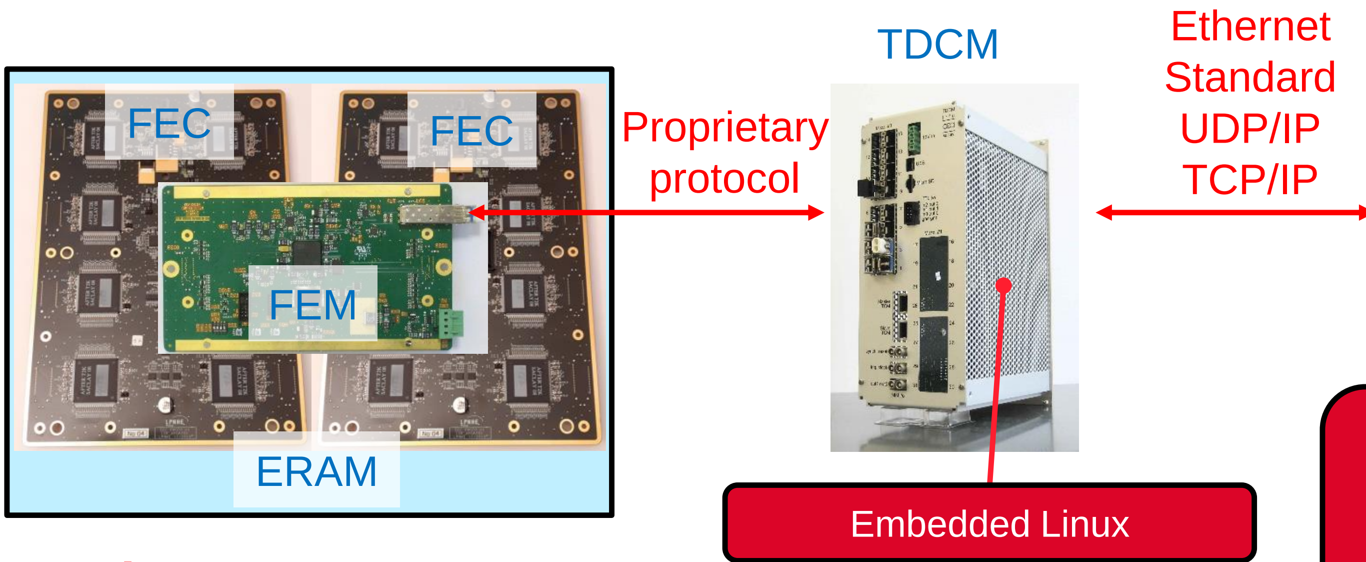
Minimal scheme

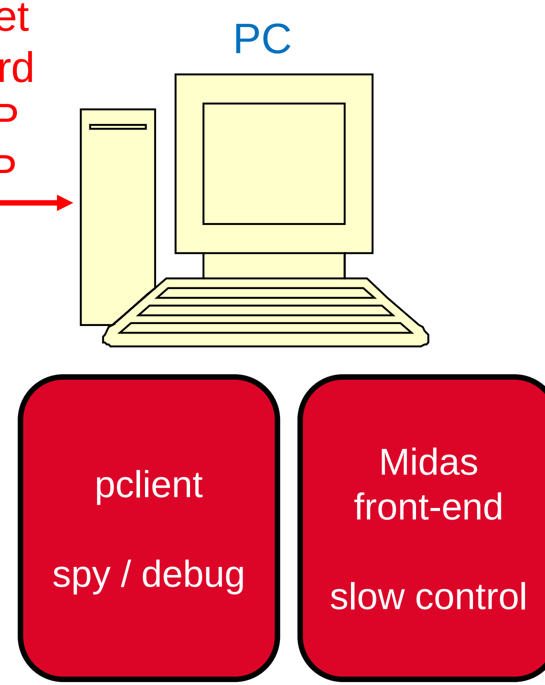
Nominal scheme

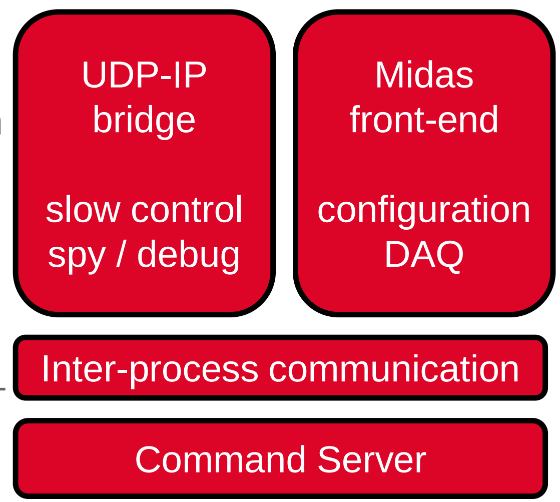
Remarks

- Minimal back-end software scheme used at DESY test beam 2019 using ARC readout
- Nominal back-end software scheme being tested at CERN with ARC readout electronics
- Both solutions require some updates to run with new FEC and FEM front-end electronics

DAQ MODEL DESY TEST BEAM 2020 – ENHANCED SCHEME







Remarks

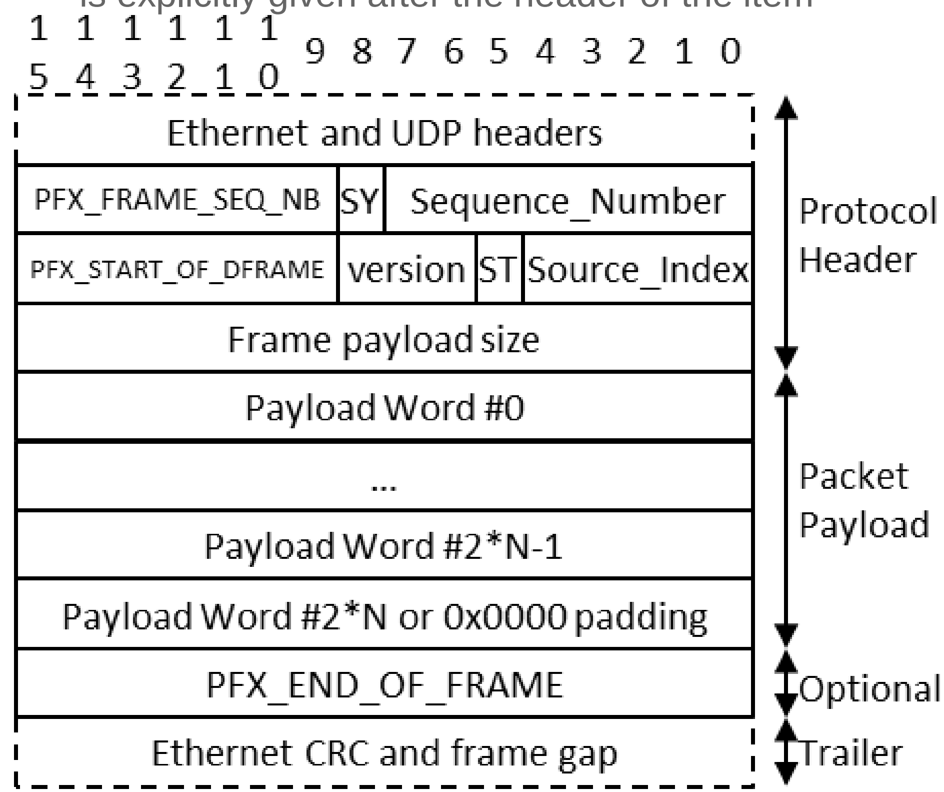
- Midas front-end program for slow control only required for final system. May run on TDCM instead of a PC
- pclient required for spy / debug, even in final system
- Not shown: A) power ON/OFF for front-end electronics: Midas fe program + PC + USB / RS-485 + 4 “PowCon” cards
  B) Slow control for LV power supplies: Midas fe program + PC + USB / CANbus

TDCM communication principles

- Currently over Gigabit Ethernet UDP/IP
- All commands, configuration, monitoring and DAQ requests are in plain ASCII format. Each frame can only contain one command
- Each configuration or monitoring command is answered with one and only one frame
- Most configuration and monitoring replies mainly composed of a signed error code followed by an ASCII string. The error code must be tested: 0 or positive on success, negative on failure. The string contains the requested value(s) or the reason that caused command failure
- DAQ replies and complex monitoring data (e.g. pedestal histograms, statistics) are formatted in binary using proprietary encoding

DAQ reply encoding principles

- Composed of successive elementary pieces of information called “Items”
- Each Item had a header of variable size (from 2 bit to 16 bit) indicating its type followed by content (from 0 bit to 1 Ethernet MTU, i.e. 8 KB with Jumbo frames)
- Item size is either implicitly known from its type, or it is explicitly given after the header of the item



LOW LEVEL EVENT DATA FORMAT

Bits: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Word (bits 15 … 0)	
Protocol Header (FEM) Previous packet in same Ethernet frame or protocol header (TDCM)	Mandatory
PFX_START_OF_EVENT | ETYPE | ST | SOURCE ID	Event Header
48_bit time stamp (16-LSBs)	
48_bit time stamp(16-middle)	
48_bit time stamp(16-MSBs)	
32-bit Event Count (16-LSBs)	
32-bit Event Count (16-LSBs)	
PFX_EXTD_CARD_CHIP_LAST_CELL_READ | Chip #0	FEM: optional data TDCM: not present
000000 | Last Cell Read Pointer #0	
PFX_EXTD_CARD_CHIP_LAST_CELL_READ | Chip #1	
000000 | Last Cell Read Pointer #1	
...	
PFX_EXTD_CARD_CHIP_LAST_CELL_READ | Chip #N	
000000 | Last Cell Read Pointer #N	
Protocol Trailer (FEM) Following packet in same Ethernet frame or protocol trailer (TDCM)	FEM: mandatory TDCM: case dependent

Bits: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Word (bits 15 … 0)	
Protocol Header (FEM) Previous packet in same Ethernet frame or protocol header (TDCM)	FEM: mandatory TDCM: case dependent
PFX_EXTD_CARD_CHIP_CHAN_HIT_IX	Data of one Channel
Card # | Chip # | Channel Hit #	
PFX_ADC | ADC value Time bin #0	
PFX_ADC | ADC value Time bin #1	
...	
PFX_ADC | ADC value Time bin #N-1	
null word (if N is odd)	
Protocol Trailer (FEM) Following packet in same Ethernet frame or protocol trailer (TDCM)	FEM: mandatory TDCM: case dependent

Bits: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Word (bits 15 … 0)	
Protocol Header (FE) Previous packet in same Ethernet frame or protocol header (TDCM)	FE: mandatory TDCM: case dependent
PFX_END_OF_EVENT | ST | SOURCE ID	Always present
Reserved for future use	
32-bit event size (16-LSBs)	
32-bit event size (16-MSBs)	
Protocol Trailer (FE) Following packet in same Ethernet frame or protocol trailer (TDCM)	FE: mandatory TDCM: case dependent

Raw event content

- Event header of TDCM (+optional event header of FEMs)
- Event body: channels data – normally zero-suppressed
- Event trailer of TDCM (+optional event trailer of FEMs)
- Keeping Ethernet frame delimiters can be useful for debug

FROM LOW LEVEL EVENT DATA FORMAT TO DATA FILES STORED ON DISK

DAQ based on pclient (.aqs files)

- Run number with date and time added at beginning of file
- Raw events stored sequentially
- Pedestals and threshold can be stored, but not other parameters (sampling rate, gain, etc.)

MIDAS DAQ in native format (.mid)

- Copy of ODB at beginning and end of run
- The data of each complete raw event are encapsulated in Midas Banks

Other formats - suggestion

- Encapsulate each raw event with preferred header / trailer information
- Keep structure and content of raw events unaltered for the possibility of post-DAQ data integrity check and debugging by de-encapsulation of successive hardware and protocol layers