

FCC@LPNHE

Detector R&D for Si-W calorimetry (CALICE)

24/04/2020

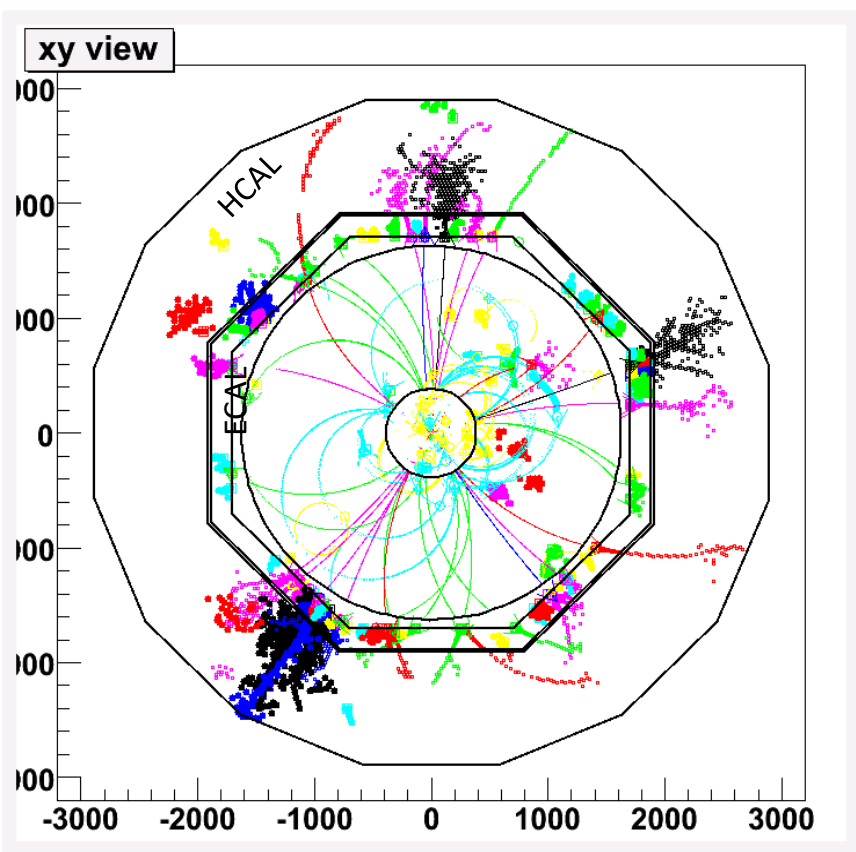
Rémi Cornat



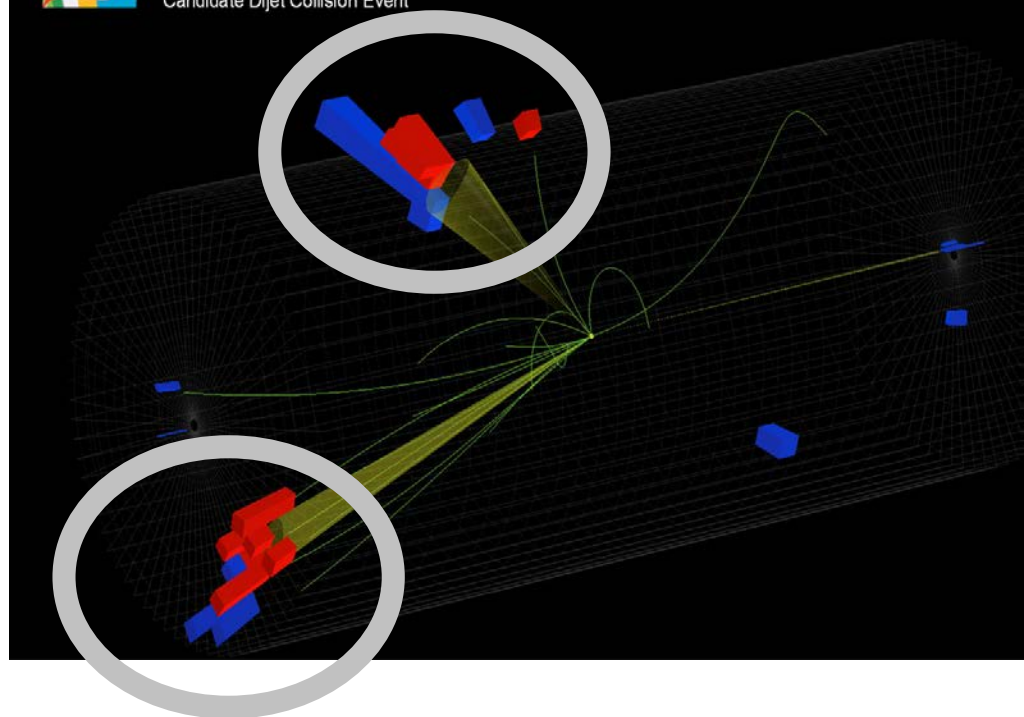
Highly granular calorimetry

From this...

to this :



CMS Experiment at the LHC, CERN
Date Recorded: 2009-12-06 07:18 GMT
Run/Event: 123596 / 6732761
Candidate Dijet Collision Event



A mix of technologies qualified with prototypes achieving
 $5000 < \text{“calorimeter grade” channels/dm}^3$,
ie. 16b dynamic, 10 to 12b resolution

Initially planned for ILC/ILD
Improved & Implemented for HGCAL@CMS
Inspiration for HGTD@ATLAS

CALICE Si-W ECAL prototypes : time line



Physics
prototype

Technological
prototype

ILD@ILC; x@FCC ; x@CPEC

Proof of concept

Achievability of
design options

Construction

- Linearity
- Resolution
- Sensors
- Very front-end

- Compactness
- Granularity
- Front-end
- Power pulsing
- 2m Long SLAB

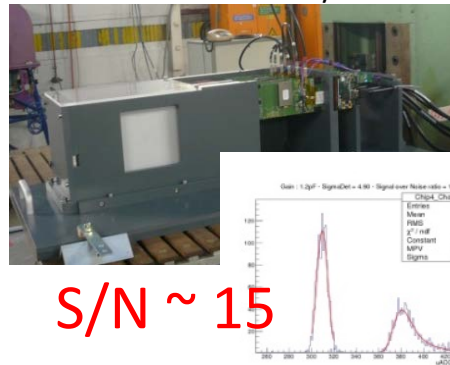
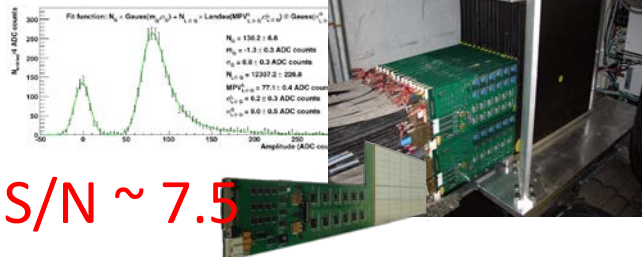
- Integration
- Environment
- Services
- Industrialization
- Tooling
- Project org.

1500 channels/dm³

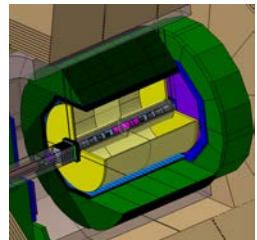
V1 : 4000 channels/dm³
V2 : 5000 channels/dm³

...10000 channels/dm³

2004-2008
30 layers
4000 channels



~24 X0, 20 cm thick
~2500 m² active detectors
~100M readout channels



Prototyping

Carbon – W
composite

LUR

ASIC (SKIROC)

ΩMEGA
Microelectronics

Simulation
Analysis

Cooling
system

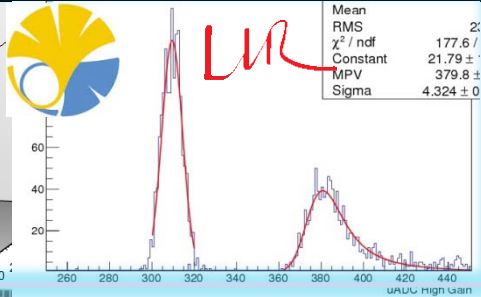
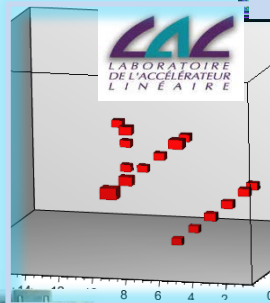
LPSC
Grenoble
Laboratoire de Physique
Subatomique et de Cosmologie

PIN diodes

LUR



KYUSHU UNIVERSITY



LUR

Sensor Gluing

LPNHE
PARIS

interconnects
integration

Power pulsing

LUR

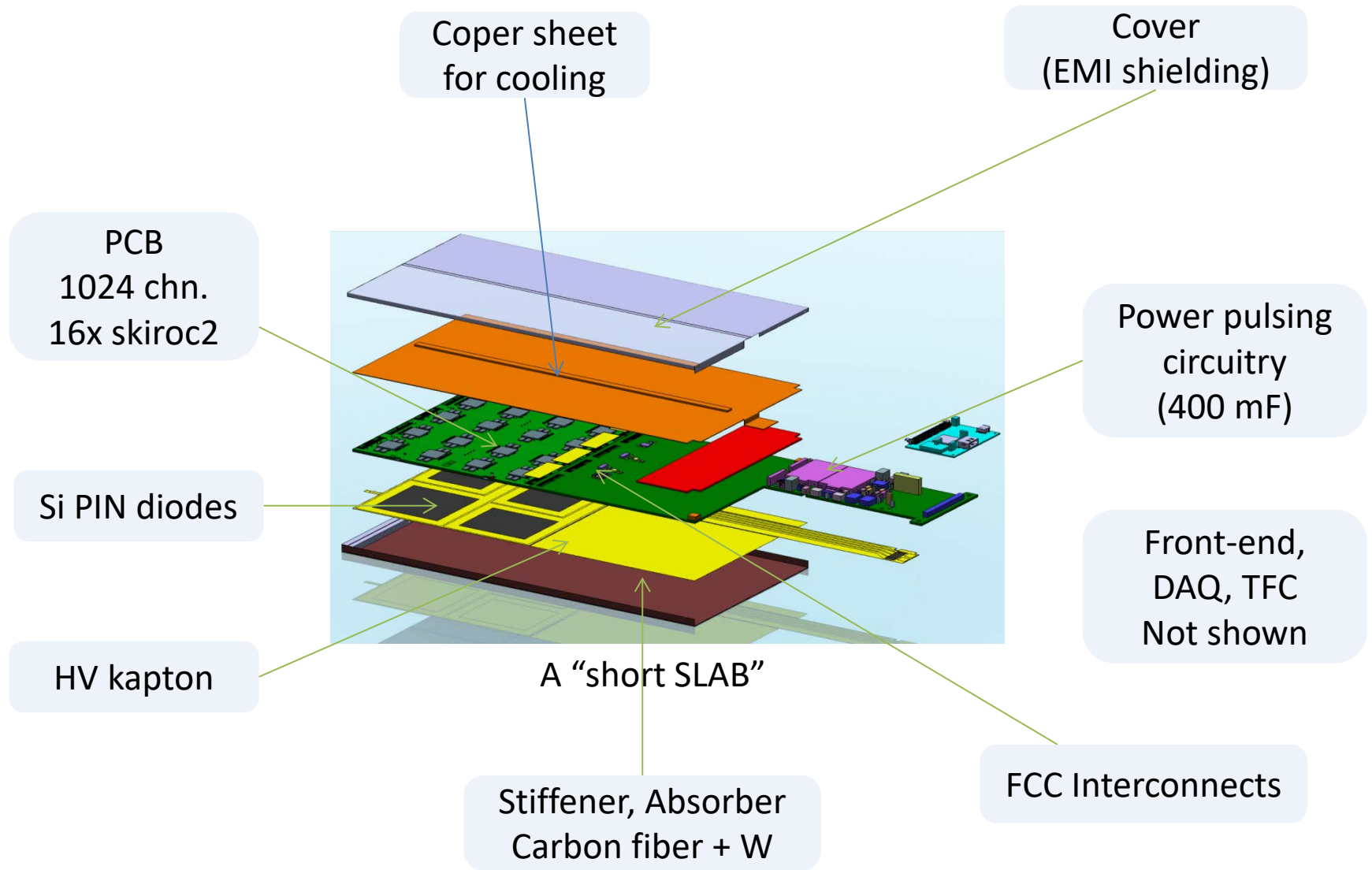
LUR DAQ

Front-end
board

LABORATOIRE
DE L'ACCELERATEUR
LINEAIRE

LABORATOIRE
DE L'ACCELERATEUR
LINEAIRE

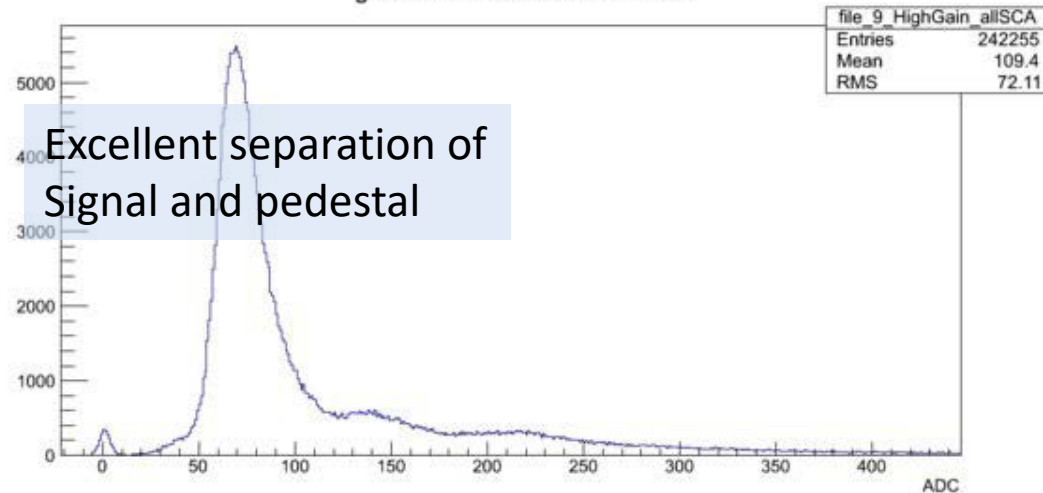
A detector module



Low energy (<6GeV e-) test beams @DESY 2012-2015

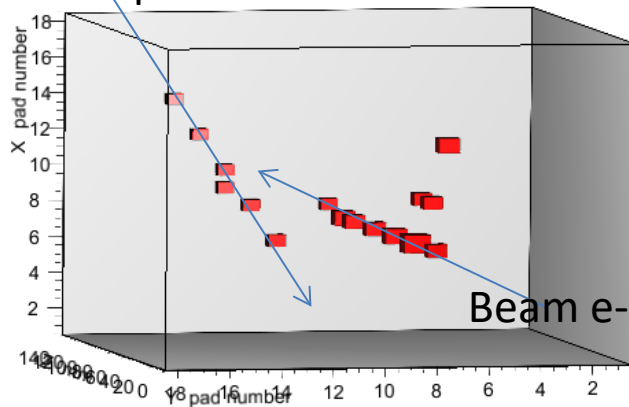
Typical channel

High Gain for all the SCA - file 9

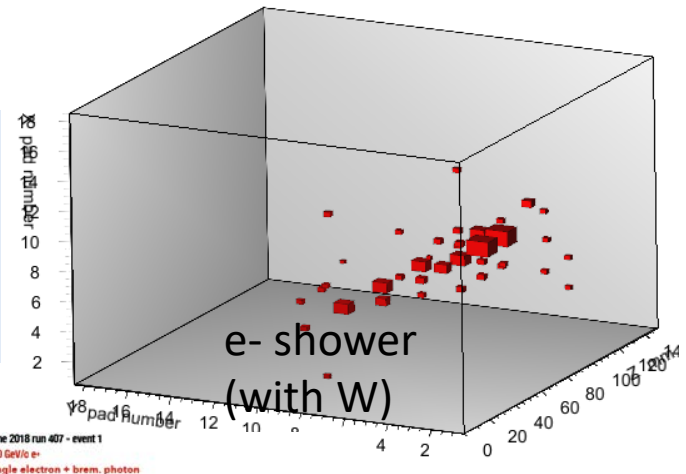


S/N = >15 better than the target (10), non uniformity understood (pixel-pcb capacitance)
Updated versions of DAQ, PCB & integration methods in 2019

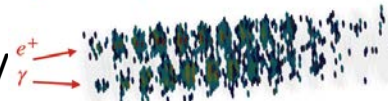
Cosmic μ



6 detector SLABS
1278 channels
10% off due to
out-of-range calib.

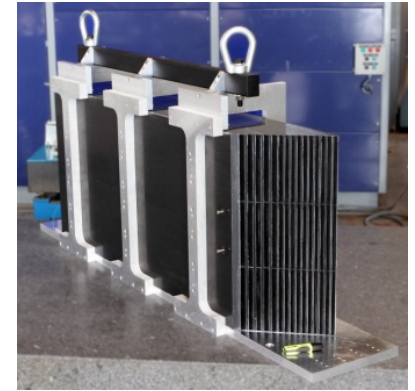
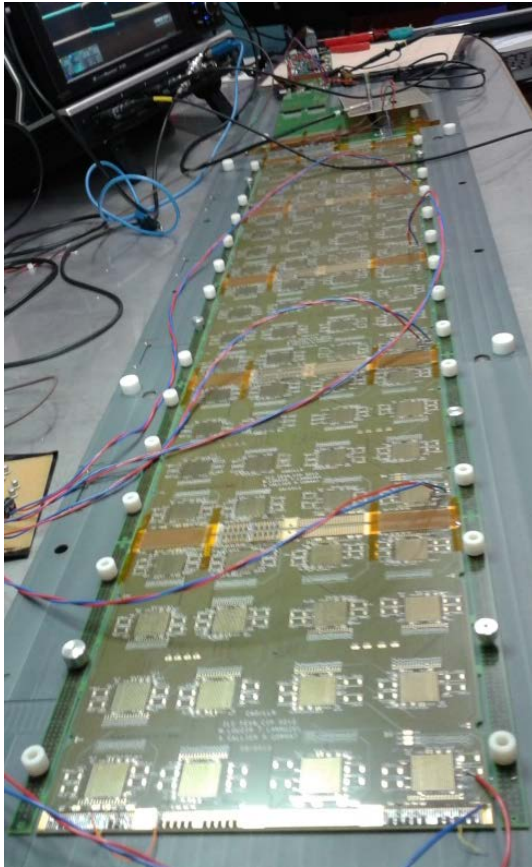


HGCAL 2020 : <https://indico.in2p3.fr/event/20042/>

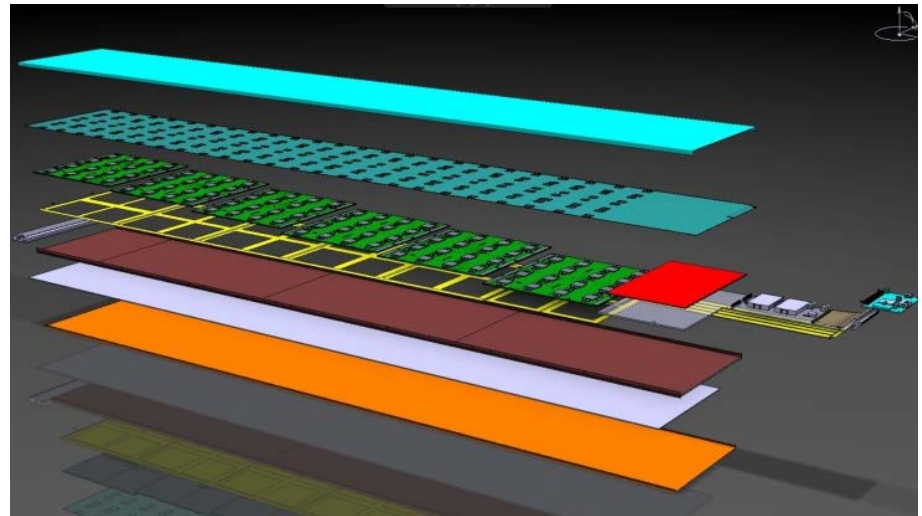


Toward a full length module

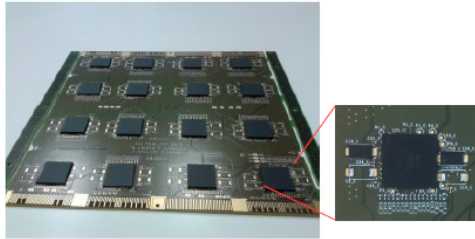
In principle, front-end boards will be chained forming up to 2m long detector SLAB, most of signals in bus



large C-W structure exists



Latest developments



DAQ@IJClab



The CORE mother



The CORE daughter



► BGA packaged chips

- Space for external decoupling capacitors
- Symmetric stacking will improve flatness,
- good for wafer gluing
- Optimal shielding of signal traces

Ultra thin PCB: Chip On Board

► **ILD tight spatial constrains:** Total space for ASICs and PCB 1.8mm (was 1.2mm since ~2007)

► **Chip-On-Board proposal:**

- Naked ASICs wirebonded.
- Cavities (~250um) for the ASICs

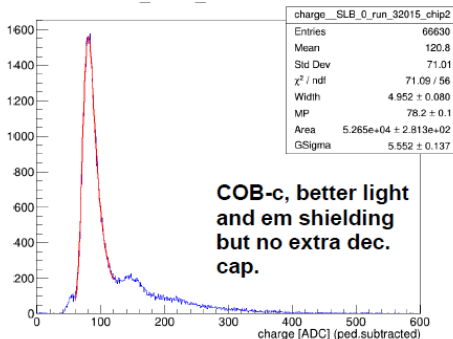
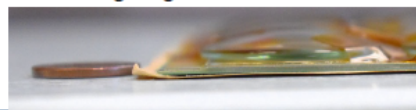
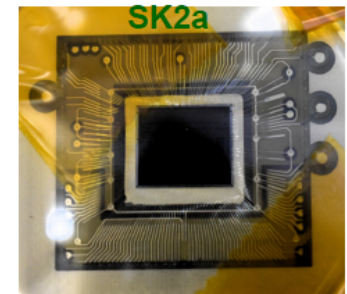
► **LAL & OMEGA** collaboration with **ITAEC/SKKU** (Sungkyunkwan University, Suwon – Korea) and **EOS** company for the PCB production.

► **10 FEV11_COB** produced.

- **1.2mm thickness** → 9 layers PCB !
- **Good Planarity** (metrology made in LAL) and electrical response.
- **No extra components** (i.e. decoupling capacitances, etc)

► **4 boards wirebonded** at **CERN** bonding lab. Also In contact with **CAPTINNOV** Platform.

- Extensively tested at LAL before gluing a full size sensor to them

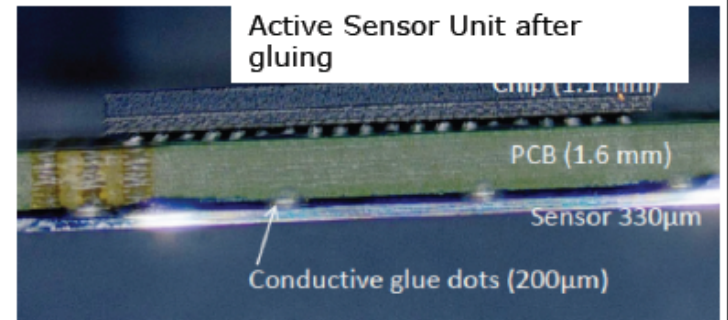
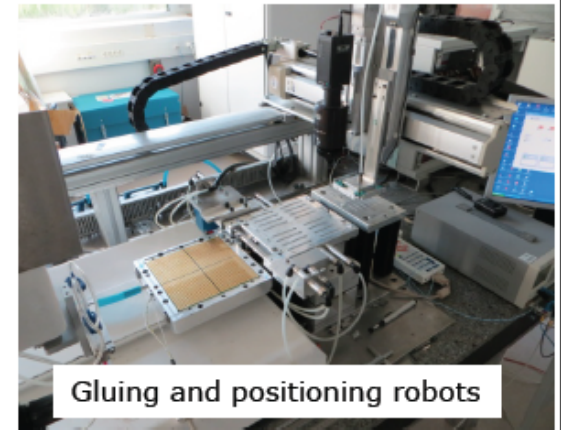


COB-c, better light and em shielding but no extra dec. cap.

Courtesy R. Poeschl, A. Irles, J. Malmi

Contribution of LPNHE

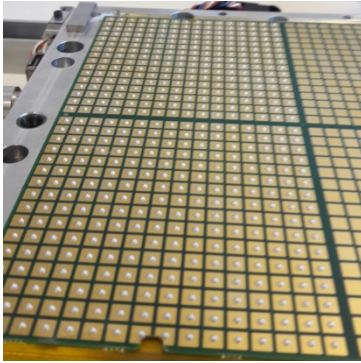
- Assembly done with gluing and positioning robots: automated system developed in the framework of the Calice R&D program for ILD SiW EM calorimeter
- **Assembly of the ultra flat active sensor unit (Chip On Board design) in 2019**
- Electrical test to control the sensors before gluing, to check the short cuts immediately after gluing, to measure the $I(V)$ curves
- PCB Metrology using a coordinate measuring machine (tri-dim machine)



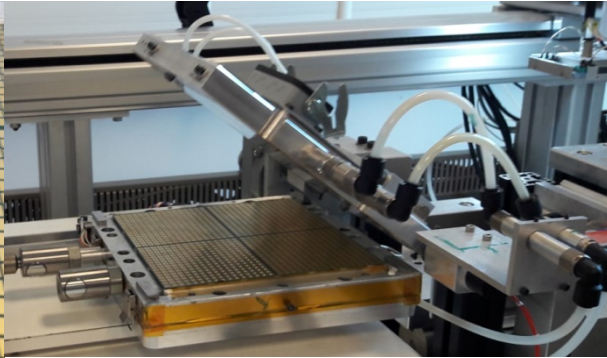
- Industrialization of the process considered – preliminary contacts with Eolane company
- Measurements are compliant with HPK data - Monthly survey has started – Wafers kept in a dry cabinet
- Metrology: Latest FEV12 batch (24 boards) is 100% within tolerances
- Software permanently updated with Python

Technical skills at LPNHE

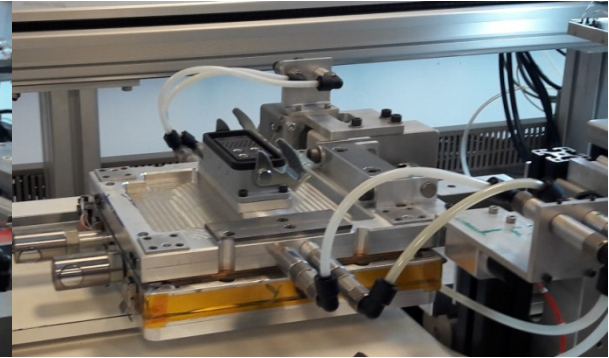
Glue dispensing



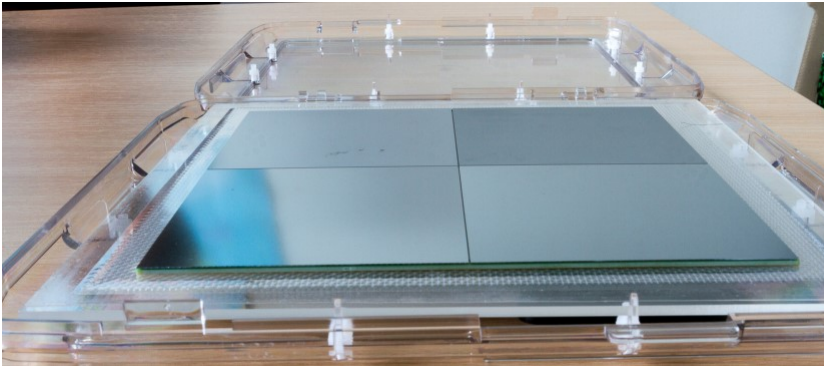
PCB-Sensors alignment



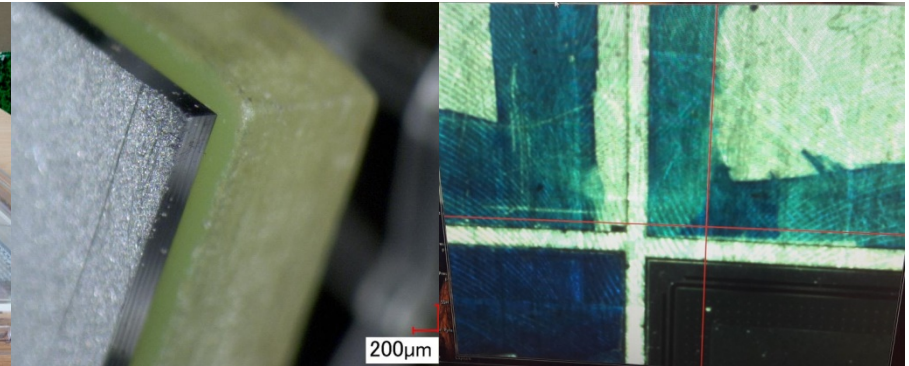
Sensors gluing



Active module sensors + PCB + VFE



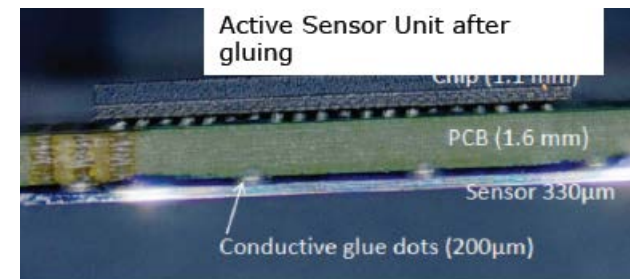
Reproducible positioning @ $\sigma < 25\mu\text{m}$



Developing dedicated robots, with reproducible movements $\sigma < 25\mu\text{m}$: glue dispensing, Si detector hybridation & metrology

Ability to machine and assemble precision mechanics (bearings, gears, guides...)

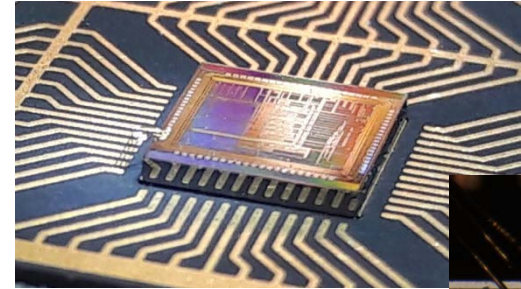
Semiconductor characterization



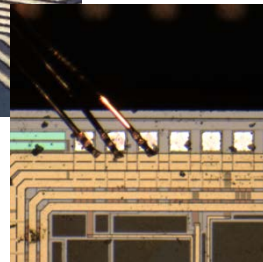
What next ?

Continue module assembly for next **Calice** tesbeams (Q4'20,...)

Developing skills in wirebonding (wedge bonding)



HGTD : gluing process



Calice & **AIDA**innova :
electronics integration = miniaturization and minimizing power consumption

In the case of an approved R&D :
Industrial transfer of the gluing & hybridation process

