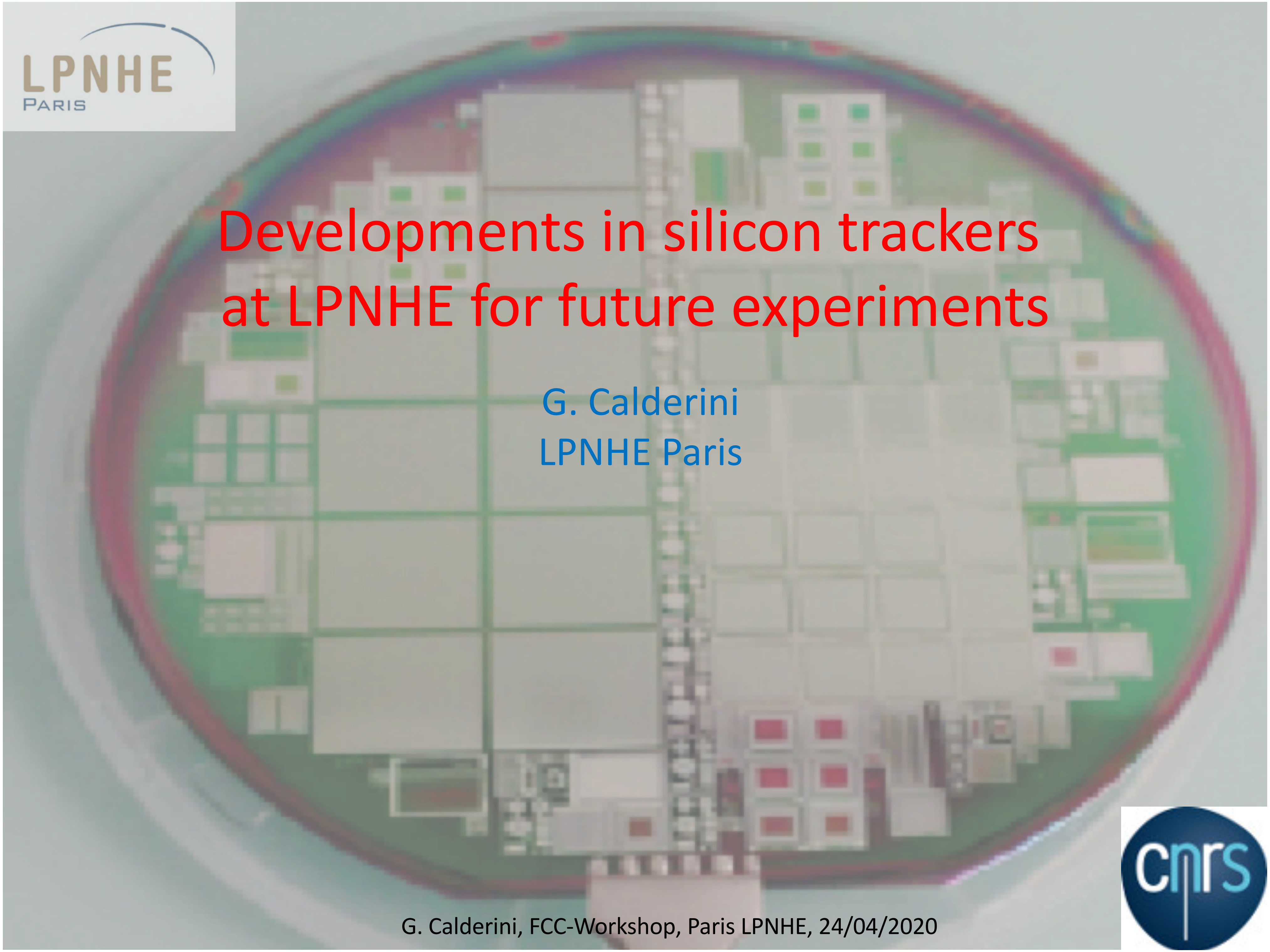


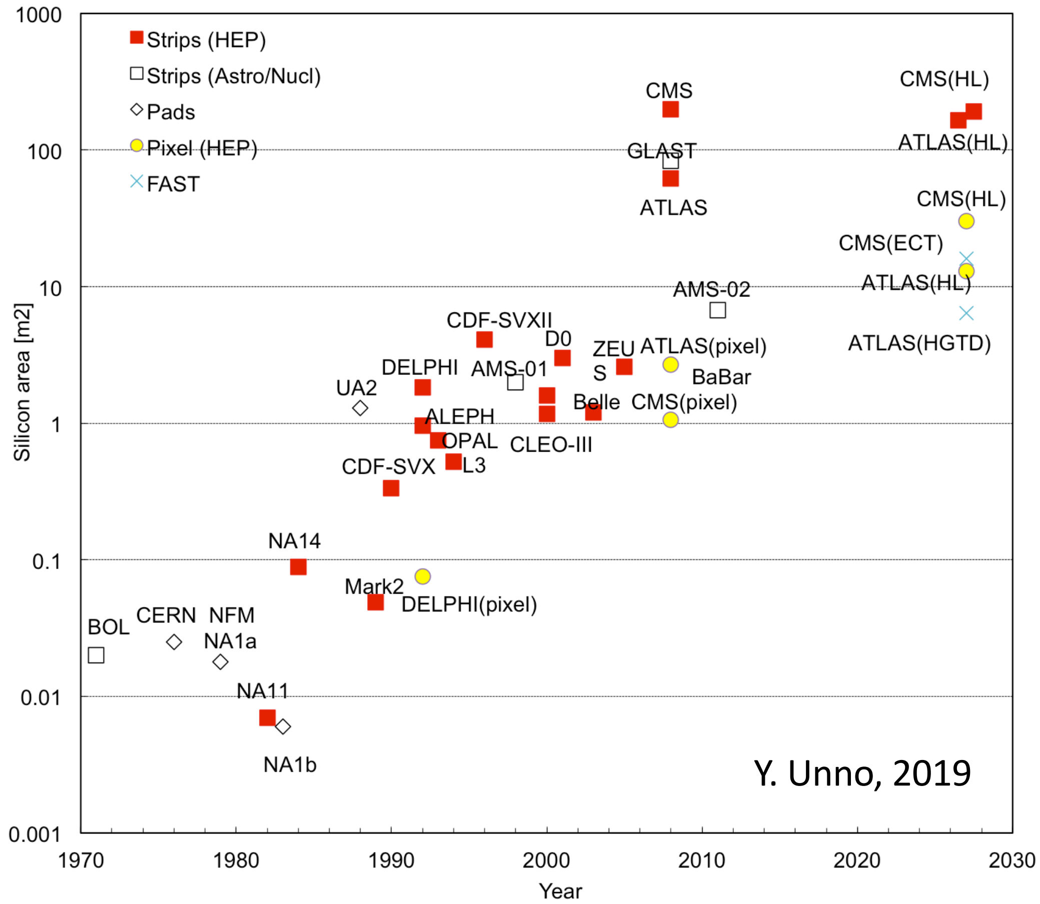
Developments in silicon trackers at LPNHE for future experiments

G. Calderini
LPNHE Paris

Since the ‘90s, silicon trackers played a crucial role in HEP experiments

Running conditions and detector requirements have changed a lot in these 40 years

Surface has increased exponentially, requirements in terms of dataflow, radiation hardness, material budget, number of channels



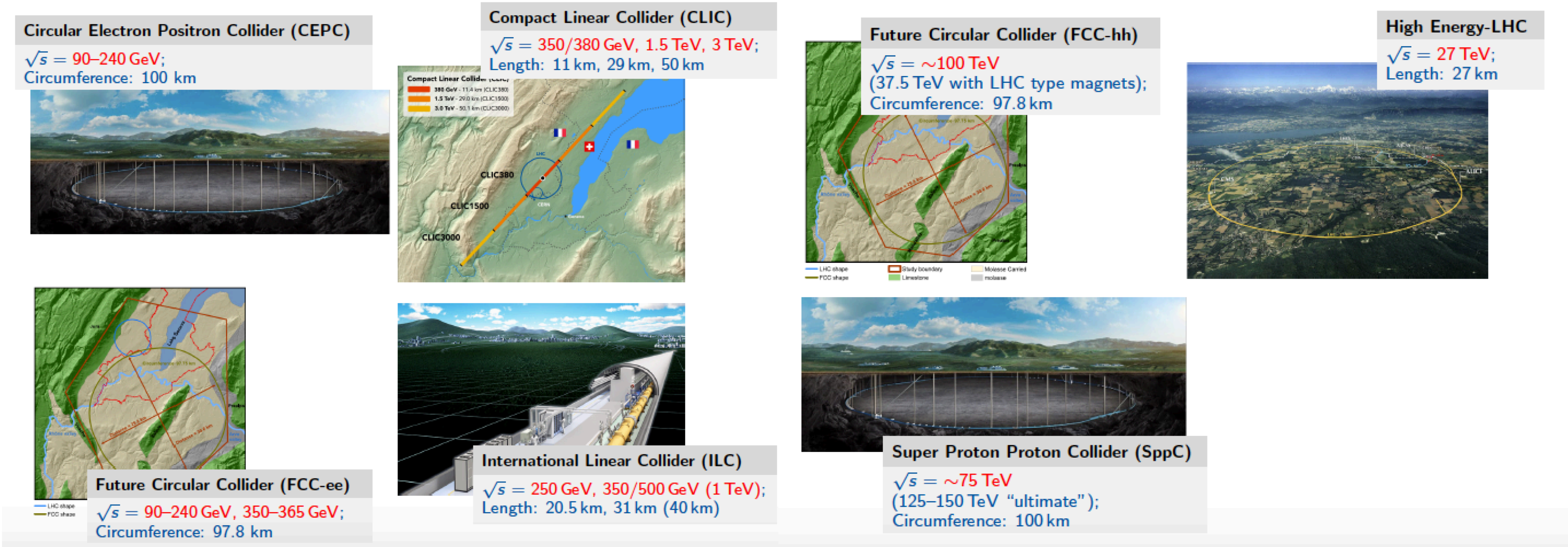
Pixels have been recently the core of most silicon tracking systems, where the running conditions are the most critical

Constant evolution which will continue in the next years for the next experiments

The required technology development for sensor, readout electronics and infrastructure (mechanics, cooling) is very different as a function of the machine

High-energy e+e- collider proposals

High-energy hadron collider proposals



At LPNHE we develop aspects of trackers which will be very important for the two classes of machines. I will concentrate on sensors and advanced cooling structures. We are also on other aspects.

For recent developments outside what we do at LPNHE, you can have examples in my previous FCC-France presentation.
https://indico.in2p3.fr/event/19693/contributions/76083/attachments/55956/74003/FCC-calderini.pdf

Silicon vertex and tracking detector parameters

Parameter / Exp.	LHC	HL-LHC	FCC-hh	FCC-ee	CLIC 3 TeV
Fluence [$n_{eq}/cm^2/y$]	N x 10^{15}	10^{16}	10^{16} - 10^{17}	<10^{10}	<10^{11}
Max. hit rate [$s^{-1}cm^{-2}$]	100 M	2-4 G****)	20 G	20 M ***)	240k
Surface inner tracker [m^2]	2	10	15	1	1
Surface outer tracker [m^2]	200	200	400	200	140
Material budget per detection layer [X_0]	0.3%*) - 2%	0.1%*) - 2%	1%	0.3%	0.2%
Pixel size inner layers [μm^2]	100x150-50x400	~50x50	25x50	25x25	<~25x25
BC spacing [ns]	25	25	25	20-3400	0.5
Hit time resolution [ns]	<~25–1k*)	0.2**)–1k*)	~10^{-2}	~1k ***)	~5

*) ALICE requirement **) LHCb requirement ***) At Z-pole running ****) max. output rate for LHCb/high intensity flavour experiments: 300-400 Gbit/s/cm²

Hadron colliders

- Very high radiation levels: $\leq 10^{18} n_{eq}/cm^2$
- Very high hit rates
- Very precise timing: $\leq$O(5 ps)

Lepton colliders

- Very small single point resolution ($\leq 3\,\mu m$)
- Very low material budget ($\leq 0.2\% X_0$/layer)

Remarks

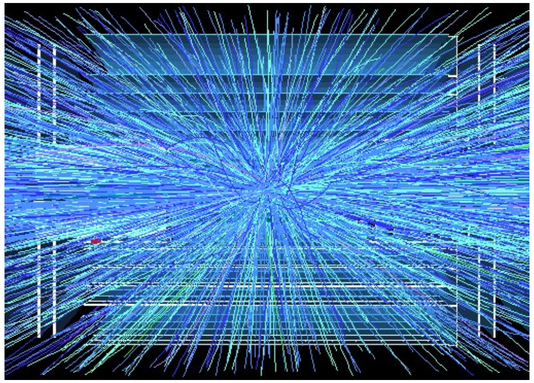
- Note that ps-level timing was not part of initial HL-LHC detector requirements
- Became available through pioneering R&D on LGAD / MCP / precise timing with silicon
- Now well motivated for vertex separation / pattern reconstruction

Fighting against radiation

This is one of the key features we developed for HL-LHC sensors

Instantaneous conditions

- pileup and high event rate
- increased occupancy



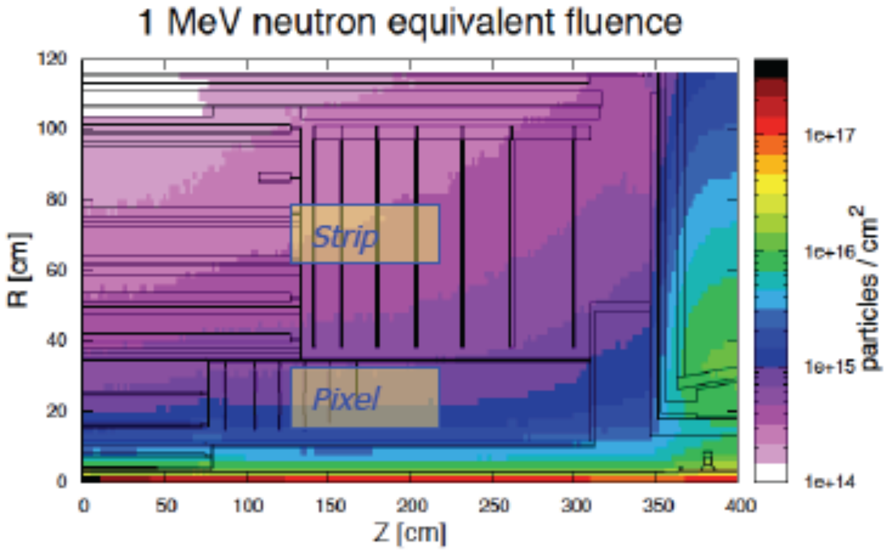
- higher granularity sensor
- SEU-robust, fast readout

- *Peak luminosity:* 5-7 x 10^{34} $cm^{-2}s^{-1}$ → ~x5-7
- *Average pile-up:* up to <μ> ~200 → ~x8
- *Integrated luminosity:* 3000 fb^{-1} → ~x10
- Requested *radiation hardness:* $2x10^{16}$ n_{eq}/cm^2 → x20

Integrated effects (radiation dose)

- leakage current
- change in operation voltage
- reduced charge collection

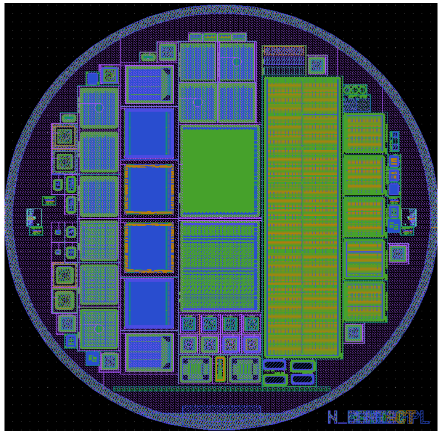
- rad-hard components
- thin sensors (partial depletion)

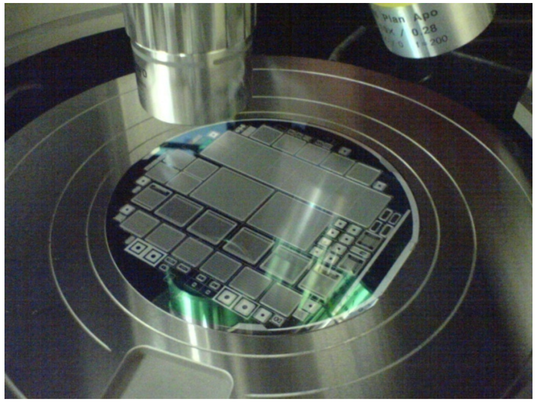


Many LPNHE productions in collaboration with FBK Trento

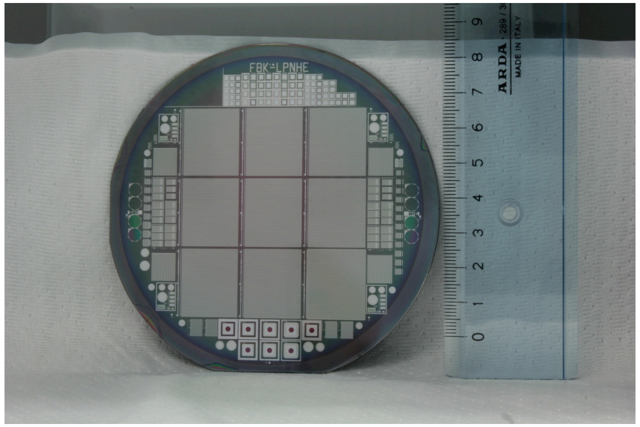
Increasing performance with respect to radiation and track multiplicity in the event

2012

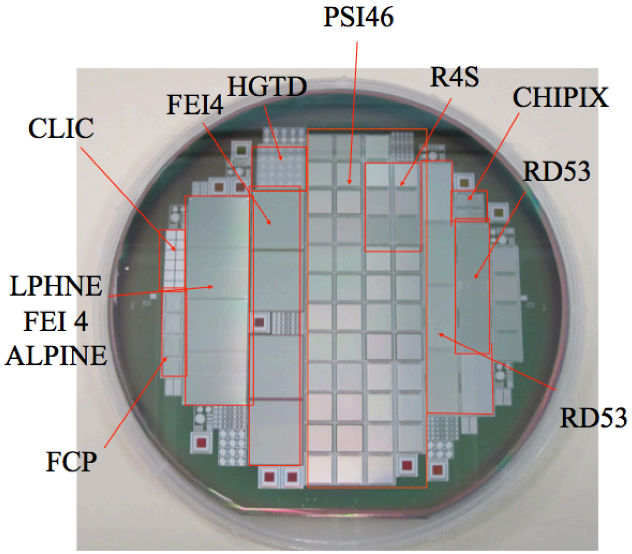




2014

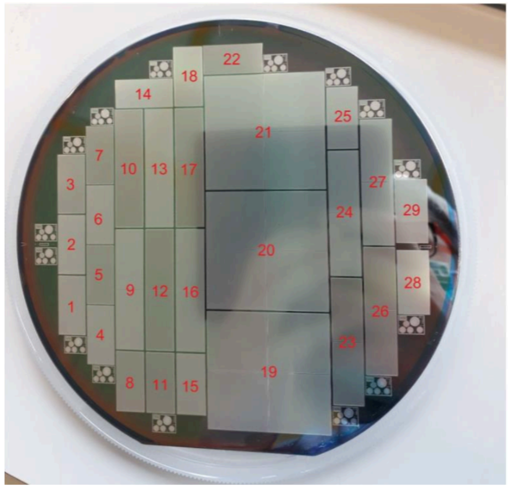


50x400 and 50x250 pixels with and without active edges; 200um thick



2016, 6-inch

50 x 250
50x50
25x100
Thin sensors
100-130 um



2018, 6-inch

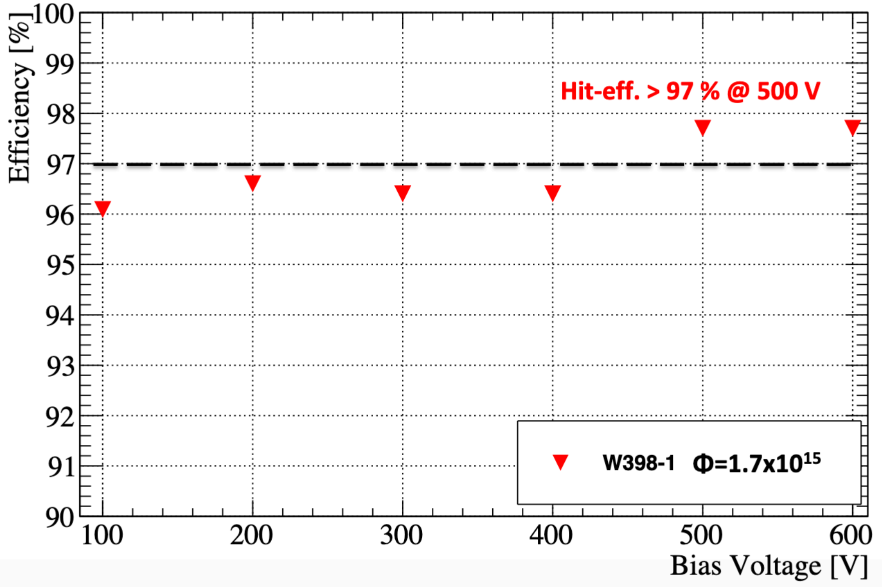
50x50
25x100
Thickness down to 50 and 100um

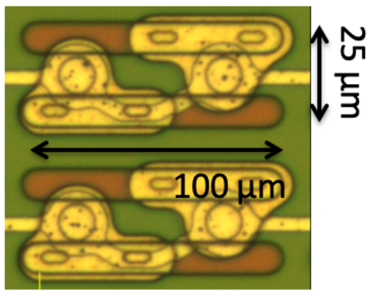
Common ATLAS-CMS

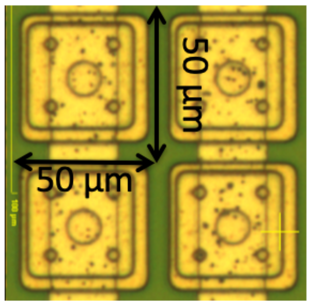
Hit efficiency after irradiation

Thanks to the reduced sensor thickness, the hit performance is still significantly high (>97%) even after irradiation

Hit efficiency

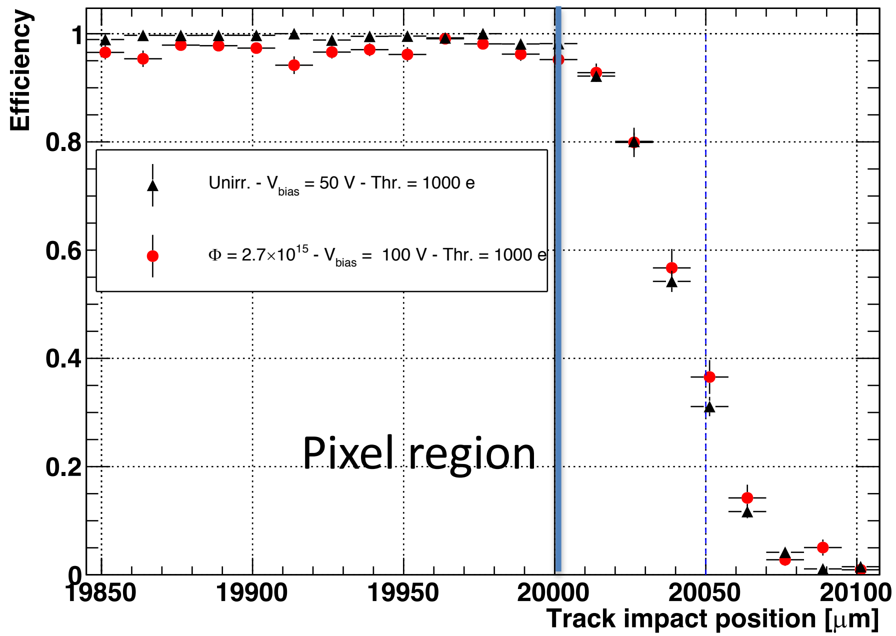






For productions featuring the active edge (deep trench) technology, the efficiency is still significant at a few tens of microns from the last pixel

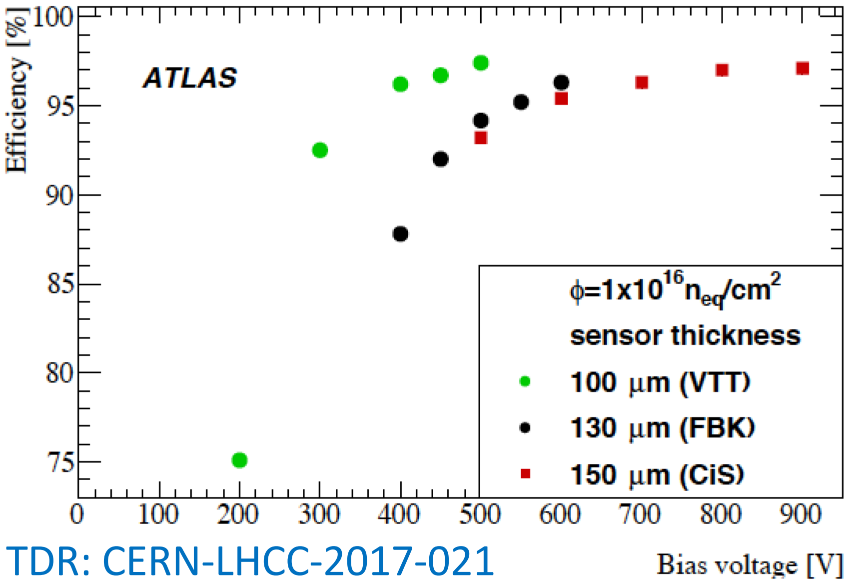
Guard ring region



Thin sensors are very performant with respect to radiation damage but also for material budget

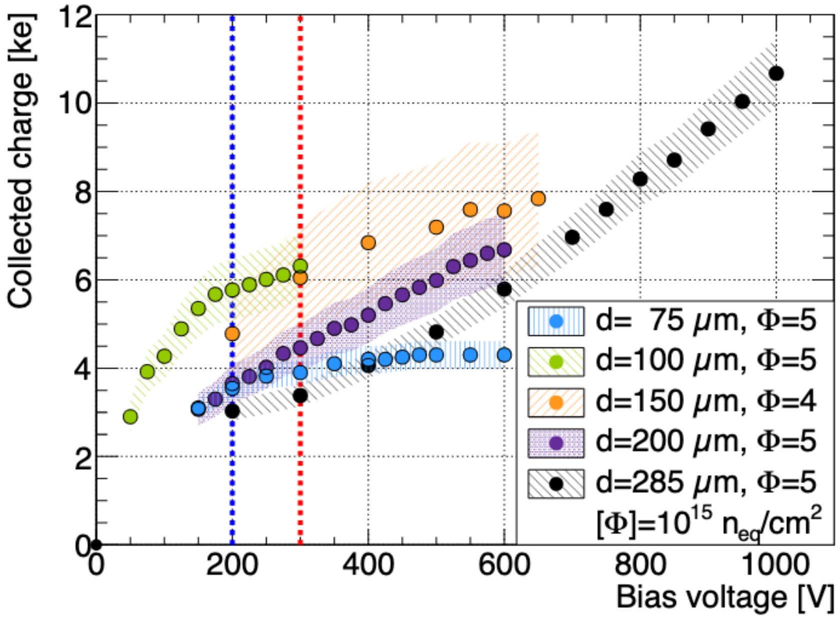
After heavy irradiation the bulk cannot be fully depleted anymore. Interest to go thin!

- After irradiation, reduced collection distance, thin sensor can be optimal
- Stronger electric field, faster collection
- Lower power dissipation
- Lower occupancy at high eta
- Less material budget



ITk TDR: CERN-LHCC-2017-021

arXiv:1612.01281



Even at very high fluence (for planar pixels), thin sensor can guarantee an excellent hit reconstruction efficiency

Small pitch limitations

Small pitch could limited by interconnection techniques

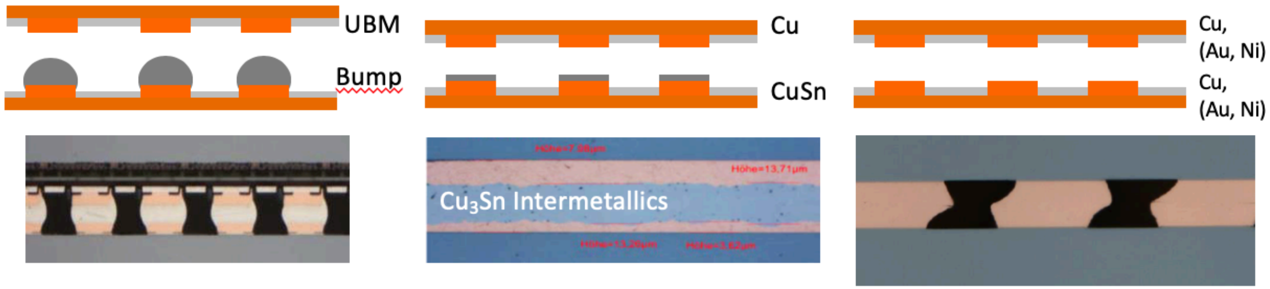
Standard solder bump bonding, but also copper pillars, is in general limited to a pixel dimension of at least few tens of microns

Advanced techniques can be used to overtake this limit

Fraunhofer
IZM

T. Fritzsch, AIDA-2020 workshop

Solder Bump Bonding	Transient Liquid Phase Bonding (TLPB/SLID)	Metal-Metal Direct Bonding



Solder Bump Bonding
- ECD solder bumps (SnAg, In, InSn, AuSn, Cu-pillar/Sn cap)
- Reflow temperature
- without or low pressure

Transient Liquid Phase Bonding (TLPB/SLID)
- ECD Cu and Cu-Sn pads
- High melting Cu_3Sn IMC
- Temperature, pressure

Metal-Metal Direct Bonding
- ECD pads (Cu, Au, Ni)
- Planarized surfaces, pre-conditioning
- Temperature, pressure

CHIP TO WAFER | CHIP TO WAFER; WAFER TO WAFER BONDING

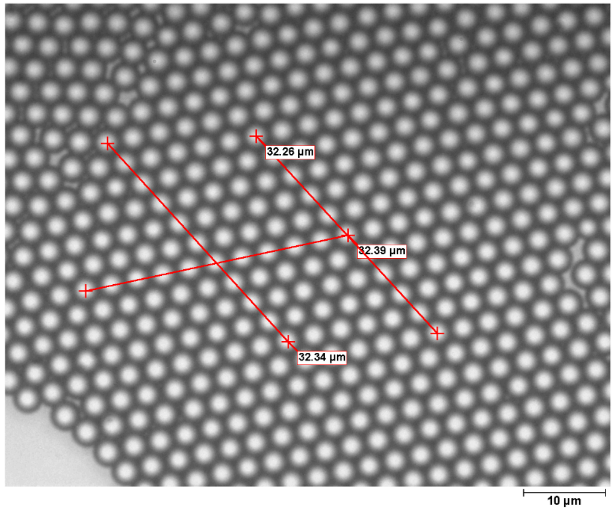
Anisotropic conductive films (ACF): LPNHE in the AIDAinnova

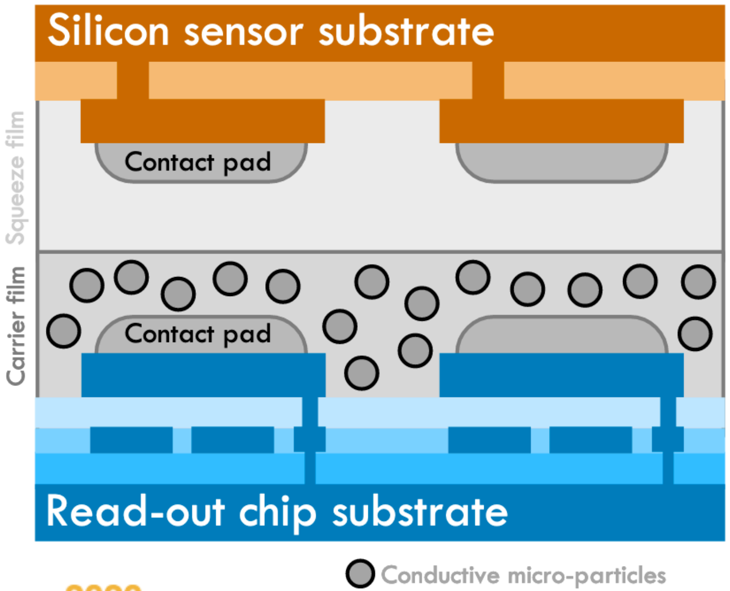
Anisotropic conductive films can also be used as interconnection technique

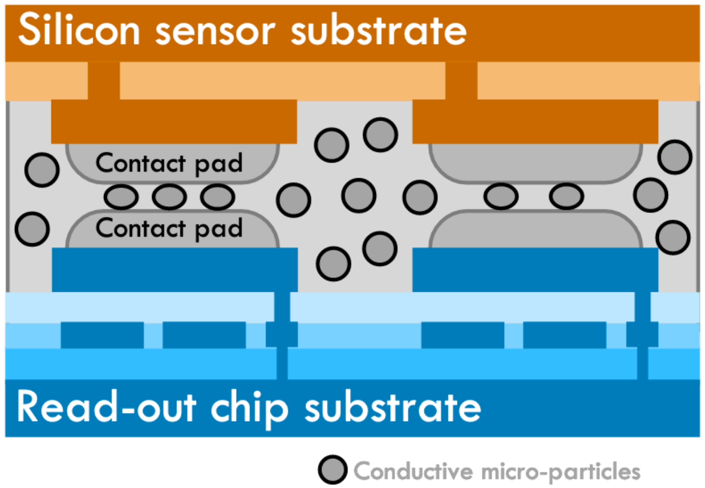
Application potentially important also from the cost point of view

Bump-bonding represent a significant fraction of the hybridization cost of pixel modules

Development is also part of AIDAinnova proposal in the hybrid detectors Working Package







M. Vicente, D. Dannheim et al.

Advanced cooling structures

Microchannels at LPNHE

Reducing material budget: a transversal challenge

Reducing the sensor thickness is not the only key to reduce the material budget

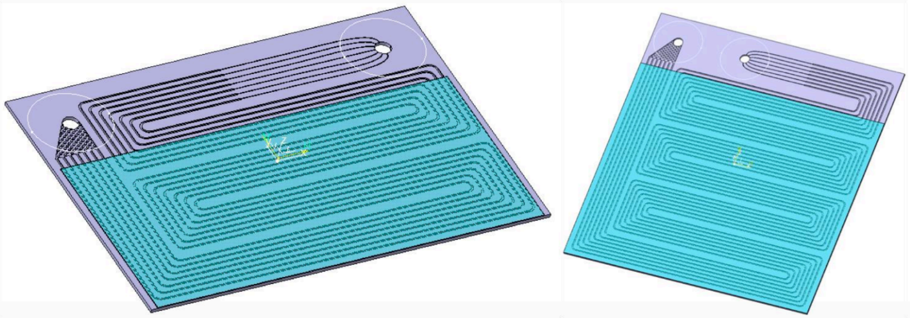
A significant fraction of x/x0 is brought by the services

Since a few years the LPNHE group is developing light cooling structures in the framework of the REFLECS, REFLECS2 project (M. Bomben) and of AIDA-2020

Micro-channel structures developed following two axes:

- develop cooling blocks for our silicon modules
- develop structures able to study the evaporative behaviour of CO_2 in channels and compare with models

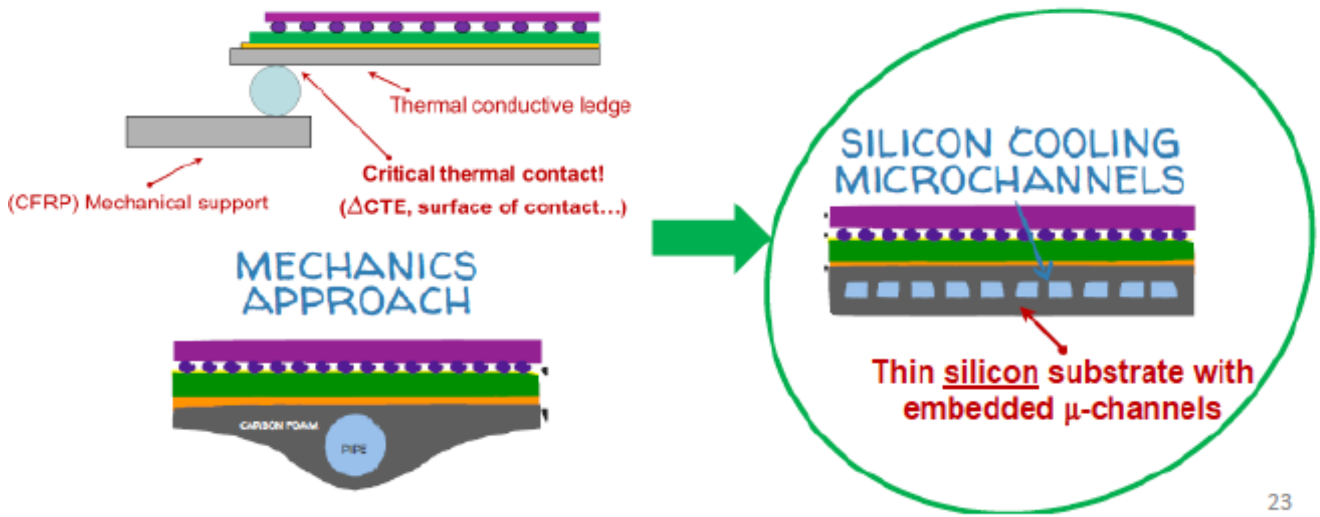
"Snake" design microchannel cooling unit size		
Design	Width [mm]	Height [mm]
Single	30.0	30.0
Double	30.0	41.3
Quad	42.4	48.0



Micro-channel cooling

More uniform cooling, less material in the system, less cooling fluid (strong point in industrial applications)

Already used in existing trackers (NA62, LHCb) but challenging at ATLAS/CMS; CO_2 pressure of tens of atmospheres!



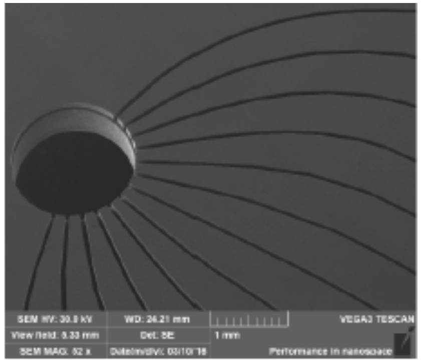
Much better cooling Thermal Figure of Merit (TFM) due to CO_2 evaporation and to uniform distribution of cooling structure

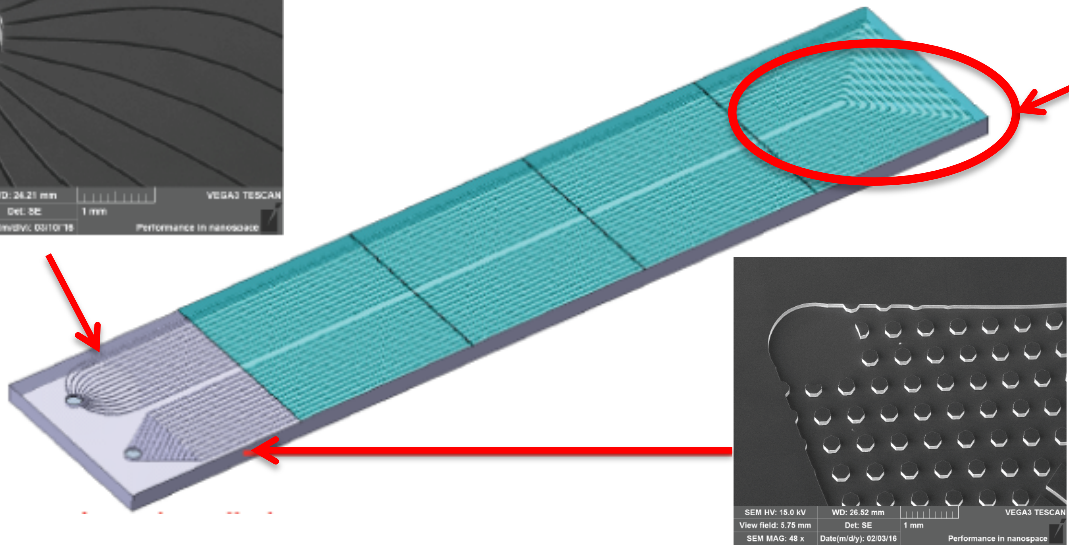
This technology can be used not only in hybrid pixels but channels can be carved directly in the readout chip. AIDAinnova development for CMOS

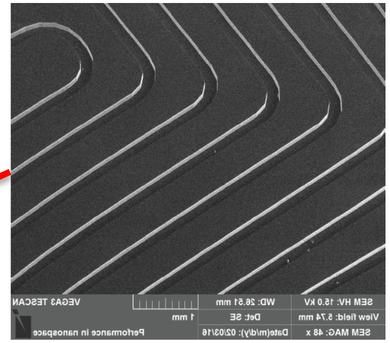
Prototypes produced by LPNHE with FBK and IEF Orsay

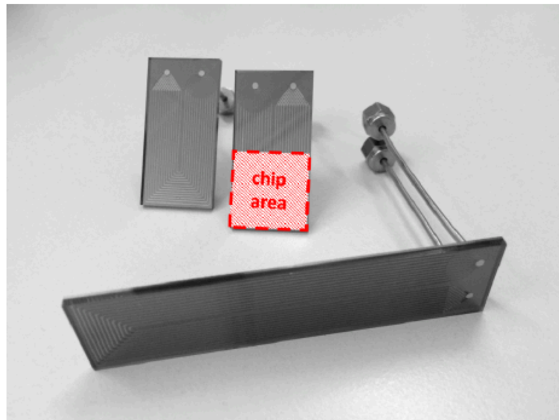
Details of the channel design

13 channels 200x120 um
Silicon walls 500um
Inlet restrictions 60x120um: same lenght 6mm for all
Inlet outlet holes 1.6 mm diameter
Pillars in the outlet: 350um diameter

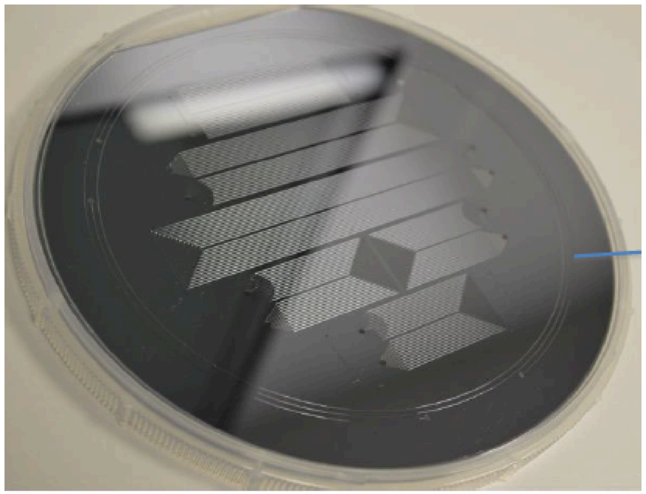


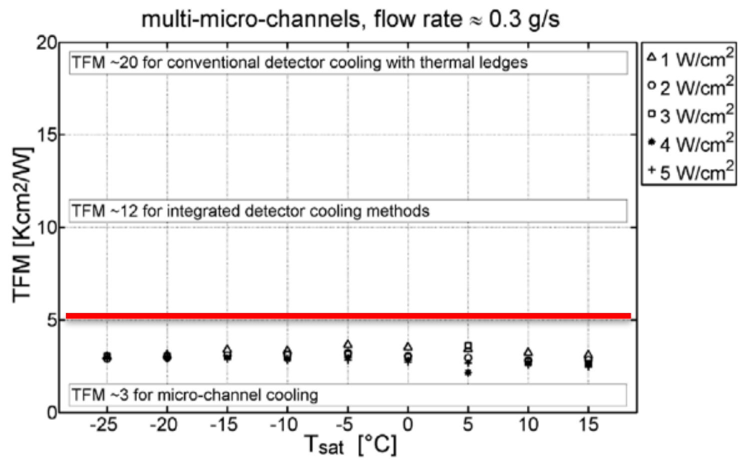






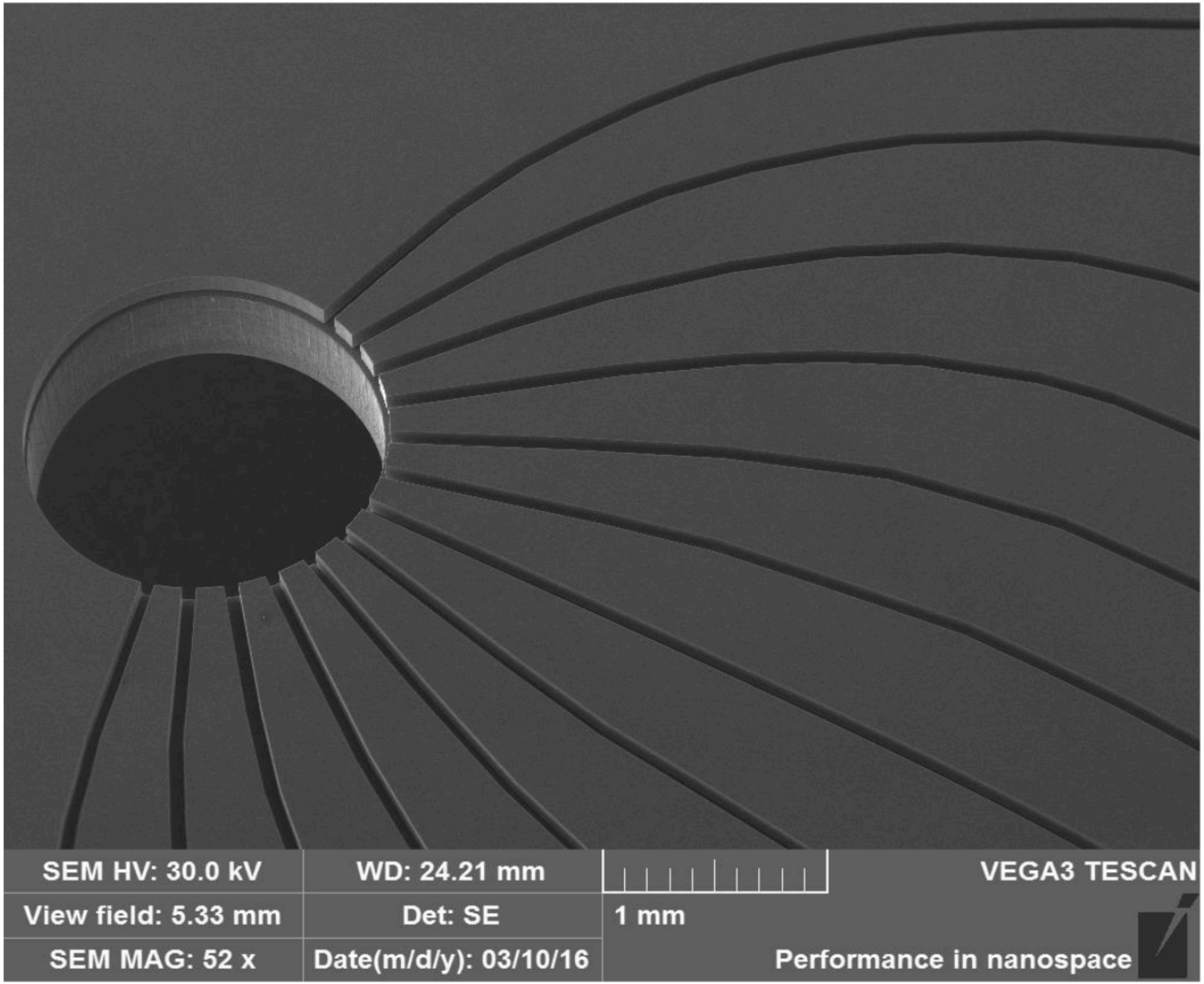
D.Hellenschmidt, M.Bomben, G.Calderini et al,
Nucl. Instrum. Meth. A 958 (2020) 162535



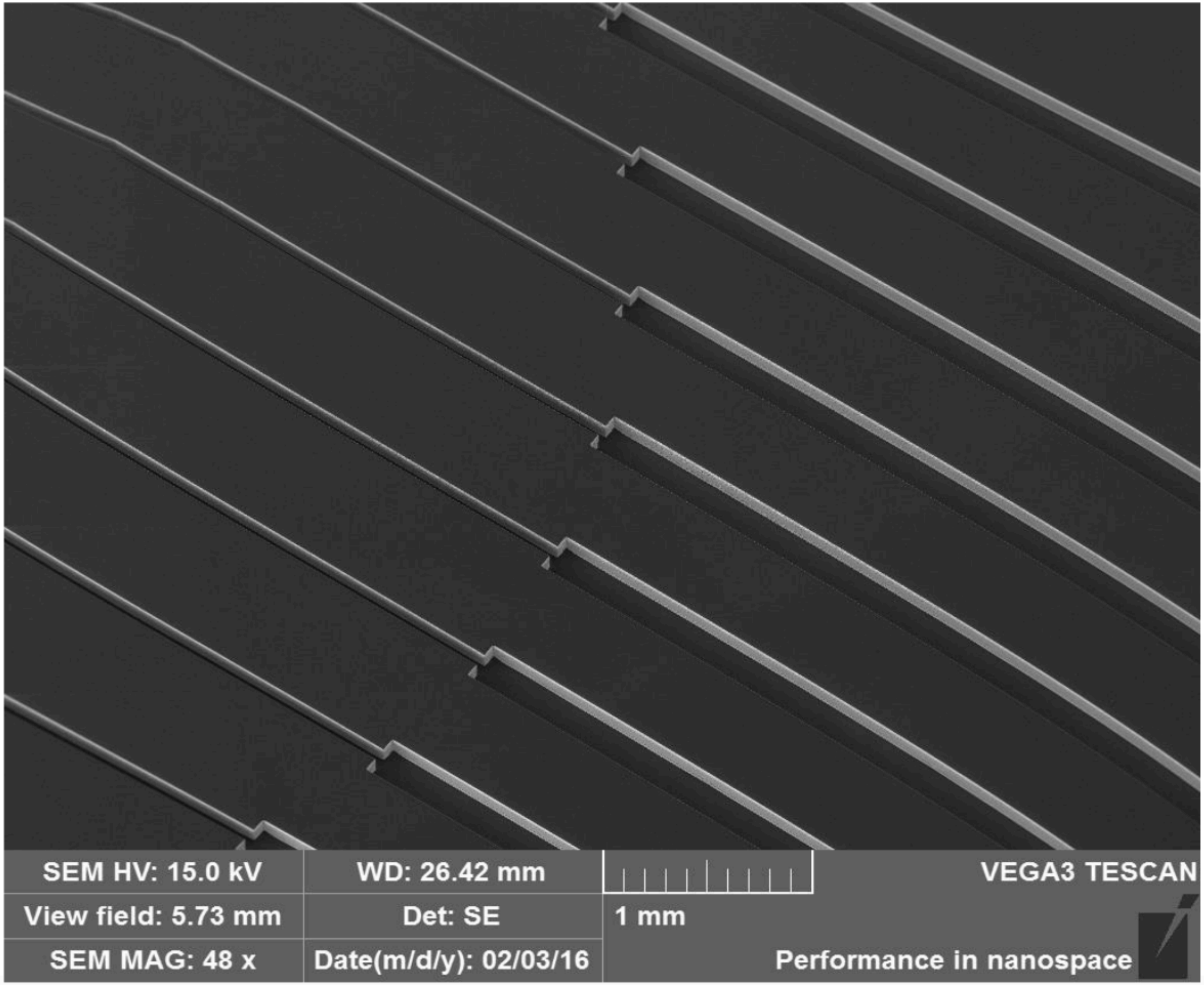


FONDAZIONE
BRUNO KESSLER

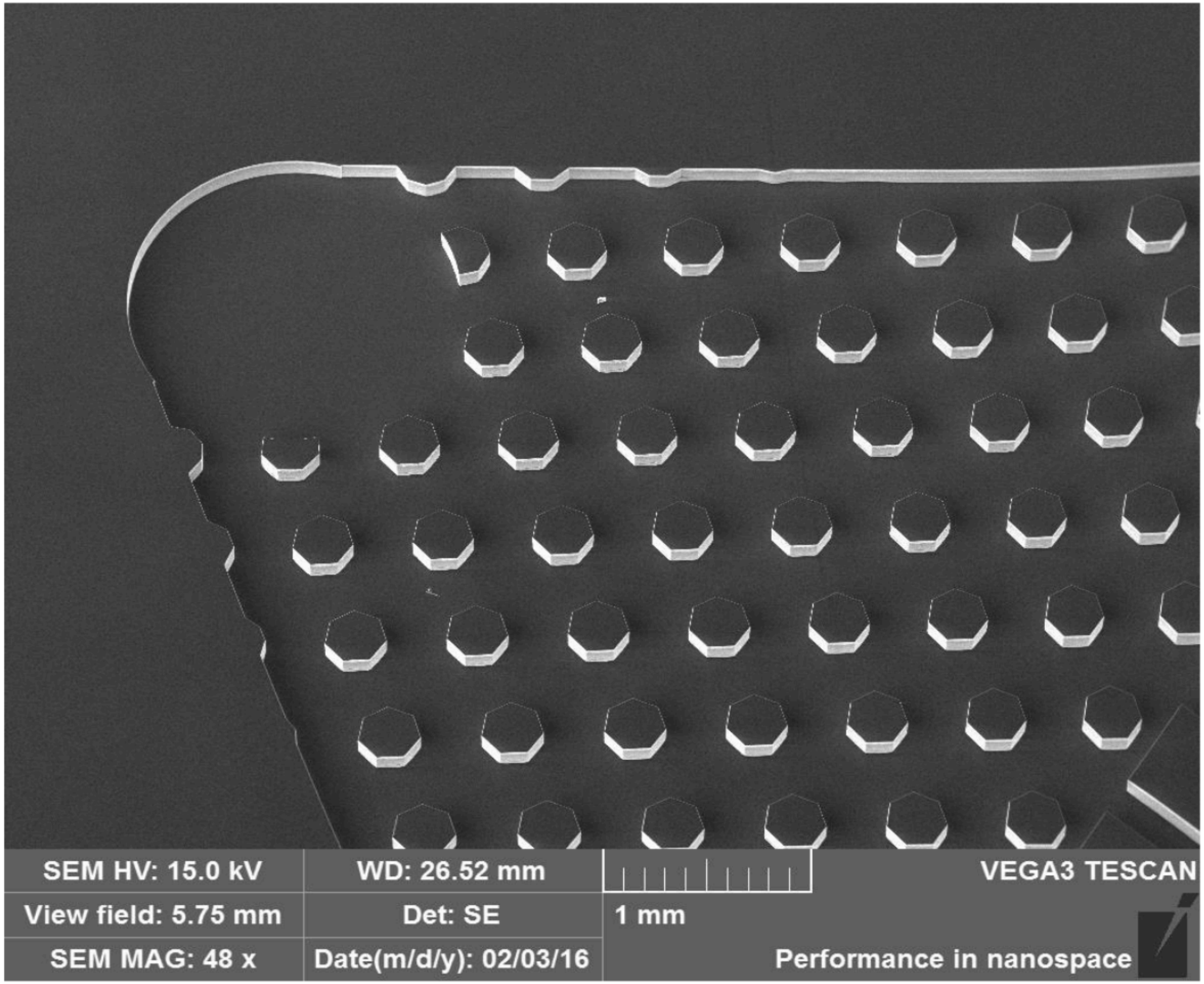
Inlet fanout



Channel size modulation to control CO2 boiling



Detail of the outlet; pillars to reduce the surface (force) on the plexiglass cover



FONDAZIONE BRUNO KESSLER

Conclusions

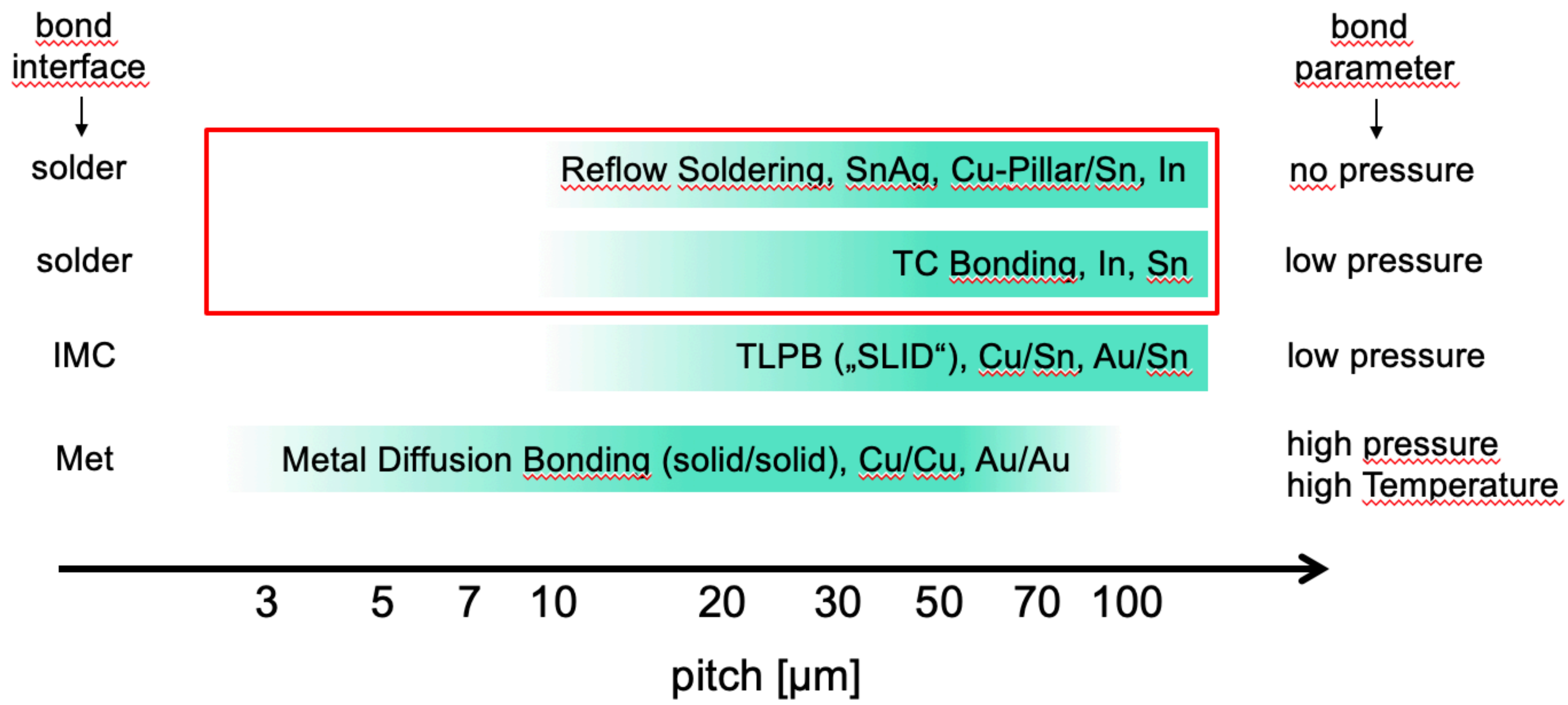
The data-taking conditions at colliders have evolved towards challenging tracking environments over the last 30 years

In parallel, a lot of technological progress has been made in detectors and in silicon trackers in particular, to cope with these new conditions

Different families of devices have been developed at LPNHE to match specific contexts; I went through some examples, there are more.

I tried to give snapshots of some areas in which there were significant recent improvements, but there are many more!

For each future machine there is already a tracker solution which is developing, but technology will evolve even more in the meantime

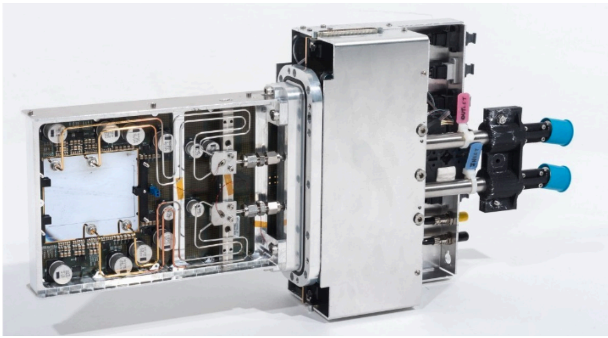

bond interface
solder
solder
IMC
Met
Reflow Soldering, SnAg, Cu-Pillar/Sn, In
TC Bonding, In, Sn
TLPB („SLID“), Cu/Sn, Au/Sn
Metal Diffusion Bonding (solid/solid), Cu/Cu, Au/Au
bond parameter
no pressure
low pressure
low pressure
high pressure
high Temperature
3
5
7
10
20
30
50
70
100
pitch [µm]

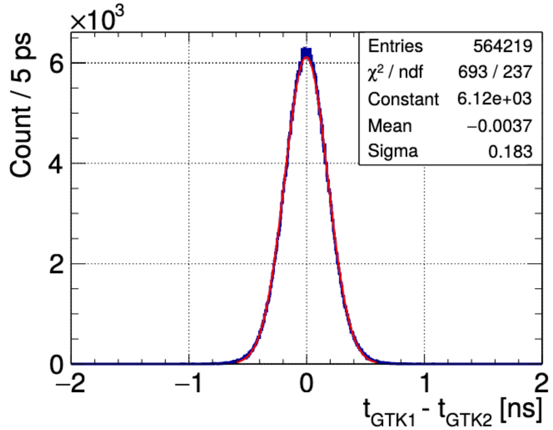
Importance of 4th coordinate: Timing

Fourth dimension is the next step of the new generations of trackers

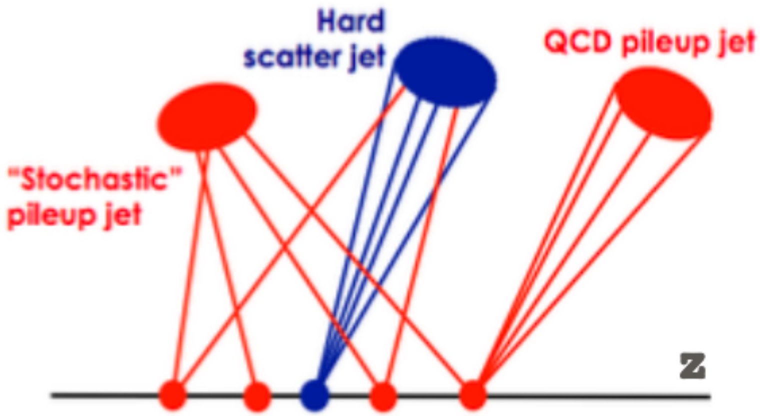
Will be able to solve ambiguities due to fast bunch crossing or pileup

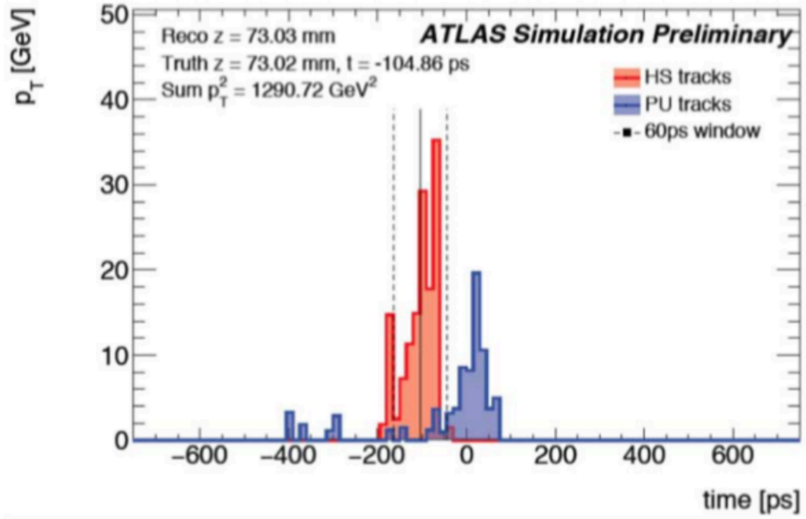
NA62 Collaboration led the path, with a resolution per station of the order of 180 ps





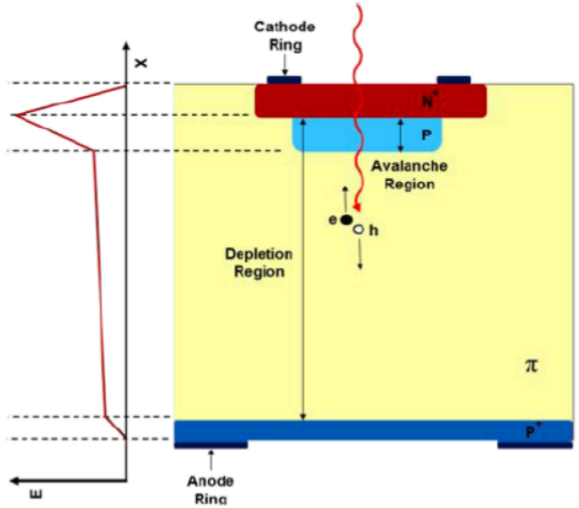
ATLAS/CMS developing timing layers





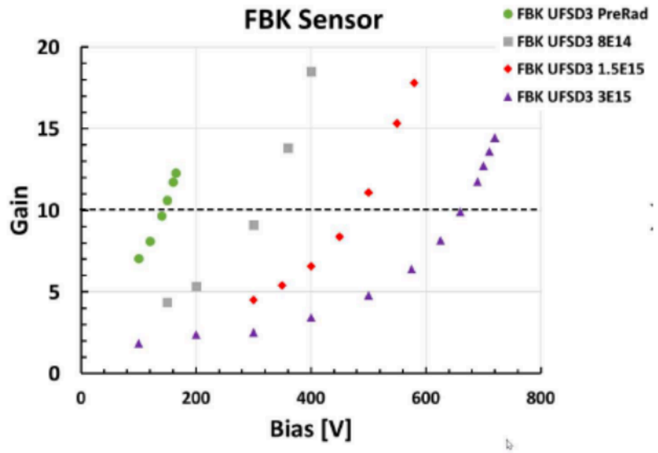
LGAD – Low Gain Avalanche Diode

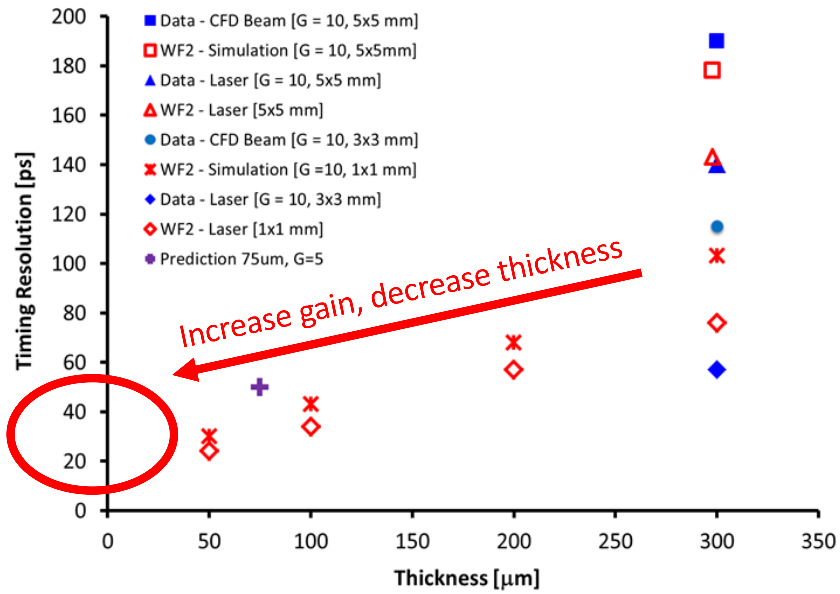
- Highly doped p+ region below the n+ implant
- This generates a multiplication layer
- Internal gain factor from 10x to 30x (before irradiation)
- Low thickness to maximize slew rate: dV/dt



$$\sigma_t \sim \frac{t_{rise}}{S/N}$$

- Gain decreases after radiation (de-activation of the gain layers)

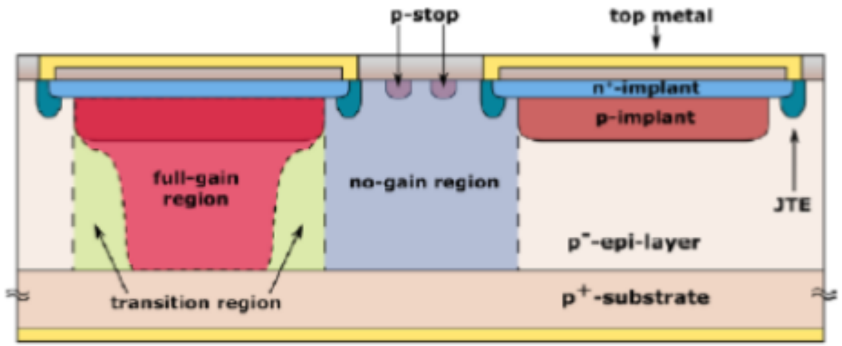




- Options under study: Gallium or Carbon co-implantation

Inverted LGAD - (I-LGAD)

In standard LGADs, the presence of a multiplication layer prevents the use of small pixel implants due to the width of the no-gain region



A few techniques are available to avoid this limitation: one is the use of Inverted-LGADS (I-LGADs) where the multiplication layer is on the opposite face

Multiplication layer divided into strip

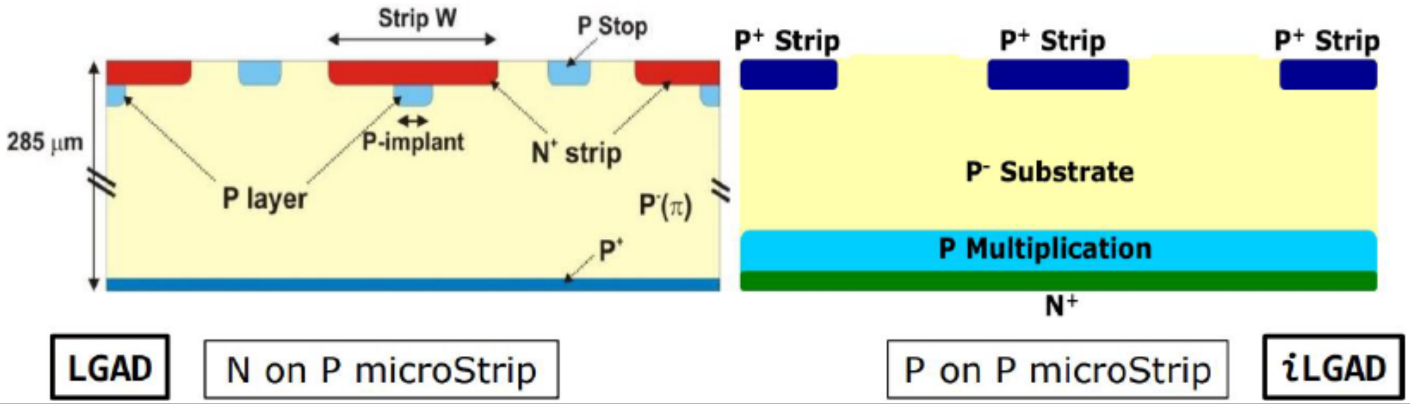
Collects negative carriers (e)

Simple single side process

Multiplication layer extended over the electrode

Collects positive carriers (h)

Complex double side process



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https://indico.cern.ch/event/666427/contributions/2881813/attachments/1603622/2544525/20180219_iLGAD_IvanVila.pdf