EXPLORING THE ITK MEETINGS JUNGLE

WEEK 16

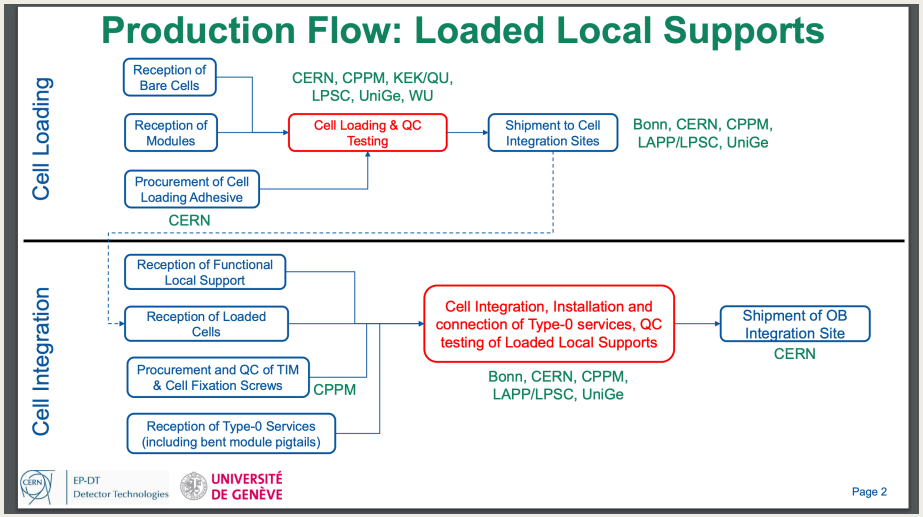
- Full detector component and corresponding QA and QC covered in WBS 2.1.5 local supports (coordinated by Jo Pater and Diego Alvarez Feito)

Retour à la case départ: QA/QC workshop @LAPP – Dec. 2019

- Session « local supports » : inclus un 2.1.5.4 = « module loading » . Rien dans EDMS

- Talk « de principe » de Diego :

https://indico.cern.ch/event/860761/contributions/3660454/attachments/1957495/3252564/0B_QCLocalSupports_DAF_VR1.pdf

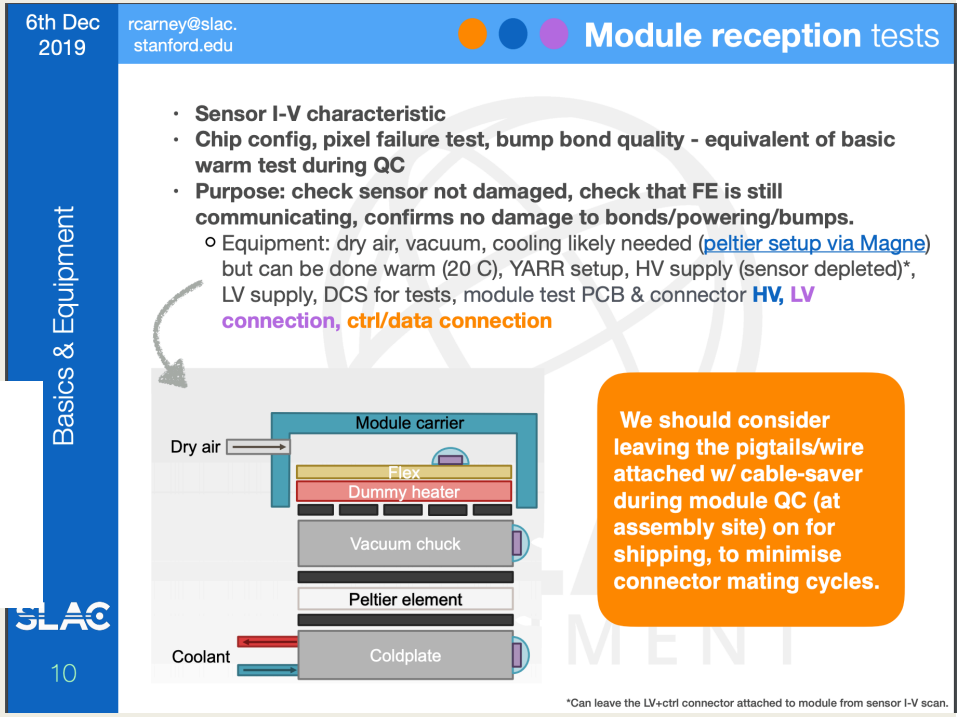


Electrical Testing	• Equipment for reception tests of modules • Equipment for tests of loaded cells	• Equipment for reception test of Type-0 services • Module testing equipment for cell reception tests • Setup (including environmental box) for electrical tests of loaded local supports (both for longerons and rings). Setup includes PSU, DAQ, temporary Type-1 services, fibres and opto-boards, **DCS**, pulse generator, etc

- Le talk de Rebecca sur « electrical testing for loading sites » semble rester la seule référence. Elle confirme qu'il n'y a pas de note (et qu'elle part sans savoir qui reprend)

https://indico.cern.ch/event/860761/contributions/3663655/attachments/1957813/3252776/rcarney_electricalTesting-postModuleAssembly_QAQCwkshp2019.pdf

- Correspond à peu près à la note Lingxin ?



5.5 Basic Electrical Tests

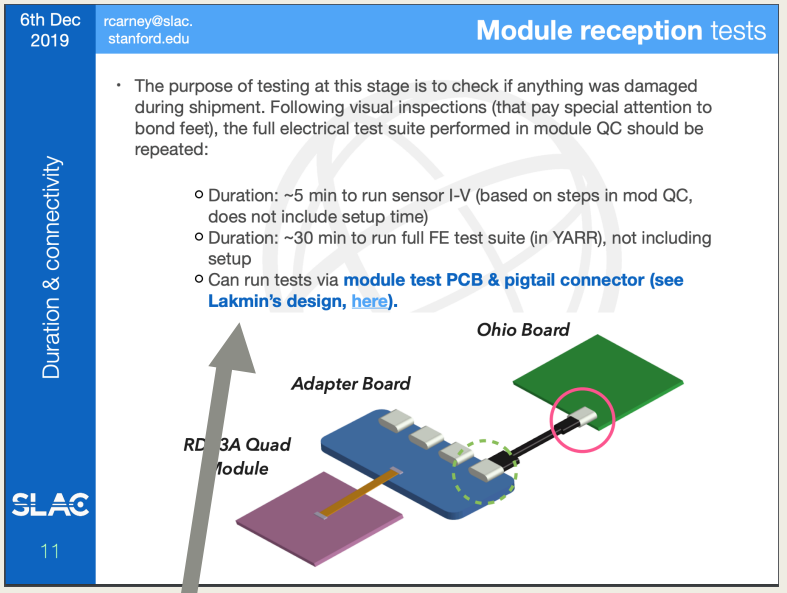
In order to verify if the module is fully functional after each stage, it is sufficient to perform a subset of the full electrical tests at high temperature. Apart from the sensor IV, where the FE should not be powered, the FE shall be powered in SLDO mode for tests that involve DAQ.

- Sensor IV (FE off)
- Register test

- Digital scan
- Analog scan
- Threshold scan
- ToT scan
- Disconnected bumps

Plan A

- Utiliser le paragraphe 5.5 de la note de Lingxin comme base (qui peut le + peut le -)
- Faire une liste des composants nécessaires → Renaud ?
- Fouiller dans les Module testing meetings des 6 derniers mois → Claire ?
  - *PSU specs – le 15.10*
  - *Adapter board – le 29.10*
  - *Interlocks – les 10.12, 14.1*
  - *Dewpoint measurement – le 17.12*
  - *Humidity - le 11.2*
  - *HV – le 18.2*
  - *LV – le 25.2*
  - *Cooling unit, visual inspection - mars et avril*



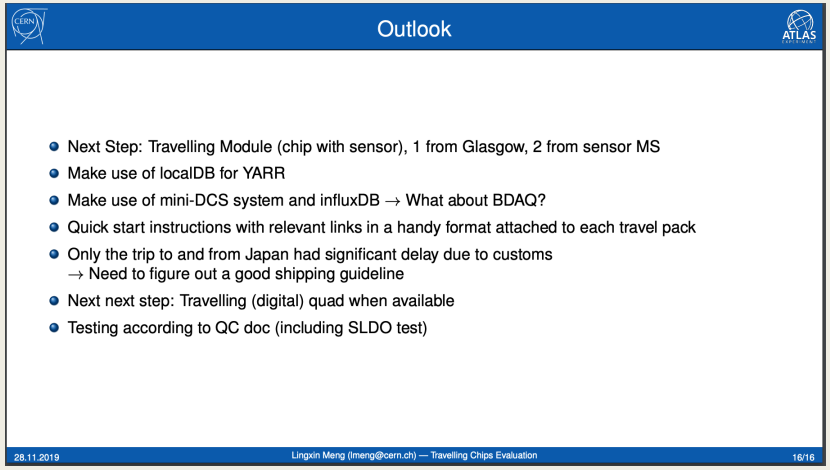
Présenté au Pixel Module Testing meeting
https://indico.cern.ch/event/861446/

Plan B

- Traveling module kit ?

https://indico.cern.ch/event/858917/contributions/3657065/attachments/1953391/3243960/20191128_TravelChipEval_lmeng.pdf

--> The travelling module exercise was done last summer, the idea was to have a module on a single chip card (a much larger PCB) that is well characterised and every institute tried to produce the same results, going through the same procedure. We had about 30 institutes joining and ended up with 3 travelling modules, which still took quite some time to go around all of them. You can find information here: https://travelling-module.readthedocs.io and the results here: https://indico.cern.ch/event/858917/contributions/3657065



Outlook

- Next Step: Travelling Module (chip with sensor), 1 from Glasgow, 2 from sensor MS
- Make use of localDB for YARR
- Make use of mini-DCS system and influxDB → What about BDAQ?
- Quick start instructions with relevant links in a handy format attached to each travel pack
- Only the trip to and from Japan had significant delay due to customs
  → Need to figure out a good shipping guideline
- Next next step: Travelling (digital) quad when available
- Testing according to QC doc (including SLDO test)

28.11.2019 Lingxin Meng (lmeng@cern.ch) — Travelling Chips Evaluation 16/16

Lab qualification for testing

- A question from PDR how we qualify testing sites
- Only qualified (at some stage) labs will receive quads for testing… but
- Assembly and test sites mostly the same site
- Evolutionary qualification (by step)
  A. Qualify for single chip card
  B. Review of equipment
  C. Qualify for room temperature module test
  D. Qualify for all temperature range module test
- How to qualify before having modules? A + B only

e.g. PSU specs survey (https://docs.google.com/spreadsheets/d/1__SXNmNmi92uliTc3N6NaWk_F7qjPgREDWn6JAHsI6M/edit?usp=sharing).

Final qualification with traveling module programme

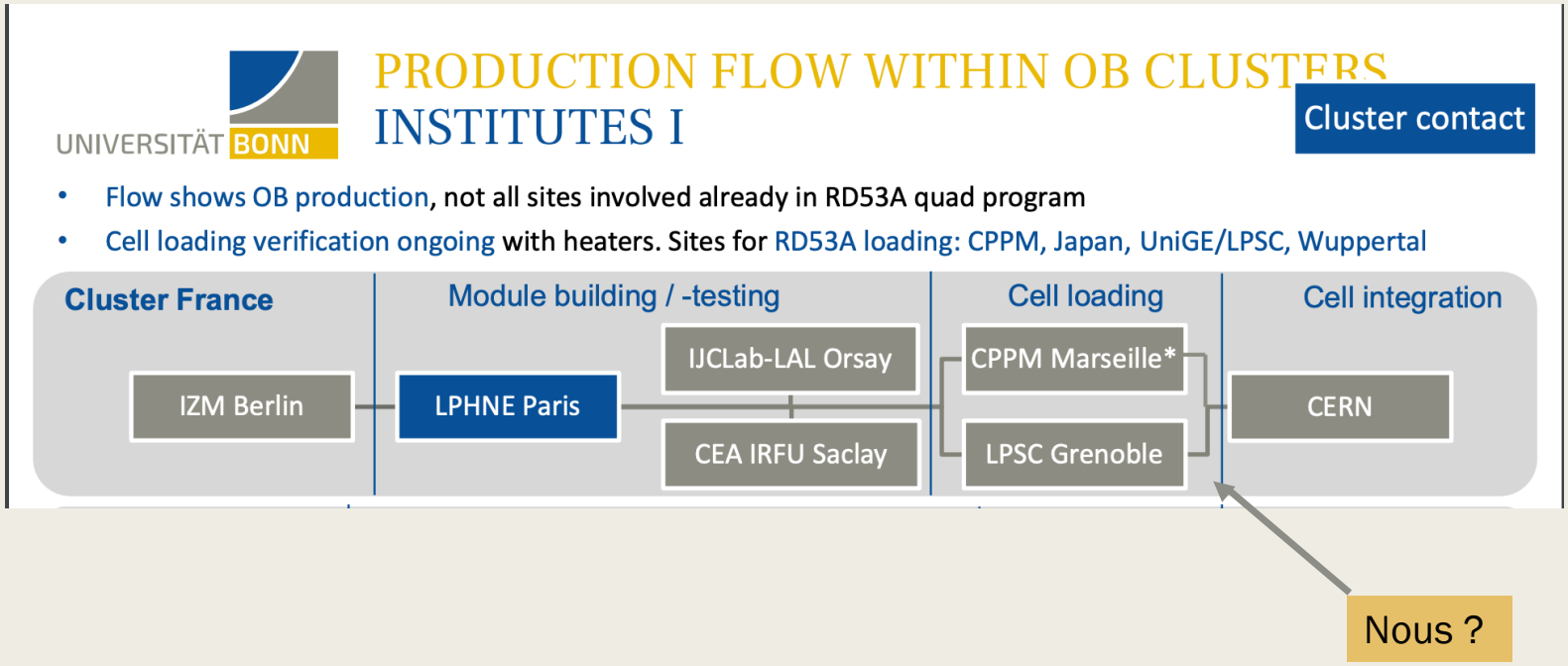
- Question: pending major work (e.g. clean room) some labs may wish to qualify only for ITkPix chip.
  - Would this be possible?
  - Qualification of clusters?

https://indico.cern.ch/event/865110 - Testing meeting du 19 Nov

Plan C

- Se mettre dans la liste d'attente quad ?

OB General meeting – modules
Talk de Pohl sur RD53A quad planning
https://indico.cern.ch/event/900883/



Réponse Eric: nan. Réponse Fabienne: faut voir. Réponse Giovanni: je peux vous envoyer quelque chose

Questions subsidiaires

- Doit-on s'occuper/monter/tester les MOPS ?

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OTHER OB SPECIFIC (?) THINGS

- no big PP0 anymore
  - data connectors to be mounted on Type-0 services → QC of loaded local supports will require data cables with the right connections/modularities
  - same for power connectors
  - will require proper MOPS interface for testing of LLS
    - not special just for OB, but not common to all substructures

- OB general meeting: modules / 16 avril
  Talk Lingxin sur tests
  https://indico.cern.ch/event/900883/

Full vs Basic Electrical Tests

Full	Basic
More like charactersation	Rather basic functionality test
Warm and cold	Warm
Sensor IV	Sensor IV
SLDO characterisation	No SLDO characterisation
Chip config/trim (e.g. Iref and voltages)	No chip config/trim check
Register test	Register test
Tuning	No tuning but basic scans with pre-tuned config
Check for disconnected bumps (source or scan)	Check for disconnected bumps (source or scan)
Conducted after wirebonding and before shipping to loading sites	Conducted between all other stages

Electrical Testing

- DCS (HV and LV voltages and currents) monitoring throughout electrical testing
- Module NTC temperature and environment temperature monitored and controlled
- Humidity monitored
- Not counting on pogo pin card → no probing on pads for QC
- Read out currents, voltages and temperature (TBD) from VMUX via ADC on chip
- Simplified SLDO procedure for QC (relies on chip selection)
- SLDO procedure that involves probing on module PCB to QA and design verification