POINT DE DÉPART: SEMAINE ITK - FEV 2020

https://indico.cern.ch/event/824593

Tooling for RD53A module build & test -- Meeting pixel modules semaine ITK de février (mer 9h)

https://indico.cern.ch/event/824593/contributions/3734134/attachments/1982075/3301330/Tooling_status_update_ITK_week_Magne_Lauritzen.pdf

We have roughly the same needs as for the final production: We will use the RD53A module production to evaluate the tools and get valuable experience.

Assembly:
- Gluing stencils
- Assembly jigs
- Data cables
- Powering
- Module carriers

Testing:
- Cooling
- DAQ/DCS system
- Interlock system
- Power boards
- Data boards

Common:
- Photographic documentation
- Shipping box

This talk will try to list all items, their status, and who is responsible for it.

Multi-module testing equipment – talk Suzanne

- https://indico.cern.ch/event/824593/contributions/3730100/attachments/1982585/3302170/ItkPixV1MultimoduleTesting-SK-060220.pdf

- Today a list of equipment already in planning for electrical testing, mainly covered by CORE budget of other WBS items
- Readout equipment will become available in the coming months and can be used to start equipping sites and get trained with FELIX readout
- In total 18 sites in Pixels with such a test setup for either loaded local support QC or reception testing. 12 starting from Q2/2021, 6 from Q3/2022

+ Suit une liste archi détaillée

LAPP ???

NEWS DE LA SEMAINE

Mardi : nouvelle version de la note testing de L.Meng

- https://cds.cern.ch/record/2702738/files/rd53amoduletesting_v0-2.pdf

5.5 Basic Electrical Tests

In order to verify if the module is fully functional after each stage, it is sufficient to perform a subset of the full electrical tests at high temperature. Apart from the sensor IV, where the FE should not be powered, the FE shall be powered in SLDO mode for tests that involve DAQ.

- Sensor IV (FE off)
- Register test

- Digital scan
- Analog scan
- Threshold scan
- ToT scan
- Disconnected bumps

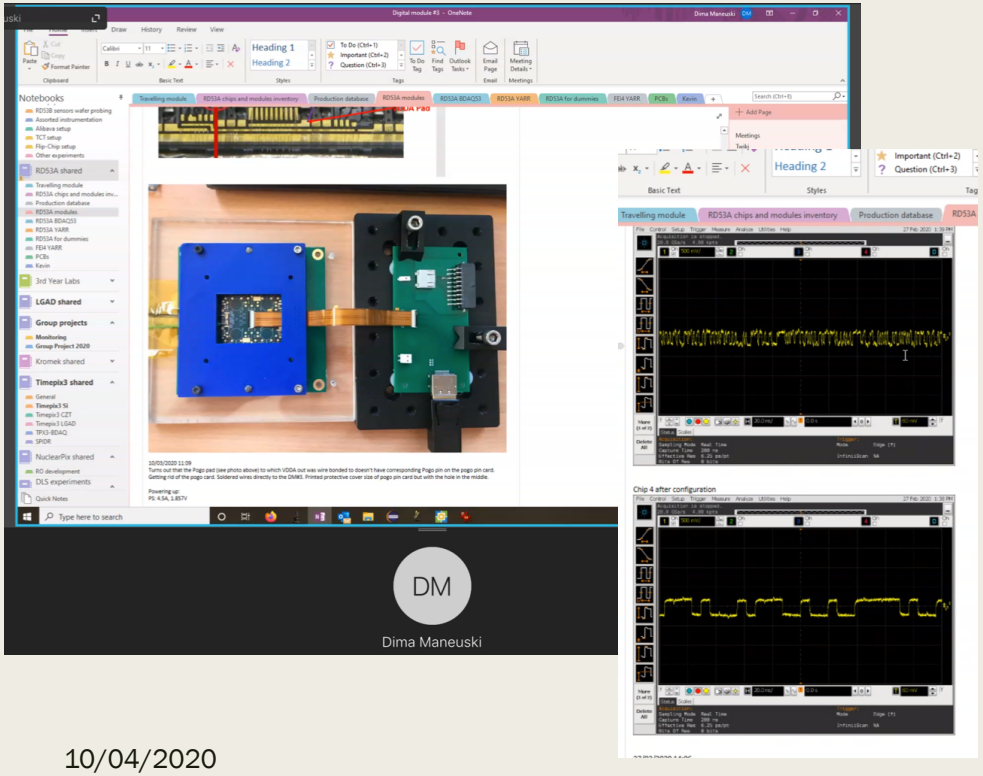
- Entendu lors du meeting de mardi 17h: « it's been decided long ago that all tests beyond single cell/triplet/quad will be described in the assembly document » … qui n'existe pas (Jessica confirme) ou pourrait être https://docs.google.com/document/d/1jmDvE_2tNZs-DXdRHX1j5ayfZ_TYyT6_3A_t328xf3g/edit?pli=1
  - *Summary talk Suzanne @ITK week de février https://indico.cern.ch/event/824593/contributions/3730098/attachments/1982650/3303125/RD53ALLtesting-06022020.pdf*

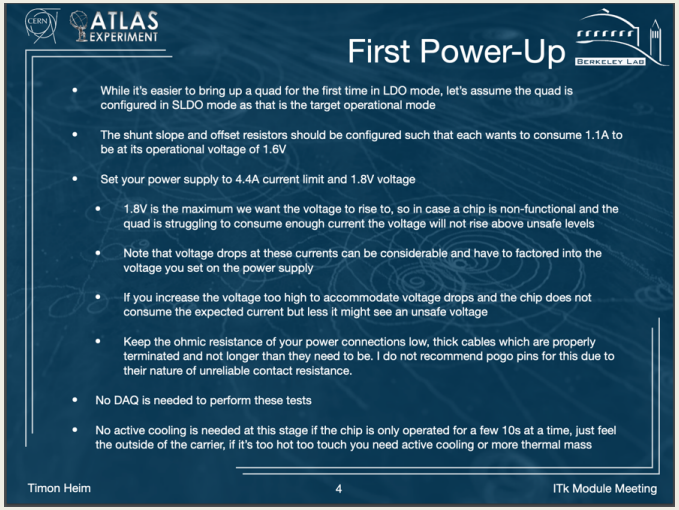
- Full detector component and corresponding QA and QC covered in WBS 2.1.5 local supports (coordinated by Jo Pater and Diego Alvarez Feito)

Jeudi: Modules weekly → all on documentation . ~ 66 connected

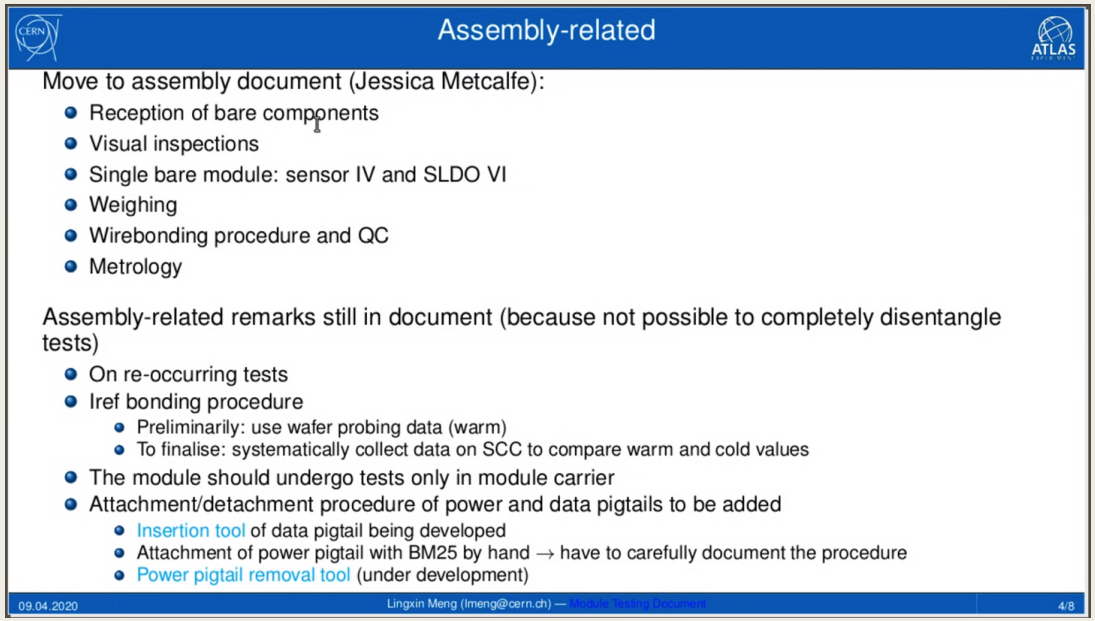
https://indico.cern.ch/event/882699/

- Step by step (verbose) startup instructions by Timon
- Discussion about where/how ground (?) can be probed





- Module QC document walk through by Lingxin
- *Discussion about CDS versus EDMS*
- *Next step for her: add a Database section*
- *Open for questions/comments up to upgrade week (?)*



Assembly-related

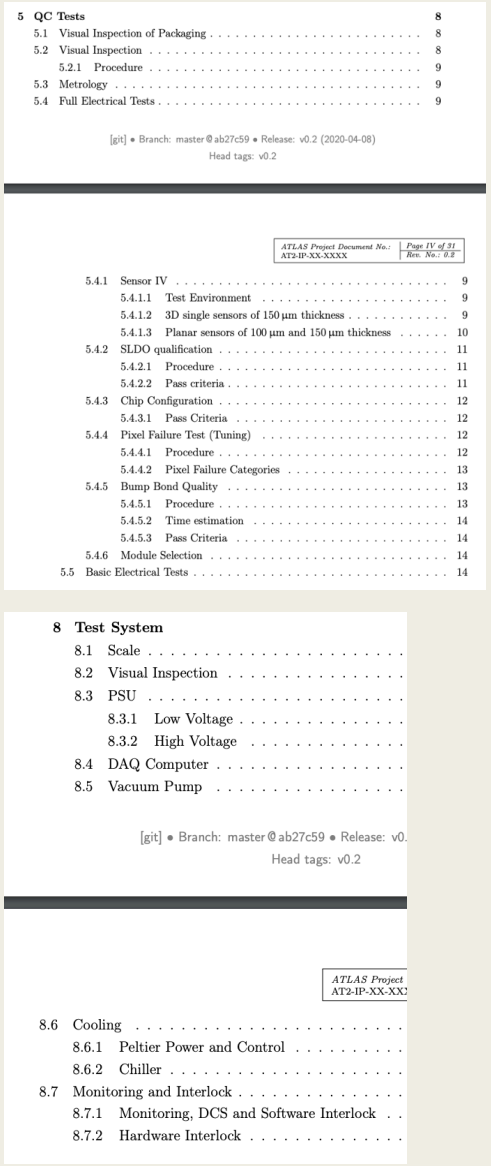
Move to assembly document (Jessica Metcalfe):

- Reception of bare components
- Visual inspections
- Single bare module: sensor IV and SLDO VI
- Weighing
- Wirebonding procedure and QC
- Metrology

Assembly-related remarks still in document (because not possible to completely disentangle tests)

- On re-occurring tests
- Iref bonding procedure
  - Preliminarily: use wafer probing data (warm)
  - To finalise: systematically collect data on SCC to compare warm and cold values
- The module should undergo tests only in module carrier
- Attachment/detachment procedure of power and data pigtails to be added
  - Insertion tool of data pigtail being developed
  - Attachment of power pigtail with BM25 by hand → have to carefully document the procedure
  - Power pigtail removal tool (under development)

09.04.2020 Lingxin Meng (lmeng@cern.ch) — Module Testing Document 4/8



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8.3 PSU . . .
8.3.1 Low Voltage . . .
8.3.2 High Voltage . . .
8.4 DAQ Computer . . .
8.5 Vacuum Pump . . .

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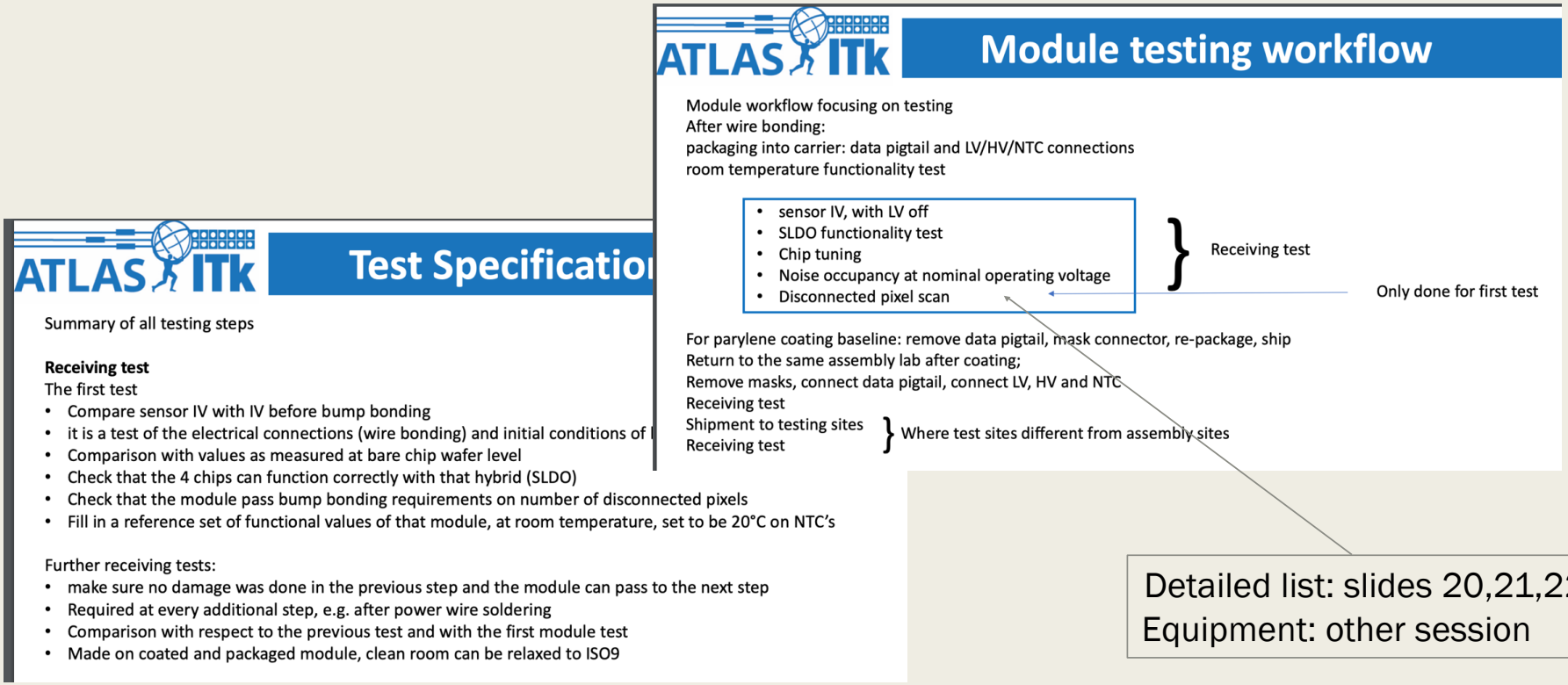
8.6 Cooling . . .
8.6.1 Peltier Power and Control . . .
8.6.2 Chiller . . .
8.7 Monitoring and Interlock . . .
8.7.1 Monitoring, DCS and Software Interlock . . .
8.7.2 Hardware Interlock . . .

EXTRA STUFF
(SEMAINE ITK DE FEV.)

Liste de tests modules – QA/QC meeting ITK week (mardi 14h)

- Définition d'un « receiving test » complet = slides 16 et 18 de https://indico.cern.ch/event/824593/contributions/3732953/attachments/1981374/3299731/Module_Testing_Dauria_ITkWeekFeb2020_V0.pdf



Detailed list: slides 20,21,22
Equipment: other session

Sensor Specifications after assembly

Sensor IV measured at 20°C with power OFF
5nA sensitivity, 5 V step, 0 to 200V with current limitation

- Max current increase < 2 * Max current of bare sensor
- Current I_L< 1.5 μA/cm² [6 μA] (Planar) I_L< 5.0 μA/cm² [30 μA] (3D)
- Breakdown voltage reduced not less than 50 V (Planar) 10 V (3D)
- Breakdown voltage margin above depletion: 70V (Planar) 20 V (3D)

Define breakdown when dI/dV > 5 μA/V

- Sans lumière, humidité ?
- Matériel = HV, LV ?
- Plots = macros de Yarr ?

Chip related parameters after assembly

Powering test

Measure R_{ext}A/D and compare with value measured by flex vendor
Power on in ShuntLDO mode
Measure IV curve of SLDO from power supply 0 to 2 V in 0.1 V step
Read all regulator outputs with MUX
Details of this procedure will be better defined during the RD53a tests
Plan to measure accurately using probe points on hybrid with spring-loaded contacts

Chip communication test

Write/Read registers
Chip serial number
Trimming:

- I_{ref} set to 4 μA
- Vref_ ADC ser to 0.9 V
- V_{DDA} , V_{DDD} set to 1.2 V

Details of this procedure will be better defined during the RD53a tests

Read out tests

Tuning procedure (per FE in RD53a)

Conditions: Power in SLDO mode, HV set at V_{depl}+50 V (planar), MaxV_{depl}+ 20 V (3D). This defined HV ON condition

1. Digital scan
2. Analog scan
3. Threshold scan before tuning
4. Global threshold tuning to 1ke
5. Pixel tuning at 1 ke
6. ToT tuning at 7 ToT for 10 ke
7. Re-tune pixels, fine tune pixels
8. Final threshold scan Comparison of dispersion with scan before tuning.
9. Noise occupancy scan: record number and map of noisy pixels
10. Stuck pixel scan

Same power conditions and final tuning, but HV off

11. Noise occupancy scan: record number and map of quiet pixels (possibly disconnected)

Same power conditions and final tuning, but HV ON as before

12. Noise occupancy scan with radioactive source illuminating the module; HV ON, 50 hits/pixel
    - record number of quiet pixels, compare with (11)
    - Obtain ToT distribution and compare with tuning (6) (for gamma and x-ray only)

Pass requirements from module spec document

Digital:

- not worse than wafer probing.
- Allow 5 new dead pixels per chip

Analog

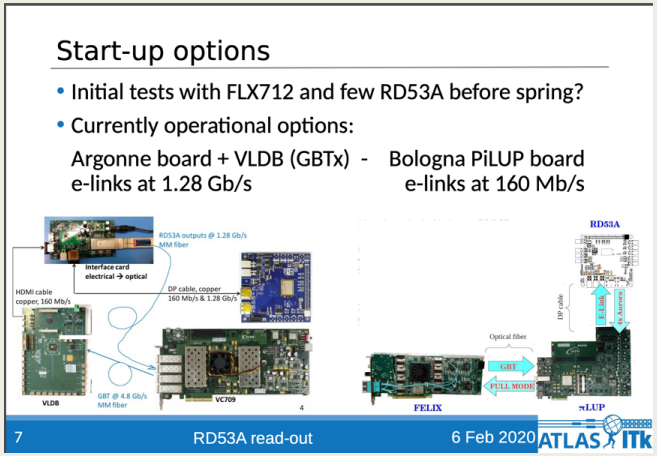
- As good as average single chip, within 5%

- Est-ce que le serial powering (e.g. intensité SLDO) peut engendrer des problèmes différents

RD53A readout for system tests

- LpGBT ? talk « RD53 read out options & timeline » https://indico.cern.ch/event/824593/contributions/3730090/attachments/1982521/3306430/RD53A_readout_schedule.pdf

- Schema for demonstrator https://indico.cern.ch/event/824593/contributions/3730229/attachments/1982864/3302770/Readout_scheme_for_RD53a_demo_zixu_ITKweek_Feb6.pdf



IS RD53A demonstrator: 19-1/2 prototypes

SLAC

Prototype 19-1:

- x1 R0/1, x1 L0 stave, x1 L1 stave, **all loaded with RD53A modules**
- YARR to test x1 SP chain after loading. Verify SP chain functionality
- Direct Felix for test x2 SP chains (one side of ring, L0/L1 staves)
- **If more Felix boards and/or aggregation ready: test whole ring**

Readout System Evolution

SLAC

- YARR, direct FELIX, RCE can all grab a small number of miniDP channels for small scale tests initially
- The bulk of the detector testing will be QC-PP0, miniDP cables, Aggregator, FELIX