# Requirements for the Power Supply System of the ATLAS ITk Pixel Detector

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*Abstract*

This document describes the requirements of the power supply system for the ATLAS ITk Pixel detector. As this document should also be used as a base for discussions with vendors a short overview on the pixel system, as far as it is relevant to the power supply system, is given. Detailed specification lists of the different power supplies required are given. Furthermore control strategies, in particular the interlock system and its interface to the power supplies are shortly described.



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*Distribution List*

## *History of Changes*

| *Rev. No.* | *Date* | *Pages* | *Description of changes* |
| --- | --- | --- | --- |
| Draft | | | |
| 1.0 | 22-June-19 | All | Initial Draft |
| 1.1 | 04-July-19 | | Implemented Comments from Electronics Meeting and Cable TF |
| 1.2 | 11-July-19 | | Implemented available comments from ITk Pixel coordinators and added some changes after discussions with procurement and electronics experts at CERN:<br>➔ Typos<br>➔ Minimum output current for LV PSU changed to 0.3 A<br>➔ Specified 'reasonably' fast loading of parameters<br>➔ Changed required norms and standards according to template from procurement<br>➔ Refined precision and accuracy<br>➔ Added crate/channel temperature monitoring<br>➔ Behaviour of HV, VPP3 and Vopto PSU if current limit is hit<br>➔ Added acceptable failure rates<br>➔ Added Requirement of sensing for Vopto PSU<br>➔ Inhibit is acceptable instead of analog interlock |
| 1.3 | 21-October-19 | | Changed monitoring requirement from "crate/channel temperature" to "crate/board temperature"<br>Changed Off-Mode requirement for LV power supply from "High-Ohmic" to "Selectable by software: High-Ohmic (>100 kOhms) or Low-Ohmic (< 10 Ohms)<br>Added a sentence to state that the "The local interface should at least provide the possibility to assess if a channel is switched on or off, and it should provide the possibility to to switch off the power supply entirely."<br>Changed requirements on ripple on LV PSU, added maximum ripple for the two ranges in mA pp, removed ripple expressed in mV pp.<br>Removed statement that 'digital regulation' is preferred for the LV power supplies and replaced it with a statement that the requirements on set current/voltage limit and measurements must be achieved over the full set current range.<br>Made list of Standards compatible with provided list in MS STEP 3 technical documentation (removed a couple of standards)<br>Added voltage ramp speed (minimum values) for VPP3 and Vopto Power Supplies |

# Contents

# 1 Conventions and Glossary

An overview on the used abbreviations and acronyms can be found in Table 1. With the exception of the power supplies for the sensor bias voltage, all power supplies in described in this document are extra-low power supplies (LV, Vopto, VPP3). The sensor bias voltage, which is referred to as 'High Voltage' in this document, must be supplied by a low voltage power supply.

| | |
| --- | --- |
| *CAN* | *Controller Area Network for the communication lines of DCS controller* |
| *HV* | *High Voltage: bias voltage of the sensors* |
| *LV* | *Low voltage: provides the power to operate the Front-End chips, in SP layout* |
| *L0…L4* | *Layers 0 to 4 of staves with horizontal or inclined sensor planes in the barrel section; L0-1 forming the barrel part of the inner system, located inside the Inner Support Tube (IST), L2-4 forming the outer barrel, located outside the IST* |
| *L0 trigger* | *lowest level (Level-0) of the trigger system, working at either 1MHz or 4MHz* |
| *Module* | *smallest physical detector unit, consisting of a sandwich of a silicon pixel sensor and 1 or 4 readout chips, mounted on a flexible circuit board; size depends on location* |
| *Optobox* | *separately placed system of opto transceiver boards for data links* |
| *PP0* | *patch panel between Type-0 and Type-I cables* |
| *PP1* | *patch panel for Type-I and Type-II service cables* |
| *PP2* | *patch panel for Type-II and Type-III service cables* |
| *PP3* | *Patch panel for Type-III and Type-IV services cables, location of DCS crates* |
| *R0…R4* | *Rings 0 to 4 with vertical sensor planes: R0-1 belonging to the inner system, located inside the IST, R2 to 4 forming the rings of the two endcaps, outside the IST* |
| *SP* | *Serial Power: Modules are connected and powered in series* |
| *SP unit* | *a group of 3 or 4 Front-End chips, powered in parallel, either on a single quad Front-End chip module, or in three single Front-End chip modules* |
| *Tilock* | *temperature sensor of hardwired Interlock System* |
| *Topto* | *Temperature monitoring for optoboards* |
| *VCAN* | *power of the DCS controller* |
| *VPP3* | *Power for the DC-DC converters at PP3, which power the DCS controllers* |
| *Vopto* | *power supply for opto transceiver board* |
| *OPC-UA* | *Open Platform Communications – Unified Architecture: information standard for industrial communication* |

***Table 1: Glossary***

# 2 Related Documents

A list of related documents is summarised in Table 2.

| | |
| --- | --- |
| Front-End Chip | ATL-COM-ITK-2017-004, CERN-RD53-PUB-19-001 |
| 3D Sensors | ATL-COM-UPGRADE-2017-001, AT2-IP-EP-0002 |
| Planar Sensors | ATL-COM-UPGRADE-2017-002, AT2-IP-EP-0006 |
| DCS controller | AT2-IP-ES-0001 |
| GBCR | AT2-IP-ES-0013 |
| Grounding and Shielding | AT2-I-EP-0001 |
| ITk Pixel Services | AT2-IP-EP-0007 |
| General MS specifications | MS-4492/EP/ESE: http://cds.cern.ch/record/2655391 |

***Table 2: Related Documents***

# 3 Description of Components

The tracking detector of the ATLAS experiment will be subject to a significant upgrade after the LHC Run 3 in 2023. The current tracking detector, consisting of several layers of silicon and gas detectors will be replaced by an all-silicon detector, the ATLAS Inner Tracker (ITk). The ITk Pixel Detector comprises the innermost layers of the ITk: about ten thousand ITk Pixel modules, consisting of a silicon sensor bump-bonded to several readout chips, will be connected in about one thousand serial powering chains.

The modules will require a supply line (LV) in order to power the readout chips, and a sensor bias line (HV) in order to deplete the silicon sensors. Data from the front-end ASICs are transmitted electrically over a distance of about 6m to optotransceiver boards (optoboards), where the electrical signals from different chips are serialised and transmitted to the off-detector readout electronics through an optical link. The active components on these optoboards will require a separate powering line (Vopto). The temperature of the sensors and the voltage drops across individual modules in a serial powering chain will be monitored by means of a module independent Detector Control System (DCS). The DCS has active components on the local supports of the ITk Pixel Detector and at PP3 in the experimental cavern. These components are powered through DC-DC converters located at PP3, which are powered from the service caverns USA15 and US15 through a small number of powering lines (VPP3).

In this document, detailed requirements are provided for the LV power supplies, the HV power supplies, the Vopto power supplies and the VPP3 power supplies. A short description of the overall system, with relevant details on the loads is given first. The required supply voltage, current and power for each of the power supply types is given. After that, safety related specifications, in particular channel grouping and interlocking, is discussed. In the last chapter, the requirements for the control of the power supplies are given.

# 4 Interfaces

The power supply outputs are directly connected to the ITk Pixel Services (and through thoses services to their respective loads). For the LV power supplies, the load is the front-end chips, which are assembled on modules and connected into serial powering chains. For the HV power supplies, the load is the sensors, which are bumpbonded to the front-end chips. For the Vopto power supplies, the loads are the Bpol12 converters which will be installed on the optobords, and the VPP3 power supplies are directly connected to the DC-DC converters located at PP3.

In addition, the power supplies are directly connected to the detector control system through an adequate remote interface and to the ITk interlock system through hardwired interlock connections.

All power supply crates will be installed in standard 19'' racks in the services caverns, and will be powered using standard 240 V or 400 V AC single or three phase power outlets.

# 5 Physical Description

There will be several flavours of ATLAS ITk Pixel Modules: The by far largest number of modules will consist of four readout chips bump-bonded to a single, 150 μm thick sensor tile. These modules will be loaded in the outer barrel and the outer endcaps (Layers 2 to 4) of the ITk Pixel Detector, and between six and 13 of these thick quad-chip modules will be connected in series in one serial powering chain. In Layer 1, modules will consist of four readout chips bump-bonded to a single, 100 μm thick sensor tile, and will be operated in serial powering chains with six or ten modules. In Layer 0, single chip modules with 3D sensors will be used. Three or four of these single chip modules will be connected in parallel (triplets or pseudo-quads), and between three and five of these triplets/pseudo-quads will be connected in a serial powering chain. On each module, a flex PCB will be glued to the sensor tile and wire-bonded to the readout asics. Passive components like filtering capacitors and resistors will be mounted on that flex PCB.

A constant current needs to be supplied to the modules in a single serial powering chain. The modules will be built in a way that the total input current to a quad chip module or triplet will be distributed as equally as possible over the parallel-powered readout chips. On each chip, Shunt-LDO regulators will generate the required chip core voltages of 1.2 V for the analog and digital parts. The I-V curves of the Shunt-LDO regulators are defined by external resistors on the module flex PCB. With a mininum drop-out voltage of 200 mV and a maximum input voltage of 2 V for the Shunt-LDO regulators, the voltage drop on each

module is expected to lie in the range between 1.4 V and 2.0 V. The readout chip current consumption will depend on the position of the chips in the detector, hence the current in a serial powering chain is dependent on the layer and section in that layer that serial powering chain is in; the current required by a single serial powering chain is expected to vary between 4.8 A and 7.5 A. The LV cables will be designed in a way that the additional voltage drop on those cables at the expected currents will vary between about 4 V and 8 V. Considering the varying number of modules in the serial powering chains, the total voltage drop across a serial powering chain on the LV line, including the LV cables, will range from 10 V to 29 V. For the operation of the detector, 1012 LV channels to power 1012 serial powering chains will be required. During the integration of the detector, the readout chips might be operated in a low power mode – for this mode, roughly the same voltage drop will be generated from the Shunt-LDO regulators on the modules, at a significantly lower input current (about 150 mA per readout chip, i.e. about 600 mA for a quad chip module and 450 mA for a triplet).

The bias voltage will be distributed to the sensors in a serial powering chain in parallel. In Layer 0, where 3D sensors with a low depletion and breakdown voltage, in particular before irradiation, are used, a single HV channel per pseudo-triplet/pseudo-quad is used. These sensors will require a depletion voltage at the order of 5 V at the start of HL-LHC operations, and a depletion voltage of up to 250 V at the end of HL-LHC operations. The sensor leakage current is expected to increase from a few nA in the beginning to about 1.5 mA for four parallelly biased single chip size sensors (quad equivalent) in L0 at the end of life at the expected sensor temperature. The thin planar sensors in Layers 1 to 4 will require depletion voltages between 5 V before irradiation and 600 V at the end of life, and will draw leakage currents between a few nA at the beginning and a nominal/maximum current of 2.3 mA/6 mA at the end of lifetime for a quad chip module. Up to 7 planar quad sensors will be connected in parallel to one HV line. Including expected voltage drops on the passive components in the HV line and the cables, the total voltage drop on the HV lines (round trip including the sensor) will be between 5 V at the beginning of the HL-LHC run and 650 V at the end of the HL-LHC run, ensuring a depletion voltage of up to 600 V on the sensor. For the operation of the detector, a total of 2228 HV channels will be required. Due to the much lower voltage, current and power required for 3D sensors compared to the planar sensors, two different HV power supply flavours are considered to be used for the two cases. A third flavour is added for extreme cases, where a significantly higher leakage current per sensor will be required, adding up to 50 mA in total for a given HV channel. The requirement of such a high power HV supply can not be excluded by the ITk Pixel design specifications, but the number of actually required channels with these characteristics is estimated to be very low. Due to the significantly increased cost and space requirements these power supplies are expected to have, it is foreseen to buy only a small number which would be installed when needed at a later point. If parallel operation of two or more channels of the HV power supplies of flavour 2 is feasible, the third flavour may be discarded at a later stage.

The monitoring system of the ITk Pixel Detector will be powered through DC-DC converters at one of the outer patch-panels. The input voltage to these DC-DC converters is expected to be in the range between 15 V and 40 V, with a current required between 0.5 A and 3 A. The voltage drop on the cables running from the services caverns to PP3 is expected to be as high as 6 V, which yields a total of up to 46 V on the VPP3 lines. A total of 86 VPP3 channels will be required for the operation of the ITk Pixel Detector.

Finally the optoboxes will require an input voltage between 8 V and 12 V for the first stage of the two stage DC-DC conversion which will be done in the optoboxes. The voltage drop on the cables is expected to be about 5 V for an expected current of about 0.88 A per line. A total of 1300 Vopto channels will be required for the operation of the ITk Pixel Detector.

A summary of the required power supplies, maximum voltage, current and power per channel is given in Table 3. The voltage and current ranges include a safety headroom. The required number of channels includes about 10% for spare units, which are expected to be required.

| Power Supply | Comment | Voltage Range | Current Range | Maximum Power | Channels Required |
| --- | --- | --- | --- | --- | --- |
| Low Voltage | Current Source | 5V to 48 V | 0.3 A to 10 A | 300 W | 1120 |
| High Voltage 1 | Voltage Source (3D sensors) | 5 V to 400 V | < 1 nA to 5 mA | 2 W | 250 |
| High Voltage 2 | Voltage Source (planar sensors) | 5 V to 750 V | < 1 nA to 24 mA | 18 W | 2200 |
| High Voltage 3 | Voltage Source (poorly thermalised sensors) | 5 V to 750 V | < 1 nA to 50 mA | 37.5 W | 100 |
| VPP3 | Voltage Source for PP3 | 5 V to 48 V | Up to 4 A | 100 W | 100 |
| Vopto | Voltage Source for Optoboards | 5 V to 20 V | Up to 1.5 A | 25 W | 1450 |

***Table 3: Overview on Required Power Supplies***

# 6 Powering

All PSU will be supplied with 240 V or 400 V AC single or three phase at 50 Hz.

# 7 Detailed Requirements on the Power Supplies

In the following, detailed specifications are given for the six flavours of power supplies. There are some general requirements which apply to all power supplies, which are summarised first.

## 7.1 General Requirements

The power supplies must be compliant with the technical requirements outlined in the technical description that has been provided for STEP 1 of the combined PSU Market Survey. Some of the requirements given in that document are clarified and detailed in this document. If a requirement from the general technical documentation is not mentioned in this document, that requirement needs to be met within the boundaries specified in the general technical documentation.

### *7.1.1 Location of Power Supplies, Environment and Mechanical Constraints*

All power supplies will be installed in an area accessible to personnel during the running of the experiment, although or the power supplies located in US15 it might take several days until access is possible. Following the routing of the cables, the power supplies will be split as evenly as possible between the two services caverns, US15 and USA15, where the impact of radiation effects and stray magnetic fields is minimised – the environment in which all power supplies are located can be regarded as non-hostile. The relative humidity will be less than 70% at a temperature between 15C and 25C. Some of the units will be required for the integration and system test activities, during which they will be operated in standard laboratory environment. The relevant values for operation and storage are summarised in Table 4.

| | |
| --- | --- |
| Operating Humidity | 10% to 90% RH, non-condensing |
| Operating Temperature | 0C to 40C |
| Storage Humidity | 10%-95% RH, non-condensing |
| Storage Temperature | -20C to 60C |

***Table 4: Operation and Storage Conditions***

All Power Supplies need to be organised in crates and modules; the crates must fit into standard 19'' racks. The power supplies will be cooled using a forced vertical airflow with heat exchangers. A modular system of controller unit and individual output modules is desirable, as plug-in boards are easier to exchange in case of failures.

Each output module should contain one or more output channels, considering the maximum admissable power consumption per crate and sufficient place for the output connectors on the front or back panels. Two different types of crates can be considered:

- Master crates, which can supervise several slave crates. They also allow stand-alone operation, foreseen for laboratory and test beam setups.
- Slave crates, which are mainly an electrical and mechanical housing for the output modules. They can be daisy chained and controlled by one master crate. This concept would help to build an economical system. How many crates can be daisy chained, depends mainly on the speed of access. A good compromise between an economical solution on one side and the speed of monitoring and control on the other side must be found.

The ideal number of channels per crate is in some cases linked to the already installed cables, which will be reused for the ITk Pixel Detector. At the same time, the total available rack space is limited, and the height for a crate containing a certain amount of modules should not exceed the limits set by the available space. Details are given in the specific requirements below.

### *7.1.2 Control*

The power supplies need to be integrated into the ATLAS DCS following the ATLAS standards. This means in particular, that an OPC server, compliant with OPC-UA, for the power supplies needs to exist, and at least one communication interface for remote control and monitoring must exist. An ethernet interface is strongly preferred. In addition, a sufficient interface for local control needs to be implemented. In particular, the requirements on the control system are

- Reasonably fast loading of parameters: a module/crate should be fully operational at most 1 minute after it has been switched on. The output should track the input by less than 500 ms.
- Local control for safety issues that require urgent actions
- Possibility to store and load last or default parameters
- High priority error reporting to reduce the data transfer would be desirable: standard monitoring loops should be done by the system itself. As soon as e.g. the status of a channel is changed, or a channels goes outside of its nominal working conditions, the change must be reported to the higher level DCS on the local control stations.

A list of parameters that should be available to the DCS is provided in the specific requirements for each of the flavours below.

The local interface should at least provide the possibility to assess if a channel is switched on or off, and it should provide the possibility to to switch off the power supply entirely.

### *7.1.3 Operator and Detector Safety Considerations*

**Interlock**

As one of the safety measures, the ITk Pixel Detector will feature a hardwired interlock system. At least one NTC per serial powering chain is directly connected to an interlock matrix crate in the service caverns, which receives additional signals from other parts of the ATLAS experiment and combines them into

interlock signals that are distributed to the power supply units and the cooling system. The complexity of the ITk Pixel Detector requires a relatively fine interlock modularity for the on-detector electronics, and a reasonably dimensioned interlock modularity for the off-detector electronics. Depending on the cost associated to the interlock granularity, an inhibit instead of a pure analog interlock may be acceptable.

In order to maximise the availability of the detector in the case of any problems, the power supplies must be designed in a way that allows interlocking of individual channels, i.e. a control unit that is used to control several channels needs to be equipped with a dedicated interlock interface for every single channel; it is required that one or more channels of one such unit can be operated normally while one or more other channels are inhibited. An exception to this rule are the VPP3 and the Vopto power supplies, where a coarser interlock granularity is acceptable.

The interlock circuits will be designed in negative logic. The voltage level on the interlock lines is therefore defined as the following:

- 0 V = interlock active, channel is inhibited
- 3.3 V = interlock inactive, channel can be operated

Every interlock input line must be equipped with a pull down resistor to ensure that the interlock is triggered also by a disconnected cable. In order to provide isolation from the rest of the electrical system, in particular the on-detector and off-detector active elements, the interlock must be implemented through an opto-coupler at the power supply.

Once an interlock has been activated, an inhibited channel must stay off, even after the interlock has been deactivated, until an operator switches the channel back on through the DCS or the local control interface. The interlock reaction time should be less than 10 ms.

In addition to the per-channel interlock, we require a global interlock for the entire crate, which follows the same logic as detailed above. It should be possible to connect the interlock signals independent from the cables that connect the power supply to the load, i.e. the connection to the interlock system should be done with a separate connector. It is acceptable to have the global interlock and the channel interlock signals on the same connector, however.

**Behaviour after a power cut**

In case of a transient loss of power, the power supply outputs should not produce any significant voltage transients that would exceed the set output voltage. Ideally, the supply should include a minimal UPS capability, such that the outputs can be automatically and rapidly be ramped to 0 in the case of loss of input power.

After a power cut, when the main power to the system has come back, all channels must remain off and should only be switched on by an operator, after a having guaranteed a proper reloading of all parameters.

**Grounding and Shielding**

All power supplies must have floating outputs, both against each other and against the power supply ground/chassis, i.e. all channels must be individually floating, common grounds are not allowed. All power lines that run from the service caverns (i.e. from the power supplies) to the on-detector electronics and the optoboxes are provided with separate return lines, at least up to PP0. The VPP3 power supplies only run from the service caverns to PP3, and each channel will have its own return line from there.

The cables that run from the power supplies to the first patch panel are shielded bundles of twisted pair cables. The secondary part of the power supply should ideally be shielded, and it would be desirable to connect the cable shield to the shield of the secondary part of the power supply. The shield of the secondary part of the power supply should be connected to the return line with a filter capacitor, which should have a capacitance at the order of 10 nF, with minimal trace inductance in the connection of this capacitor. The chassis of each power supply will be electrically connected to the rack, which is earthed – therefore, no connection between the floating parts of the power supply and the chassis are allowed. While any connection between the cable shields and the floating parts of the power supplies on the one hand and the chassis of the power supply on the other hand is not allowed during the operation of the LHC, such a connection may be required for testing of the power supplies and cables. If the floating shield of the secondary part of the PSU cannot be connected to the cable shield, it should therefore be possible to connect

the cable shield to the PSU chassis, while at the same time the cables must be designed in a way that allows to break this connection at a later point.

The reference for the LV and HV power supplies will be provided at PP0/EoS, the reference for the Vopto power supplies will be provided at the optoboards and the reference for VPP3 will be provided at PP3.

**Sensing**

Sensing lines are only foreseen for the Vopto power supplies.

**Input**

All PSU will be supplied with 240 V or 400 V AC single or three phase at 50 Hz. The power factor should be > 0.9 (EN61000-3-2). The inrush current should be smaller than 20 times the nominal input current for less than 1ms (ETSI ETS 300 132-1). The efficiency of all power supplies should be higher than 80% above 40% of the nominal load (average efficiency for the full crate including the controller unit).

**Norms and Standards**

All power supplies must be compliant with the norms and standards summarised in Table 5.

| | |
| --- | --- |
| Saftey Standards: | IEC/EN 60950-1, IEC/EN 61558-1 (or equivalent) |
| CERN safety regulations: | IS-23 and IS-41 |
| Physical rack frame dimensions: | IEC 60297-2 |
| Inrush Current: | ETSI ETS 300 132-1 |
| Fast transient and surge immunity: | EN61000-4-4, EN61000-4-5 |
| Harmonic current emission: | EN61000-3-2 |
| EMC: | EN61000-6-1, EN61000-6-2, EN61000-6-3, EN61000-6-4 |
| EMC: | CISPR22 (EN55022) Class B and CISPR24 (EN55024) |
| Ethernet Standard: | IEEE standard 802.3, SNMP v3: RFCs 3413 to 3415 |
| ROHS compliance: | WEEE Directive 2012/19/EU |
| OPC server compliance: | OPC-UA (Unified Architecture, OPC foundation) |
| CE European marking and related regulations | |

***Table 5: Norms and Standards***

## 7.2 Low Voltage Power Supplies

For the operation of the serial powering chains, a constant current is required; while the output voltage of the power supply would ideally be constant as well, certain failure modes can induce a change in the required output voltage of a serial powering chain. Since the current consumption of each serial powering chain will depend on the position of that serial powering chain in the detector, it must be possible to set the output current to a desired value, which the power supply should provide without exceeding a previously set voltage limit. If the voltage limit is reached, the power supply should change its behaviour from a current source to a voltage source and reduce the output current until the output voltage is below the limit. If a certain minimum current threshold is hit, the channel should be switched off completely. This threshold should be configurable. The delivered current should be measured on both the HIGH and LOW output ports. Details for the low voltage power supplies are summarised in Table 6. Parameters that need to be available for the DCS are listed in Table 7. The modularity should be between 8 and 12 channels per 3U crate. The set current/voltage limit and measurement precision and resolution must be achieved over the full output current/output volage range.

| | Min Value | Max Value |
|---|---|---|
| **Output Current** | 0.3 A | 10.0 A |
| **Delivered Voltage** | 1.4 V | 48 V |
| **Power** | 0 W | 300 W |
| **Floating** | \|50 V\| | \|50 V\| |
| **Capacitance from floating ground to chassis ground** | - | 1 uF |
| **Ripple for f <= 20 MHz** | - | 4 mA pp |
| **Ripple for f > 20 MHz** | - | 0.15 mA pp |
| **Programmable Ramp (up and down, separately configurable)** | 1 A/s | 10.000 A/s |
| **Set Current Precision/Resolution** | 0.5% / 8 bits | - |
| **Set Voltage Limit Precision/Resolution** | 0.5% / 8 bits | - |
| **Measured Current Precision/Resolution HIGH** | 0.5% / 8 bits | - |
| **Measured Current Precision/Resolution LOW** | 0.5% / 8 bits | - |
| **Measured Terminal Voltage Precision/Resolution** | 0.5% / 8 bits | - |
| **Long Term Stability** | - | 0.2 % / 10 K |
| **Off-Mode** | This should be selectable between either High-Ohmic (> 100 kOhms) or Low-Ohmic (< 10 Ohms). | |
| **Maximum Overvoltage for fast Load Change** | - | 0.3 Ohms / 5 us: 400 mV |

***Table 6: Specifications for Low Voltage Power Supplies (Current Sources)***

| **Monitoring** | **Control** |
|---|---|
| actual current LOW | |
| actual current HIGH | |
| actual voltage | |
| set current | |
| voltage limit | |
| ramp up speed | |
| lower current limit for switch-off | |
| channel status: ON, OFF | |
| crate/board temperature | |
| channel status: OVC, OVV, UNV, CHANGING, interlock status | |
| crate status, in particular interlock status | |

***Table 7: Low Voltage PSU Parameters for the DCS***

## 7.3 High Voltage Power Supplies

We may require up to three different flavours of high voltage power supplies, depending on the flavour of the sensor the power supplies are powering. The power supplies must be constant voltage supplies, with adjustable voltages between 5 V and 750 V. For the HV power supply flavours 2 and 3 it is important that a low-ohmic off-mode is implemented in the power supply. Flavour 3 will only be needed during the second half of the life-time of the ITk Pixel Detector, if at all. Procurement of these items may be delayed, if no suitable supplies are available, or if a re-evaluation of the risk of having a full, badly thermalized local support shows that the risk of requiring such a supply is sufficiently low. For all flavours, the power supplies are required to deliver stable, constant voltage over the full range of values given in the Table 8 to Table 11. For flavours 1 and 2, the modularity should be 8, 16, 24 or 32 channels per module, for flavour 3 a

lower number is acceptable. If feasible, an acceptable option for flavour 3 would be the parallel operation of two or more channels of flavour 2.

A configurable current limit is required for all HV power supplies. If that current limit is hit, the power supply should change its behaviour and reduce the output voltage until the output current stabilizes below said current limit. A programmable lower voltage threshold should be available as well. If the output voltage goes below that threshold due to the current limit, the channel should switch off automatically.

In addition to the incoming interlock signals as described in section 7.1.3, the HV power supplies must provide an outgoing signal to the DCS. A single signal per module or crate is sufficient. If all channels on that module or crate are switched off, a positive 3.3 V should be applied to that wire, if at least one channel on the module or crate is switched on, the voltage should drop to 0 V.

It should be possible to mount all three different flavours of HV power supplies in the same crate, even exchanging one power supply of one flavour with a different flavour in the same crate should be possible.

Note that all output voltages for these power supplies shall be negative with respect to the ground reference.

| | Min Value | Max Value |
| --- | --- | --- |
| **Output Voltage** | 5 V | 400 V |
| **Delivered Current** | - | 5 mA |
| **Power** | 0 W | 2 W |
| **Floating** | \|50 V\| | \|50 V\| |
| **Capacitance from floating ground to chassis ground** | - | 100 nF |
| **Ripple for f <= 20 MHz** | - | 20 mVpp |
| **Ripple for f > 20 MHz** | - | 1 mVpp |
| **DC regulation at load** | - | ±200 mV |
| **programmable setting step** | 100 mV | |
| **hardware current limit** | - | 5 mA |
| **resolution of software current limitation** | 1 uA – 10 uA | - |
| **Programmable Ramp** | 1 V/s | 1 V/s - 50 V/s |
| **Emergency Ramp-Down** | - | 100 V/s - 400 V/s |
| **Over(under)-voltage trip reaction time** | - | 10 ms to 1 s |
| **Overcurrent trip reaction time** | - | 10 ms |
| **output voltage measurement resolution** | - | 100 mV |
| **output voltage measurement precision** | - | ±200 mV |
| **output current measurement resolution** | - | 1 uA |
| **output current measurement precision** | 0.02% | - |
| **Off-Mode** | Low Ohmic ( < 10 Ohm) or High Ohmic | |
| **Long Term Stability** | - | 0.2 % / 10 K |

***Table 8: Requirements for the HV Power Supply 1***

| Monitoring | Control |
|---|---|
| actual current | |
| actual voltage | |
| set voltage | |
| current limit | |
| ramp up speed | |
| channel status: ON, OFF | |
| crate/board temperature | |
| channel status: OVC, OVV, UNV, CHANGING, interlock status | |
| crate status, in particular interlock status | |

*Table 9: Parameters for the HV Power Supplies for the DCS*

| | Min Value | Max Value |
|---|---|---|
| **Output Voltage** | 5 V | 750 V |
| **Delivered Current** | - | 24 mA |
| **Power** | 0 W | 18 W |
| **Floating** | \|50 V\| | \|50 V\| |
| **Capacitance from floating ground to chassis ground** | - | 100 nF |
| **Ripple for f <= 20 MHz** | - | 20 mVpp |
| **Ripple for f > 20 MHz** | - | 1 mVpp |
| **DC regulation at load** | - | ±200 mV |
| **programmable setting step** | 100 mV | |
| **hardware current limit** | - | 24 mA |
| **resolution of software current limitation** | 1 uA – 10 uA | - |
| **Programmable Ramp** | 1 V/s | 1 V/s - 50 V/s |
| **Emergency Ramp-Down** | - | 100 V/s - 750 V/s |
| **Over(under)-voltage trip reaction time** | - | 10 ms to 1 s |
| **Overcurrent trip reaction time** | - | 10 ms |
| **output voltage measurement resolution** | - | 100 mV |
| **output voltage measurement precision** | - | ±200 mV |
| **output current measurement resolution** | - | 1 uA |
| **output current measurement precision** | 0.02% | - |
| **Off-Mode** | Low Ohmic ( < 10 Ohm) | |
| **Long Term Stability** | - | 0.2 % / 10 K |

*Table 10: Requirements for the HV Power Supply 2*

| | Min Value | Max Value |
| --- | --- | --- |
| **Output Voltage** | 5 V | 750 V |
| **Delivered Current** | - | 50 mA |
| **Power** | 0 W | 37.5 W |
| **Floating** | \|50 V\| | \|50 V\| |
| **Capacitance from floating ground to chassis ground** | - | 100 nF |
| **Ripple for f <= 20 MHz** | - | 20 mVpp |
| **Ripple for f > 20 MHz** | - | 1 mVpp |
| **DC regulation at load** | - | ±200 mV |
| **programmable setting step** | 100 mV | |
| **hardware current limit** | - | 50 mA |
| **resolution of software current limitation** | 1 uA – 10 uA | - |
| **Programmable Ramp** | 1 V/s | 1 V/s - 50 V/s |
| **Emergency Ramp-Down** | - | 100 V/s - 750 V/s |
| **Over(under)-voltage trip reaction time** | - | 10 ms to 1 s |
| **Overcurrent trip reaction time** | - | 10 ms |
| **output voltage measurement resolution** | - | 100 mV |
| **output voltage measurement precision** | - | ±200 mV |
| **output current measurement resolution** | - | 1 uA |
| **output current measurement precision** | 0.02% | - |
| **Off-Mode** | Low Ohmic ( < 10 Ohm) | |
| **Long Term Stability** | - | 0.2 % / 10 K |

***Table 11: Requirements for the HV Power Supply 3***

## 7.4 VPP3 Power Supplies

These power supplies must be constant voltage sources that supply DC-DC and possibly other voltage regulators at PP3. The requirements are summarised in Table 12 and Table 13. We aim for a space consumption of about 10U for about 80 channels in a 19'' rack. A programmable current limit needs to be available. If the output current exceeds that current limit for a given channel, that channel should be switched off. The channel status should indicate the fact that the channel was switched off due to an excess output current.

| | Min Value | Max Value |
|---|---|---|
| **Output Voltage** | 0 V | 48 V |
| **Delivered Current** | 0 A | 4.0 A |
| **Power** | 0 W | 100 W |
| **Floating** | \|50 V\| | \|50 V\| |
| **Capacitance from floating ground to chassis ground** | - | 1 uF |
| **Ripple for f <= 20 MHz** | | 20 mVpp |
| **Ripple for f > 20 MHz** | | 1 mVpp |
| **Voltage Ramp** | Faster than 48 V / 1 s | |
| **Set Voltage Precision/Resolution** | 0.5% / 8 bits | - |
| **Set Current Limit Precision/Resolution** | 0.5% / 8 bits | - |
| **Measured Terminal Voltage Precision/Resolution** | 0.5% / 8 bits | |
| **Measured Current Precision/Resolution** | 0.5% / 8 bits | |
| **Long Term Stability** | - | 0.2 % / 10 K |
| **Off-Mode** | High Ohmic ( > 100 kOhm) or Low Ohmic | |

***Table 12: Requirements for the VPP3 Power Supplies***

| **Monitoring** | **Control** |
|---|---|
| actual current | |
| actual voltage | |
| set voltage | |
| current limit | |
| ramp up speed | |
| channel status: ON, OFF | |
| crate/board temperature | |
| channel status: OVC, OVV, UNV, CHANGING, interlock status | |
| crate status, in particular interlock status | |

***Table 13: Parameters for the VPP3 Power Supplies for the DCS***

## 7.5 Vopto Power Supplies

The Vopto Power Supplies will provide a constant voltage to the DC-DC converters in the optoboxes. The requirements on those power supplies are summarised in Table 14 and Table 15. We aim for a space consumption of about 10U for about 80 channels in a 19'' rack. These power supplies must include the option for remote voltage sensing. A programmable current limit needs to be available. If the output current exceeds that current limit for a given channel, that channel should be switched off. The channel status should indicate the fact that the channel was switched off due to an excess output current.

| | Min Value | Max Value |
| --- | --- | --- |
| **Output Voltage** | 0 V | 20 V |
| **Delivered Current** | 0 A | 1.5 A |
| **Power** | 0 W | 25 W |
| **Floating** | \|50 V\| | \|50 V\| |
| **Capacitance from floating ground to chassis ground** | - | 1 uF |
| **Ripple for f <= 20 MHz** | | 20 mVpp |
| **Ripple for f > 20 MHz** | | 1 mVpp |
| **Voltage Ramp** | Faster than 20 V / 0.5 s | |
| **Set Voltage Precision/Resolution** | 0.5% / 8 bits | - |
| **Set Current Limit Precision/Resolution** | 0.5% / 8 bits | - |
| **Measured Terminal Voltage Precision/Resolution** | 0.5% / 8 bits | |
| **Measured Current Precision/Resolution** | 0.5% / 8 bits | |
| **Long Term Stability** | - | 0.2 % / 10 K |
| **Off-Mode** | High Ohmic ( > 100 kOhm) or Low Ohmic | |

***Table 14: Requirements for the Vopto Power Supplies***

| **Monitoring** | **Control** |
| --- | --- |
| actual current | |
| terminal voltage | |
| sense voltage | |
| set voltage | |
| current limit | |
| channel status: ON, OFF | |
| crate/board temperature | |
| channel status: OVC, OVV, UNV, CHANGING, interlock status | |
| crate status, in particular interlock status | |

***Table 15: Parameters for the Vopto Power Supplies for the DCS***

# 8 Radiation Tolerance and other special requirements

The power supplies will be located in the ATLAS service caverns, where no special requirements in terms of radiation hardness must be met.

# 9 Testing, Validation and Commissioning

Upon reception/after installation in the service caverns, the power supplies will be tested with dummy loads. Nominal output voltage and currents, output and current meausrements, ramp-up/ramp-down times, communication with the DCS, interlock functionality and behaviour in case of a power cut will be tested.

# 10 Reliability Matters

## 10.1 Consequences of Failures

The LV power supplies will power one serial powering chain per channel, and several serial powering chains will be connected to the same crate. A failure of a power supply channel or crate would affect between 0.1% and 1% of the ITk pixel detector at the time. Depending on the exact failure mode, the availability of the detector will suffer temporarily (until the power supply can be replaced) or permanently.

For the HV power supplies, the situation is similar. A single channel failure will affect 0.05% to 0.5% of the detector modules. If a full module or crate fails, the effect is multiplied by the number of channels. Depending on the exact failure mode, the availability of the detector will suffer temporarily (until the power supply can be replaced) or permanently.

For the Vopto power supplies, a single channel failure will affect the readout for several modules. Again, between 0.1% and 1% of the detector modules will be affected by a single channel failure.

A failure of a single channel of the VPP3 power supplies will have an impact on the monitoring of about 1% of the detector, or about 5% of the optoboxes. If any damage is inflicted on the active elements at PP3, these can be replaced.

## 10.2 Prior Knowledge of Expected Reliability

In particular the LV power supplies have been know for occasionally malfunctioning on power up, due to a high inrush current. The HV power supplies have shown unexpected behaviour in the case of an interlock/after the interlock has been deactivated. Observed failures could mostly be repaired or fixed by firmware updates, although partially with significant delay.

## 10.3 Measures Proposed to Insure Reliability of Component and System

Failed parts can be replaced, if sufficient spares are available. It is planned to buy some spares/store pre-production units from the loading and integration sites to be used as replacements in case of failures. In addition, it is expected that most failure modes for these power supplies are recoverable by repairing the affected units. About 10% extra units will be procured for integration and loading purposes, but also as spares. About 5% are expected to be available as spares for the operation. 10% recoverable failure rate over the course of 10 years of operation, and 1% non-recoverable failures are considered acceptable.

## 10.4 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

## 10.5 Quality Control to Validate Reliability Specifications during Production

The manufacturer shall perform all required tests and provide adequate documentation of test results as proof for the compliance to all specifications, norms and standards. Acceptance tests performed by the ATLAS collaboration shall include tests of the communication interface, the interlock functionality, output voltage and current accuracy and precision for different working points with dummy loads, and for sample the behaviour in case of a power cut, etc.