Insights for FCC-ee / CEPC Tracking and Vertexing, based on Linear Collider Experience

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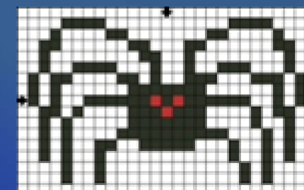
RPC DHCAL

Scintillator ECAL



Collaborations

FCAL

CLICPix

LCTPC

DEPFET

SOI

ChronoPixel

SDHCAL

TPAC

RPC Muon

GEM DHCAL

KPIX

Silicon ECAL (ILD)

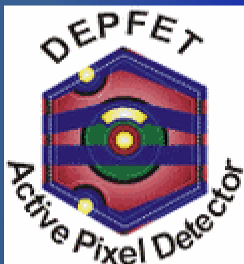
VIP

Dual Readout

Silicon ECAL (SiD)

CMOS MAPS

Many forms of Linear Collider Detector R&D efforts:



- Large collaborations: CALICE, LCTPC, FCAL
- Collection of many efforts such as vertex R&Ds
- Individual group R&D activities
- Efforts currently not directly included in the concept groups (ILD, SiD, CLICdp), which may become important for LC in future

FPCCD

Scintillator HCAL

Linear Collider Collaboration Detector R&D Liaison Report

http://www.linearcollider.org/physics-detectors/working-group-detector-rd-liaison

Last public version (Dec. 18, 2018) → Submitted as supplemental LCC input to the European Strategy Update

LINEAR COLLIDER COLLABORATION

Detector R&D Report

Deadline for submissions: May 15th, 2020
DRAFT
VERSION 2020.1

Editors

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LINEAR COLLIDER COLLABORATION
Designing the world's next great particle accelerator

- ✓ Get a « snapshot » of the R&D efforts, even if they are not officially integrated into ILC, SiD, CLICdp → technologies might become relevant in the future
- ✓ "Publicize" the technology and provide an update of the R&D developments since ILC DBD / CLIC CDR
- ✓ Provide an entry point for new groups to help them to learn about the current landscape and the areas where they might be interested contribute

The suggested content of the inputs is as follows:

- Introduction. Brief overview of the technology (past R&D efforts with references);
- Recent milestones since ILC DBD and CLIC CDR to avoid description of historical data;
- Engineering challenges for a given detector technology in order to encourage new groups to contribute to the engineering aspects and not only to the generic R&D;
- Future plans in the years to come and the list of collaborating institutes contributing to the given R&D technology;
- Application of the R&D outside of ILC with references, if technology is already used.

Linear Collider Collaboration Detector R&D Liaison Report

http://www.linearcollider.org/physics-detectors/working-group-detector-rd-liaison

- ✓ More than 50 individual groups contacts, 170 pp. & summary tables
- ✓ Chapters on: Vertex detectors, Silicon Trackers, Gaseous Trackers, Calorimeters (ECAL/HCAL), Forward Calorimetry (FCAL), Muon System
- ✓ Should not be considered as the summary to select between technologies
  → general overview of the landscape of the LC R&D activities

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
ChronoPix	University of Oregon Yale University Sarnoff Corporation	ChronoPix is a monolithic CMOS pixelated sensor with the ability to record up to two time stamps per pixel during the bunch train. Hits are read out in the time between bunches.	April 2014: Device tests of prototype 2 inform the design of prototype 3 to be submitted to foundry	Prototype 3 was manufactured in September 2014. Tests have shown that problems revealed in prototype 2 were solved.
CMOS MAPS	IPHC Strasbourg DESY, Hamburg University of Bristol University of Frankfurt	The CMOS pixel sensor uses as a sensitive volume the 10 µm–20 µm thin high-resistivity epitaxial Si-layer deposited on low resistivity substrate of commercial CMOS processed chips. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion.	2016 : production of CPS for the ALICE-ITS upgrade 2018/19 : production of CPS for the micro-vertex detector of the CBM experiment at FAIR/GSI 2018/19 : validation of light double-sided ladder concept combining highly granular sensors on one side with timestamping sensors on the other side < 2020 : validation of power pulsing of double-sdied ladders inside a high magnetic field 2022/23 : finalisation of the R&D on various CPS adapted to the different layers of a very high performance vertex detector at the ILC	Until 2018-2019: Development and production of CPS for the ALICE-ITS and CBM-MVD Development of various CPS optimised for the different layers of a vertex detector at the ILC, with emphasis on bunch tagging Development of low material double-sided ladders
DEPFET	University of Barcelona, Spain University of Bonn, Germany Heidelberg University, Germany Giessen University, Germany University of Göttingen KIT Karlsruhe, Germany IFJ PAN, Krakow, Poland MPI Munich MPG HLL Munich, Germany Charles University, Prague, Czech Republic IFIC, CSIC-UVEG, Valencia, Spain DESY, Hamburg, Germany IFCA, CSIC-UC, Santander, Spain	The DEPFET technology implements a single active element within the active pixel by integrating a p-MOS transistor in each pixel on the fully depleted, detector-grade bulk silicon. Additional n-implants near the transistor act as a trap for charge carriers created in the substrate (internal gate), so that they are collected beneath the transistor gate.	2014: Full-scale 75 µm thin Belle II ladder in beam test at DESY	Development of die-attach technology Full-scale test of all ASICs on ladder Integration of read-out and steering ASICs on pixel sensor using flip-chip technique and microscopic solder ball bump-bonding Production of Belle II vertex detector modules Tests of the last version of the DHP chips Engineering design for all-silicon module with petal geometry required for ILC Detailed characterization of device response ...ign of ancillary ASICs, taking full responsibility for ...re design cycles of the FE read-out chip, called Drain ...ent Digitizer
FPCCD	KEK Shinshu University Tohoku University JAXA, Japan Aerospace Exploration ...	Fine Pixel CCD sensors have pixel sizes of 5 ... depleted epitaxial layer ...	... system and demon- ... cooling between −40 °C and 15 °C	...acterization of FPCCD sensors including beam tests ...adiation damage studies ...opment of FPCCD sensors with a pixel size of 5 µm ...struction of prototype ladders for the inner layers of a vertex detector Development of readout electronics downstream of ASICs Development of larger FPCCD sensors and prototype ladders for outer layers Development of readout electronics with a small footprint Construction of a real size engineering prototype and cooling test
3D Pixels	Brown University Cornell University Fermilab Northern Illinois University SLAC University of Illinois Chicago	3D technology allows very fine pitch (4 µm) integration of sensors with multiple layers of electronics, allows interconnection oto both the top and bottom of devices, and provides techniques for low mass, thinned devices.	Completed multi-year effort to demonstrate commercial 3D technology, consisting of 0.13 mm CMOS interconnected with Direct Oxide bonding technology and access using TSV. Received readout wafers with thickness of 25 µm, processed with TSV and DBI to connect to 3D electronics Currently working on active edge demonstrator devices	Complete the 3D active edge project Apply concepts to x-ray imaging devices Re-start ILC developments pending renewed funding
SOI	KEK University of Tsukuba Tohoku University Osaka University	In the Silicon-On-Insulator (SOI) technology the sensing and processing functionalities are separated in different layers; the sensing is provided by a high-resistive substrate connected through an insulating layer with the processing layer.		Sep 2014: Complete architecture study for the ILC pixel detector Mar 2015: Design and fabrication of first test chip for the ILC Dec 2015: Beam test of the chip
CLICPix	Cambridge University CERN University of Geneva Karlsruhe Institute of Technology (KIT) University of Liverpool SLAC Institute of Space Science Bucharest Spanish Network for Linear Colliders	Hybrid pixel-detector technology comprising fast, low-power and small-pitch readout. ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar or active HV-CMOS sensors via low-mass interconnects.	Beam tests of prototype assemblies with ultra-thin sensors (50 µm–300 µm) CLICpix demonstrator ASIC in 65 nm technology Beam tests of assemblies with capacitive coupling between CCPDv3 HV-CMOS active sensors and CLICpix ASICs Power-pulsing demonstrator with dummy loads Prototypes of carbon-fibre ladder supports Full-scale thermal mockup of the CLIC vertex-detector region	Demonstration modules for all major components in time for the next update of the European Strategy for Particle Physics in 2018/19

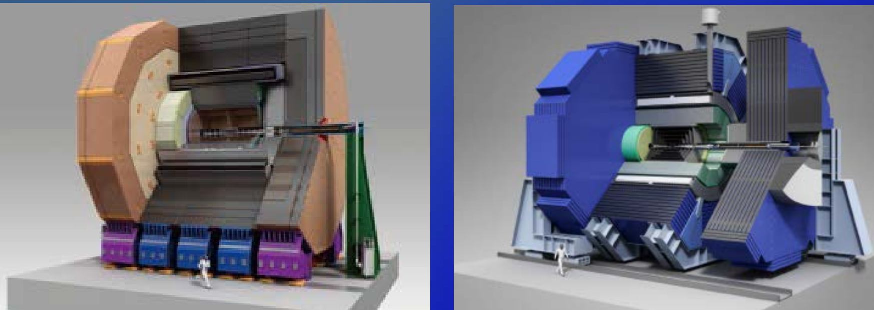
Vertex detector: summary table

R&D Technology	Participating Institutes	Description / Concept	Milestones	Future Activities
Asian GEM	Saga, KEK, Hiroshima, Kindai, Kogakuin, Iwate, Nagasaki IAS, Tsinghua	Design of an endcap readout module with a stack of two thicker laser etched polymer-based GEMs and pads	2010-2013: Several test beam campaigns were performed with three readout modules.	During test beam activities the stability of the HV was not as good as in lab tests. The origin of the discharges is being investigated. A modified module with a gating device will be designed and constructed in the next step, and pad plane adapted for the SALTRO is also planned. (2016/17)
GEM	DESY, Hamburg Bonn Siegen	Design of an endcap readout module with a stack of three standard CERN GEMs and pads	2009-2013: Several test beam campaigns were performed with three readout modules.	Though no problems occurred during the test beam, the HV-stability is still being investigated. A new module with gating device, reduced local field distortions and pad plane adapted for the SALTRO is planned. (2016/17)
Resistive Micromegas	CEA Saclay, Carleton	Design of an endcap readout module with a Micromegas gas amplification stage, a resistive layer for charge dispersion and integrated readout. Construction of 11 modules.	2010-2015: Several test beam campaigns were performed with up to seven readout modules, covering the complete LP-endplate.	New materials as resistive layer are being investigated. A module with lower local field distortions is planned.
GridPix ConceptGEM + pixel readout	Bonn, NIKHEF, CEA Saclay Bonn, Siegen	Design of an endcap readout module with a highly pixelized readout with GridPixes. These devices consist of a Micromegas mesh built by postprocessing technology on a pixel ASIC. Alternatively a GEM-stack is used as a gas amplification stage.	2009-2015: Several test beam campaigns with up to three modules were performed. The three modules featured a total of 160 GridPixes and this test beam was performed in March/April 2015. This demonstrated that a large area could be covered with GridPixes and about 100 GridPixes per module could be operated.	2017: The successor chip Timepix3 will be implemented in the readout chain and a test beam with several Timepix-3 chips is planned. This new chips fulfills basic requirements for an operation in an ILD environment.
Field cage	DESY	Design and construction of a TPC field cage	2009: A first prototype has been built and is used as a test device at DESY	A new field cage with improved geometrical precision is under construction at DESY. (2017)
Electronics	Lund, CERN, CEA Saclay	Design of a readout electronics fit for test beam operation at T24/1 at DESY and for investigation the requirements of the ILD-TPC electronics.	2009: Sofar, readout systems based on the AFTER and the ALTRO chip have ... channels ...	...based on the SALTRO-16 chip is being ...). Simulations on the impact of key ...ameters on the TPC-performance are
DAQ	Lund, ULB-VUB, Hubei	Design of a ...		...tem for the SALTRO-16 based read... ...s being prepared and will be avail... ...soon.
Endcap	Cornell	... at T24/1 at DESY.	...endplate was implemented ... CAD program and in 2009 a first endcap for the test beam setup has been produced several years ago. A new version also fulfills the requirements of the material budget and will be used from 2015 onwards.	Simulations optimizing the module size are planned.
	CEA Saclay, DESY	Mechanical studies for ILD-TPC regarding the effect of pressure, weight, hanging/support schemes on the mechanical deformation of the endplate and field cage.	First studies have been done.	More detailed studies are planned
Calibration	BNL, CERN, Indiana, Kolkata	Laser calibration system, Alignment/calibration of the TPC, Integration with other tracking systems		
Study of systematic effects	Victoria, Kolkata	Field distortions are a major source uncertainties in track reconstruction. The sources of these distortions are studied and minimized.		
Analysis software	DESY, Carleton, CEA Saclay, KEK, Saga, Siegen, Tsinghua	Development of a software package MarlinTPC, which serves all groups for reconstructing and analyzing the test beam data and for simulation, reconstruction and analysis of ILD events.	MarlinTPC is well developed and the key analysis tool for all analyses.	Further improvements are continually made.
Ion backflow/Gating	Japanese Univers., KEK, Tsinghua, Kolkata, DESY	The ion back flow from gas amplification stages is a major source for time dependent field distortions and has to be suppressed as much as possible. With simulations and experimental setups the minimization of ion production and the reduction of the back flow by a gating device are under study. Field distortions are a major source uncertainties in track reconstruction. The sources of these distortions are studied and minimized.	Simulations have shown, that all gas amplification stages release too many ions into the drift volume and a gating device is necessary. 2014: A first MPGD-based device, a Gating-GEM, has been produced and is being compared to a standard wire gate.	2016: module sized GEM-gates will be available. Then the impact of the gate on the TPC-performance will be studied by using a UV-laser facility at KEK, and in test beams.
Cooling	KEK, Saga, NIKHEF, Saclay, Kolkata	Cooling is important to divert the heat produced by the readout electronics at the endplate. The temperature influences the gas gain and drift properties in the gas and has to be kept as stable as possible to achieve a reliable measurement.	2014: A CO_2 cooling plant has been purchased and setup at the test beam site. First results show a significantly reduced temperature gradient due to heating at the endplate.	Cooling of the SALTRO-16 based module will be studied with a mockup which emulates heat and mechanical conditions of the module. Then, the SALTRO-16 based module will be built with the CO_2 cooling pipes.

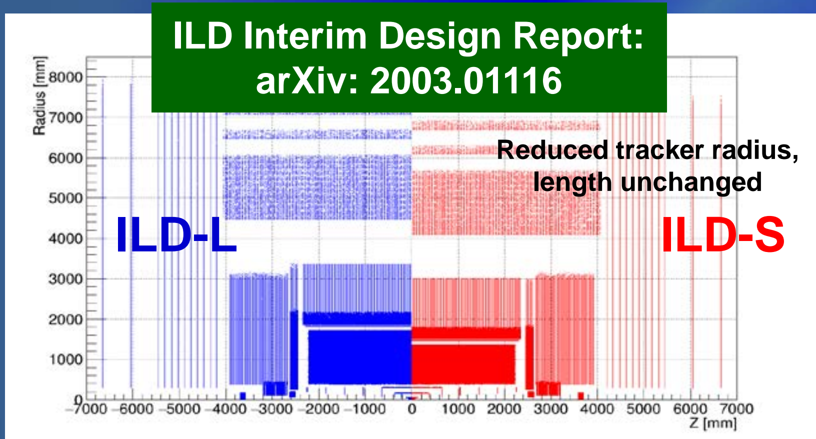
Gaseous Tracker: summary table

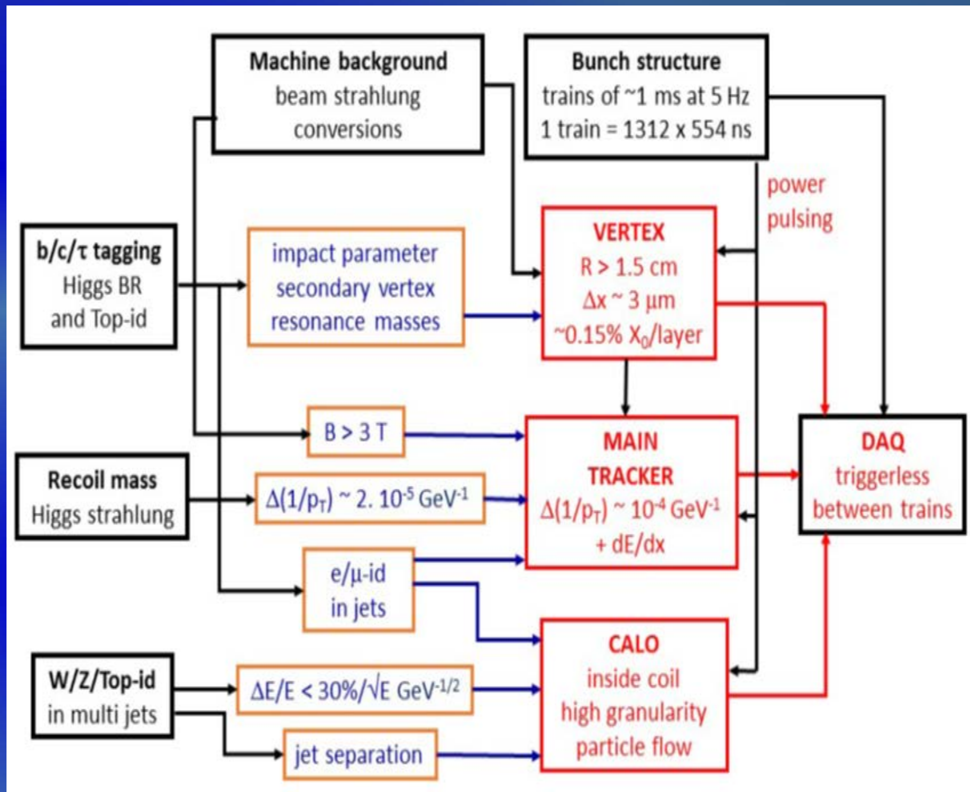
Final Detector R&D Report is planned for July 2020 (by the end of the LCC Mandate)

Two Validated Detector Concepts: ILD and SiD



Re-optimisation: Large (L) & small (S) options





ILD_L / ILD_S	SiD
Both optimized for PFA Performance: ~ $B \cdot R_{ECAL,inner}^2$ (two-track separation @ ECAL)	
B = 3.5 T / 4 T	B = 5 T
$R_{ECAL,inner}$ = 1.8 / 1.46 m	$R_{ECAL,inner}$ = 1.27 m
Si + TPC tracking Outer radius: 1.77 / 1.43 m	Silicon Tracking only Outer radius: 1.22 m

ILD vs SiD: Two Tracking Complementary Approaches

Gaseous Tracking (ILD):

- Si + Gaseous Tracking System:

- VXD: long barrel of 3 double layers

  0.3% X_0 / layer, $\sigma_{sp} \lesssim 3\ \mu m$

- Intermediate Si-tracker (SIT, SET, FTD)
  SIT/FTD: silicon pixel sensors (e.g. CMOS)
  SET: silicon strip sensors

- Time Projection Chamber with MPGD-readout
  High hit redundancy (200 hits / track)
  → 3D tracking / pattern recognition;
  → dE/dx information for PID

Silicon Tracking (SiD):

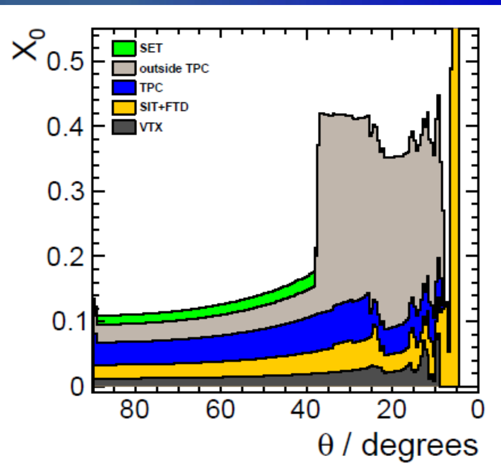
- All Si-Tracking (concept proven by CMS)

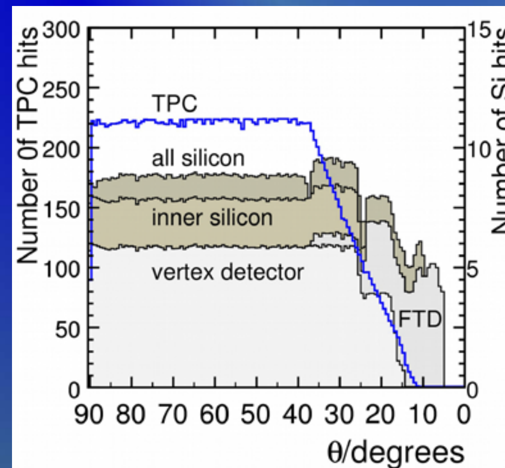
- VXD: short barrel of 5 single layers

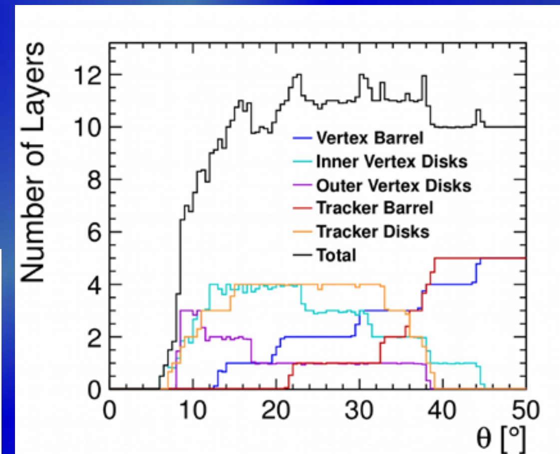
  0.15% X_0 / layer, $\sigma_{sp} \lesssim$ 3-5 μm

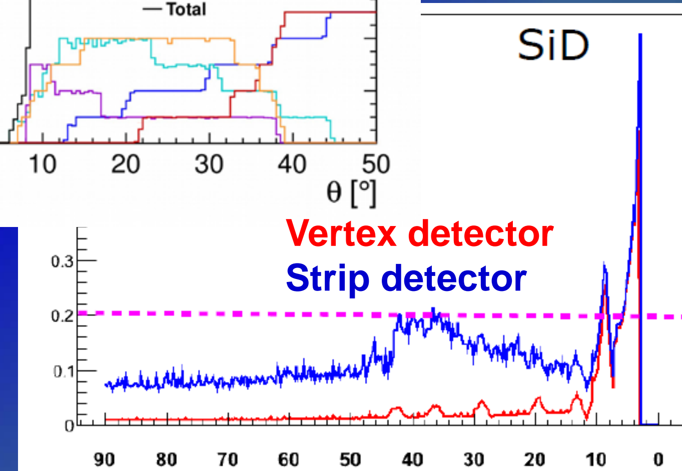
- 5 layers Silicon-strip tracker
  (25um strips, 50 um readout pitch)

- Few highly precise hits (max. 12)
- Robustness, single bunch time stamping









Vertex Technologies for Linear Collider: State-of-the-Art

Exploiting the ILC low duty cycle 0(10^{-3}): triggerless readout, power-pulsing

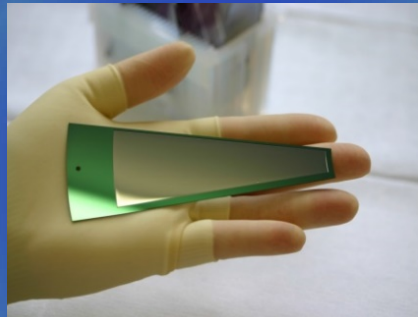
see → M. Winter talk

Readout strategies:

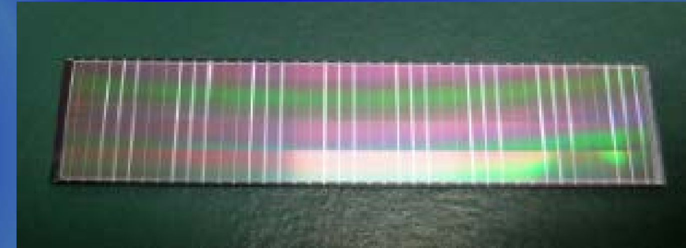
- continuous during the train with power cycling → mechanic. stress from Lorentz forces in B-field
- delayed after the train → either ~5μm pitch for occupancy or in-pixel time-stamping

CMOS (CPS): continuous readout, speed, pixel dim., stiching

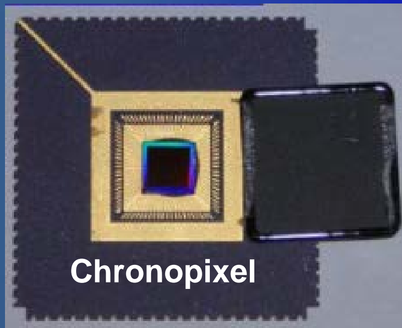
DEPFET: continuous readout, 75 / 50 um thick (Belle II / ILC)



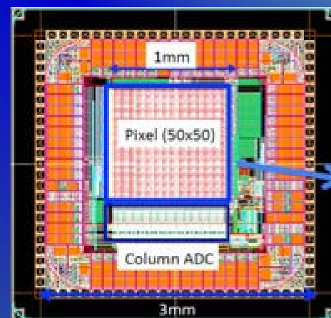
Fine pixel CCD: delayed readout, 5 um pitch, 50 um thickness

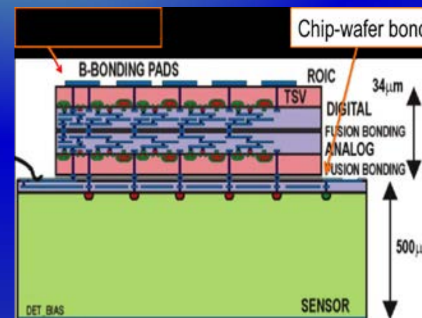


Chronopixel: delayed readout, monolithic CMOS, 50 um thick

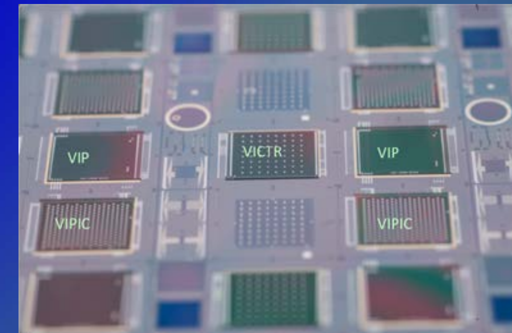


SOI: delayed / continuous readout; suited for 3D integration





3D Integration (in-pixel data processing, currently on-hold): MWR in 2010 VICTR(CMS),VIP(ILC),VIPIC(X-rays)



Sensor's contribution to the total material budget of vertex detectors is 15-30%

Vertex Technologies for Linear Collider: Challenges

Last detector to be installed; technology choices/construction for ILC is still to be over 5-10 years

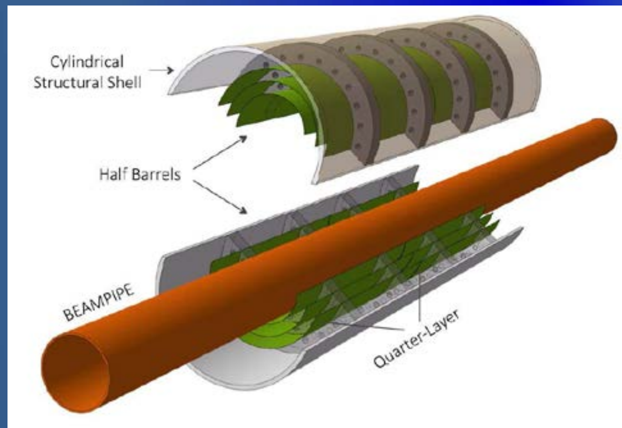
Technology	Examples	Small pixels	Low mass	Low power	Fast timing
Monolithic CMOS MAPS	Mimosa CPS	++	++	**++**	-
Integrated sensor/amplif. + separate r/o	DEPFET, FPCCD	+/++	0	+	-
Monolithic CMOS with depletion	HV-CMOS, HR-CMOS	+	++	**0**	**+**
3D integrated	Tezzaron, SOI	++	+	0	++
Hybrid **D. Dannheim**	CLICpix+planar sensor, HV-CMOS hybrid	+	0	+	++

LC vertex-detector challenges

- $\sim 1\,\mathrm{m}^2$ surface
- Single point resolution of $\sigma < 3-5\,\mu\mathrm{m}$
  - $\rightarrow$ Pixel pitch $\approx 17-25\,\mu\mathrm{m}$
- Low power dissipation of $\lesssim 50\,\mathrm{mW/cm}^2$
- Material budget $< 0.1-0.3\,\%X_0$ per layer
  - $\rightarrow$ Thin sensors and ASICs, low-mass support, power pulsing, air cooling
- Time stamping
  - $\rightarrow\sim 10\,\mathrm{ns}$ (CLIC)
  - $\rightarrow\sim 300\,\mathrm{ns} - \mu\mathrm{s}$ dep. on technology (ILC)

Challenges (beam backgrounds, cooling, material budget) addressed by emerging R&D steps:

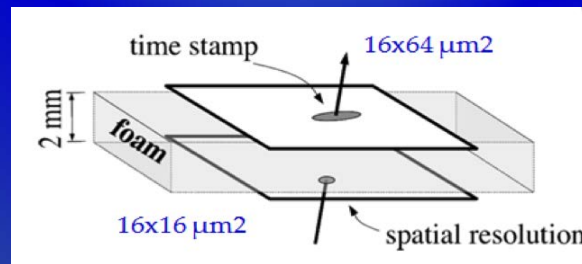
- ✓ Material budget reduction → reduce impact of mechanical supports, services, overlap of modules/ladders
- ✓ Beam related (beamstrahlung) bkg. suppression → evolve time stamping toward a few 100 ns (bunch-tagging)



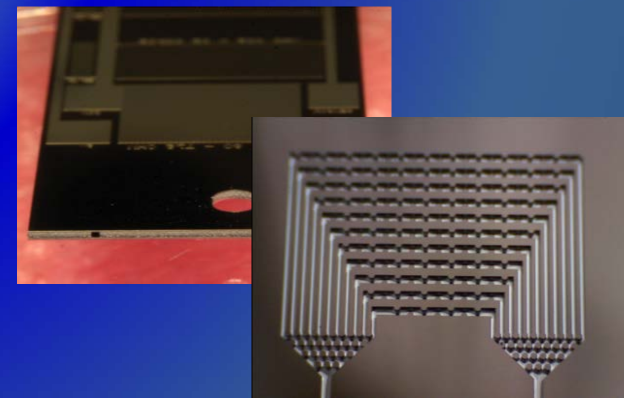
CMOS (CPS): Industrial stitching & curved CPS along goals of ALICE-ITS3, possibly with 65 nm process

see → M. Winter talk

CMOS (CPS): 2-sided ladders: mini-vectors with high spatial resolution & time stamping



Introduce NN in CPS to mitigate data flow from beam-related background



Microchannel cooling: DEPFET in collaboration with AIDA2020

Momentum and Impact Parameter Resolution Performance

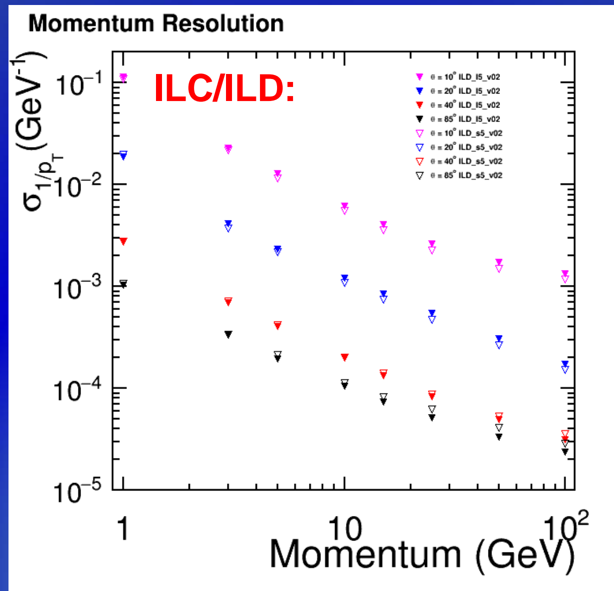
Track momentum resolution:

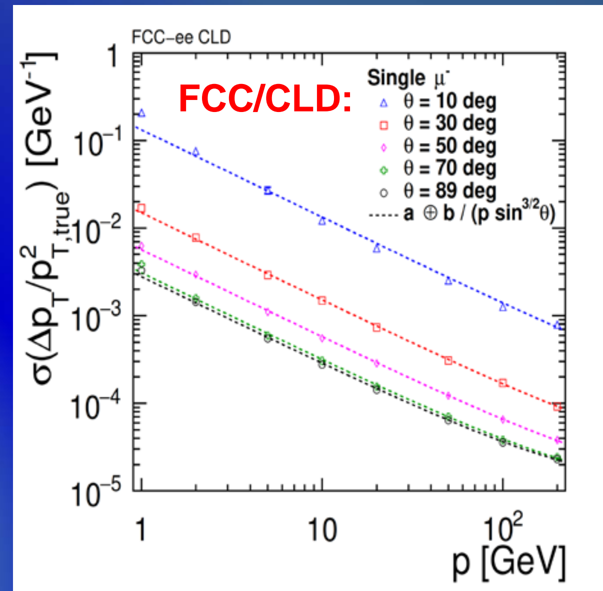
$$\sigma(\Delta p_T/p_T^2) = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

track radius measurement — multiple scattering

- P_T resolution @ 100 GeV ≈2-3 x 10−5 GeV−2 for both ILD & CLD (single muons)

- ILD-S/ILD-L both meet asymptotic momentum resolution goal





arXiv: 2003.01116

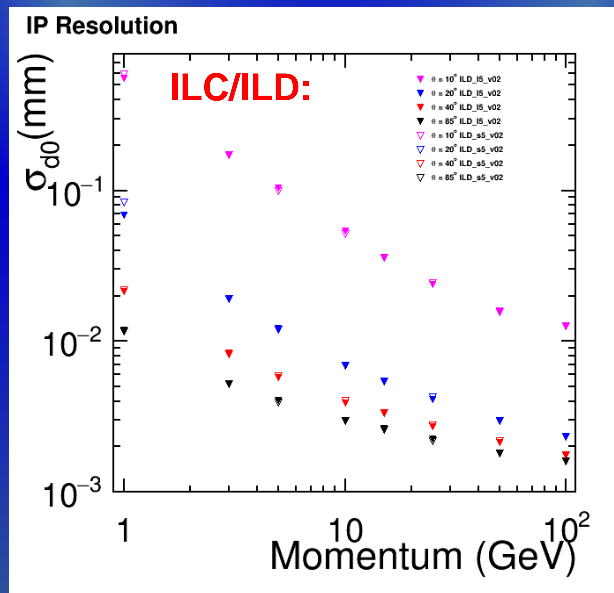
arXiv: 1911.12230

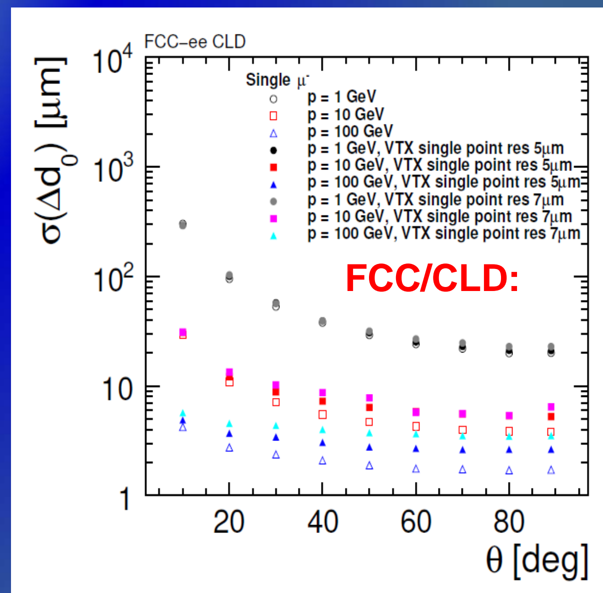
Impact parameter resolution:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3(\theta))}.$$

- $\sigma(d0)$ resolution is affected by the layout of vertex detector and single point resolution

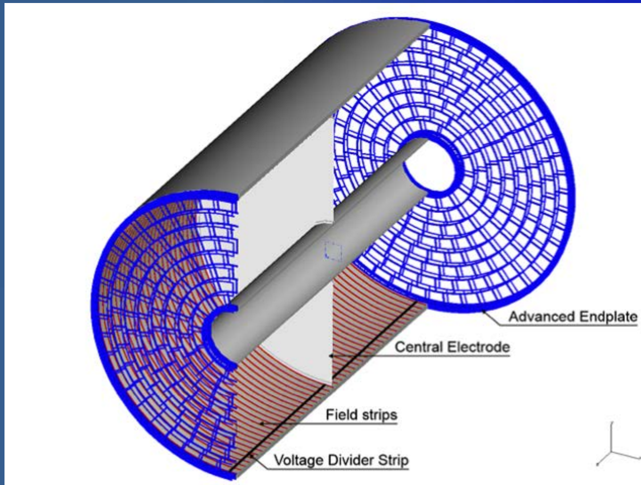
- Single point resolution has a large impact (50%) on $\sigma(d0)$ at high p_T (CLD study, similar for CEPC)





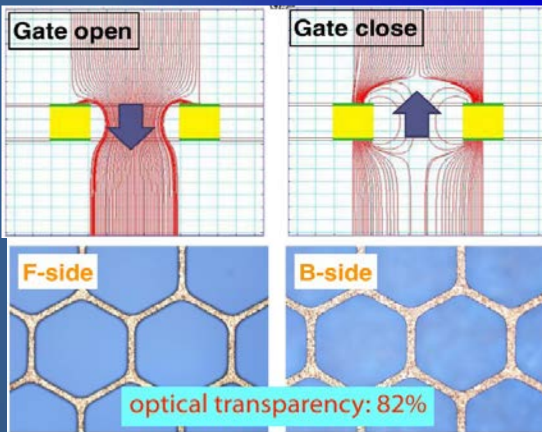
ILC TPC with MPGD-Based Readout

MPGDs are foreseen as TPC readout for ILC (endcap size~10 m^2):

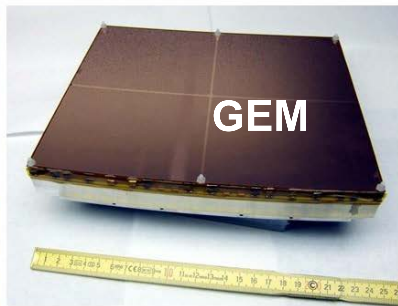


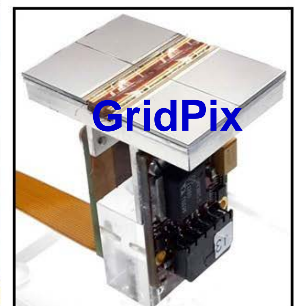
Machine-induced bkg. and ions from gas amplification create track distortions
=> Gating is needed

- Wire gate is an option
- Alternatively: GEM-gate

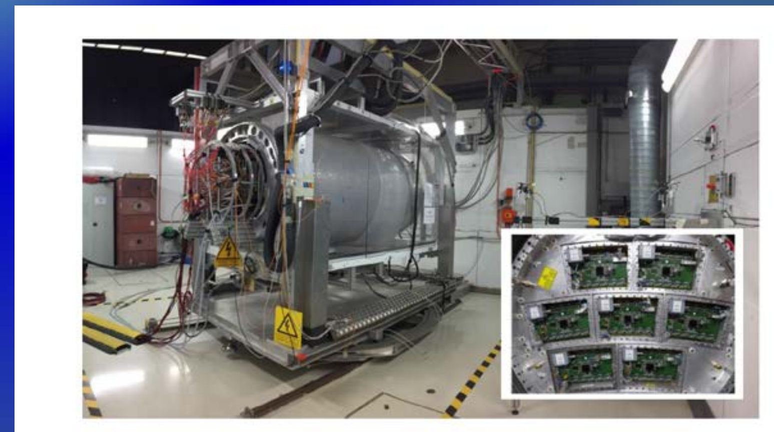


- Standard "pad readout" (~ few mm^2): 8 rows of det. modules (17×23 cm2); 240 modules per endcap
  - → Wet-etched triple GEMs
  - → Laser-etched double-GEMs 100μm thick ("Asian")
  - → Resistive MM with dispersive anode
- Pixel readout (55x 55mm^2): ~100-120 chips per module → 25000-30000 per endcap (GridPix)
  - → GEM + pixel readout
  - → InGrid (integrated Micromegas grid with pixel readout)





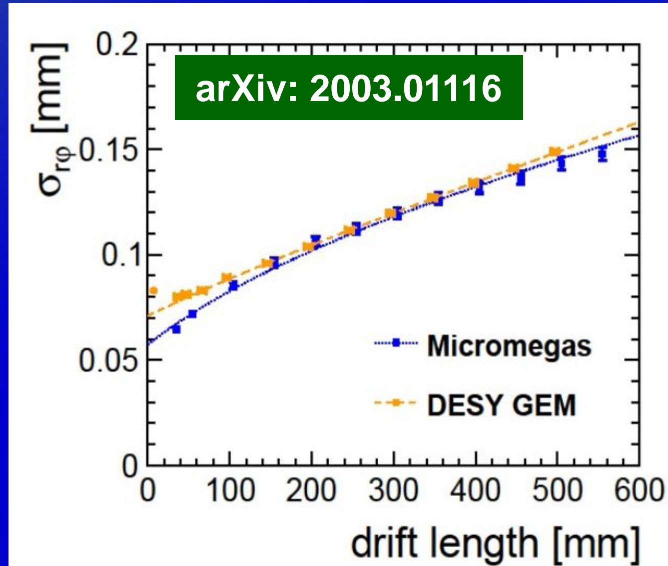
The Large TPC Test-setup @DESY

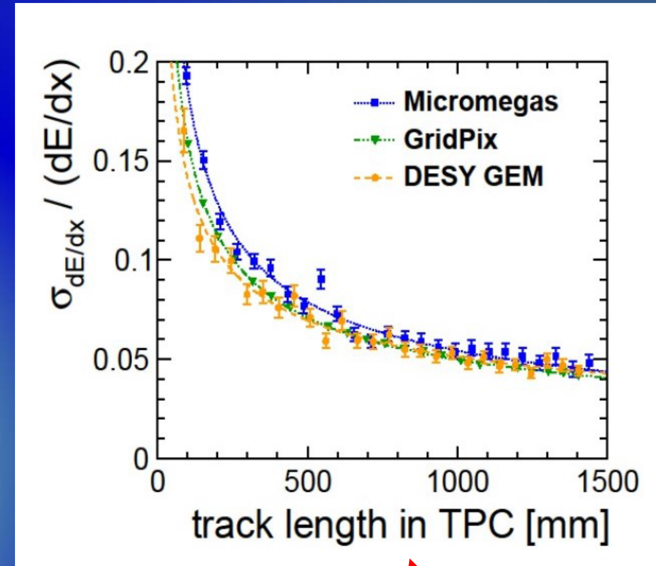


Central Tracker: TPC Performance

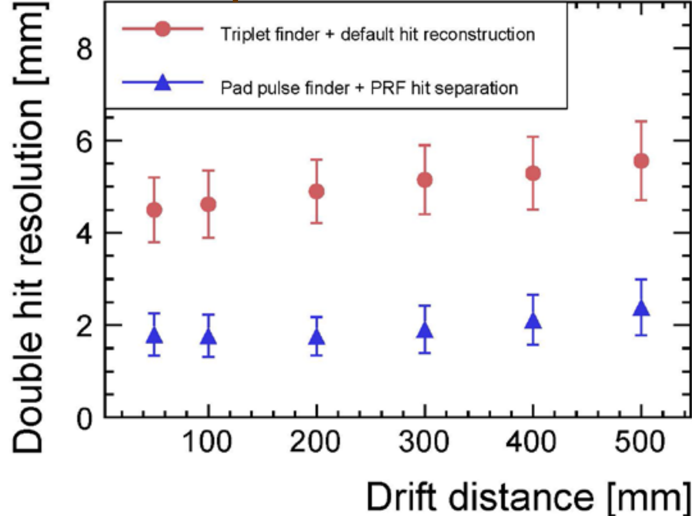
Target requirement of a spatial resolution of 100 um in transverse plane and dE/dx resolution < 5% have been reached with all technologies (GEM, MM and GridPix)

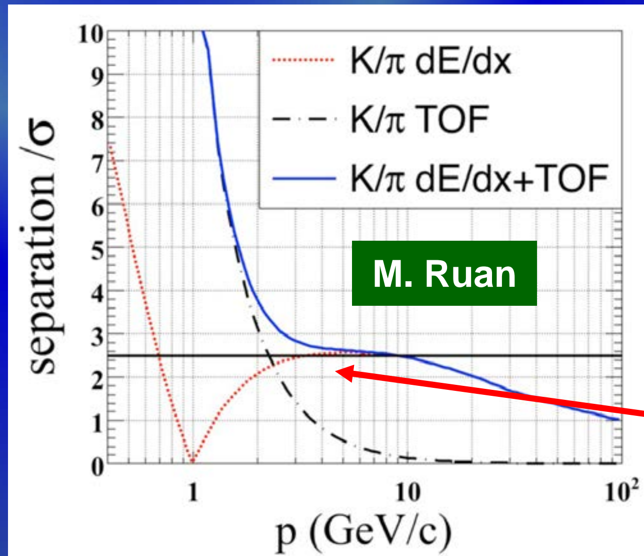
- ✓ GEM: requires ~ 1mm pads & sufficient diffusion
- ✓ MM: charge spreading using resistive-anode capacitive readout
- ✓ Gridpix: < 300 um pitch / digital readout





dE/dx <4 % can be achieved with Gridpix (cluster-counting)



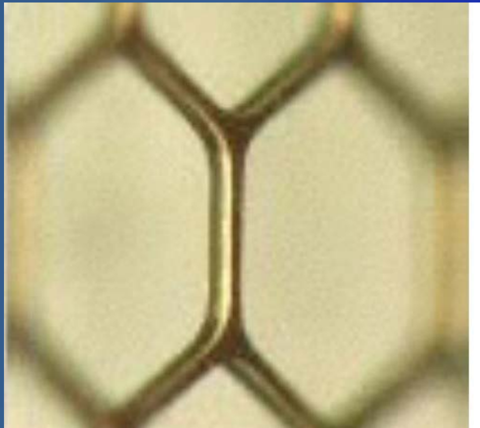


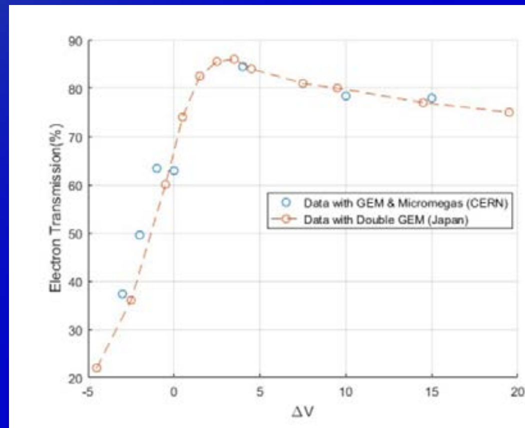
If dE/dx combined with ToF using SiECAL, p<10GeV region covered

Central Tracker: Pixel TPC for Z-Pole Running

ILC: gating scheme, based on large-aperture GEM

→ Exploit ILC bunch structure (gate opens 50 us before the first bunch and closes 50 us after the last bunch)





Estimate the charge in the TPC as it can cause distortions:

P. Kluit

- At ILC beam-beam effects are dominant
- TLEP and FCC-ee studies → $\gamma\gamma$-background is very small at Z

✓ Rough estimations at L = $32 \cdot 10^{34}$ cm^{-2} s^{-1} indicate primary ionisation causes accumulated charge at an ILC250 level

✓ Ion backflow (IBF) can give a lot of additional charge
→ so IBF must be controlled (IBF = 5/1.5 → 80 / 14 um)

✓ Measuring IBF for Gridpix is a priority, expected $\mathcal{O}$(1‰)

✓ At CEPC gating can greatly reduce IBF (@ Z-pole):
- max drift time of 30 μs < average Z interval 100 μs (10 kHz)
- will cause some leveling due to dead time

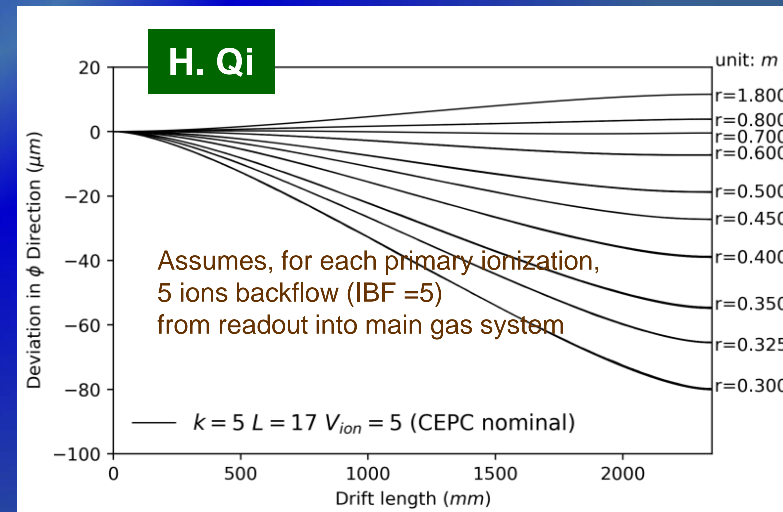
Circular colliders (e.g. CEPC):

✓ H/top running → pad / pixels are OK (@10^{35} ion backflow and space charge can be calibrated by laser system);

✓ Z running (@10^{36})→ occupancy is too high at low radii (overlapping tracks)

→ Study pixel - TPC to replace pad - TPC for Z-pole running

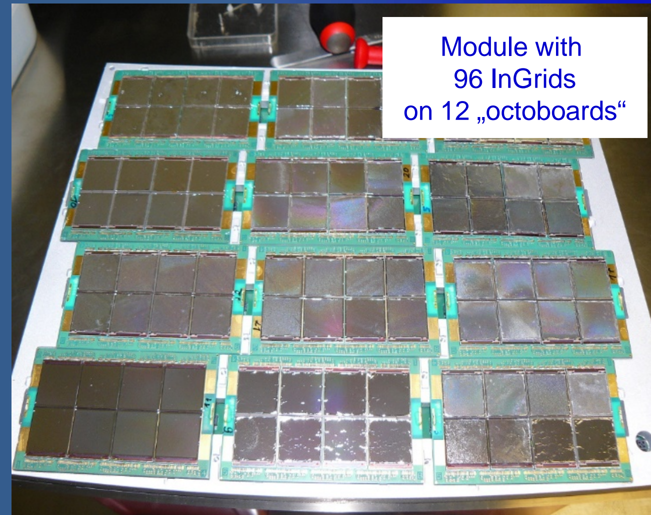
Future R&D needed:
- Optimal pad size to improve track resolution;
- Pixel size > 200 um or large → cost reduction



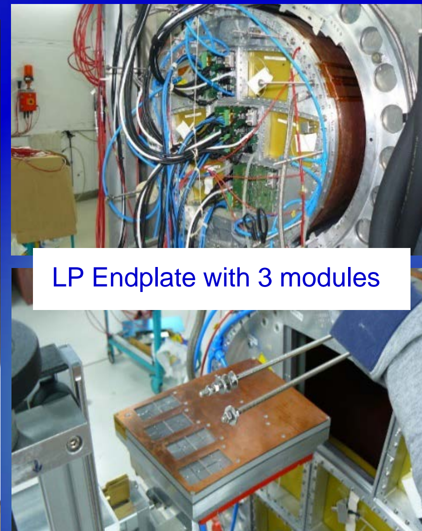
Central Tracker: GridPix TPC Readout

Feasibility is shown @ DESY test-beam with 160 InGrids

3 modules for Large TPC Prototype : 1 x 96 InGrid, 2 x 24 InGrids
320 cm² active area, 10,5 mio. channels, new SRS Readout system



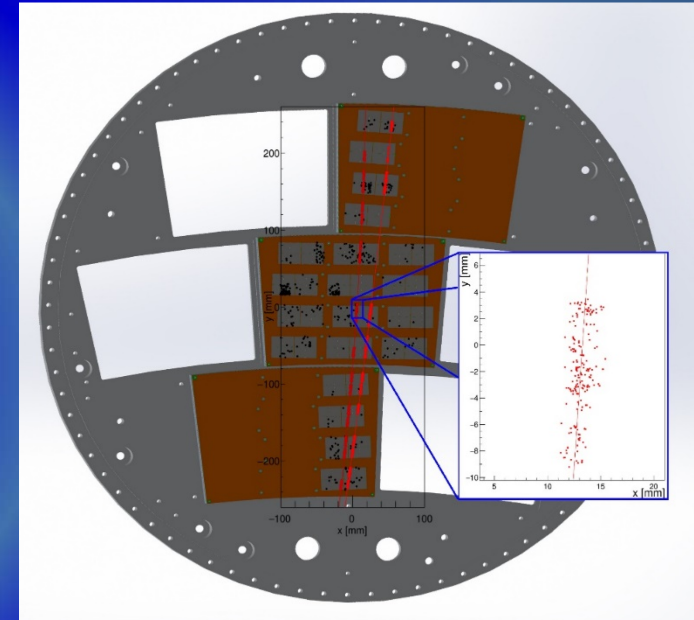
Module with 96 InGrids on 12 „octoboards“



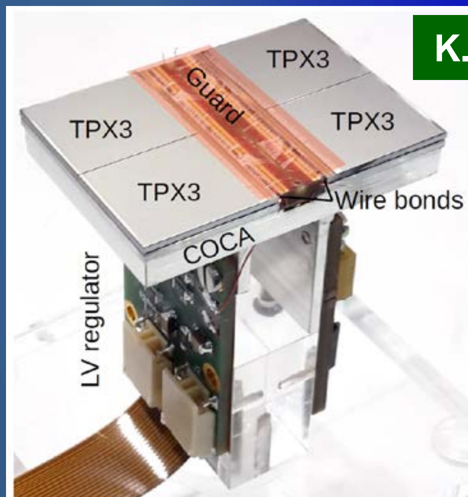
LP Endplate with 3 modules

50 cm track length with about 3000 hits

→ each representing an electron from the primary ionisation
→ demanding for track reconstruction, especially in case of curved tracks



Quad board (Timepix3) → development of 8 quad detector (2020)



K. I

Physics properties of pixel TPC:

- Improved dE/dx by cluster counting
- Improved meas.of low angle tracks
- Excellent double track seperation
- Much reduced hodoscope effect
- Lower occupancy @ high rates
- Fully digital read out (TOT)

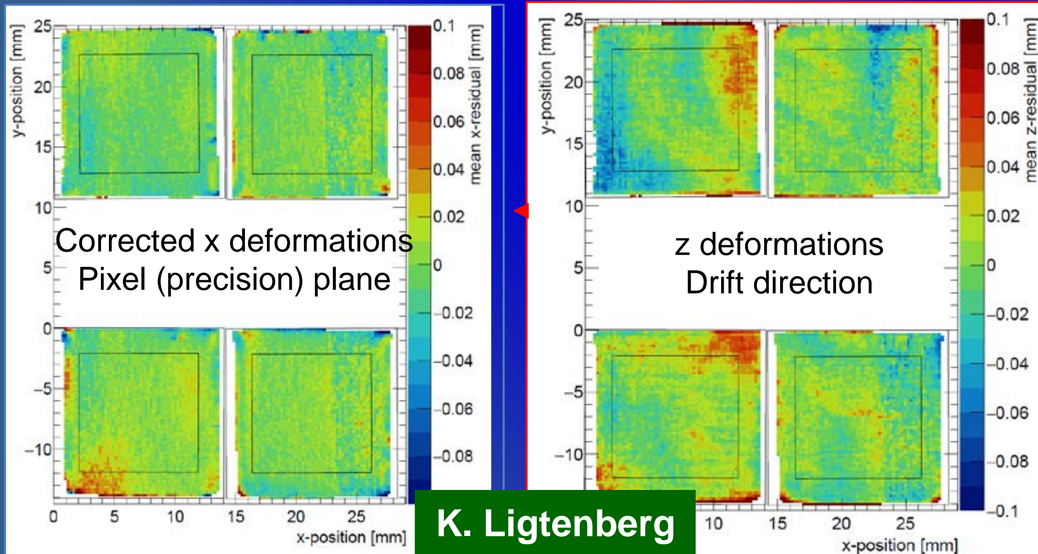
Critical Items for a TPC Readout Technology Choice

Several aspects are important:

- ❑ Minimize power consumption (detector/electronics)
- ❑ Sufficient cooling (e.g. little material, e.g. CO_2 colling)
- ❑ Thin detector (radiation length)
- ❑ Minimize z- and xy-readout plane destortions

Deformation challenge: Quad / pixel module

Considerable effort to reach very high precision mechanical mounting (10-20 um) of the quad and 8-quad module

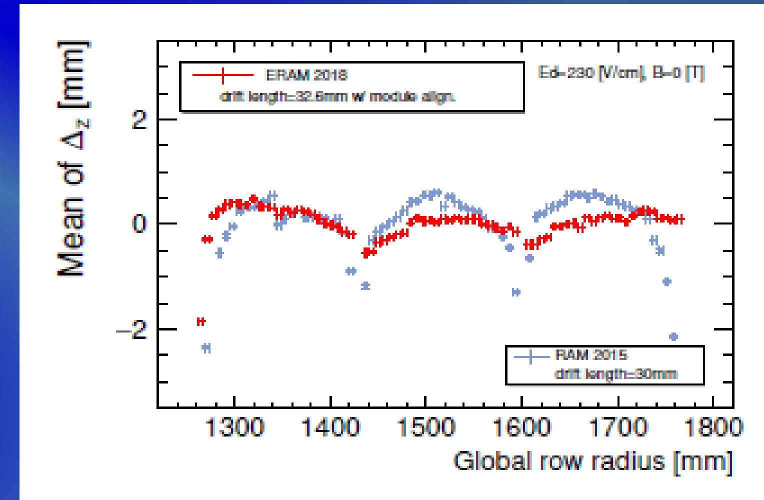


K. Ligtenberg

- ➢ GEM-Based readout paper: arXiv:1604.00935
- ➢ MM-Based readout paper (in preparation)

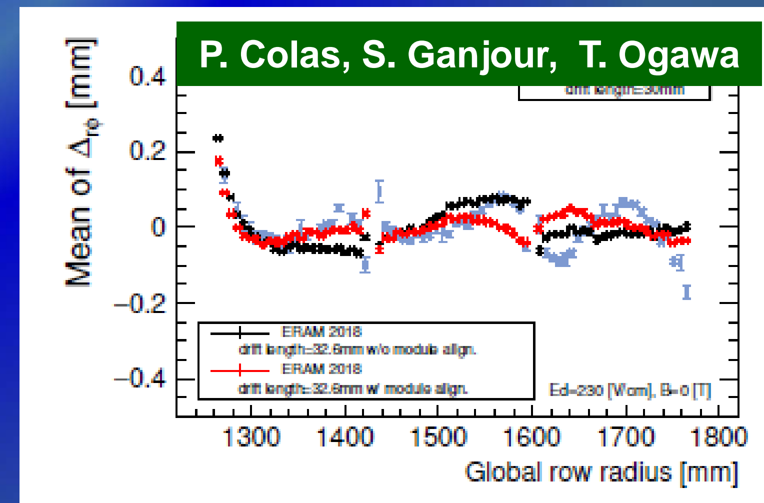
Distortion challenge: module flatness

control of mechanics (deformations if not rigid enough) → give rise to ExB effects



Distortion challenge: module edges

xy-plane (with new encapsulated anode)



P. Colas, S. Ganjour, T. Ogawa

Vertex and Central Trackers: Challenges

All-Silicon tracker (ILC/SiD, CLICdp, FCC/CLD, CEPC/FST)

- ✓ ILC: number of layers; thin detectors, time-stamping capability, minimize material budget (2D/ stitching); power savings / engineering;
- ✓ Circular colliders: continuous operation → power-pulsing is not possible (aim less power consumption & active (increased) cooling) → increased material budget;

Silicon + TPC (ILC/ILD, CEPC baseline)

- ✓ ILC: use of GEM-grid gating;
  CC: can TPC stand for (extremely) high readout rate; ion feedback – can it cope @ Z-pole;
- ✓ Calibration and detector alignment;
- ✓ Low power consumption FEE ASIC;
- ✓ Mechanical (field cage rigidity) and distortion (field cage quality, module flatness) challenges;

Silicon + Wire/Drift Chamber (FCC/IDEA, CEPC/IDEA)

- ✓ Can it cope with high rates @ Z-pole;
- ✓ Half as many hits as in TPC → more Si-layers → momentum resolution sufficient ?;
- ✓ Aging effects: hydrocarbon-based mixtures are not trustable for long-term operation in DC → search for different gas mixtures;
- ✓ Very long wires (~4m), study/optimize wires material;
- ✓ dE/dx by cluster counting (depends on N_{hits} in DC);

PID requested by flavor physics (TPC/DC have superior capability over Si) → see G. Wilkinson talk