Topical Workshop on Electronics for Particle Physics - TWEPP 2019

Santiago de Compostela September 2-6, 2019

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Introduction

- The TWEPP workshop is covering the aspects of :
  - Electronics for particle physics experiments, and accelerator instrumentation of general interest to users
- The purpose of the workshop is to :
  - Present results and original concepts for electronic research and development relevant to LHC experiments
  - Review the status of electronics for the LHC experiments
  - Identify and encourage common efforts for the development of electronics
  - Promote information exchange and collaboration in the relevant engineering and physics communities
- Covered topics :
  - ASIC
  - Optoelectronics and Links
  - Packaging and Interconnects
  - Power, Grounding and Shielding
  - Production, Testing and Reliability
  - Programmable Logic, Design Tools and Methods
  - Systems, Planning, Installation, Commissioning and Running Experience
  - Radiation Tolerant Components and Systems

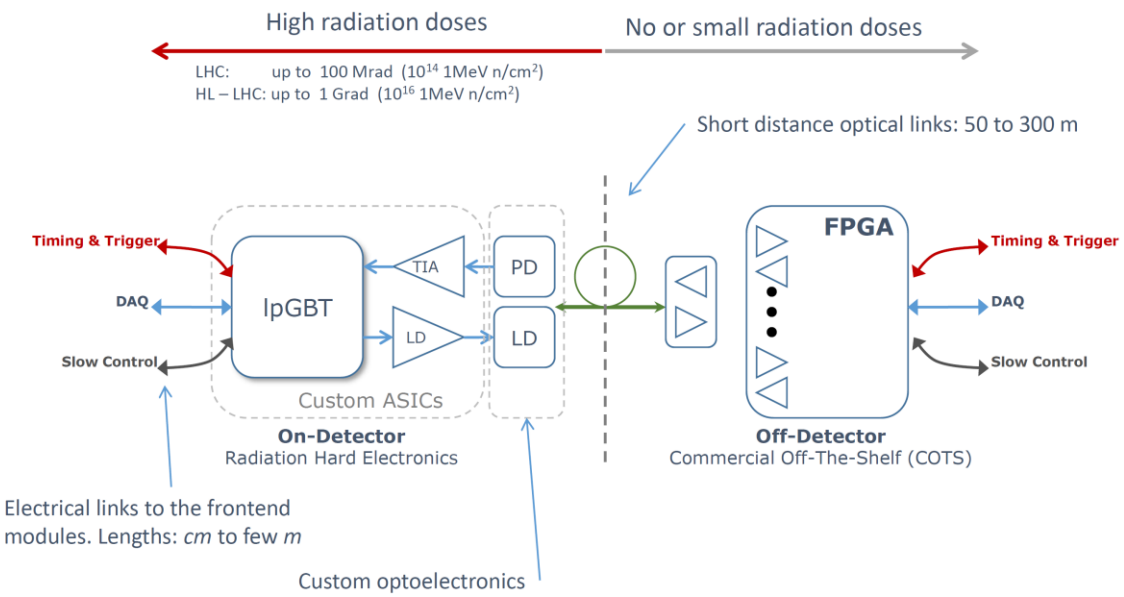
ASIC contributions

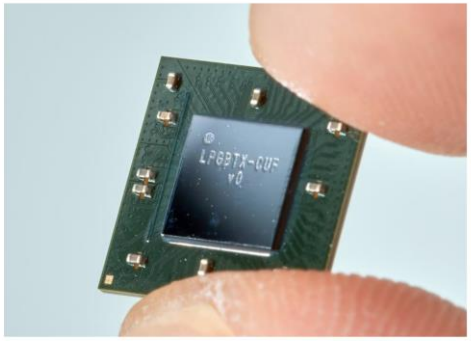
- 21 oral presentations
  - Data transfer lpGBT (7)
  - Readout Chips ROC (10)
    - Monolithic pixels ROC (4)
    - Readout chips for Timing Layers (3)
    - Other Readout chips - Fast data readout (3)
  - IP blocks: PLL/CDR, Monitoring ADC (3)
- 24 posters
  - Data Transfer (1)
  - Readout Chips ROC (10)
    - Monolithic pixels ROC (3)
    - Readout chips for Timing Layers (3)
    - Readout chips for MicroMegas detector
    - Fast readout data
  - ASICs for cryogenic environment
  - ASICs for Detector Control System (DCS) and monitoring

lpGBT project

1. Project description
2. CPPM contribution
3. Prospectives

lpGBT project





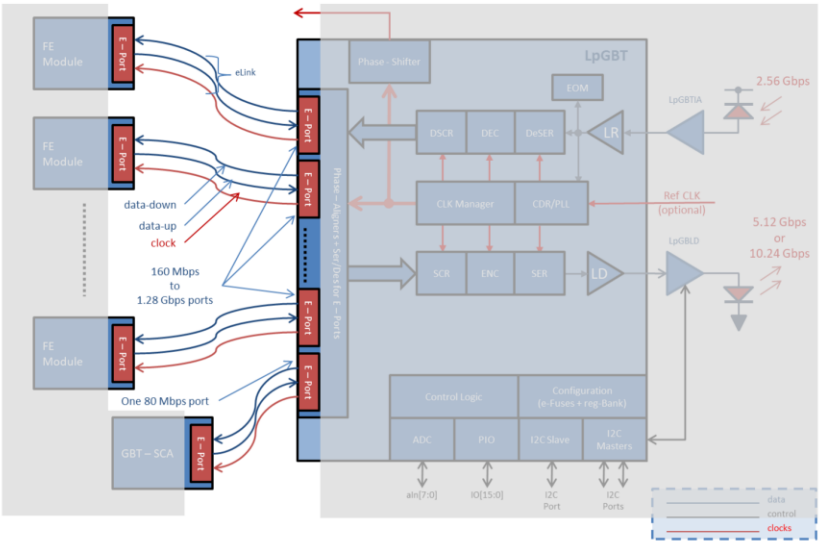
Pin count: 289 (17 x 17)
Pitch: 0.5 mm
Size: 9 mm x 9 mm x 1.25 mm

- More than a “Communications ASIC”
- Rates : **5.12 or 10.24 Gbps** (for uplinks) and **2.56 Gbps** (for downlinks)
- Enables the implementation of Radiation Tolerant Links : DAQ, Trigger, Slow control
  - Designed for radiation hardness
    - Total Ionizing Dose (TID): 200 Mrad
    - Extensive SEU protection (TMR)
- Implements Control and Monitoring Functions :
  - I2C Masters, 16 –bit General Purpose I/O port, Output reset pin, 10 –bit ADC (8 multiplexed inputs), 8 –bit voltage DAC, 8 –bit current DAC, Temperature sensor

The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC, P.Moreira et al.

lpGBT communication

- The counting room
  - Optical fibre links
- The FE modules / ASICs
  - Electrical links (eLinks)
- The Number and Bandwidth of eLinks is programmable
- For Down eLinks
  - Bandwidth: 80/160/320 Mbps
  - Count: 16/8/4
- For Up eLinks



Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Example of the RD53 FE chip
Control command : 320 Mbps
Output Data : 4 × 1.28 Gbps/s

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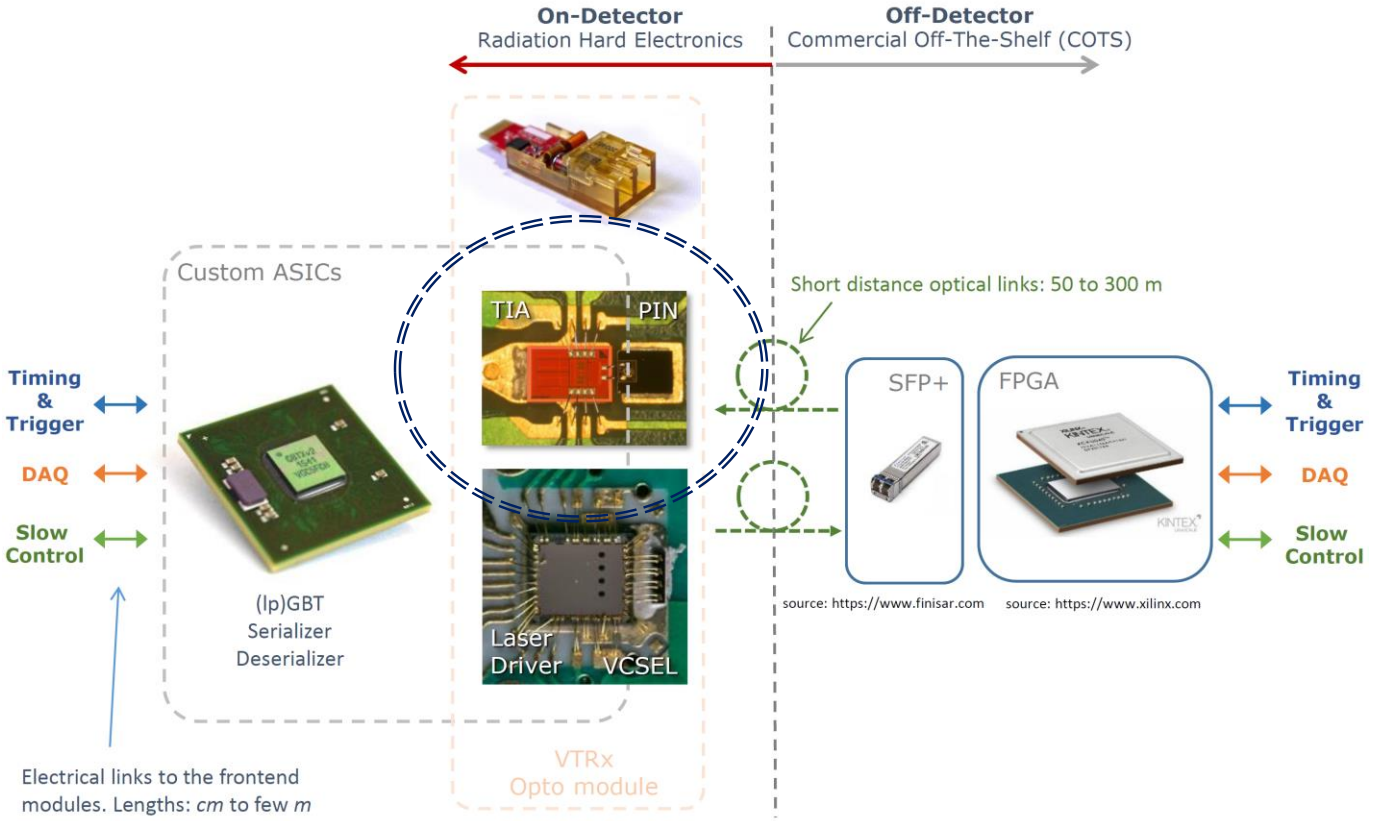
The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC, P.Moreira et al.

CPPM participation

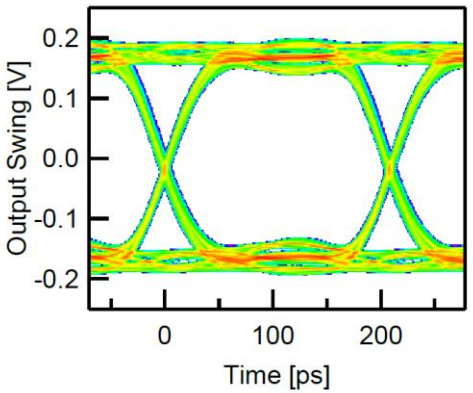


- GBTIA : 5 Gbps fully differential transimpedance amplifier
  - Designed for **photodiode capacitance values lower than 500 fF**
  - Sensitivity of −19 dBm with a BER of 10^{-12}
  - Radiation tolerant up to 200 Mrad
  - Wafer tests for production

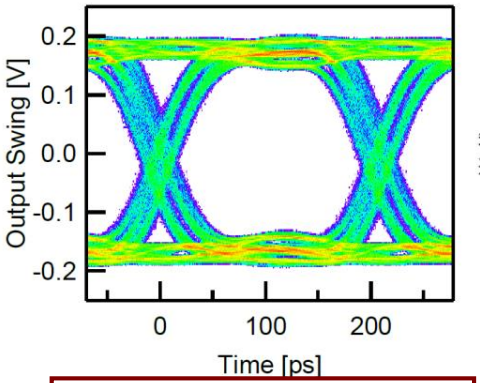
A 5-Gb/s Radiation-Tolerant CMOS Optical Receiver, Menouni, M. ; Tianzuo Xi ; Ping Gui ; Moreira, P IEEE TNS

GBTIA → lpGBTIA

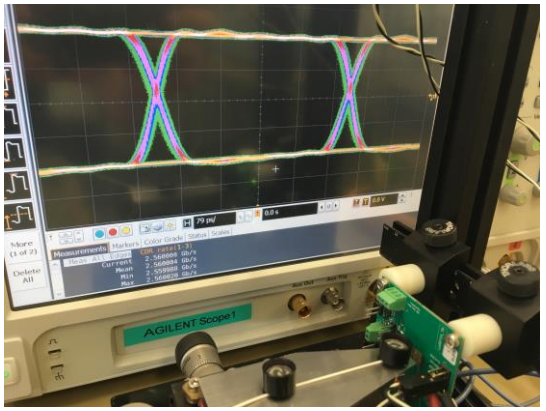
- InGaAs photodiode :
  - Advantage : Lower degradation of the responsivity with irradiation
  - Drawback : Strong increase of the junction capacitance with irradiation
- The GBTIA post-irradiation eye diagram shows a strong increase of the deterministic jitter
  - Jitter levels incompatible with the lpGBT applications, mainly for clock recovery
- lpGBTIA designed to cope with the InGaAs photodiode capacitance increase
  - Process CMOS 65nm
  - A constant output swing of 400 mV
  - For a power supply of 2.5 V the power consumption is 73 mW
  - For -6 dBm input :
  - Rise time = 30 ps
  - Total jitter = 0.15 UI @ BER = 10^{-12}



GBTIA : 2.56 Gbit/s
Pre-Irradiation



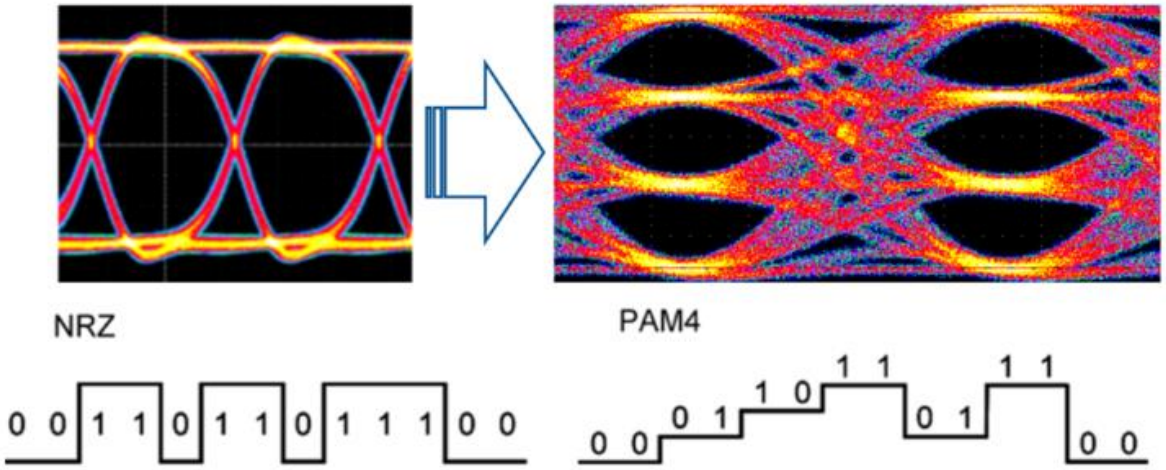
GBTIA : 2.56 Gbit/s
With Irradiated InGas photodiode



Eye diagram 2.56 Gbit/s
Optical power = -6 dBm
Differential

The lpGBTIA, a 2.5 Gbps Radiation-Tolerant Optical Receiver using InGaAs photodetector, M. Menouni et al.

Outlook ideas

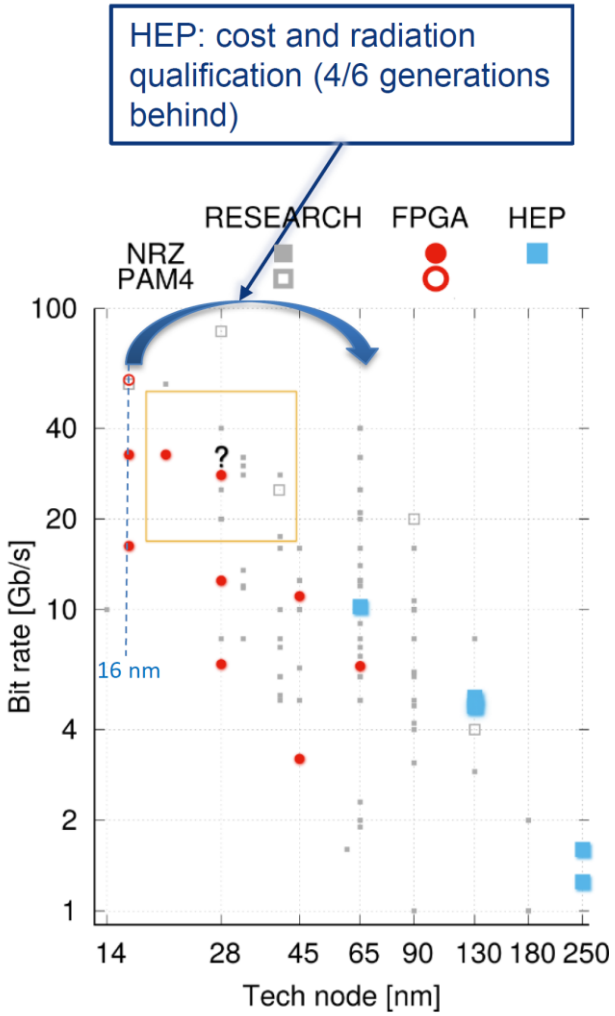


- Pulse – Amplitude – Modulation with 4 amplitude levels PAM-4
- “Symbols represent two bits
  - Level 0: 00
  - Level 1: 01
  - Level 2: 10
  - Level 3: 11
- PAM-4 enables twice the transmission capacity when compared with NRZ
- Two bits transmitted each symbol period

- PAM-4 standard within the IEEE 802.3 Ethernet and Optical Internetworking Forum (OIF)
- Data rates are highly correlated with the technology nodes
- State of Art of the Commercial systems based on FPGA :
  - 116 Gbps PAM-4 from Intel & Xilinx
- Radiation hard ASICs :
  - Research papers showed that 40 Gbps NRZ possible for nodes ≤ 65 nm
  - PAM-4 : 28 nm or below ?

Outlook ideas

- Data rate is correlated with the technology node
- PAM-4 → doubles the transmission capacity
  - 116 Gbps or 58 Gbps ? (TID effects)
- Several technology nodes can be envisaged
- The 28nm becomes the workhorse
  - Irradiation tests already started at CERN and other HEP institutes
  - CPPM contribution to this task?
    - Tests
    - TID effect Modeling
- Other ideas :
  - Building block for PAM4 :
    - PIN – Receivers
    - Laser / VCSEL Drivers
    - ADCs
    - PLL & CDR
    - Serializers & DeSerializers
    - Drivers and receivers for electrical cables
- This work can be conducted in collaboration with CERN and involving other in2p3 labs
- A document is currently being prepared



Serial Links Beyond 10 Gbps : P.Moreira , ACES 2018

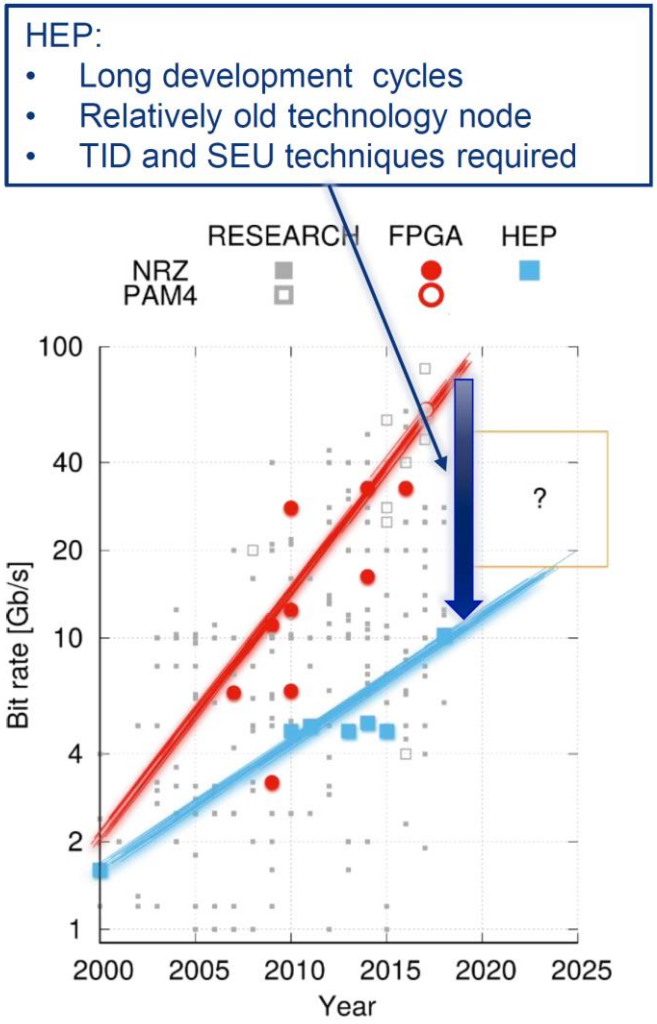
Thank you for your attention

Futur developments

- Développements futurs de liens haute vitesse (optiques ou électriques) dépendent de :
  - Machine et des niveaux de radiation :
    - HL – LHC: > 100 Mrad
    - CLIC: < 1 Mrad
    - FCC: > 1Grad
  - Type du détecteur (Detectors à pixels, Calorimètres)
  - Vitesse requise pour la transmission
  - Puissance
- programme R&D (2020 – 2025) :
  - Upgrade HL-LHC (“LS4”)
  - Préparer la voie pour d’autres projets futurs (FCC, ...)
  - Quantité de données très importante
  - Environnement niveaux d’irradiation extrêmes

Performances actuelles

- Performances des ASICs pour la physique des particules sont limitées :
  - Longs cycles de développement
  - Qualification pour la tolérance à la dose
  - Utilisation d'anciennes générations de process (accès et coût)
  - Techniques de design Circuit:
    - Tolérance à la TID et aux SEU
- Pour les R&D 2020 to 2025
  - Cibler 20 - 40 Gb/s
  - Compatibilité avec les performances des FPGA



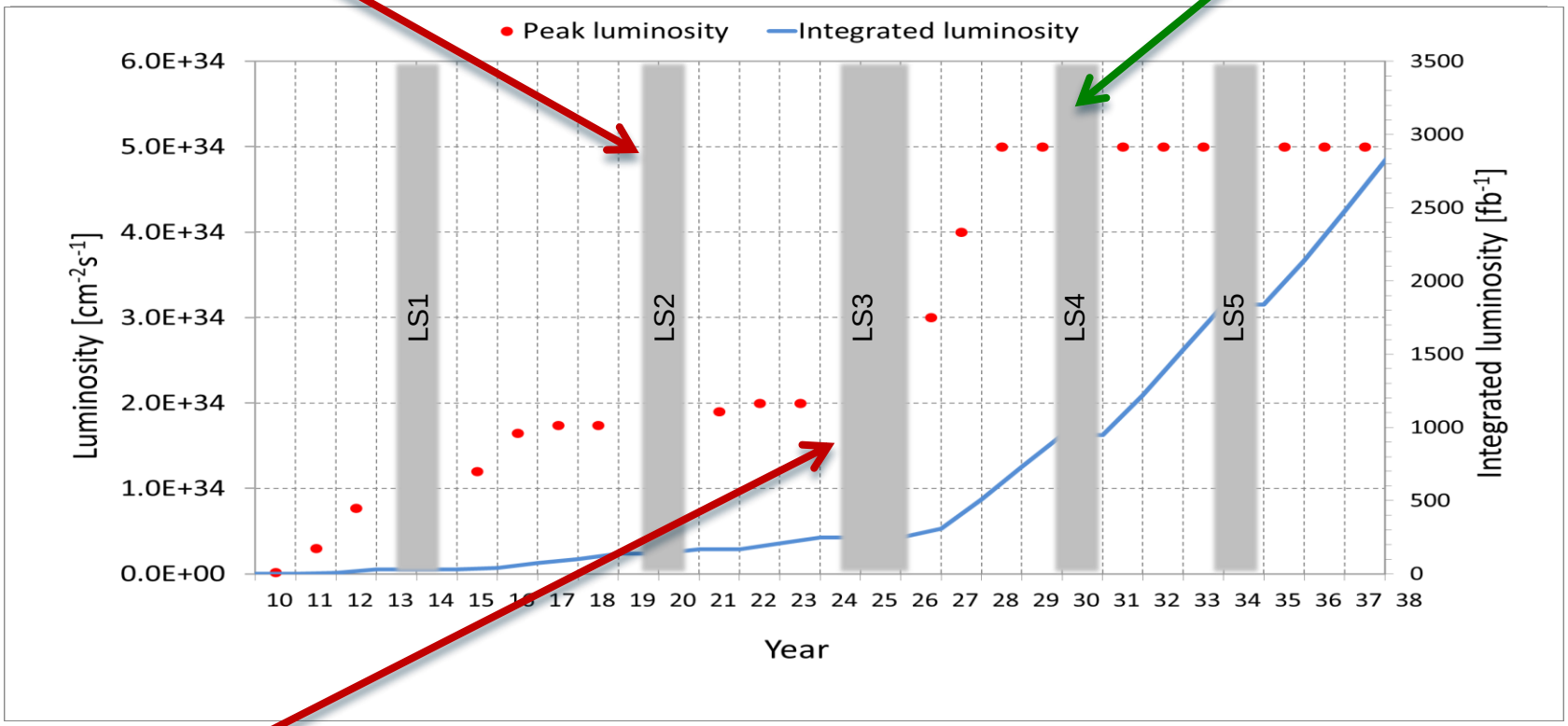
Radiation hardness

- Radiation hardness is the major technical challenge:
  - High-Speed CMOS Asics currently being used by the HEP community will not survive TID doses higher than **100 / 200 Mrad**
  - Experience in qualifying active optoelectronic components points to the exclusion of opto-devices for radiation environments exceeding **3×10^{15} n/cm2**
  - The radiation resistance is not changing with **new generations of optoelectronic components**
- Possible Solutions:
  - Explore new commercial IC technologies
    - Large qualification work
  - Explore new optoelectronic devices:
    - Optical modulators with external and remote laser source
  - Explore electrical links for extreme radiation environments:
    - Large bandwidths in low mass cables might be difficult to achieve (RD53)

Planning du LHC

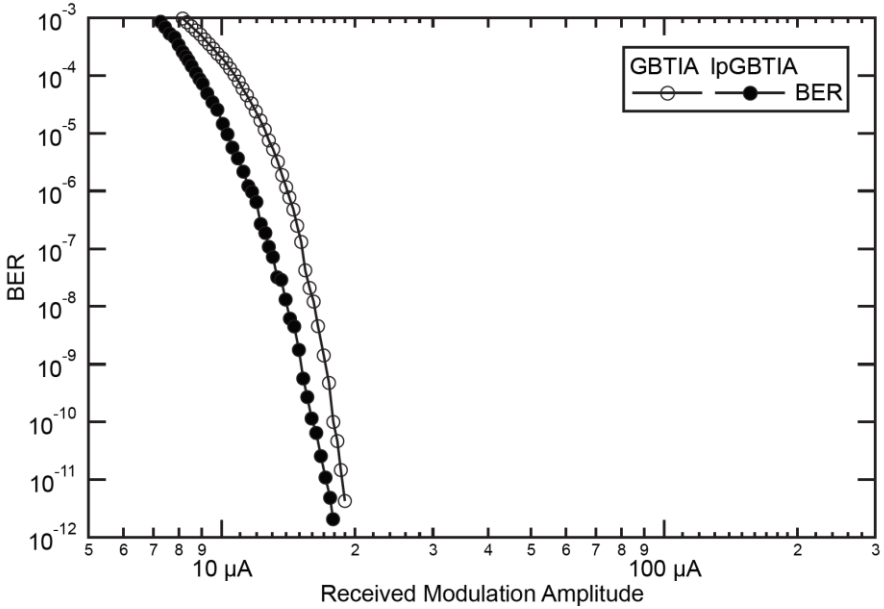
PHASE I Upgrade
ALICE, LHCb major upgrade
ATLAS, CMS, minor upgrade

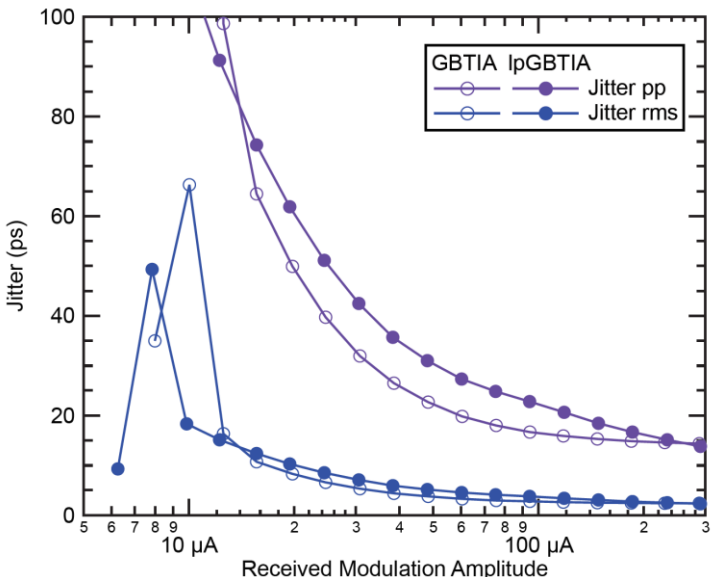
PHASE III Upgrade
R&D: 2020 - 2025

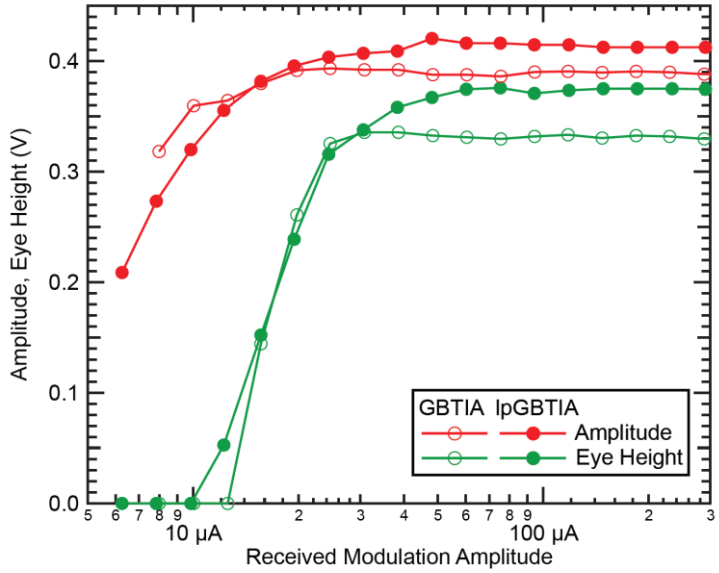


PHASE II Upgrade
ATLAS, CMS major upgrade

lpGBTIA performance

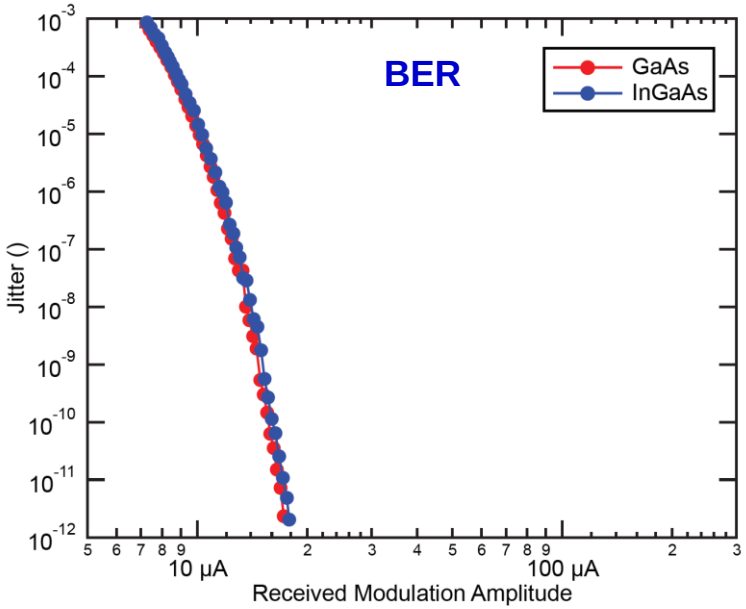


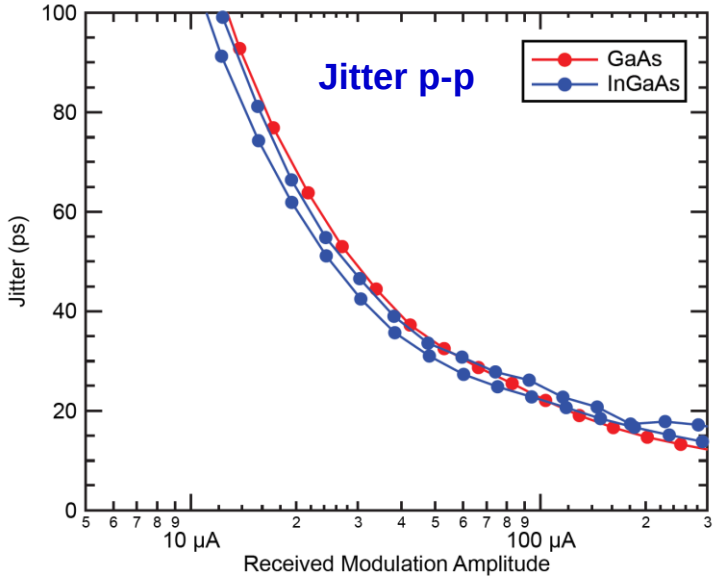


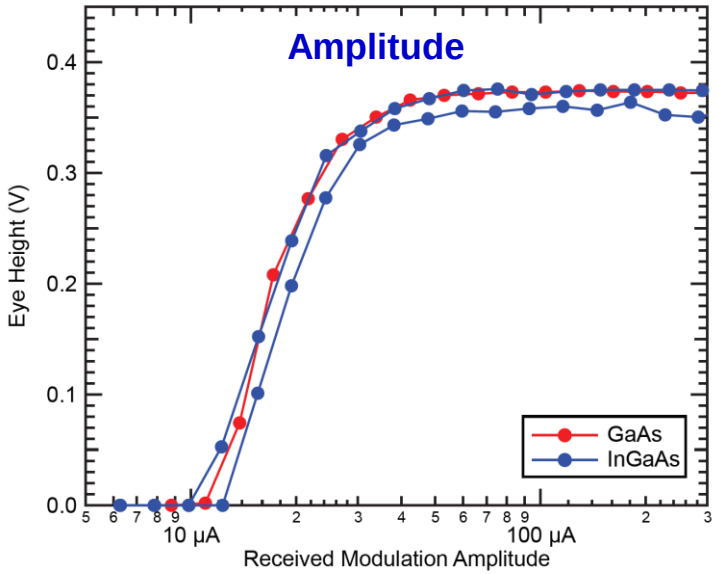


- Pre-irradiation results
- InGaAs photodiode capacitance <400 fF
- At 2.56 Gbps, the lpGBTIA is showing similar results as for the GBTIA receiver
  - Similar Sensitivity, Eye amplitude, Eye height
  - The measured Jitter is higher for the lpGBTIA due to non-50% crossing point

lpGBTIA performances



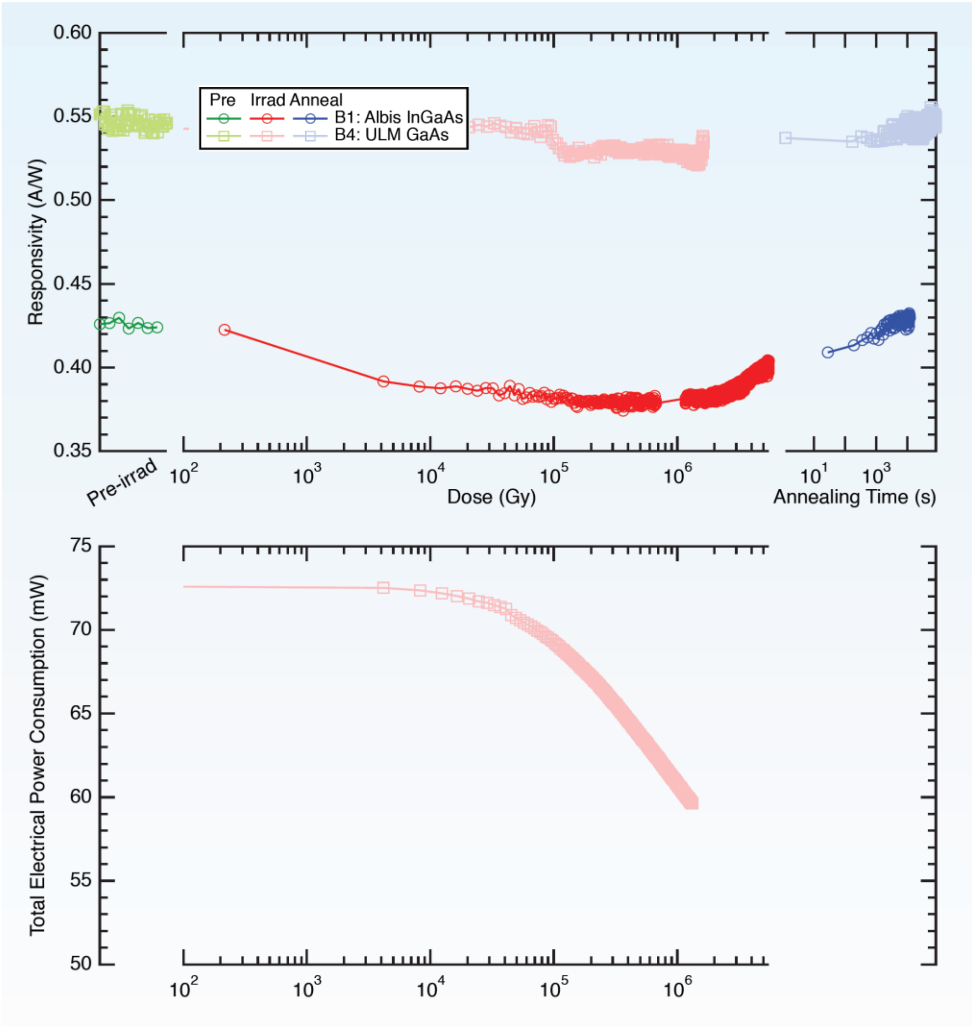




- Pre-irradiation results performances are very similar for receivers based on InGaAs or on GaAs photodiode
  - Negligible leakage current for both devices
  - Similar junction capacitance before irradiation (< 400 fF)

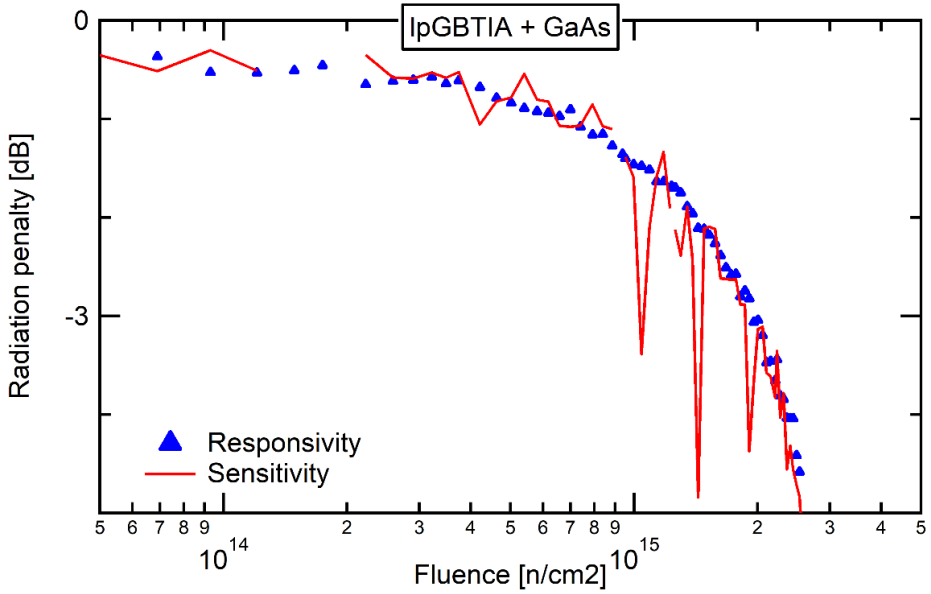
Xray Irradiation

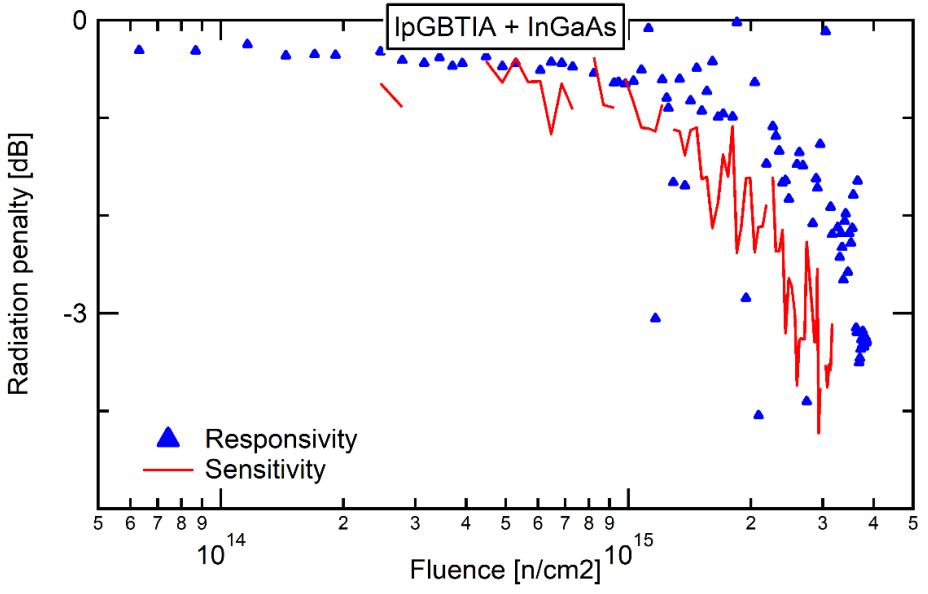
- 2 samples were measured
  - B1: Albis InGaAs photodiode tested up to 550 Mrad
  - B4: ULM GaAs photodiode tested up to 160 Mrad
- Dose rate : 9 Mrad/hour
- External power applied to both 2.5 V and 1.2 V pads
- The power consumption decreases with the TID
  - Thick oxide transistors used for 2.5V to 2V conversion
- The responsivity loss is < 15% for the InGaAs sample and recovers its initial value with annealing
- Sensitivity and jitter not affected
- Eye-parameters vs input optical power seems unchanged regarding the pre-irradiation values



Neutron Irradiation

- Several samples exposed to 20 MeV neutrons at the Cyclotron of Louvain la Neuve (T2 beamline)
- Receiver based on InGaAs photodiode is showing better results than GaAs after irradiation in terms of sensitivity or responsivity
  - Validating the architecture choice





Conclusion and Perspectives

- The 2.56 Gbps lpGBTIA receiver is developed with the commercial 65 nm process
- The design maintains good performance coping well with the shift of the InGaAs photodiode parameters with irradiation
  - Leakage current and junction capacitance increase
- A new photodiode bias circuit is proposed and implemented in order to maintain the photodiode capacitance at a reasonable value
- The optical receiver based on the lpGBTIA and InGaAs photodiode was tested and showed good performance at 2.56 Gbps
- Several samples were irradiated with X-ray and 20 MeV neutrons
- Irradiation tests showed that the performances in terms of responsivity and sensitivity are still acceptable for $3x10^{15}$ n/cm2
- Increase of the power consumption while irradiated
  - Still to be understood
  - Heavy – Ions and Two-Photon SEU tests to be done soon

Main measurements

- The main receiver side parameters are : responsivity and sensitivity
- Measured by attenuating the input signal with predefined steps and measuring :
  - The photocurrent level (RSSI signal)
  - The Bit Error Rate (BER)
  - The input optical power at each attenuation step
- The responsivity is derived from a linear fit of the photo current versus the input optical power
- The sensitivity is defined as the input optical modulation amplitude producing a BER of 10^{-9}
- The signal amplitude, the eye height and the Jitter are extracted from the measured eye diagram

Le chip GBTIA

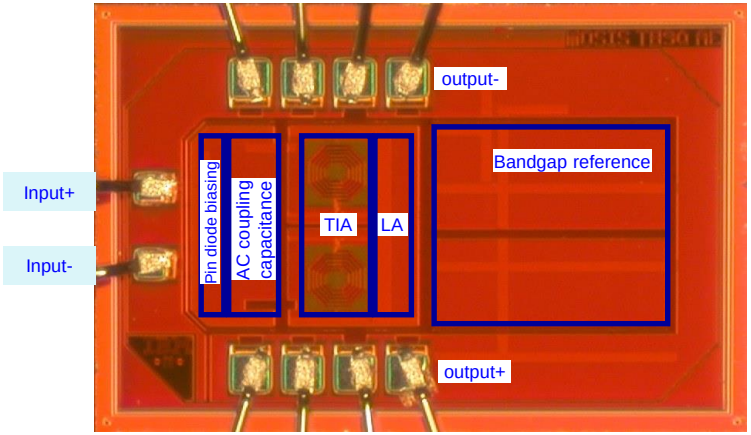
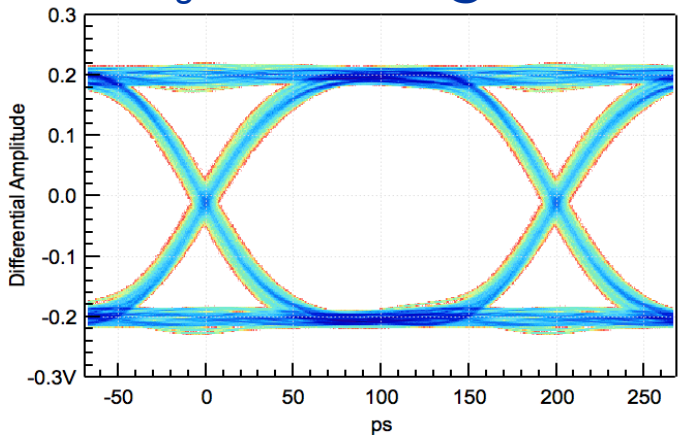


Diagramme de l'œil @ 5 Gb/s



GBTIA-ROSA

- Process CMOS 0.13 µm.
  - ❑ n-MOSFET : f_T de l'ordre de 100–120 GHz
  - ❑ Taille du chip : 0.75 mm × 1.25 mm
- Excellentes performances
- 5 Gbits/s : sensibilité de -19 dBm pour BER=10^{-12}
- Consommation < 120 mW
- Tolérance aux radiations > 200 Mrad
- Nouveau design en 65 nm pour début 2018