Status of Hyper-Kamiokande

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Neutrino LLR meeting, 2020/01/31, Palaiseau

I. Status of the construction/fundings

Status of Hyper-Kamiokande

- 13th of December :

  → The Japanese cabinet has approved construction of Hyper-K !

  → Needs to be approved by Japanese Diet (Parliament).

  → Construction start this April 2020.

  → First data taking in 2027.

- The budget has been approved for 649 oku-yens (10^8 yens ~ 1 million $):
  - 75 % for Japan (so 490 oku-yens).
  - 25 % for international contribution (160 oku-yens).

+ Japan will receive 73 oku-yens for JPARC beamline upgrade

What is approved ?

- Budget approved by MEXT :

Components	Japan	Overs
Cavern	246	-
Tank and	125	-
Photo-detection	70	147
Water system	37	-
Management,	24	-
Total	502	147

Components	Japan	Overs
J-PARC upgrade	33	-
ND/IWCD facility	10	-
ND/IWCD	-	30
Total	43	30

20 % coverage of 20'' B&L PMTs.

- What is not covered by Japan:

1. Additional 20 % photocoverage to reach same 40 % as SK.

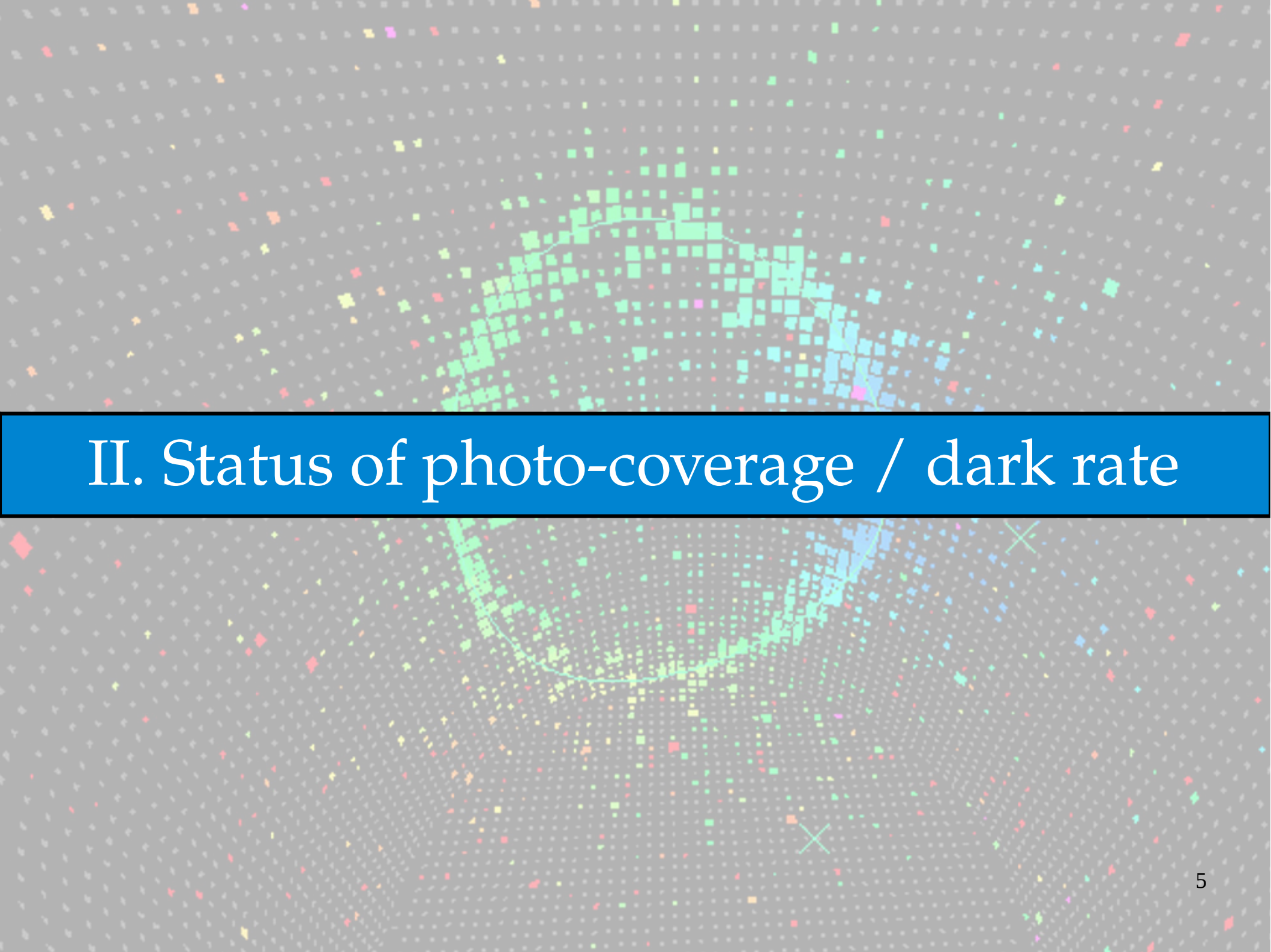
→ Fund additional/complementary/different PMTs ?

2. Price for electronics is not included → If Japan funds it, PC ↓.

→ Fund component of the PMTs electronics ?

3. 75 % of the price of IWCD (everything apart from excavation).

→ Fund mechanics/PMT/electronics/water system of IWCD ?

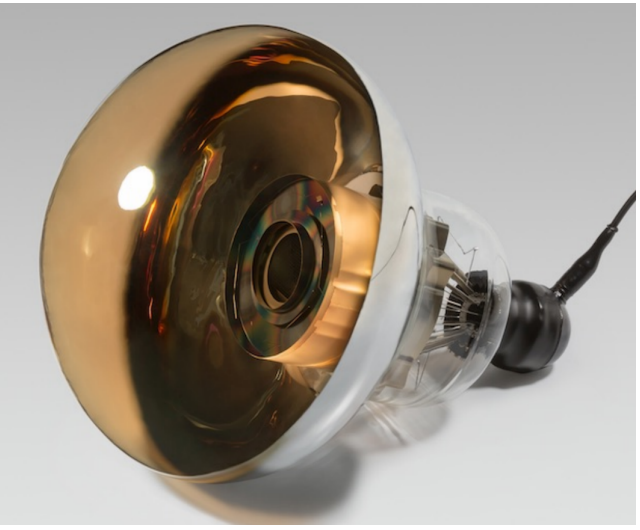


II. Status of photo-coverage / dark rate

Status of Hyper-Kamiokande

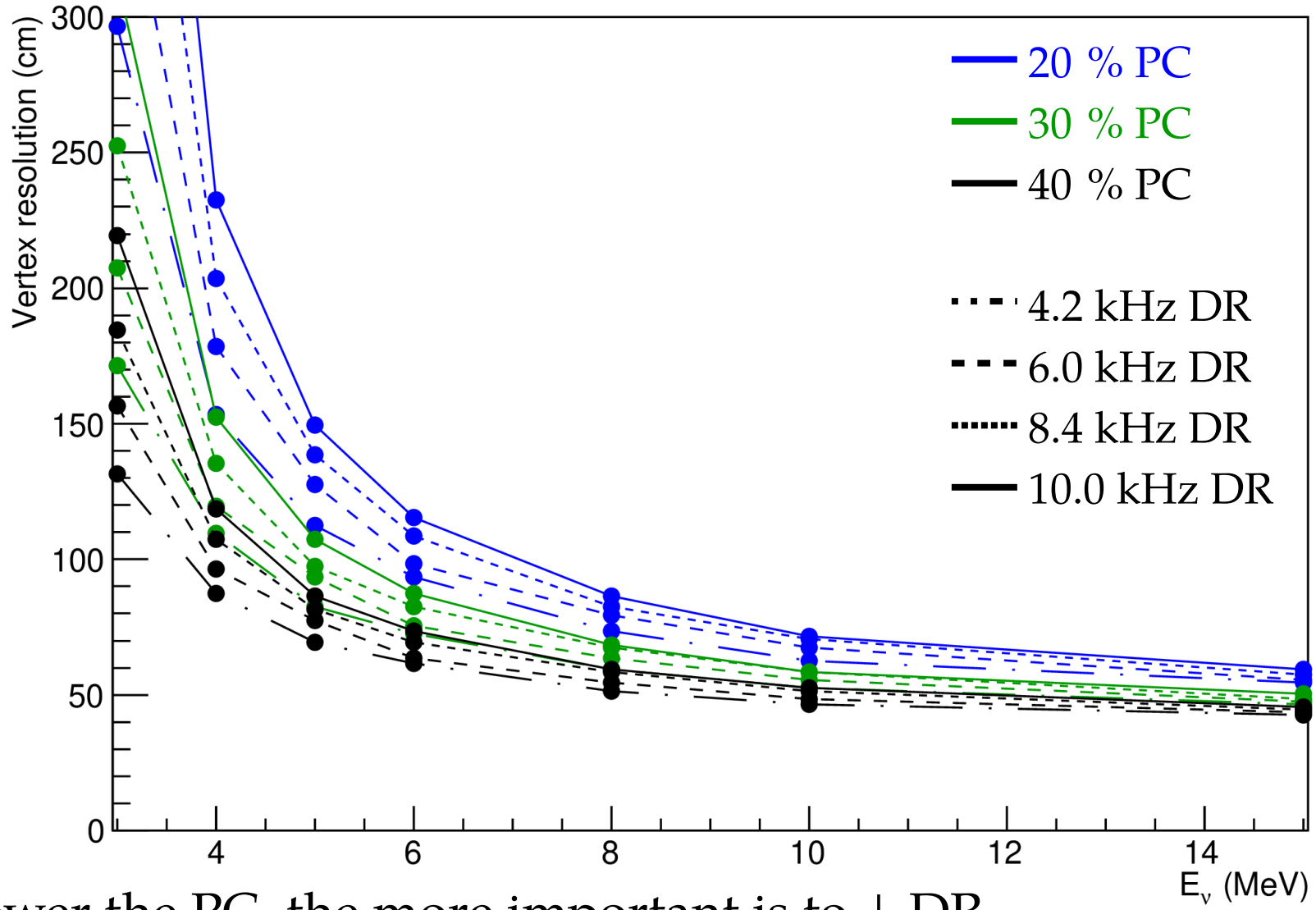
- Budget for 20'' PMTs is not completely fixed
  → If other countries takes care of other tasks : more $ for PMTs.
- Also, the price of one PMT is not fixed :
  → Bidding/Tender (Appel d'offre) will be made namely between 2 companies : Hamamatsu (B&L PMTs) and NNVT (MCP PMTs).

	Hamamatsu B&L PMT	NNVT MCP PMT	SK PMT
QExCE	31 % x 95 %	30 % x 95 %	22 % x 70 %
TTS	2.6 ns	4.3 ns	6.7 ns
Dark-rate	4.2 kHz	8 kHz ?	4.2 kHz



- MCP cheaper than B&L ?
  → Higher DR but higher PC ?
  + Competition to ↓ price.
- Not excluded to have a mix of 2 PMT types

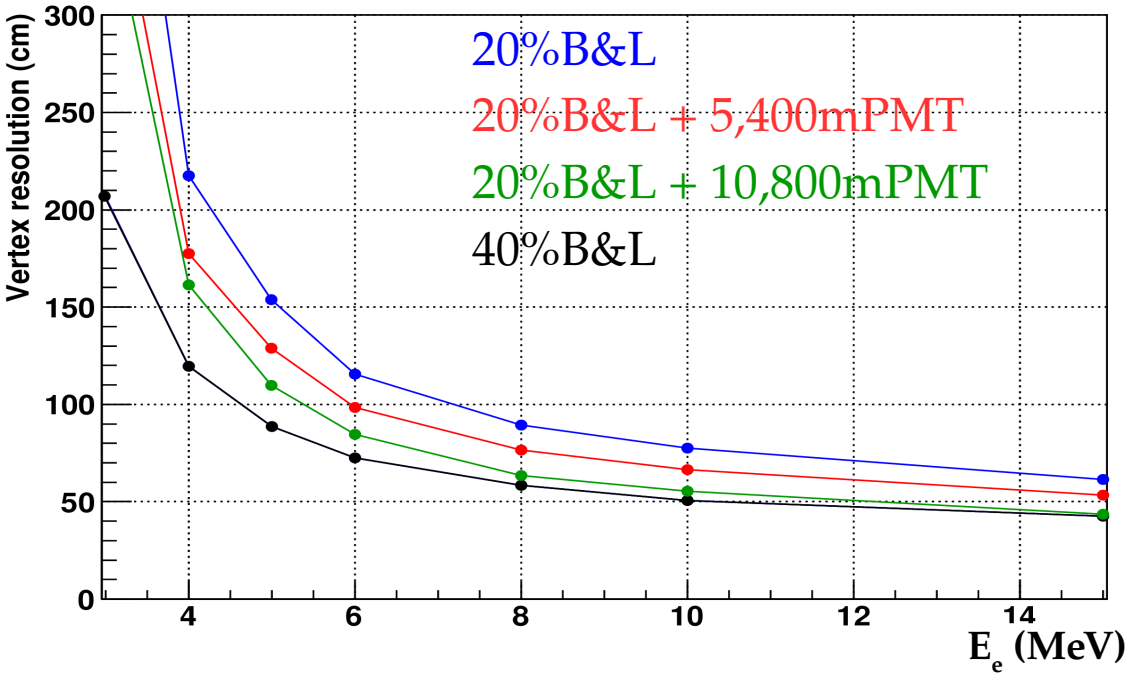
Results for various 20″ configurations



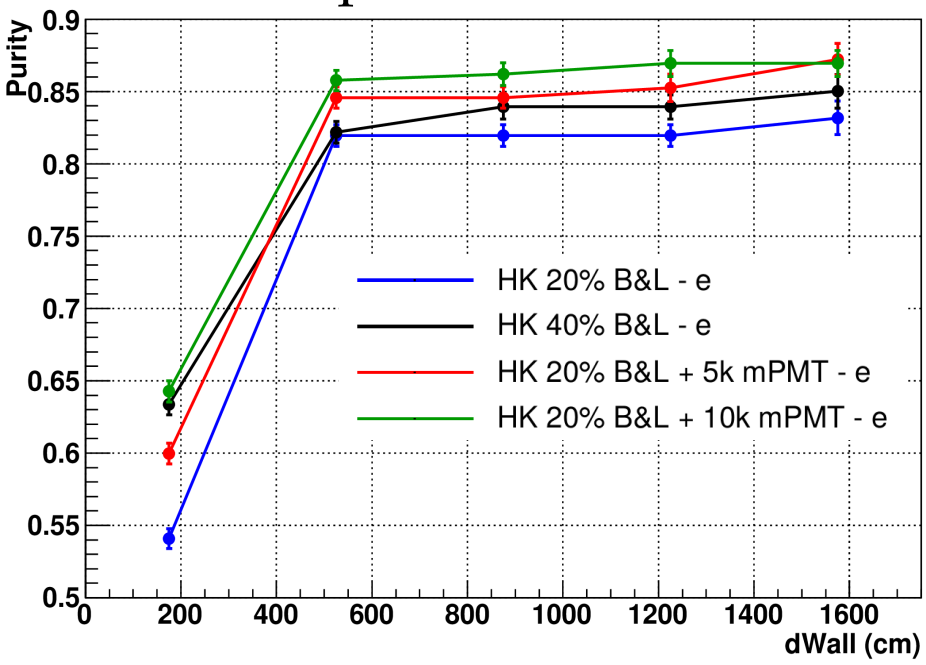
- The lower the PC, the more important is to ↓ DR.
- LE threshold largely changed when ↑ PC from 20 % to 30 %.
- If DR ≤ 8.4 kHz, it is more efficient to ↑ PC by 10 points than ↓ DR.
- 30 % PC – 4.2kHz ↔ 40 % PC – 7.0 kHz.

Results for various mPMT configurations

B&L 8.4 kHz – 3″ PMT 100 Hz



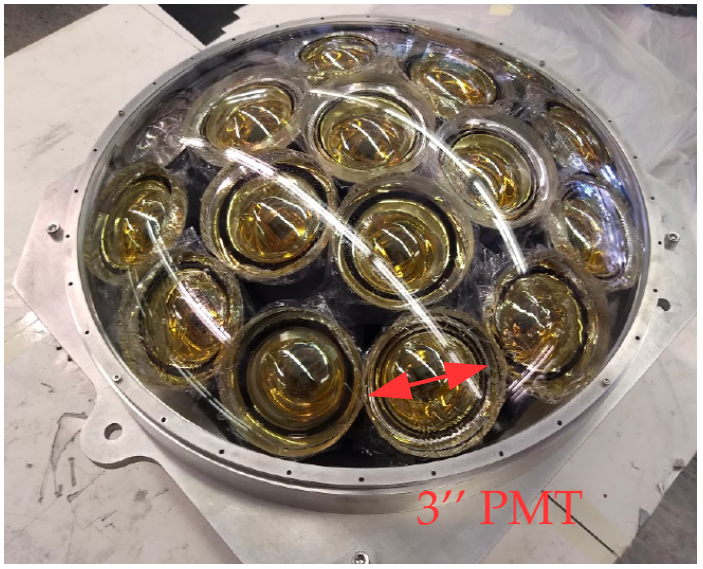
E/π^0 separation @500MeV



- Multi-PMTs are also considered. They impact both low and high energy.

- LE : ↓ LE threshold → probe upturn. ↑ FV.

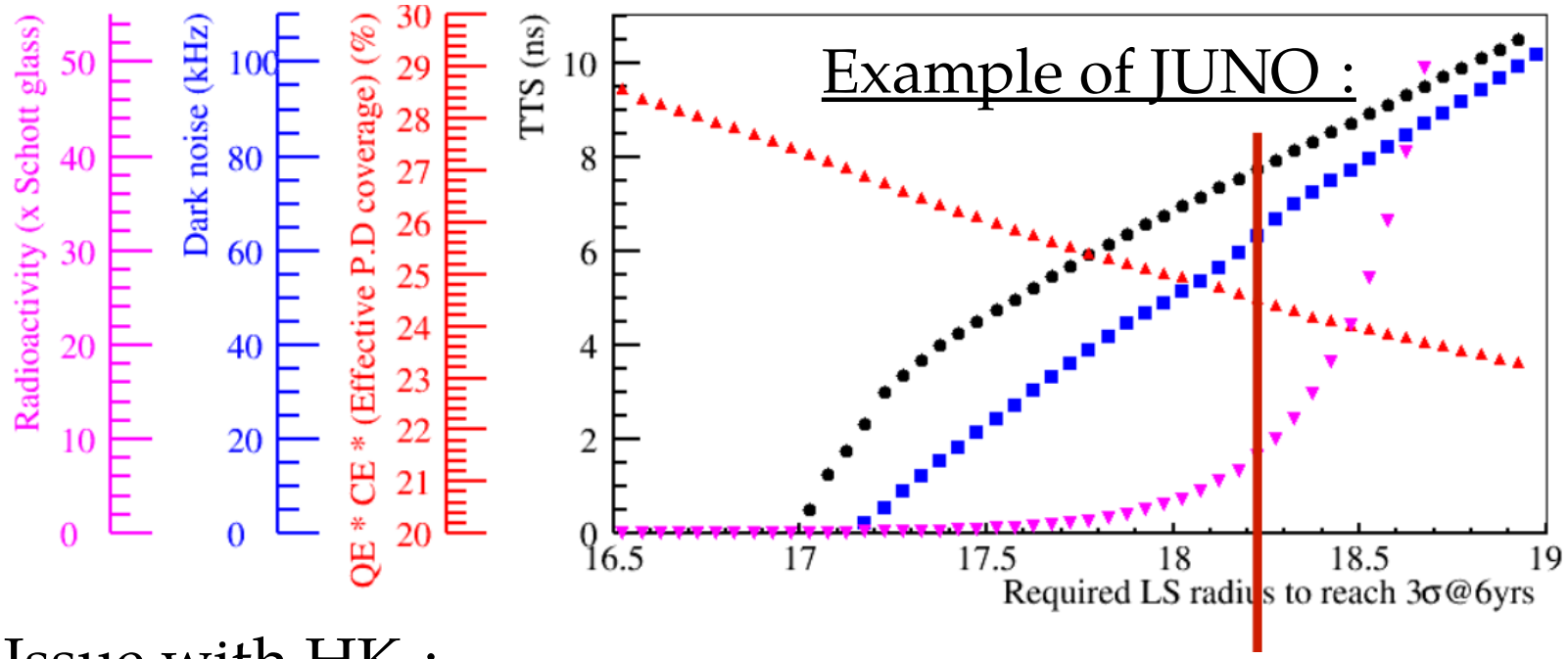
- HE : ↑ vertex resolution and PID.
  ↑ multi-ring reconstruction
  ↑ charge linearity → ↓ E-bias systematics.



Bidding score

To make a decision, we are :

- Writing TN studying impact of PMT configurations on physics : 2020/01
- Writing 3 TN : B&L, MCP and mPMT hardware TN : 2020/02.
- Making a bidding score of configurations « a la JUNO » : 2020/02 ?



Scale PMT Spec for LS quantity to reach 3σ@ 6year

Issue with HK :

- Physics spread from ~MeV to several GeV → Need a bidding score for each physics ?
- We still do not have all software to evaluate impact on physics.

What next ?

- Need to make a decision this year about the proportions of B&L and MCP PMTs → PMT production should start in 2020 to be ready in 2027.

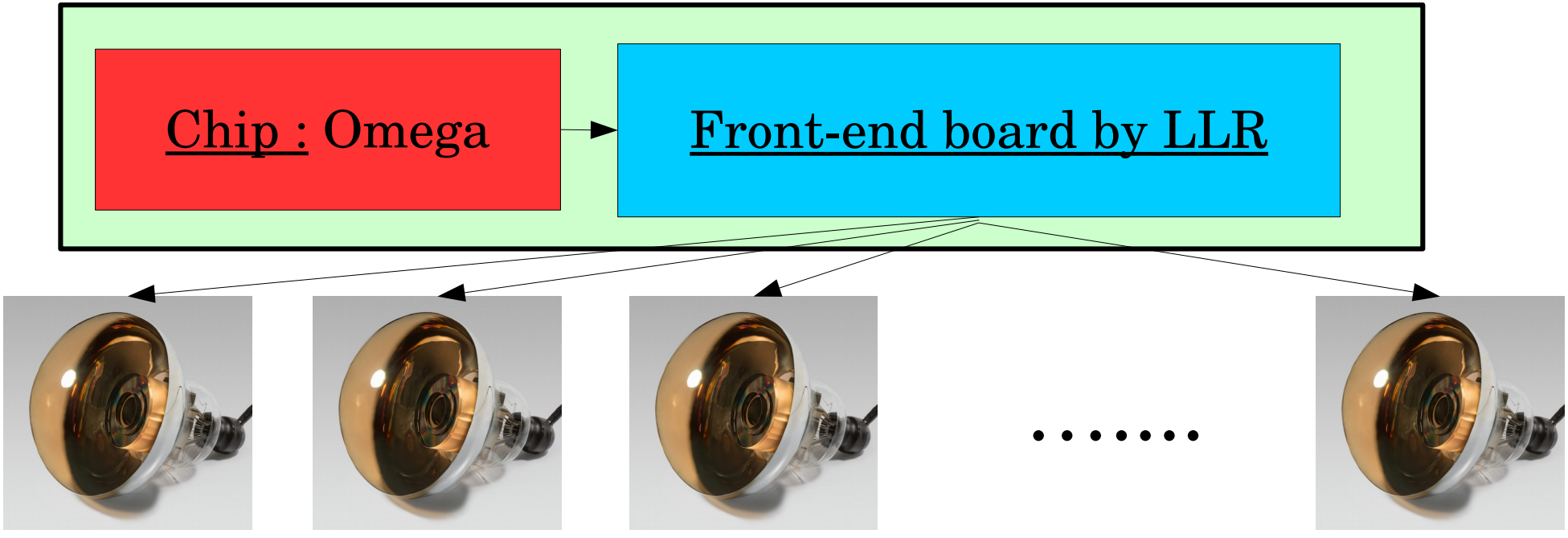
- For multi-PMT, we will have discussions → May try to push the idea that each country funds a dedicated topic of mPMT, instead of just buying N % of them → Discussion tonight Japanese Time (3 p.m CET)

III. LLR/Omega proposal for electronics

Our proposal for Hyper-Kamiokande

- Electronic expertize on Front-End development for ν-detectors.
- Long-standing collaboration between Omega and LLR engineers on various projects : WAGASCI, ND280-upgrade for T2K, HGCAL etc.
- Omega and LLR are physically in the same site (Ecole polytechnique)

→ Proposal : Develop the front-end electronics of the 20'' PMTs.



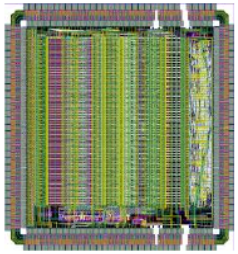
What Omega chips are availables ?

- Various chips for SiPM and PMT detectors:

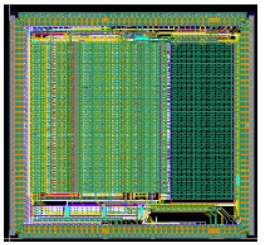
Chip	detector	ch	DR (C)
MAROC	PMT	64	-2f-50p
SPIROC	SiPM	36	+10f-200p
SKIROC	Si	64	+0.3f-10p
HARDROC	RPC	64	-2f-10p
PARISROC	PM	16	-5f-50p
SPACIROC	PMT	64	-5f-15p
MICROROC	µMegas	64	-0.2f-0.5p
CATIROC	PM	16	50fC-300pC

http://omega.in2p3.fr

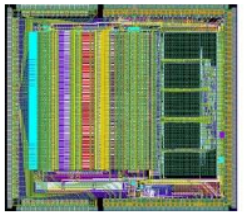
MAROC3



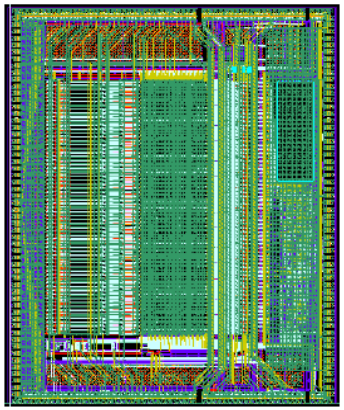
HARDROC2



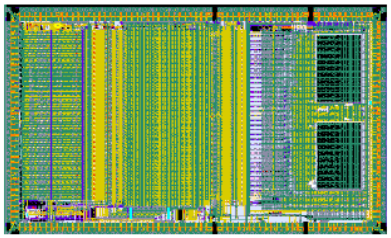
MICROROC1



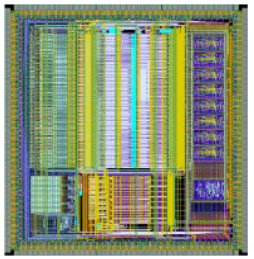
SKIROC2



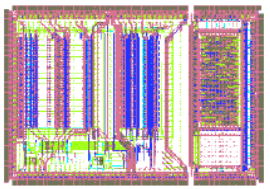
SPIROC2



SPACIROC



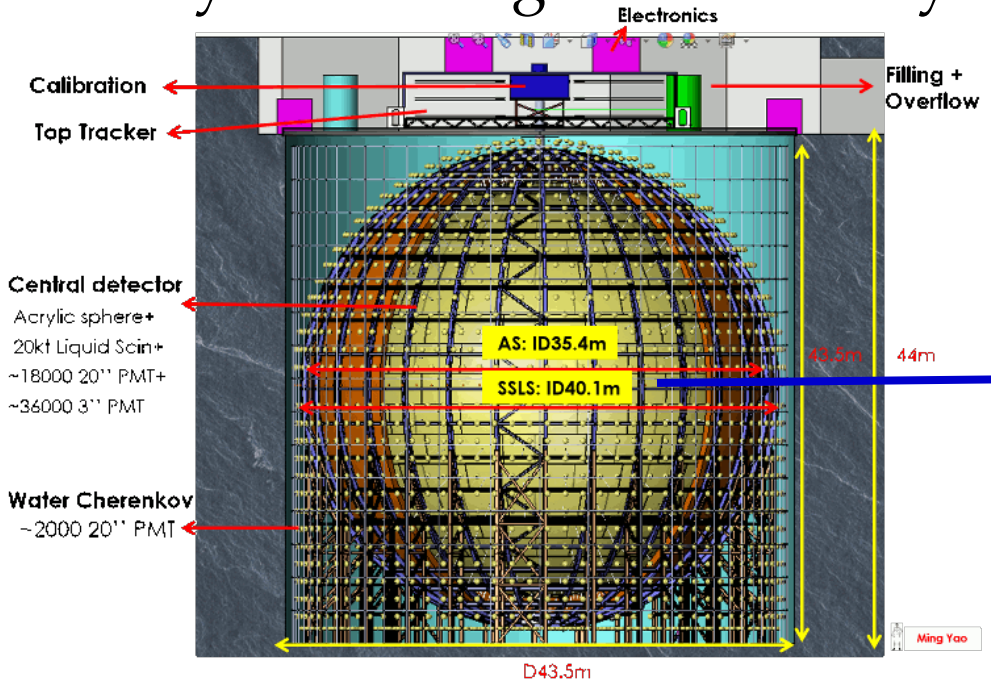
PARISROC2

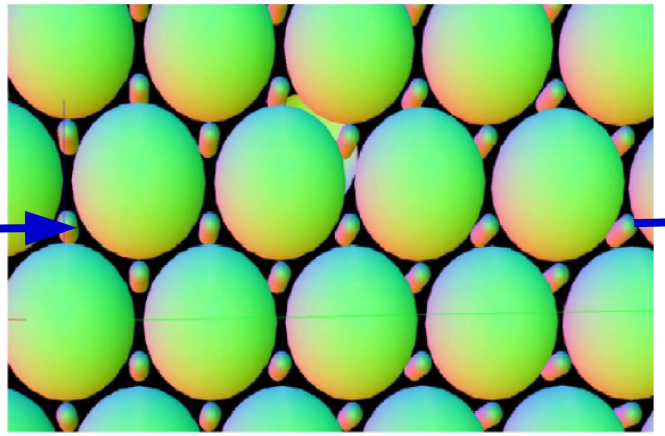


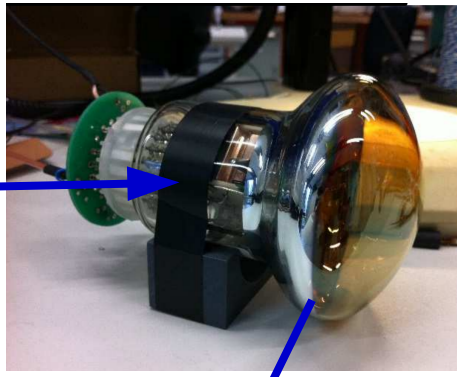
- CATIROC is a good basis to start development.

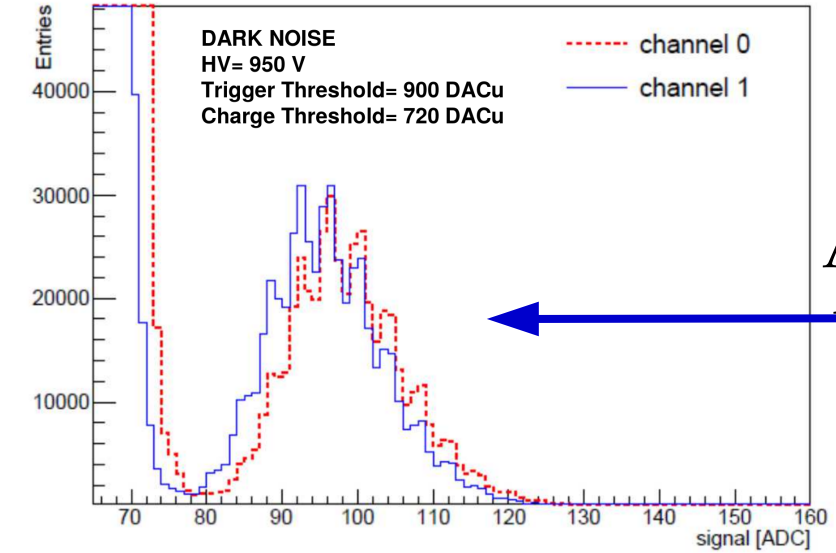
CATIROC chip for JUNO

- CATIROC readout JUNO 3'' PMTs : Similar requirements than HK 20'' ?
  → Dynamic range considerably higher for 20'' (3'' mostly receives 1p.e.).





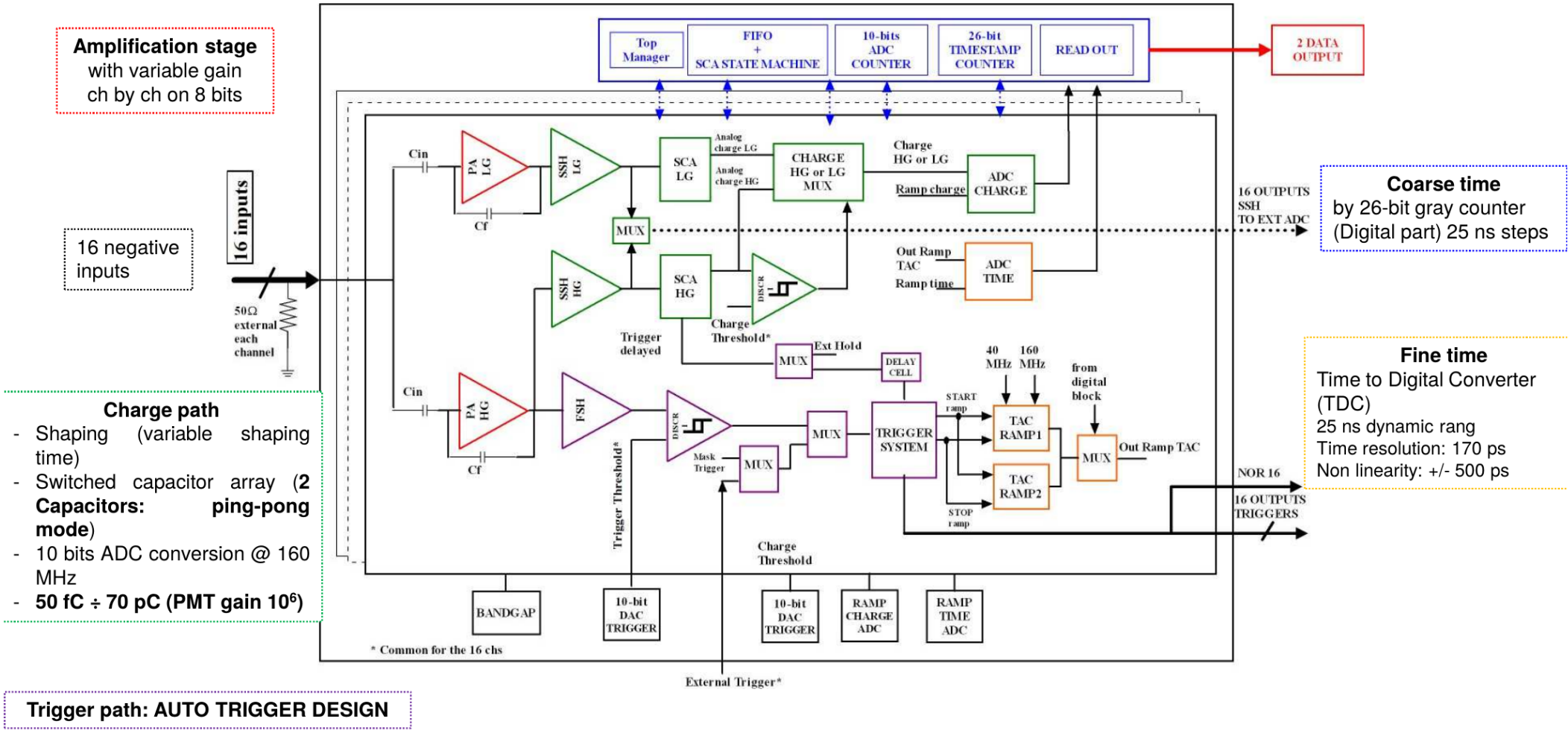




Analog output read by FPGA on Front-End board.

The CATIROC chip

- 16 auto-triggered channels.
- Each channel has 2 responses (HG and LG) provided by 10bits ADC operating at 160 MHz.
- Timing response is provided by : a digital slow clock of 40 MHz (25ns) + a TDC → Reach 170 p.s resolution.



Summary of the CATIROC

- CATIROC performances vs HK requirements.

Trigger	Self triggering for each channel
Nb channels	16 to bring ideally to 24
Discriminator threshold	0.25 p.e. → so far tested with 0.3 p.e
Channel dead time	6.4 µs → < 1 µs : use new/faster ADCs.
Charge dynamic range	From From 0.1 to 400 p.e → 0.1 to 1250 p.e : use 12 bits ADC
Charge resolution	0.05 p.e. RMS < 25 p.e → < 0.07 RMS at 1 p.e, < 0.05 otherwise
Timing resolution	RMS < 0.3 ns at 1 p.e. → 170 ps at 1 p.e
Power consumption	1 W/ ch → 21 mW/ch

- The CATIROC chip is a very good basis.
  → Some points to clearly improves.
  → Ω is willing to develop a new chip generation solution for HK and large-underground detectors.

Requirements satistified ?
- Yes
- No but not an issue.
- No but very close.
- Needs improvements.

From CATIROC → New Chip + ASICS

Omega

C. De La Taille.

S. Conforti Di Lorenzo

- High interest to develop a CATIROC successor for HK/ undeground experiments
- Development of a new chip to match HK requirements

  → ~12 months required.

LLR

F. Gastaldi, J. Nanni

O. Drapier, P. Paganini, B. Quilain

- High interest from both the physicsts and engineers to develop the Front-End Board
- Currently investigating support from our engineering team.

Several meetings

→ Latest on 01/24

- Main goal : have a first version of the new chip by early 2021.

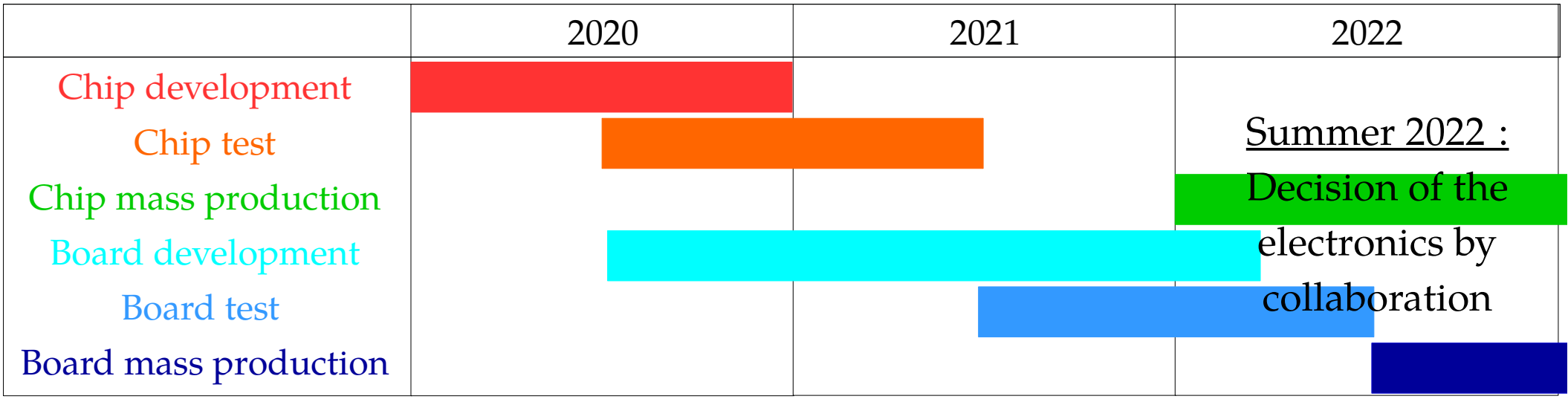
- The board will start to be constructed in parallel to the new chip, starting from late 2020.

  → Similar to CATIROC boards.

Requirements for Hyper-K

- If we wish to be on time, we need to start NOW (in the next 6 months)
  → Otherwise, I frankly think we can forget about it.

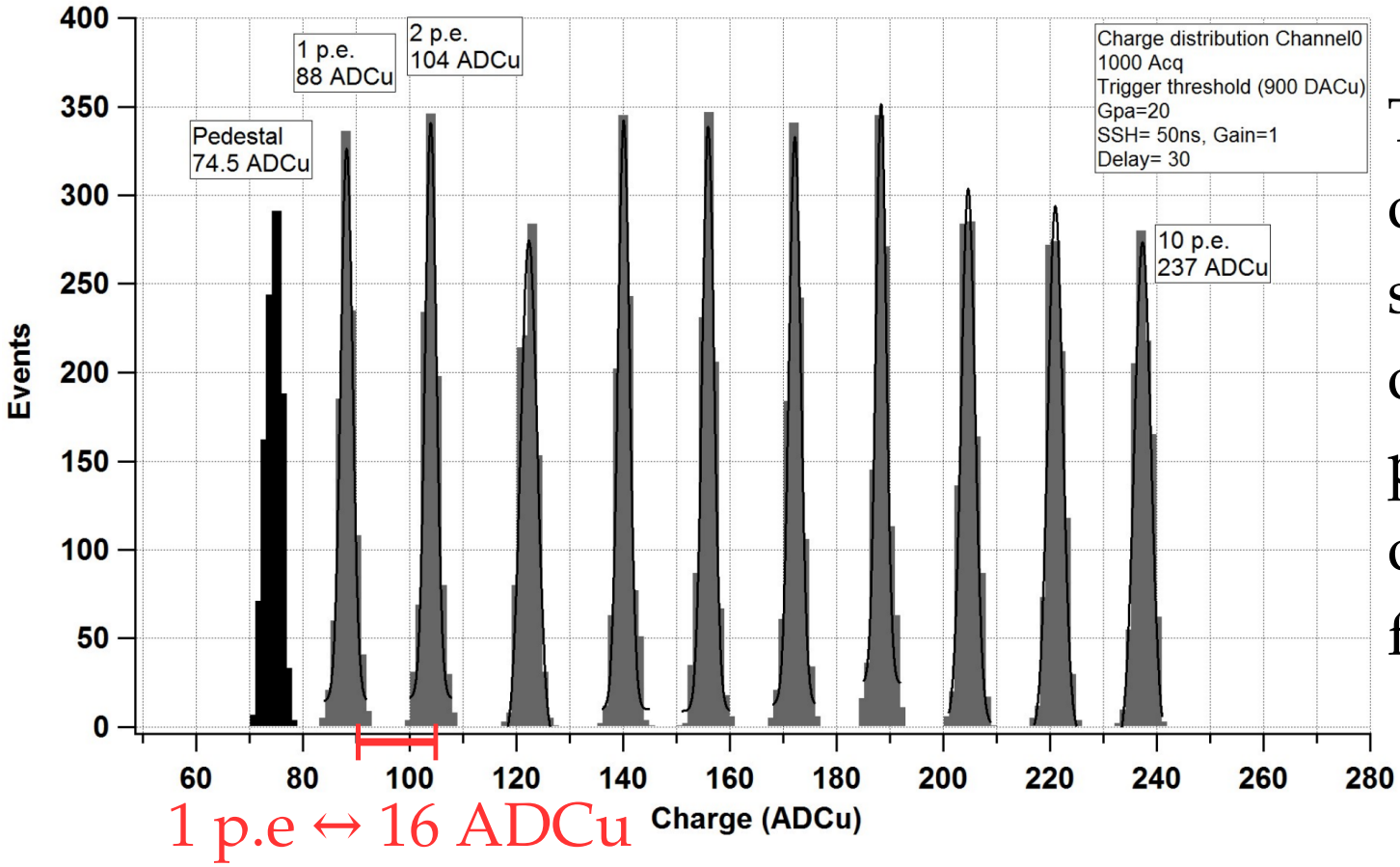
- <u>The first priority is the chip development</u>
  → Need to convince Omega to start developement in first half of 2020.
  → Will continue meetings, but would need an external support : IN2P3 after DUNE TDR, ANR, ERC etc.
  → Issue is that ANR/ERC takes some time… → Can be fine for long term support, but we need funds to start earlier.



Additional slides

Charge resolution

- HK TR states 0.05 p.e resolution for a signal up to 25 p.e.

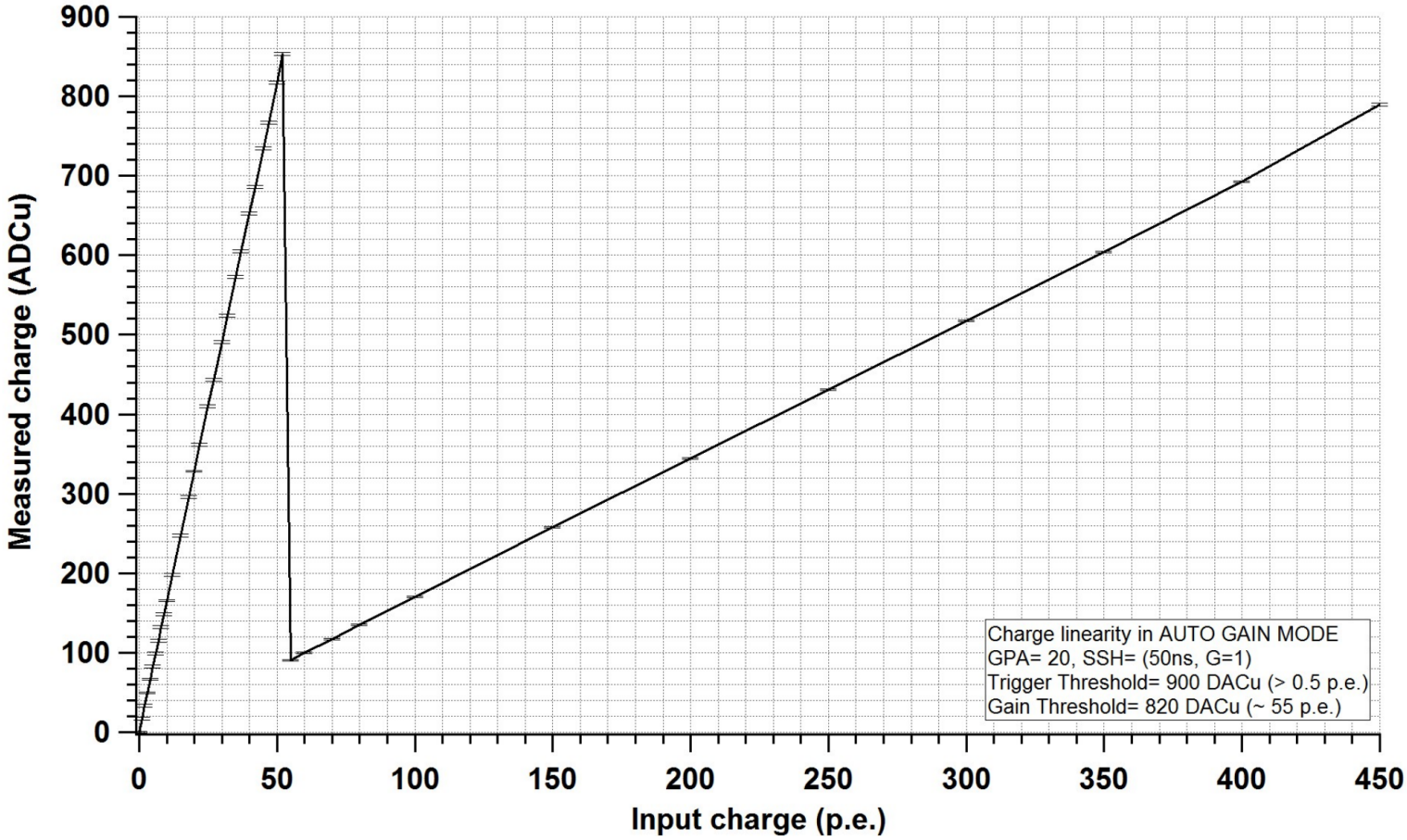


The CATIROC is operated with a slow shaper time of 50ns, and with a preamplifier gain of 20 for HG and 1 for LG.

- RMS of each pic is quite constant = 1.2 ADCu.
  → For this HG value, RMS = 0.07 p.e.
  → Could increase the gain to reach 0.05 p.e (but would need higher dynamic range → 12 bits ADC?).

Charge linearity and range

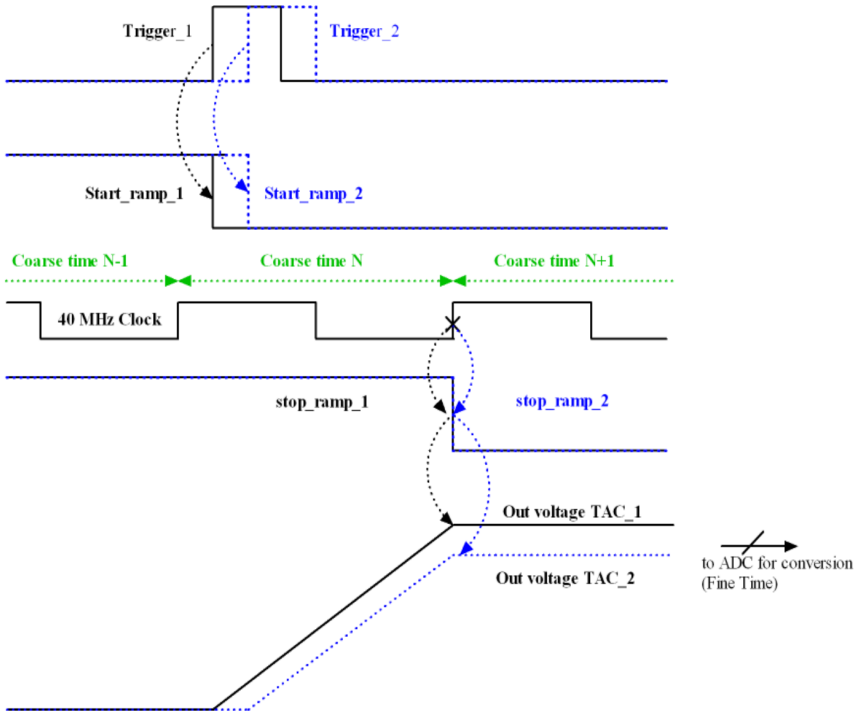
- CATIROC operated in same conditions as previous slide.

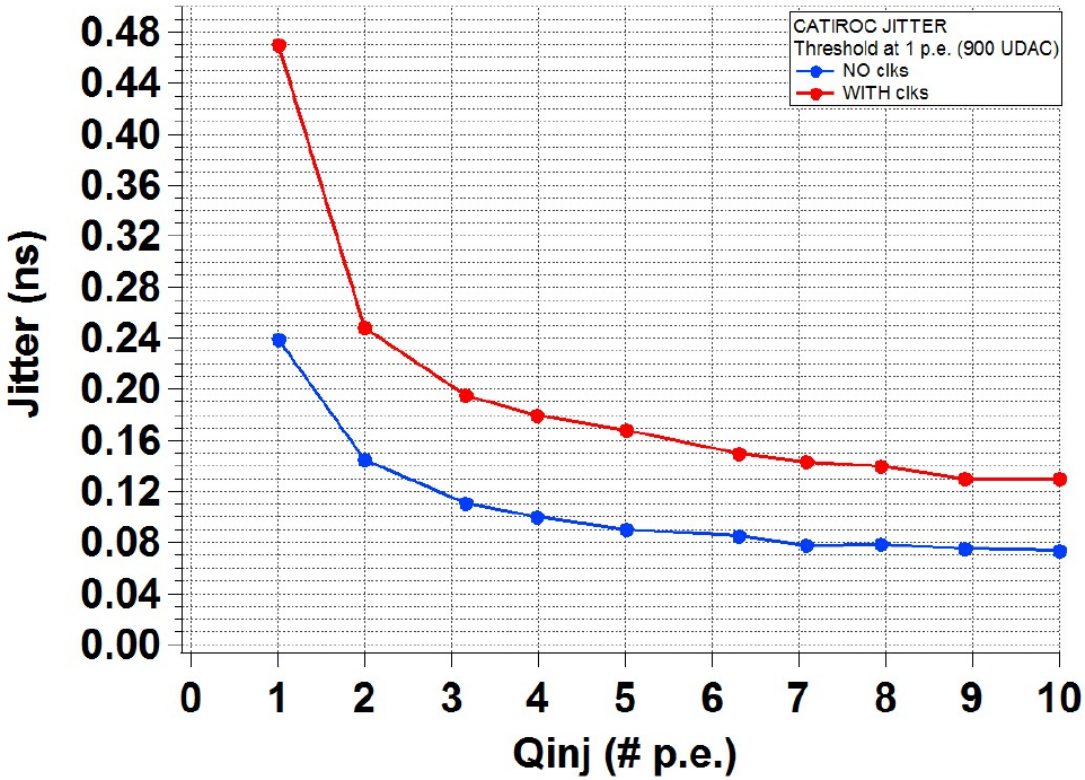


- Linearity < 0.7 % up to 450 p.e → Good linearity over the dynamic range
  → 10 bit ADC : we expect the dynamic range to be limited for high p.e.
  → Has been ok for 3'' PMTs of JUNO, but should change for 20'' of HK.
  → 12 bits ADC ?

Timing resolution

- Timing response is provided by :
  - A coarse time : a digital slow clock of 40 MHz (25ns) → 26 bit registered.
  - A fine time : + a TDC → Reach 170 p.s resolution.





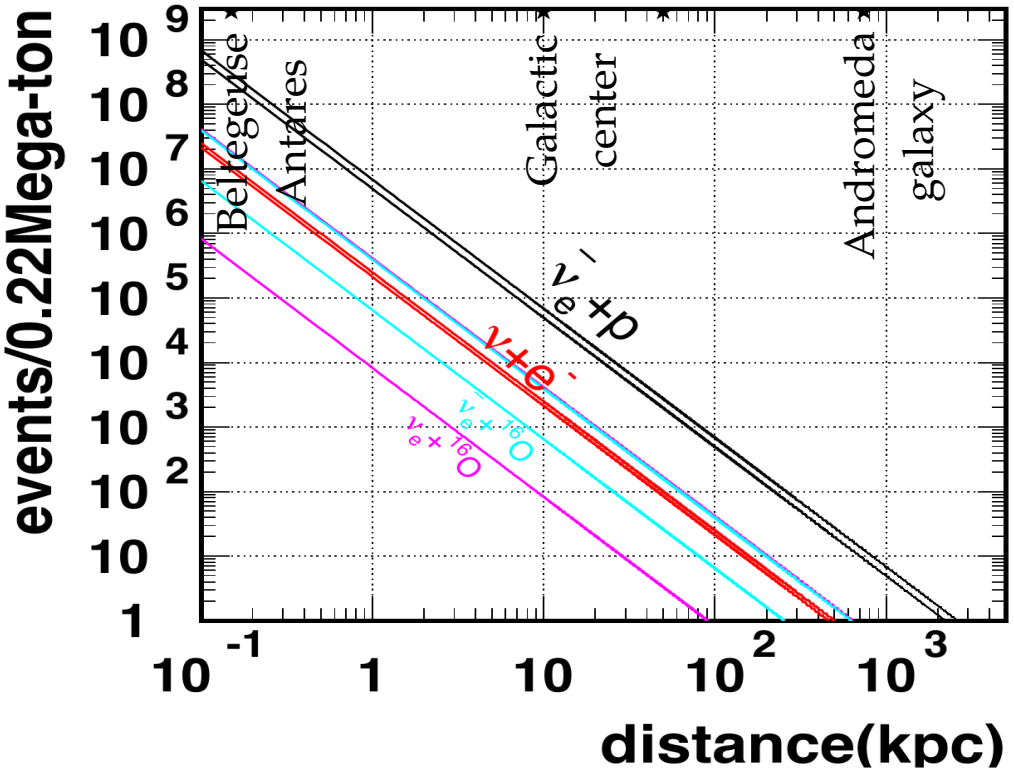
- Resolution limited by :
  - Fast shaper rise time (5ns, so for a S/N of 30 → 160ps).
  - A coupling to the digital clock.

Requirements for Hyper-K deadtime

- Dead time : what is mainly limiting dead time is the SN.
  → We assume a 500 light-year = 150 pcs (~ Beltegeuse).
  → Receive 75M events in the first second, and then, 105M events in 10s.

- 1 event of 10 MeV ↔ 20 p.e. at 40 % PC ↔ 20 hits at LE/events
  → So, have ~ 1500Mhits in 1s, so roughly, 40kHz / channel.

Item	Assumptions and estimates
Number of ID PMTs	40,000
Dark rate/PMT	10 kHz
Noise rate	3.2 GB/s
Noise rate (per board)	2.0 MB/s
Event rate	75M events (0 to 1 s) 105M events (1 to 10 s)
Data rate (10 s)	327 GB
Data rate (10 s per board)	0.17 GB

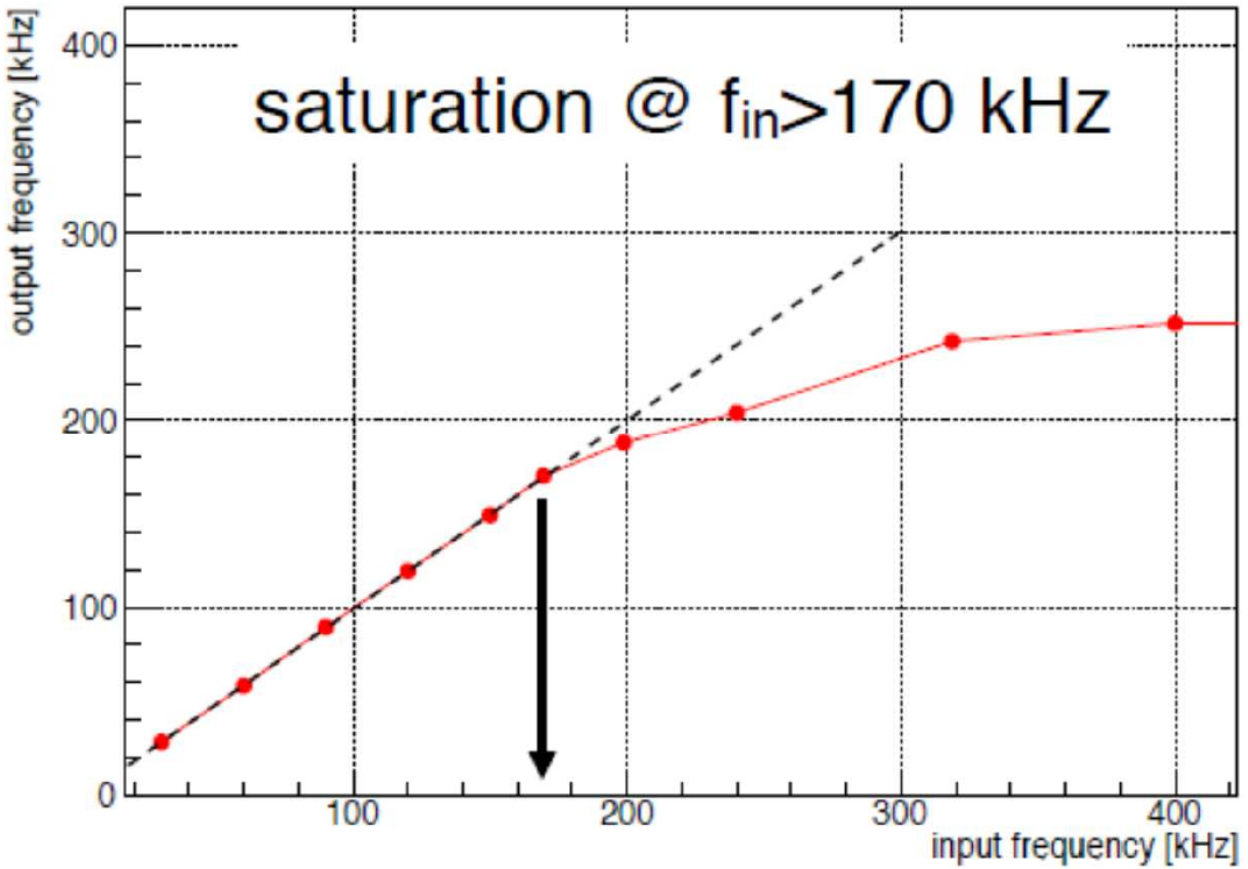


- HK TR assumes 1 MHz (to be conservative?) → < 1μs dead time.

CATIROC dead time

- Charge conversion is done in the chip by a 10 bit Wilkinson ADC operated at 160 MHz → Every 6.25ns.

- Conversion Time = ADC Period x 2^{Nbits} = 6.4 µs (150 kHz).



- So deadtime of 6.4 µs does not match the < 1 µs criterion for 150 pcs SN.
  → How can we improve this ?

Beyond the CATIROC chip

- C. De La Taille (Omega leader) :
  With current ADC technologies, the conversion speed could be improved by ~100 times : from 6 μs to 60ns.

- Then, we could put a 12 bits ADC digitizer
  → Increase the conversion time by a factor 4 compared to 10 bits.
  → Dead time ~ 240 ns → Still < 1 μs.
  → Would allow charge linear up to ~ 1600 p.e → > 1250 p.e.

- We could slightly increases the preamplifier HG value to improve charge resolution from 0.07 p.e to 0.05 p.e.

- Could modify the number of channels to 24 → Or have 2 chips / box.
  → Approximatively 1,000 to 2,000 chips.
  → Largely < production capabilities of Ω (produce > 100,000 for CMS).
  → Note that board production is another story….