

The SK2HK « Rise » european grant

O.Drapier, réunion de groupe

January 21st, 2020

The SK2HK project

Work

WP1

Management
& Coordination
AGH, CNRS, JU, NCBJ,
UAM, UW, WUT

WP2 Data

CNRS, UAM, UW

WP3 Analysis

CNRS, NCBJ, UW, UAM

WP4 Detectors

AGH, CNRS, JU, UAM, WUT

WP5 Training & Communication

AGH, CNRS, JU, NCBJ,
UAM, UW, WUT

Physics

Neutrino Mass Hierarchy
Leptonic Charge-Parity violation
Oscillation mixing parameters
CNRS, NCBJ, UAM, UW

Nearby Supernova CNRS, UAM

DSNB CNRS, UAM, UW

Grand Unification NCBJ, UAM

Experiments

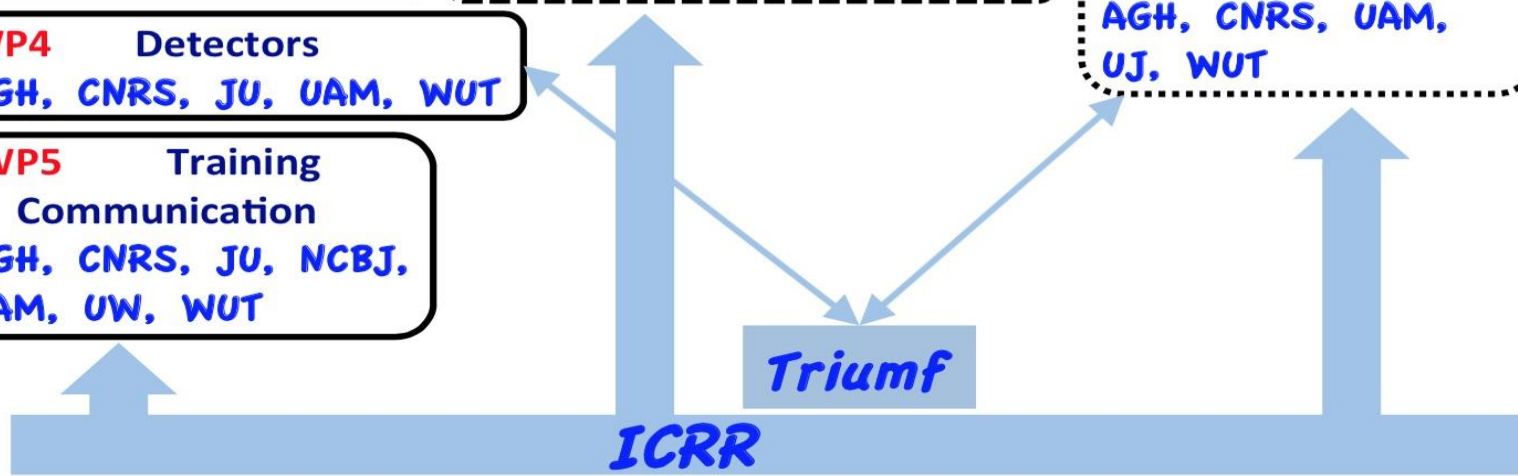
Super-
Kamiokande
CNRS, UAM, UW

SuperK-Gd
CNRS, UAM, UW

Hyper-Kamiokande
T2HK
AGH, CNRS, UAM,
UJ, WUT

Triumf

ICRR



Our commitments :

Participation to « work packages »

« Deliverables »

« Secondments »

- Deliverables are
 - Documents (theses, reports)
 - Organization of meetings, workshops
 - Organization of either a general HK collaboration meeting, or the « II European Workshop on Water Cherenkov Precision Detectors for Neutrinos and Nucleon Decay »
- Secondments are travels to ICRR, related to the transition SK → HK
 - SK, SK-Gd SHIFTS, TOKAI SHIFTS EXCLUDED (T2K shifts @ SK ~ OK)
 - Any work related to HK or T2HK (HK coll. meeting excluded if alone)
 - HK Coll meeting + on site work to prepare HK : eligible

LLR Responsibilities in SK2HK Work Packages

- WP1: Management and coordination
 - Task 1.2: Organization of 5 meetings
 - All institutes involved
- WP2: Data
 - Task 2.2: lead data taking with SK/Gd
 - EP, UAM and UW heavily involved
- WP3: Analysis
 - Lead by EP, see Sonia's talk
 - Task 3.1: lead DSNB searches
 - UAM and UW involved
 - Task 3.3: supervise 2 PhD works on Low E
 - Related to task 5.1 (WP5)
- WP4: Detectors
 - Task 4.4: Lead development of a « cone generator »
 - Efficiency for π^0 reconstruction
- WP5: Communication and training
 - Task 5.3: organize the “II European Workshop on Water Cherenkov Precision Detectors for Neutrino and Nucleon Decay Physics” in France or Spain

What do we get ? How does it work ?

- ~ 145 (170) k€ Total over 4 years
- Each time a SINGLE PERSON cumulates ONE MONTH in Japan :
 - 2100 € for travel and accomodation expenses
 - 1800 € for other expenses :
 - networking/training/WP work/outreach/...
 - (+700 €) for administrative support (CNRS / LAB)
- We must try to spend part of the expenses from the SK2HK budget WITHOUT overshooting this budget
- If we do not effectively perform the travels, no problem BUT the corresponding money returns to EU !!
- Travel must be eligible
- Must have « SK2HK » in the title
- Please KEEP ALL papers, receipts, proofs, etc ..

Status of the Super- FGD electronics

O.Drapier, réunion de groupe

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summary

- General status
- LV power distribution
- Some facts concerning mechanics
- Overall setup for crates and cable connection
- Other topics

General status (meeting every other Friday)

- FEB desing under way : technical meetings every Thursday between LLR (Hardware) and UniGe: (Firmware)
 - Need level translators for FPGA / citiroc communication
 - FPGA : 1.8V / not usable for CITI : 3.3 ↔ 1.8V translators under study
 - Adjustable delays in the FPGA : 35ps steps (S. Cap)
 - Reprogramming the FPGA remotely (S. Cap)
 - Citiroc news: Two months delay for mass prod
 - Many chips available for prototypes, so no incidence on schedule
- Backplanes and Optical Concentrators → U.S. groups
 - Starting soon to discuss detailed interfaces
 - List needed lines in Digital Backplane
- DAQ ? Sync / Clk board ? To be discussed (UniGe ?)

LV power

- One FEB LV needs:
 - 1.1 V 4.5 A
 - 3.8 V 2.7 A
 - 5.3 V 0.5 A
 - - 3.8 V 1.1 A
- U.S. groups in charge of finding a solution (critical):
 - External PS ? → CABLES !!!
 - In-magnet LV Modules ? → HIGH CURRENT / VERY BIG AIR COILS !!!
 - On-board DC/DCs ? → NOISE / QUITE BIG AIR COILS !!!
- Any mix of these ? Need to test in-field behavior, need to precisely evaluate possibility for external cables
- Decision made of a mezzanine board:
 - Designed @ U.Pittsburgh
 - Prototype FEB could host the LV mezzanine
 - Integrated on board for final production, if proven to work

Analog cables



Bending the cables:

Radius = 0.125" ~ a pen

FEB & Cable design

- CAD design inherited from this SAMTEC proto (more details in sFGD talks)
- 2 types of connectors at MPPC PCB sides & PPanel (quite compact).. **low profile**

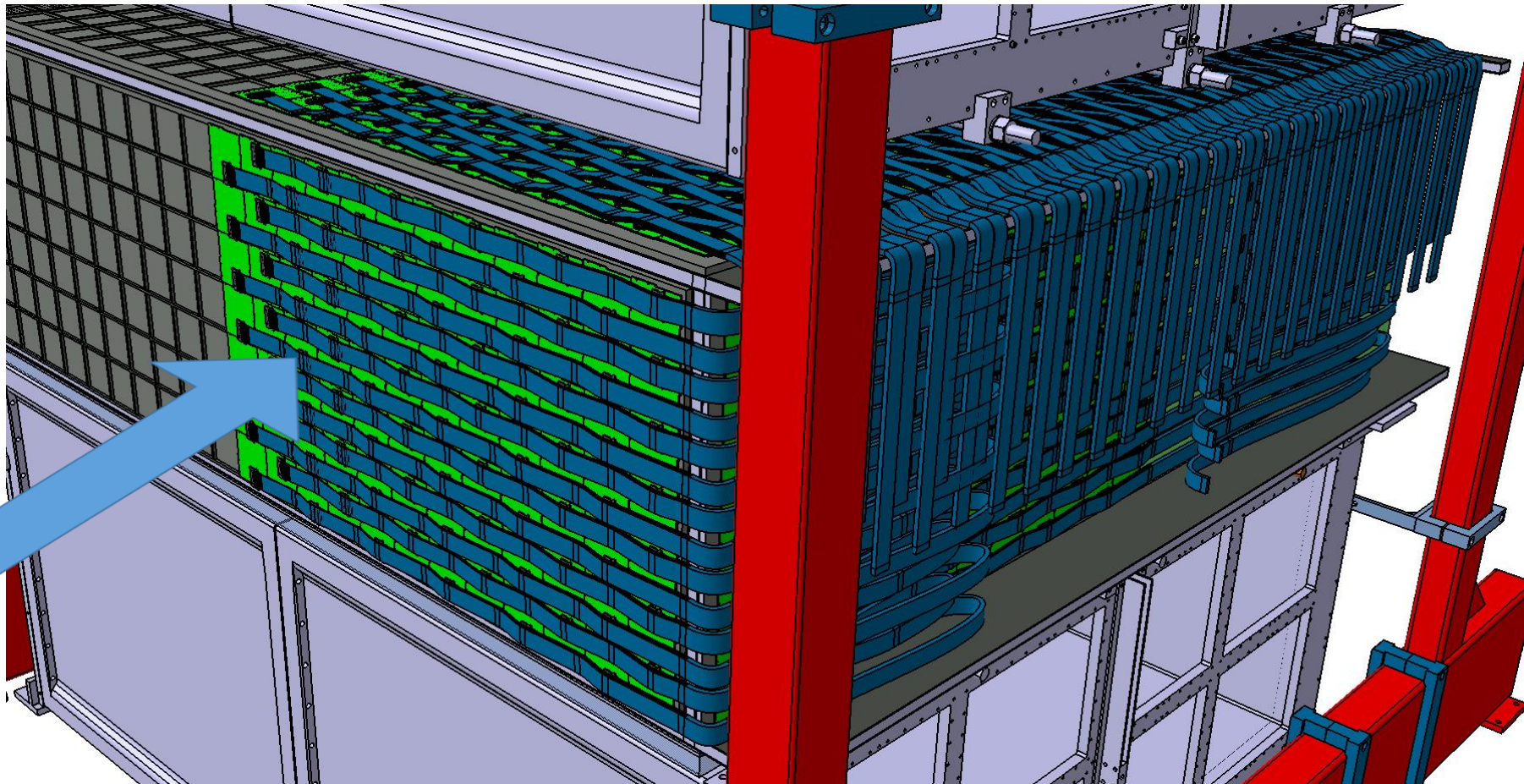


Cable bundles



FEB Design & Crate size assessment

Reminder of cable bundle envelopes



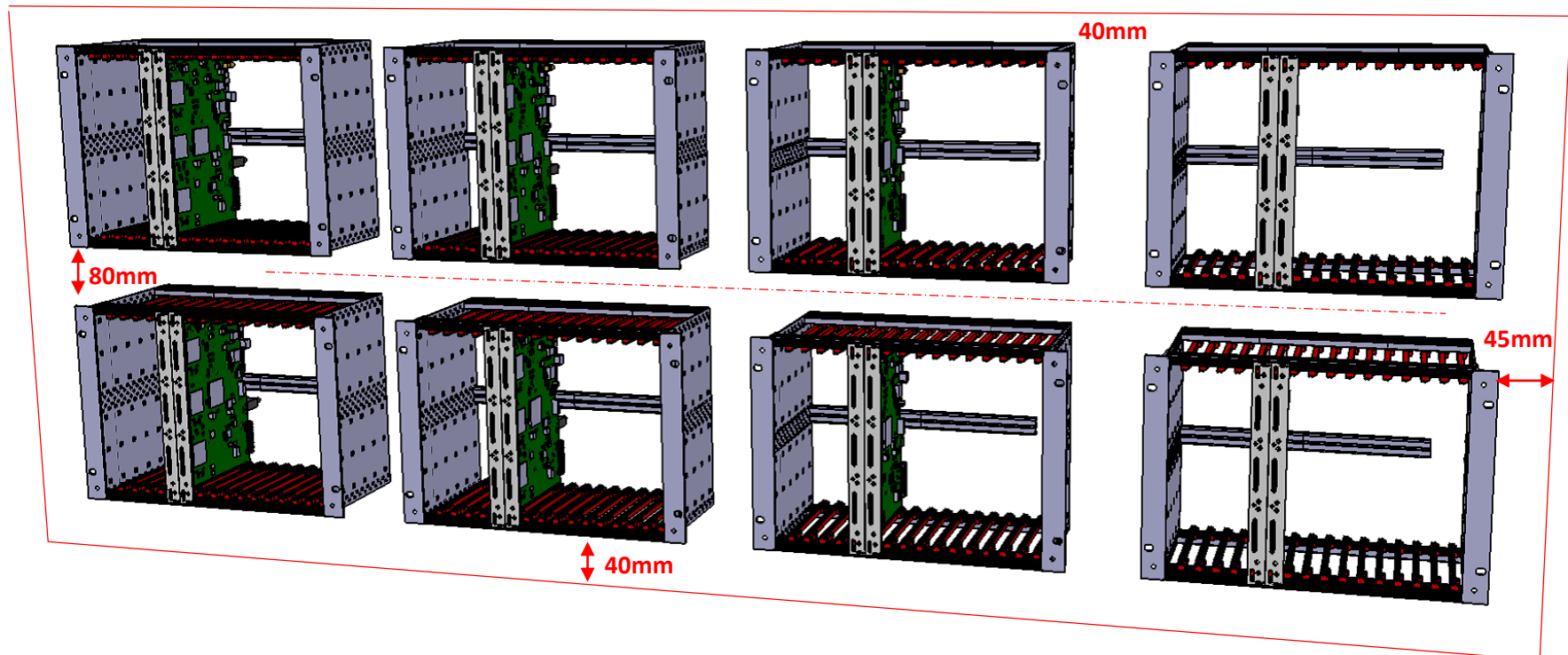
Crates



FEB Design & Crate size assessment

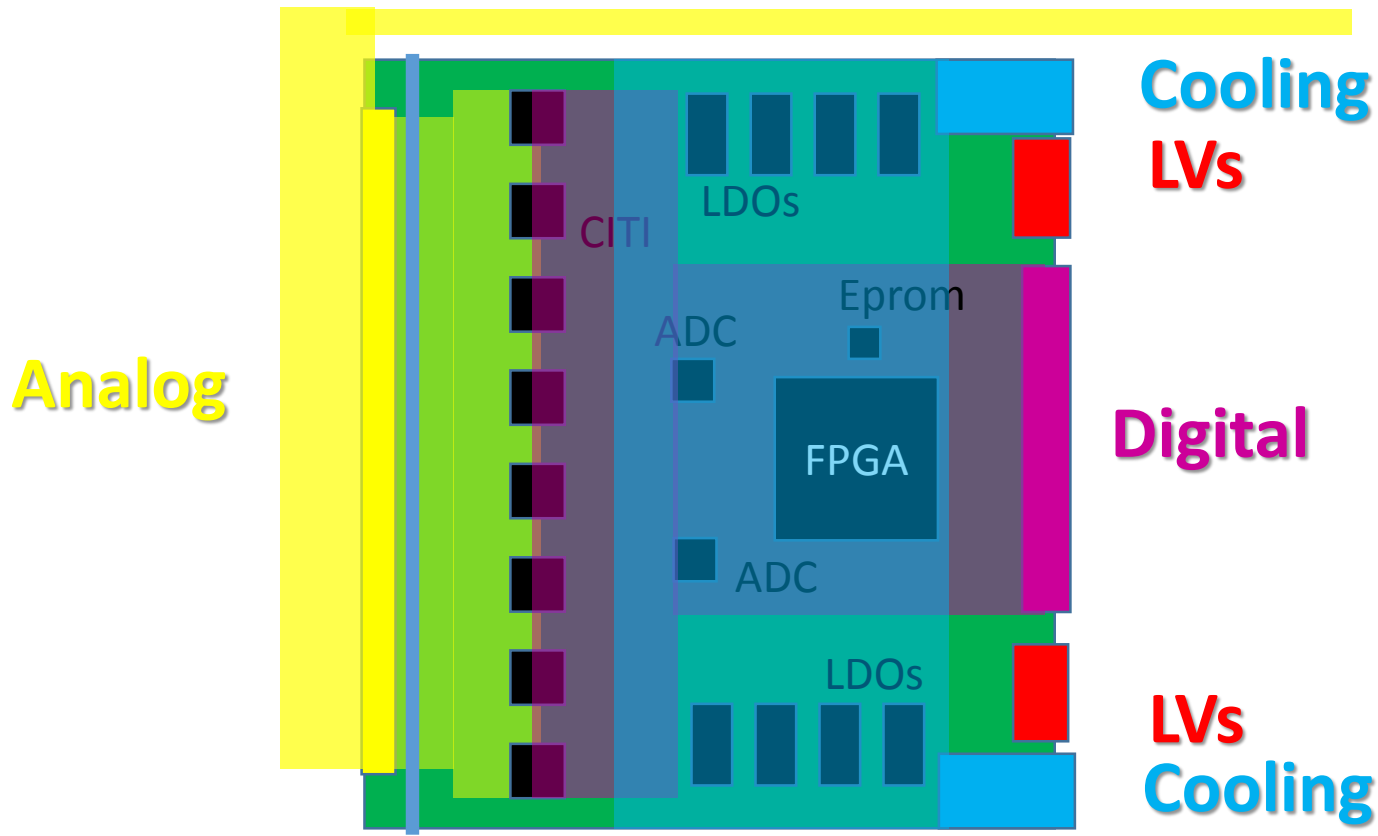
Based on past experience (CTA camera and Baby MIND)

- Extrapolation to the sFGD side assembly (2 rows, each crate is centred / envelope)
- Envelope that is used / sFGD: **1900mm x 692mm x 300mm** (80mm is taken for cables)

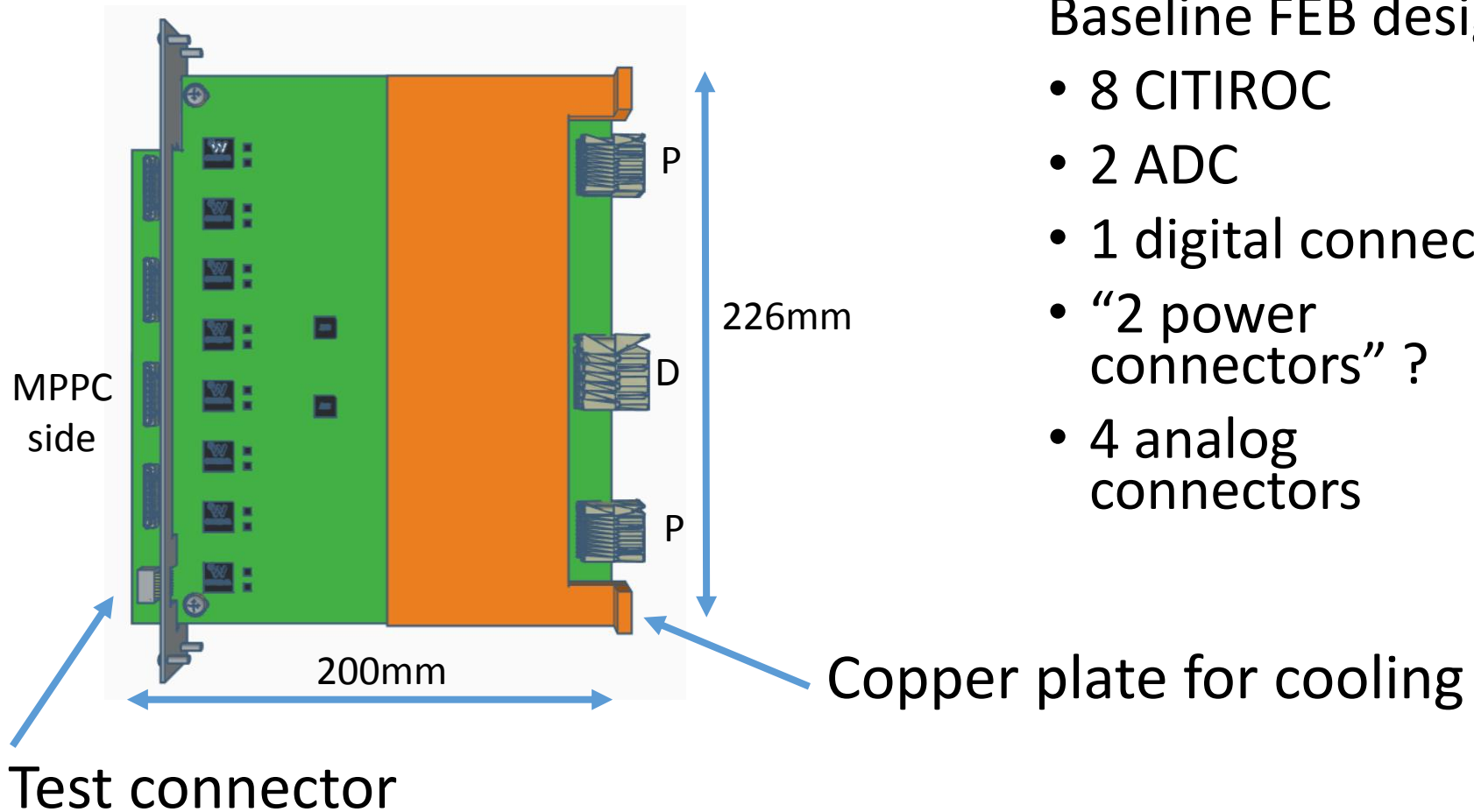


Improved version

- LVs and digital connectors to backplane, at the rear
- Analog connectors on board extension going through front panel
- Cooling at the rear, no need to remove circuit, larger board
- Cooling bar closer to the heat sources
- No reduction of board area



FEB mechanical design (next slides by J. Nanni)

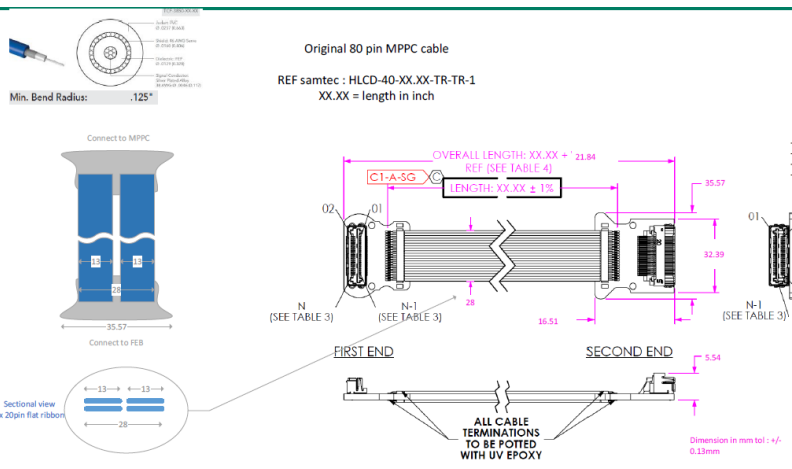


Baseline FEB design:

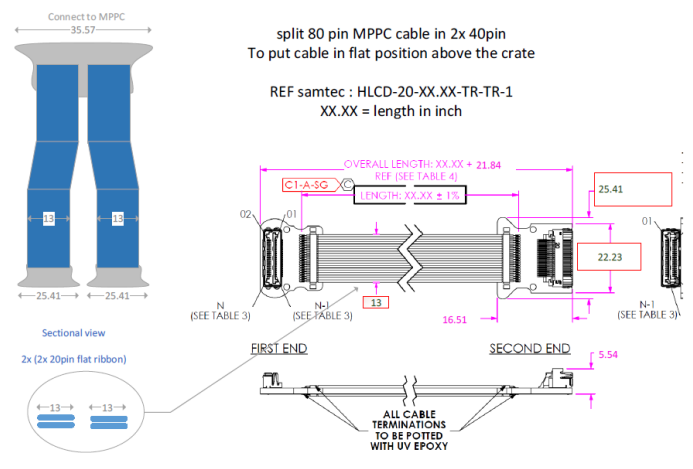
- 8 CITIROC
- 2 ADC
- 1 digital connector
- “2 power connectors” ?
- 4 analog connectors

Proposal to split analog cables

Standard/commercial solution



Idea of custom solution



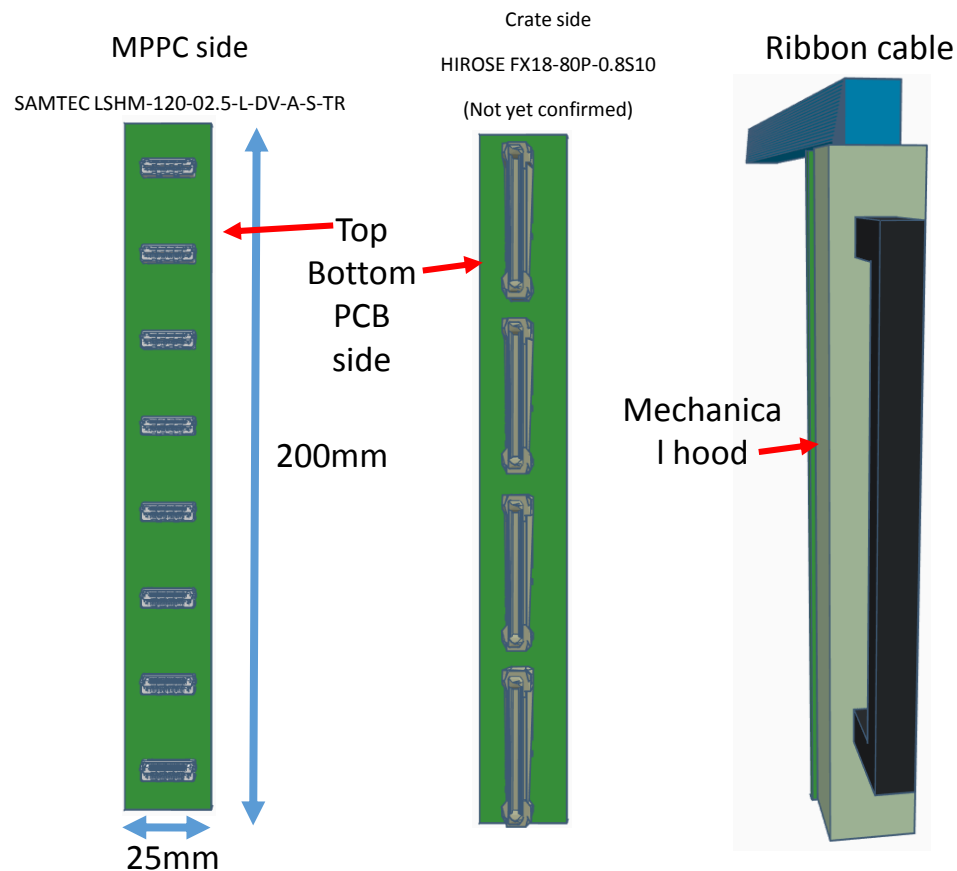
Specifications : Design of a PCB front plane

Advantages:

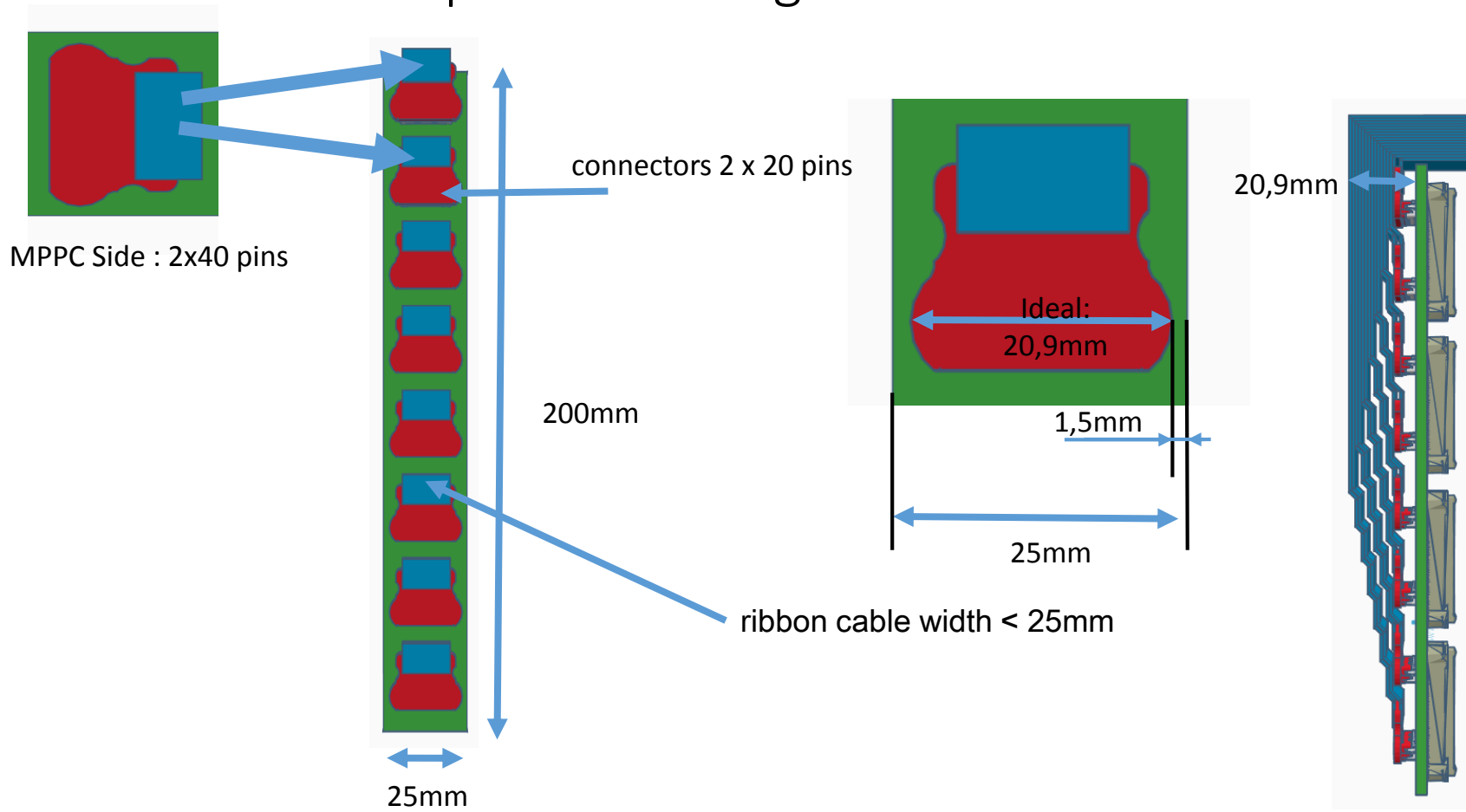
- Easy to plug/unplug on the dedicated FEB
- No risk of damage to the analog cable

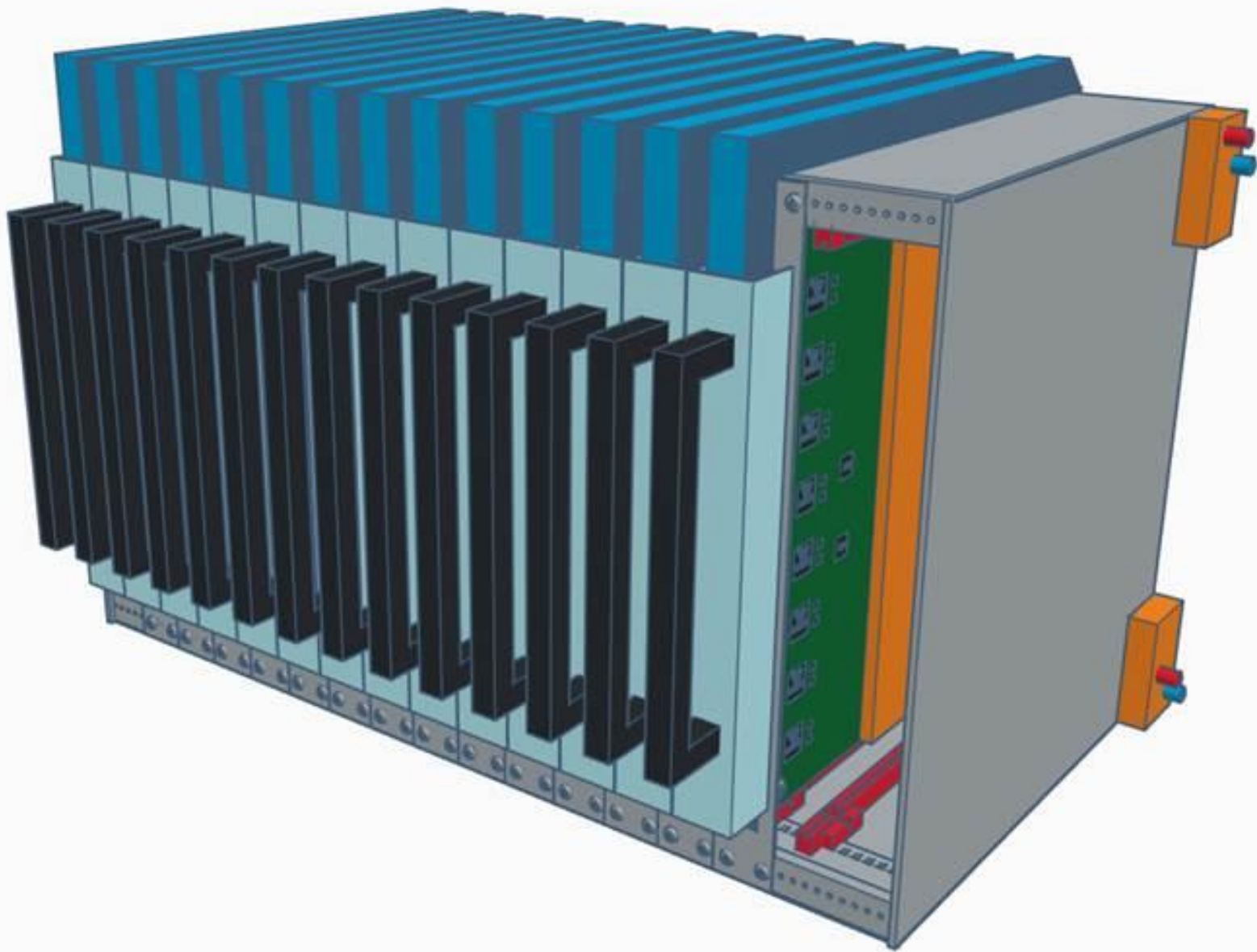
Constraints:

- Needs high precision
- Strength ? Need for screws/clips ?



Specifications given to Samtec





Other topics

- Critical: think seriously about analog cable routing
- Critical: make decision concerning cables from outside for high currents (room for PS near the magnet ? B field there ?)
- Critical: calculate precise heat dissipation and cooling power together with pipe routing
- Critical: start studying the mechanical structure
- Critical: prepare a plan for installation !
- Sign a final collaboration agreement UniGe ↔ LLR
- Sign NDA UniGe ↔ U.S. groups
- Prepare a plan for test benche(s)
- Share DAQ + Clk/Sync responsibilities