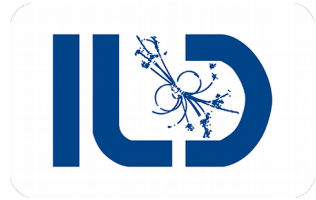


Test Beam 2020/03: Preparation Meeting



IJCLab-CNRS/IN2P3
SiW-ECAL CALICE



This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168



Outline

- Status of the SLBoard v2 and DAQ
- Status of the FEV10/11 integration into the SLBoard system.
- Wafer gluing and chip encapsulating
- Status of the FEV13 integration on the new system.
- Status of the Mechanical structure.
- Status of the cabling + patch panels.
- Status of the Commissioning procedure.

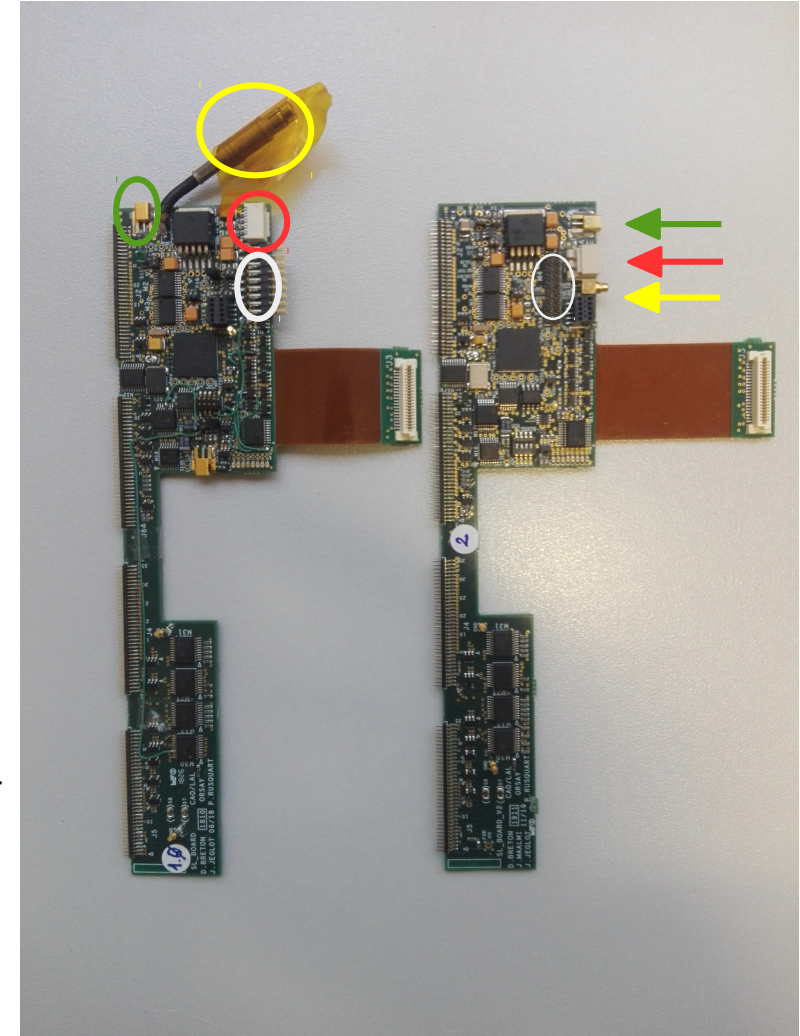
- Transport
- Attendance
- Discussions

Twiki page (under construction)

<https://twiki.cern.ch/twiki/bin/view/CALICE/SiWDESY202003>

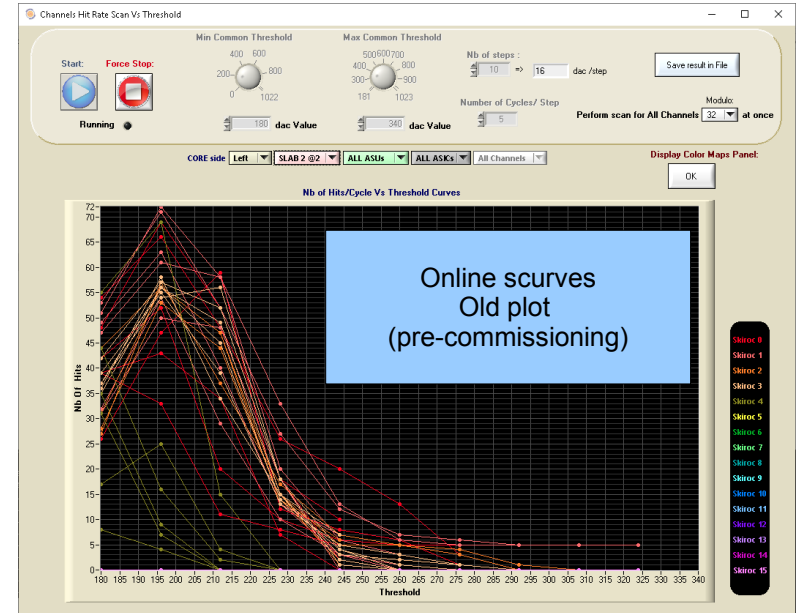
SLBoard v2

- Non exhaustive list of modifications
 - Useless circuitry has been removed
 - Repositioning of components → better access for cable plugging
 - Improved selection of input plugs.
 - Kapton length increased (from 40 to 60 mm)
 - A switch for slot number encoding.
 - DAC for Skiroc ADC calibration. The FPGA produces pulses for autonomous functional calibration of both gain.
 - Flash EPROM for permanent information storage.
- Production status: 4 cabled SLboard + 18 waiting for the debugging results
- **Most new features have been tested (all with satisfactory results)**
 - DAC for Skiroc ADC calibration has been satisfactorily tested but it is under optimization.
 - Flash EPROM not yet tested.
 - HV is available on the SL_Board but not yet tested.



DAQ & FirmWare news

- Post beam test debugging done:
 - i.e. Save histogram files when performing online scurves
- Kapton-Core
 - All 15 slots are operative.
 - Next setp read 15 slabs at the same time.
- SLBoard FW loading possible through the Kapton.
- FW/SW adaptations for the new SL-Board features are finalized.

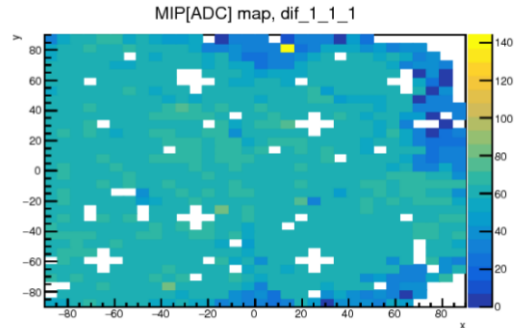


FEV10/11 Integration into the SL-Board system

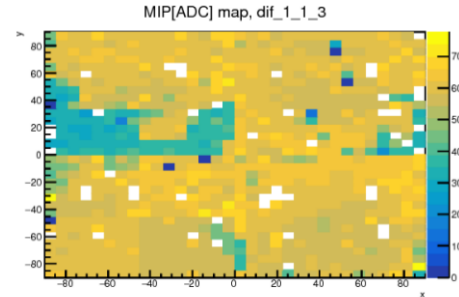
- 9/10 of the 13-22 slabs are at LAL.
- Kapton connectors have been removed as well as the SMBs for all of them
 - SLAB 14 & 16 have been tested with SLBoard (v1)
 - The rest are being progressively equipped with the female gradcon connectors and being tested.
 - Except the slab 15 (FEV 10)
- Remark: we found an incompatibility issue between male & female connectors of the Antelec producer.
 - No compatibility issue between Gradcon & Antelec.
 - We found out after several FEV11 were already equipped with Antelecs → a couple of days delay
 - Issue being discussed with Antelec.
- “New” FEV10 from LPNHE fully equipped with 320 um wafers but never equipped with the SMB
 - to be equipped with SL-Boards?

FEV10/11 status

SLAB	DESY 2017		CERN 2018		Comments
	status	calibrated cells	status	calibrated cells	
13	Red	0%	Red	0%	Glue spilled in the SMBv. Recoverable for 2020
14	Red	0%	Red	0%	Error in the SR retour → fixed for 2020
15	Red	0%	Red	0%	Stopped working during the 2017 commissioning. Recoverable for 2020 ?
16	Green	92%	Yellow	?	At CERN : low performance on the corners of the ASU and SMB interface
17	Green	93%	Green	95%	
18	Green	94%	Yellow	?	At CERN : a pattern of lower MIP values is seen in the center of the ASU
19	Green	93%	Green	93%	
20	Green	94%	Green	96%	
21	Yellow	54%	Red	0%	Stopped working at DESY 2018
22	Green	84%	Green	87%	



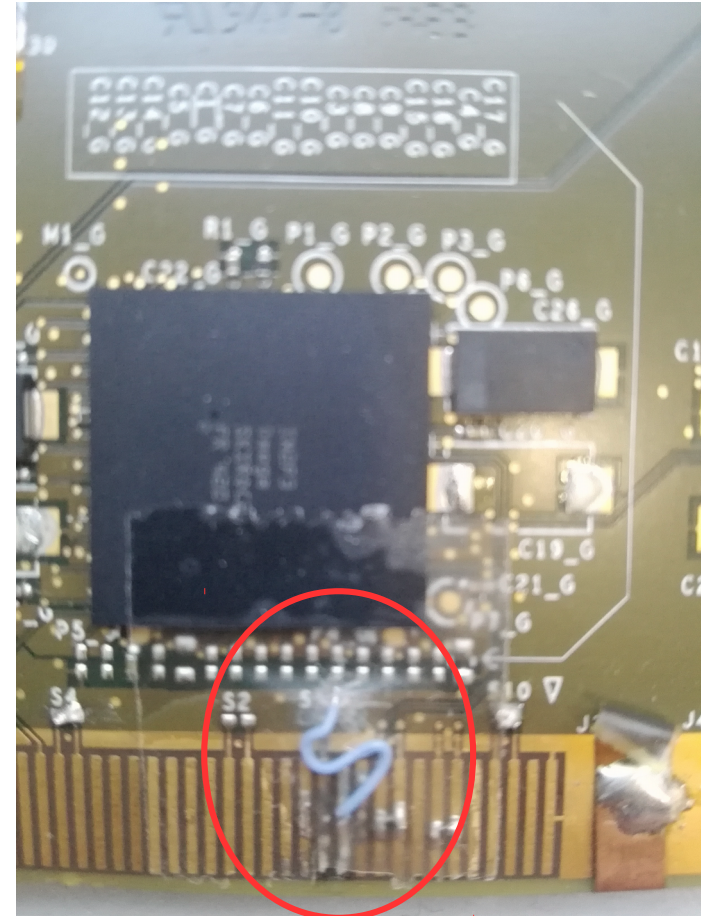
● Slab 16



● Slab 18

SLAB 14: recovered for data taking

- Slab not tested at DESY 2017 due to a problem of the Signal/Slow Control Return lines that blocked the readout.
- First slab used to test the “disassembly procedure” (November 2019)
- Satisfactory DAQ tests done by bypassing 4 chips.
- Status: slab fully recovered and commissioned → similar performance than the other FEV11 had during 2017



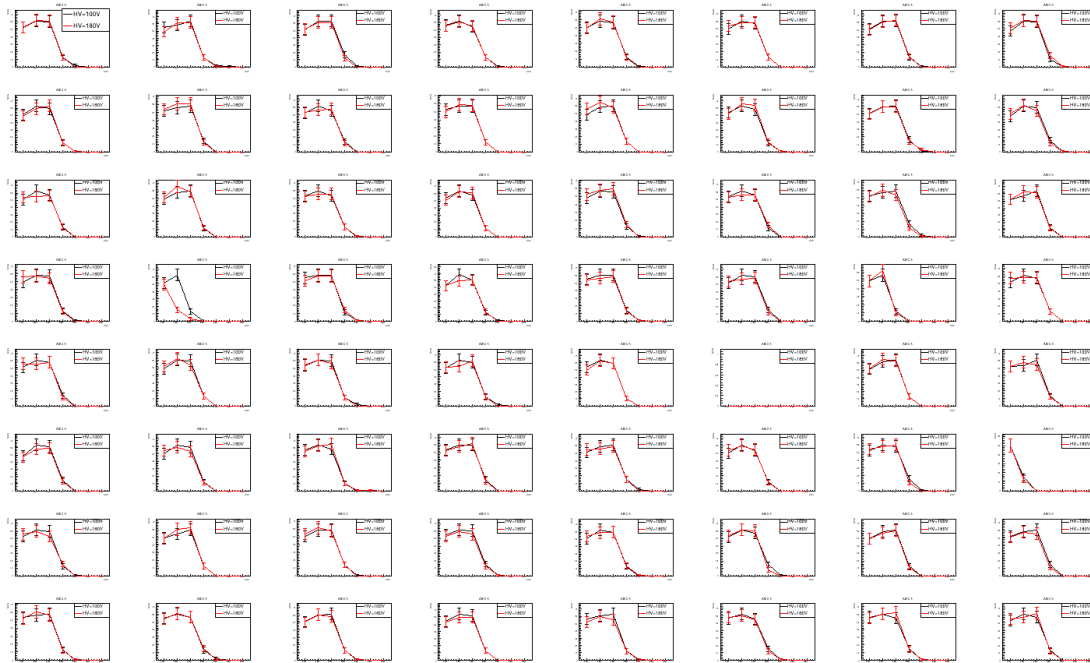
SLAB 14: HV 100 V vs HV 180 V

➤ This board has large leakage currents (since the first time that I have tested in 2017)

- HV100V → ~ 15-18 uA; HV180V → ~ 30 uA
- No differences in performance have been observed (s-curves and cosmic runs)
- Constant results for several runs over more than 2 weeks.

➤ s-curves on ASIC 5

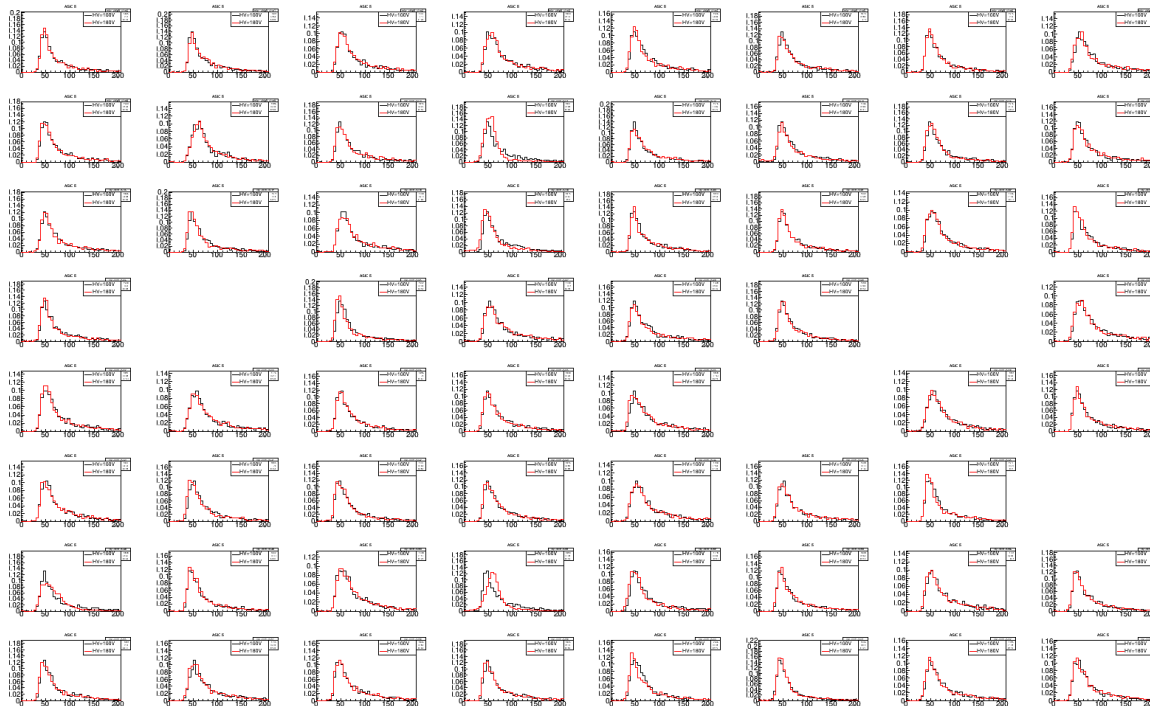
- Red = HV180 V
- Black = HV100 V



SLAB 14: HV 100 V vs HV 180 V

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➤ MIP distributions on ASIC 5

- Red = HV180 V
- Black = HV100 V

SLAB 14: HV 100 V vs HV 180 V

Conclusions:

- We recovered a “lost” slab
 - Similar attempts ongoing for slab 13 and 21
 - What about 15? It is a FEV10... not a priority.
- We don't see differences in performance operating the SLAB at 180V or 100V.
 - We foresee to use 2 different HV PS in the beam test
 - But in case that we don't do it, it will not cause major issues.

FEV 12 “*threshold issue*” *isolved*

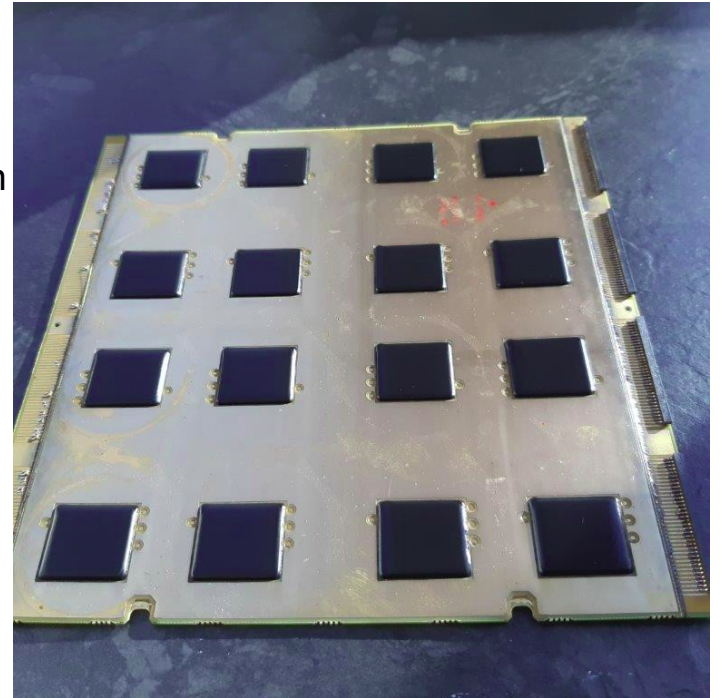
- We solved the problem with the “thresholds” observed in the Test beam.
- Test beam diagnosis: threshold value inversion
- Good diagnosis: baseline reference shift for the DAC due to a wrong cabling of the FEV
 - SK2: an extra resistance in the PCB was needed to fix the development mistake that made the threshold dynamic range to small.
 - Not needed in SK2a.
- All the resistances have been removed and the FEV12 have been re-tested satisfactorily

Plans for wafer gluing at LPNHE: FEV12

- 7 more 500 um wafers are available at LPNHE (from LLR)
- FEV12 -1
 - Is at LPNHE right now being prepared for the gluing of 3 more wafers.
- FEV12-2 is at LAL (for DAQ tests)
 - Will travel to LPNHE by the beginning of February (?) for the gluing of 3 more wafers.
- LAL/LPNHE are working on special mask to facilitate the gluing of the wafers into the FEV12 without removing the connectors.
 - This was already last year done for the COB

CHIP encapsulation FEV11_COB

- COBs are now at Hybrid (for encapsulation)
 - COB-a (1 real wafer plus a fake wafer) to be used as test for encapsulation
 - COB-c to be fully equipped with 3 more wafers.
 - COB-d to be fully equipped with 4 wafers.
- To be recovered the 27 January.
- Note: Hybrid will try to recover the ASIC #8 of COB-a which is misworking.
 - By fixing broken wires



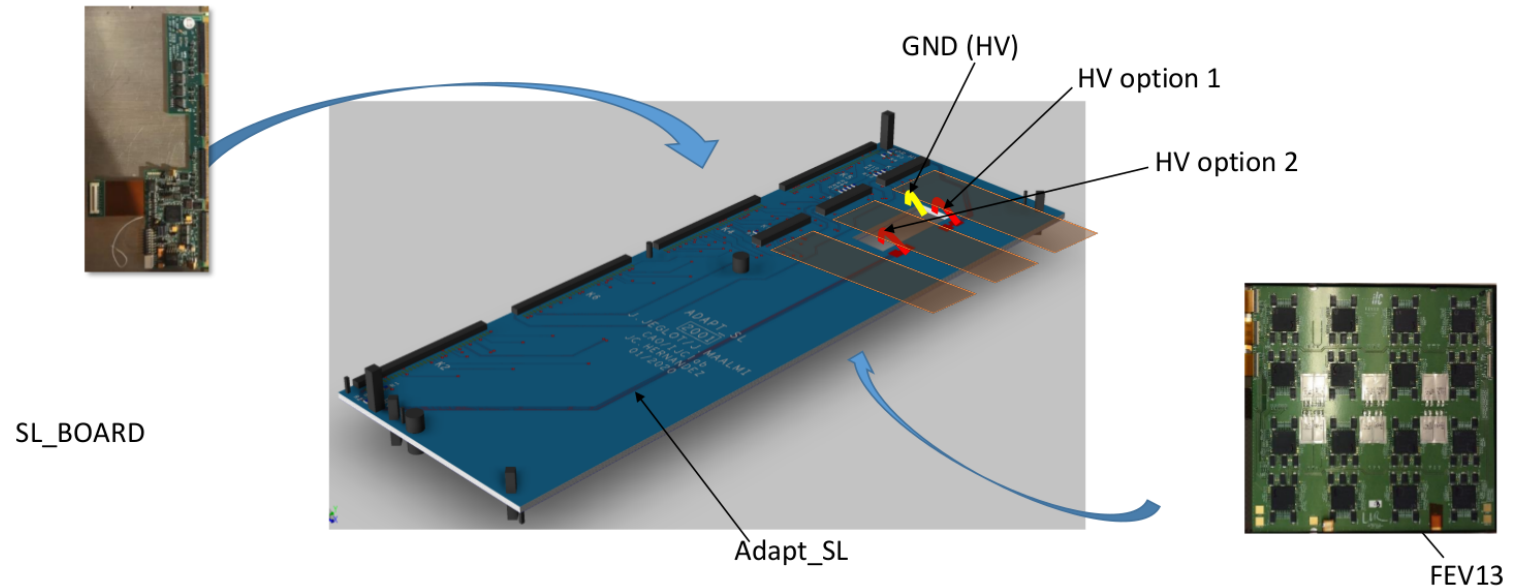
Plans for wafer gluing at LPNHE: FEV11_COB

- Plan to fully equip with wafers the COB-c and COB-d
 - Mid february (?)

FEV 13 integration with th SLBoard system

- Design finished.
- FW modifications done.
- Production to be started soon.
 - XX to be produced
 - XX to be equipped

SL-ADAPT for FEV13



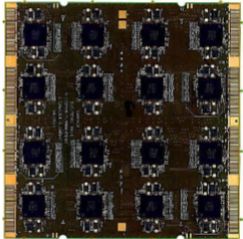
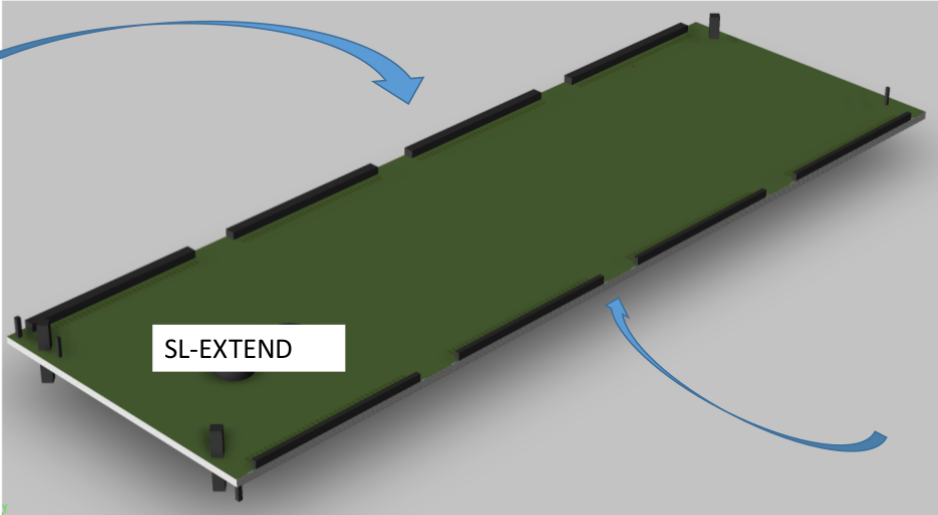
- ADAPT SL:
 - 4 GRADCONN mâle
 - 3 connectors AYF414035A + USL00-40 I-x (40 pins 11 gnd)

Design jeglot/Maalmi
CAO jc. Hernandez

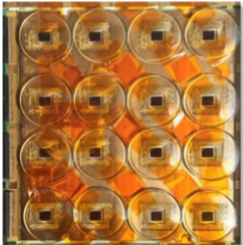
FEV 13 integration with th SLBoard system



SL_BOARD



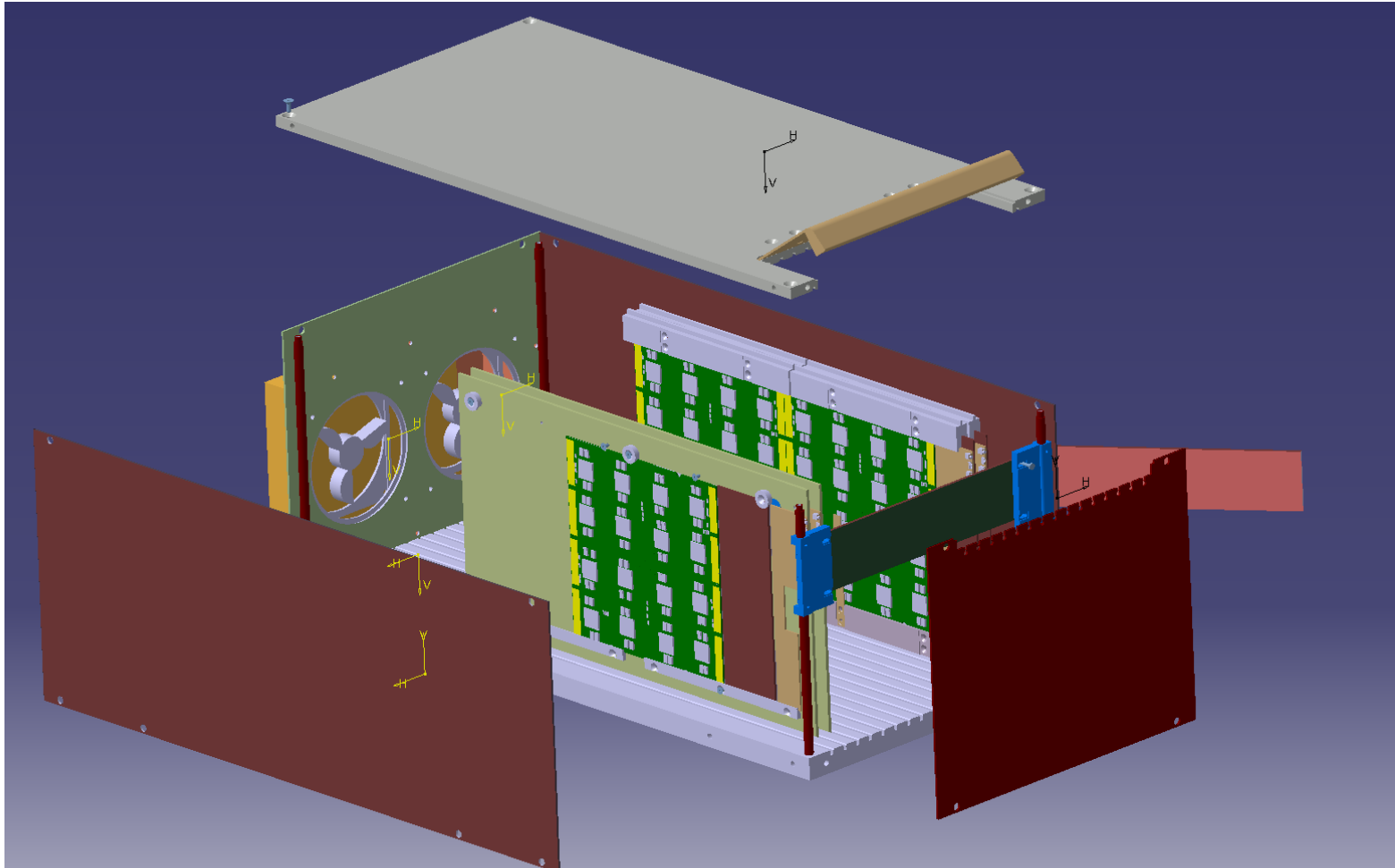
FEV11 or FEV12



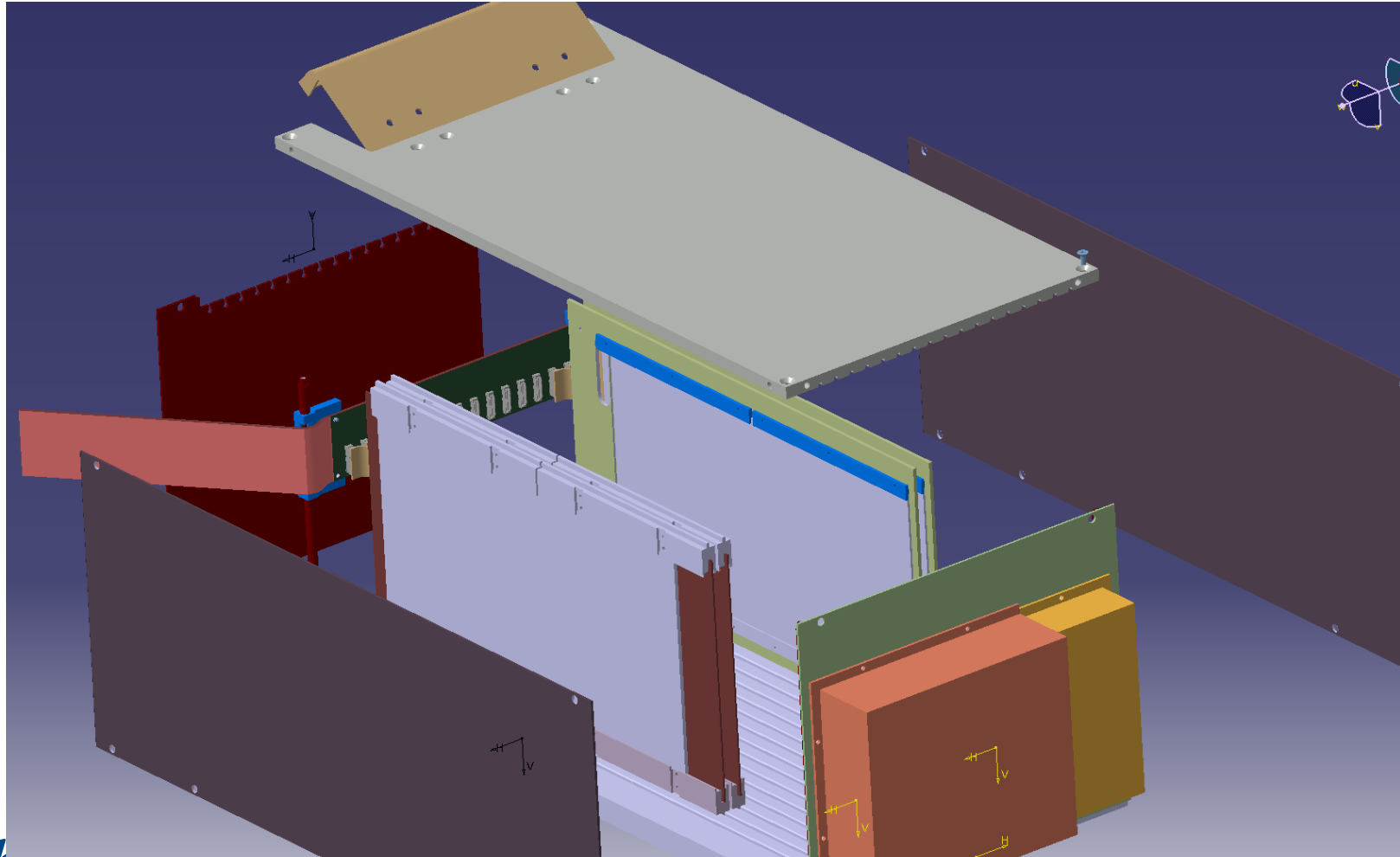
COB (Chip On Board)FEV

Design jeglot
CAO jc. Hernandez

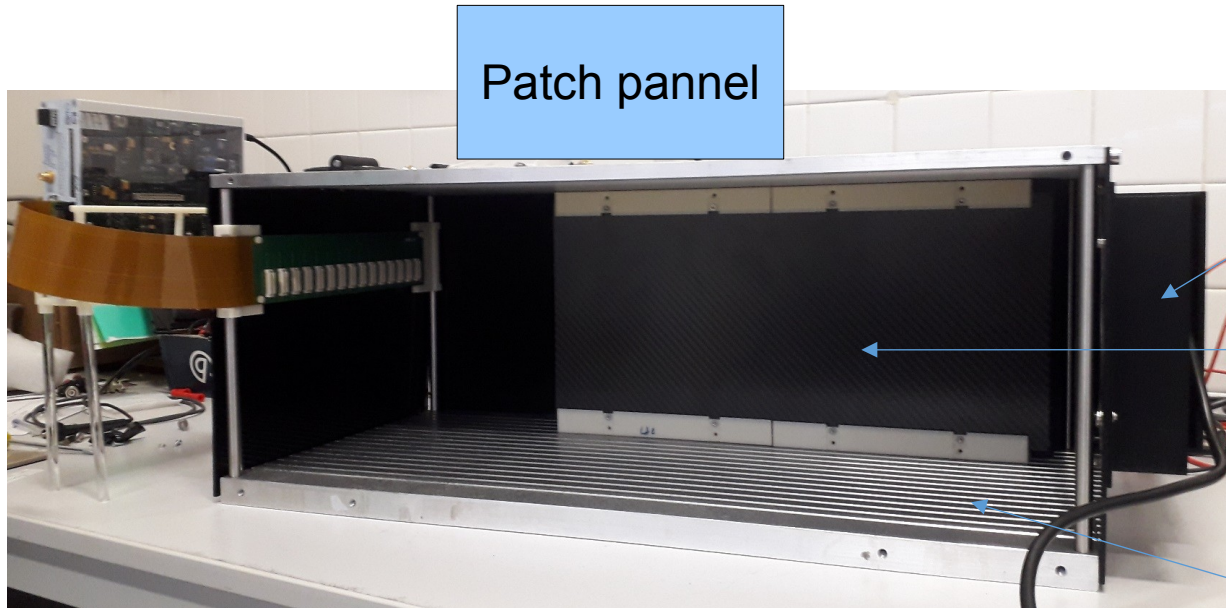
Status of the mechanical support



Status of the mechanical support



Status of the mechanical support



Patch panel

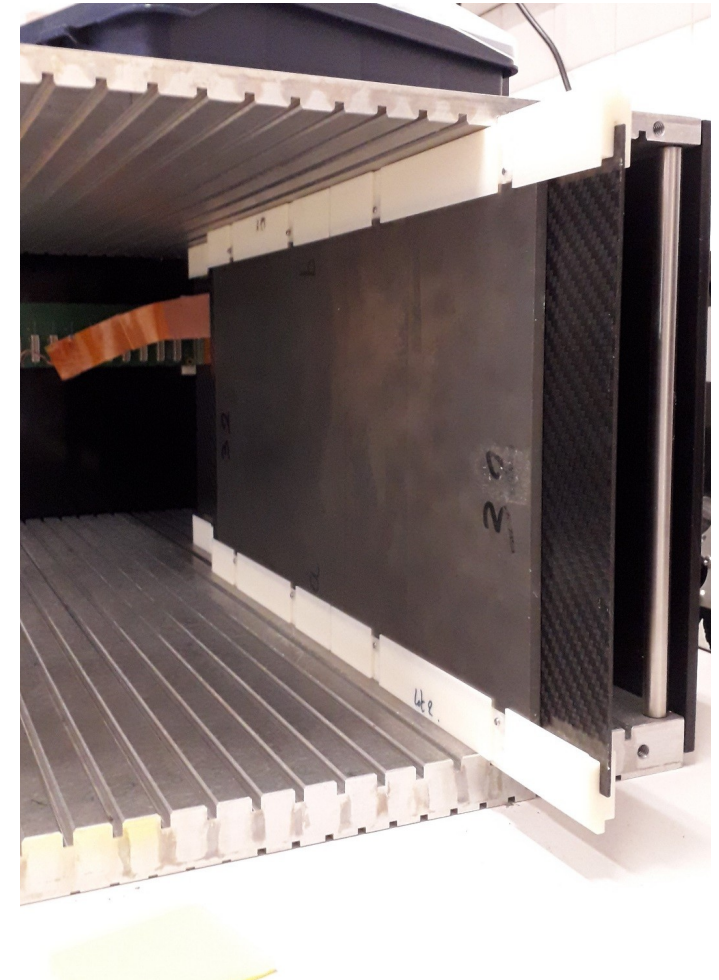
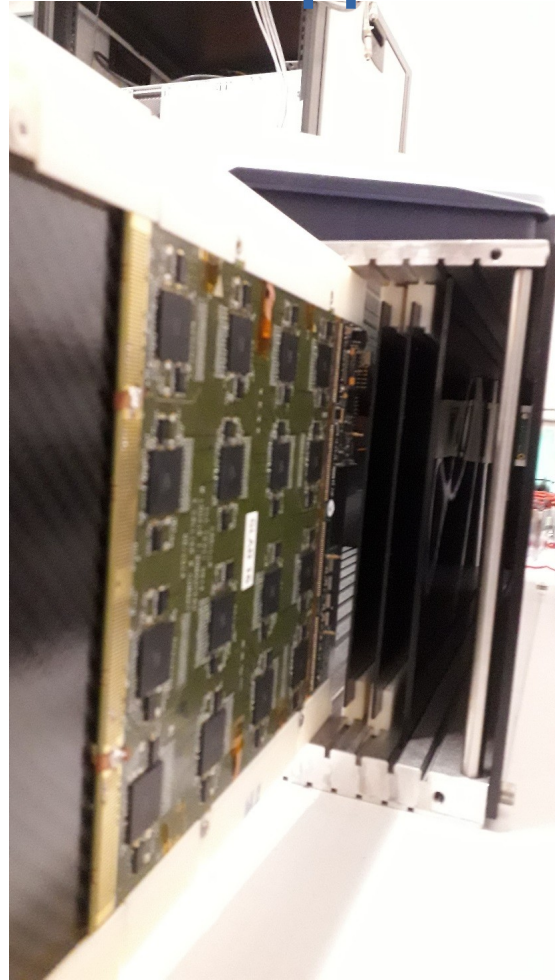
fans

Carbon plate which support ASU and W plate

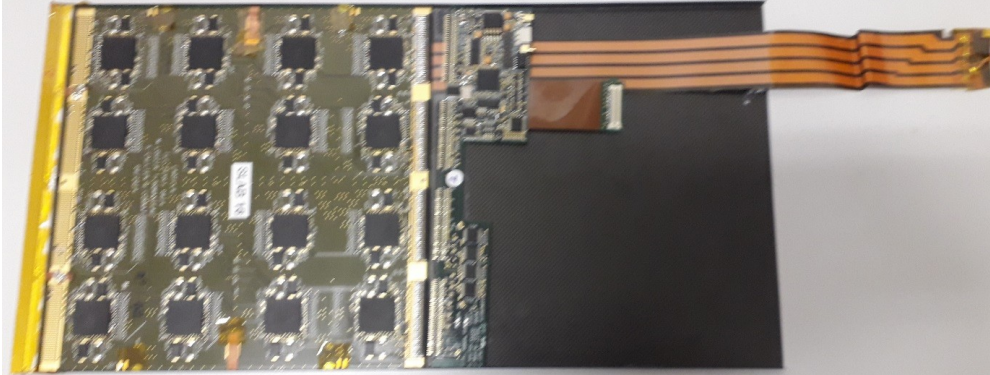
17 rails to align ASU+ SL board in front of the 15 slots of the « core kapton »

Status of the mechanical support

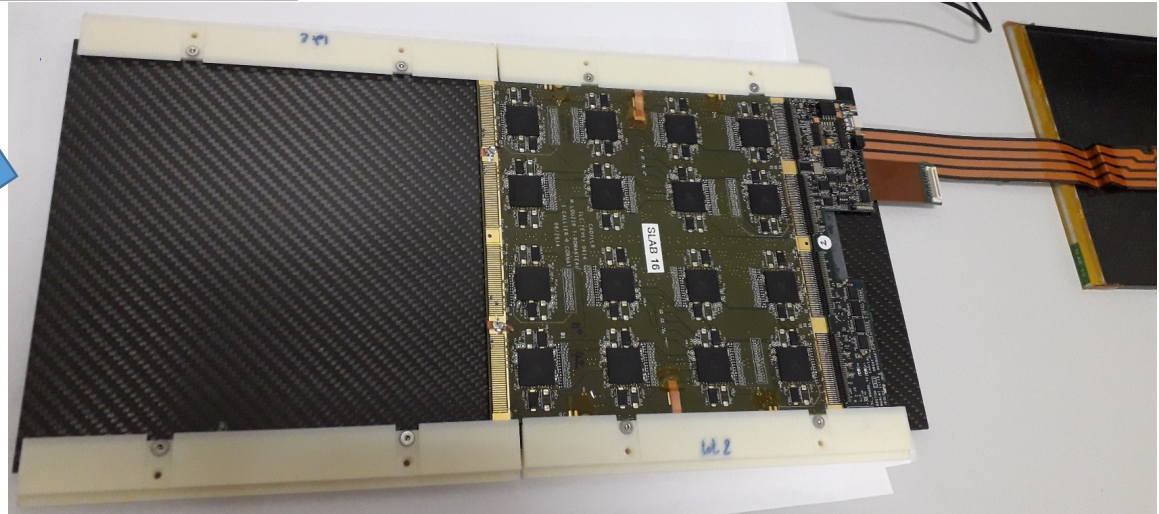
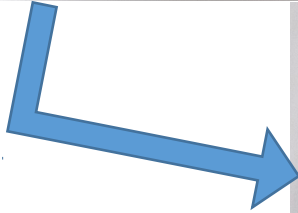
Carbon plate:
support one
side the
tungsten plate /
the other side
the SL board + 1
or 2 ASU



Status of the mechanical support



ASU + HV kapton take off
the » U carbon shape of the
LLR » and fixed on the
carbon plate, slide on the
rail



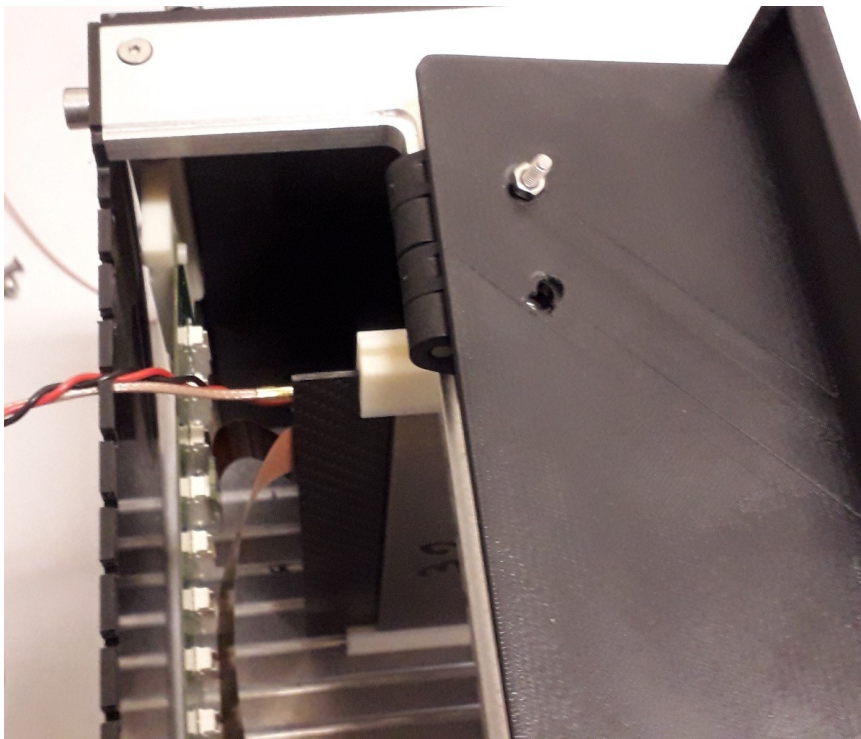
Status of the mechanical support



View of 4 support plates adapted to the thickness of the COB and FEV electronic card and the different thickness of the W plates.

Right side : old plastic support which can align ASU with other thickness like « Japanese slab: ASU + their carbon protection »

Status of the mechanical support

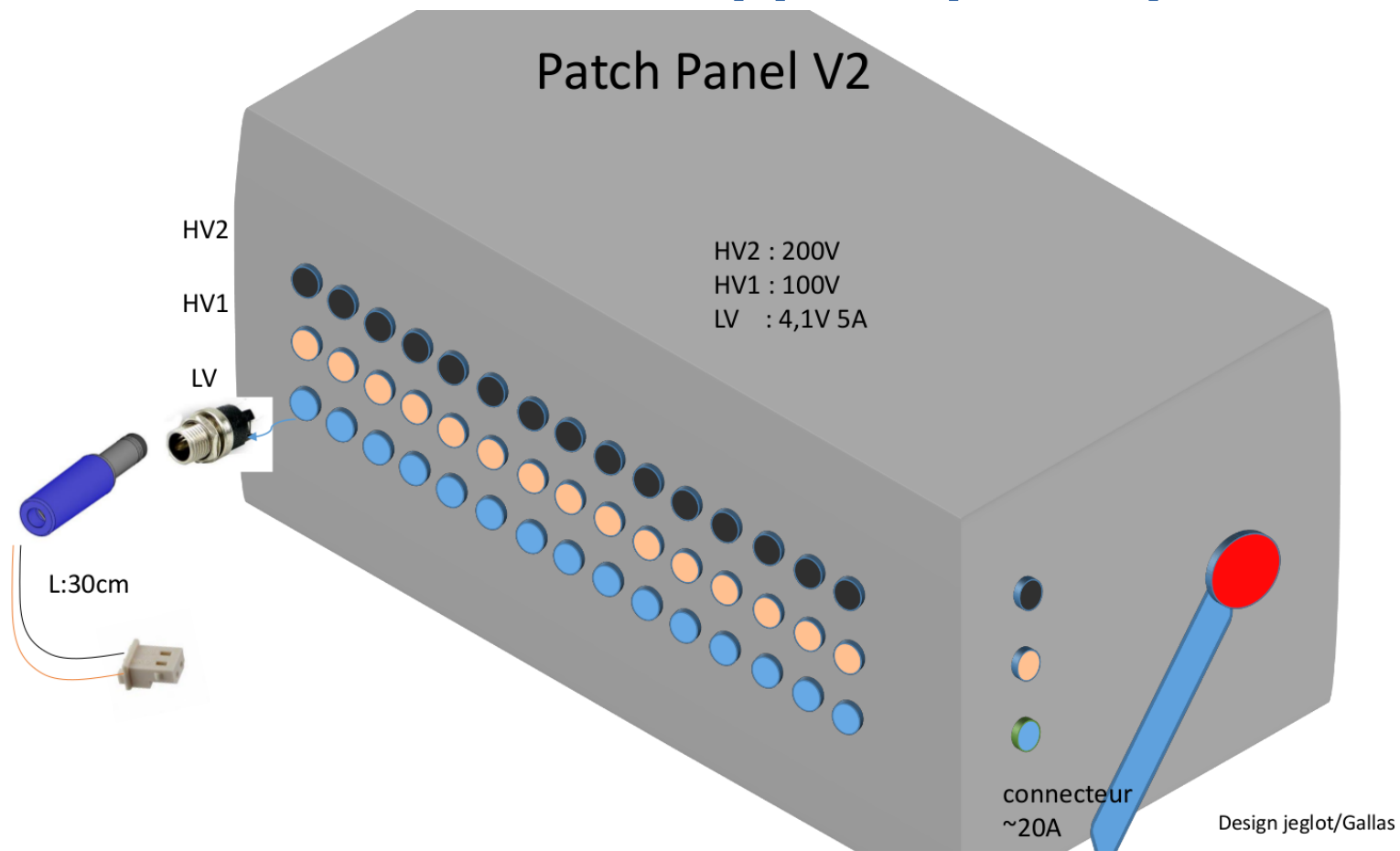


Connections in/out
the box per slab:

- flexible kapton + plug
- -1 LV red/black cable
- - 2 HV cables



Status of the mechanical support: patch pannel



Commissioning procedure

- Slow warm up of the automatization of the procedure with the new DAQ
- Manually done for SLAB14 and the COBs → very similar results compared with 2017, but less masking of channels if we use SK2a.
 - For a “trained” user, the manual process does not take much more than the automatized one (for one or two slabs)
- Do we want to use the TDC?
 - What are the physics motivations to use it at DESY?
 - What are the proper settings?
 - Proposal for DESY: use forced High Gain and TDC.
 - All this needs some readaptations of the DAQ software. Not in the top of the list of priorities.

Transportation & Attendance

➤ LAL van

- ~20 March (Roman + ?)

➤ Attendance

- Doodle to be created
- LAL: 3 physicists, 4 engineers, 2 master students
- LLR: (?)
- Omega: (?)
- Kyushu (?)
- Tokyo U (?)
- CERN: (?)
- SKKU: 1 PhD student (or postdoc)
- CIEMAT: 1 PhD student