

R & T TIMED

- Integrate WR in μ TCA crate
 - Only the WR switch function
 - Sync-E switch in MCH slot frequency transfer.
 - Test on the shelf solution
 - Development of custom board

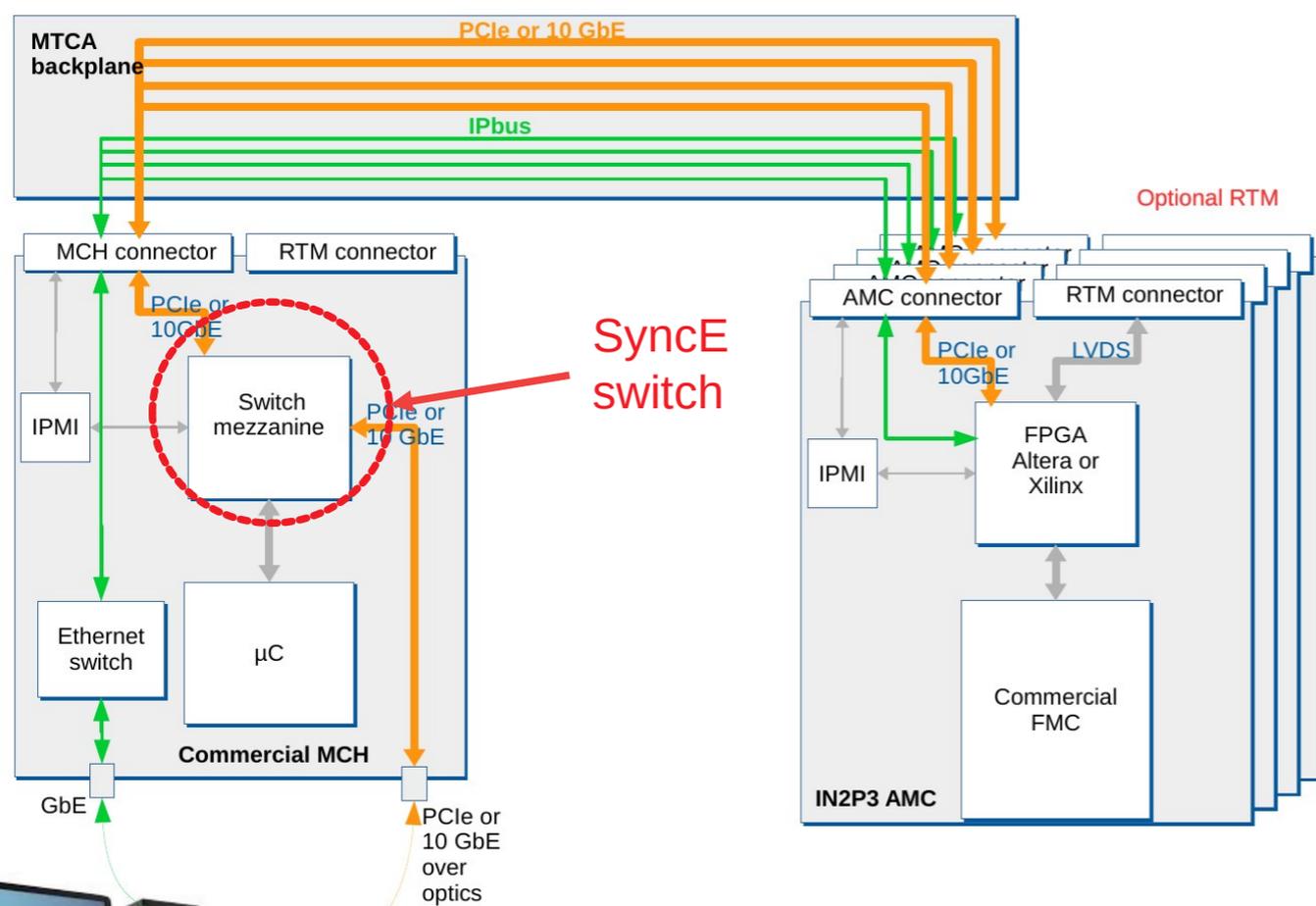
- Improvement of the WR performance
 - Soft PLL Reponse time
 - Components upgrading
 - MP replacement

- Integration of WR external component by firmware functions.
 - Integrate PLL
 - Analog VCXO by numeric bloc

R & T TIMED : WR Crate integration



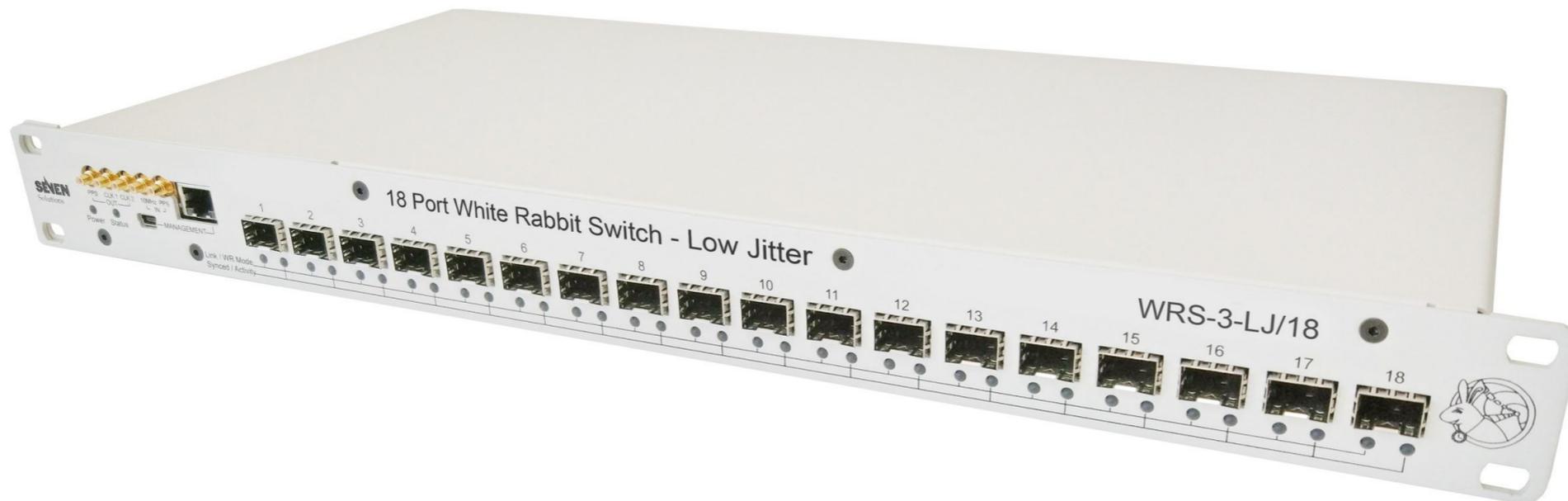
- Continuation of DAQGEN project
 - Only switch functionality (no GM)
 - Sync-E function on MCH board
 - Test MCH on the shelf product
 - N.A.T MCH SyncE in design
 - Custom MCH to design
 - Switch function to design



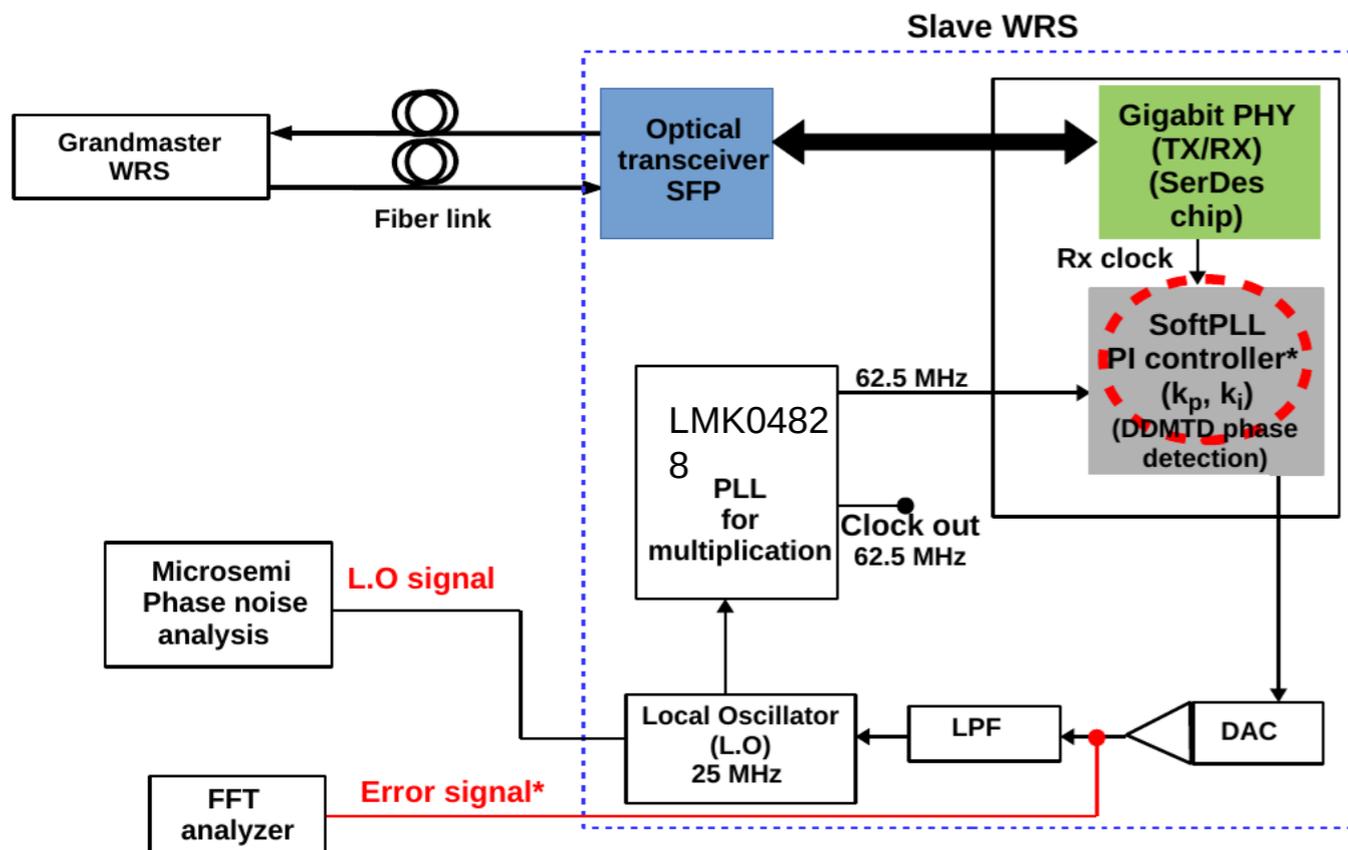
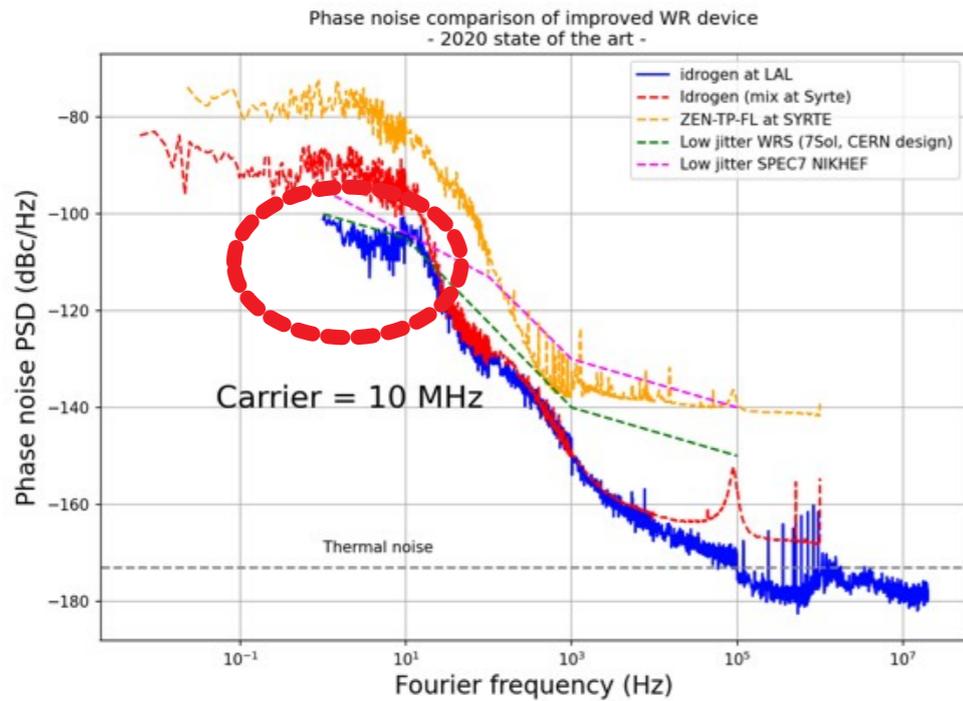
- Question
 - SI solution du commerce opérationnelle :
 - Développement d'une brique SyncE pour d'autre standard ?



Grand master : time distribution

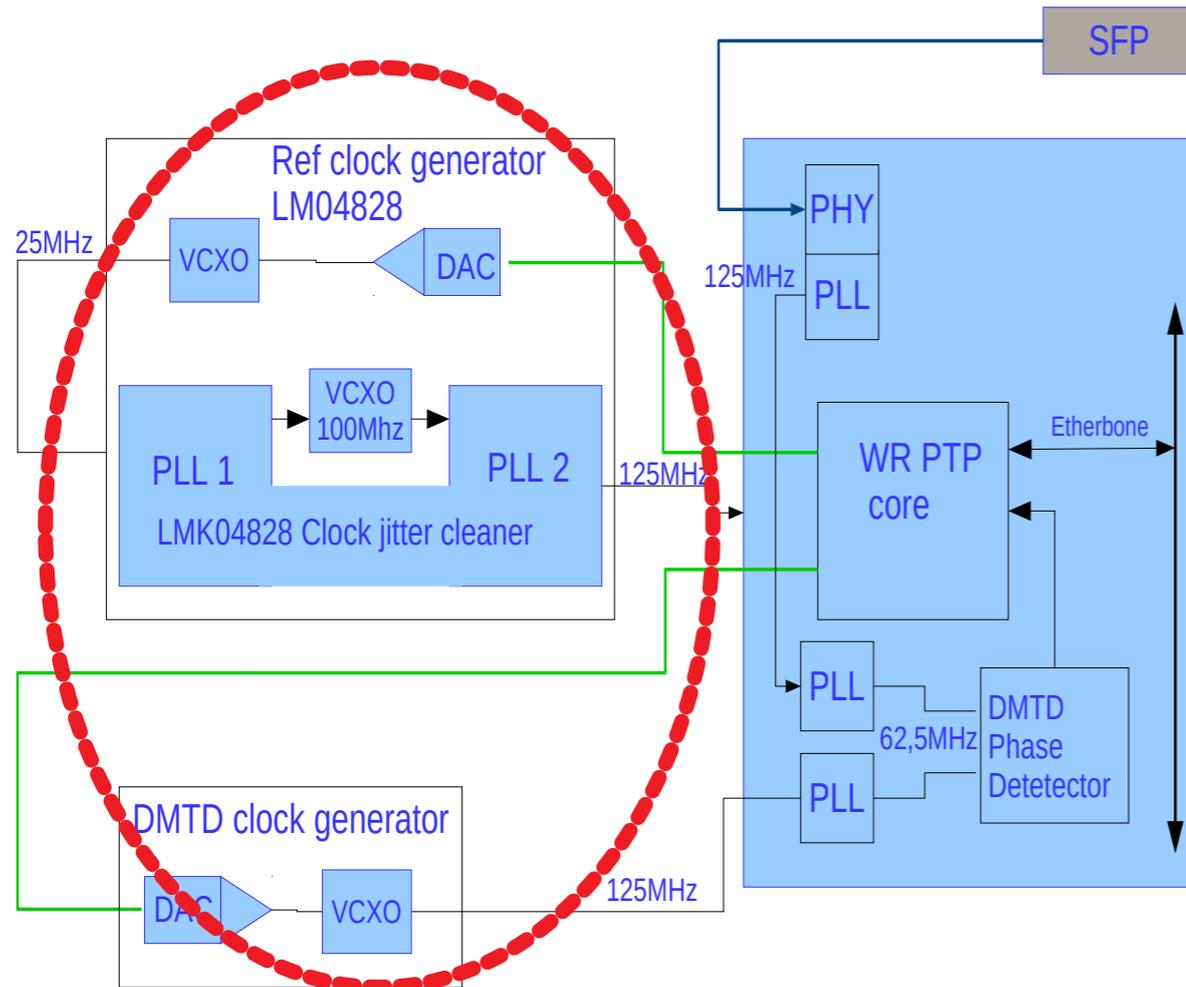


R & T TIMED : Increasing performances



- Collaboration with SYRTE Laboratory
- μ P upgrading
 - Replacement of the universal μ P base on logic bloc by dedicated μ P (NIOS) or hardware μ P (SOC)
- Components upgrading
 - VCXO selection
 - Increase Frequency
- Soft PLL modification
 - Decrease the reponse time
 - Gain intégrator optimisation
 - Replacement ot the internal μ P

R & T TIMED : Firmware integration



- External PLL integration
- Internal reconfiguration
- μ P Software upgrade
- VCXO intégration
- Derived from video IP
- **FPGA manufacturer dependent**

Application Note: 7 Series FPGAs and Zynq-7000 AP SoCs



XAPP589 (v2.3) April 29, 2015

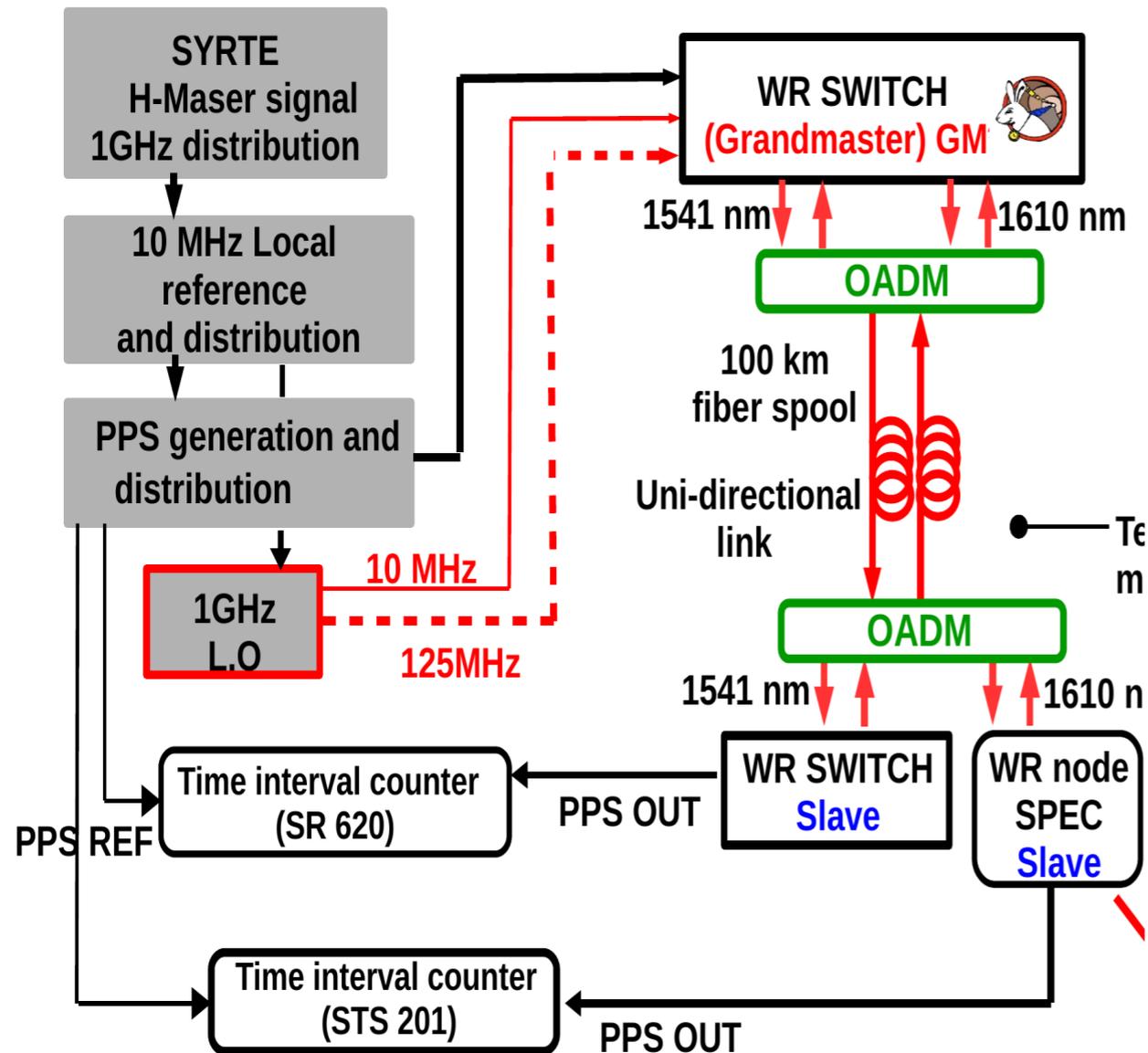
All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)

Authors: David Taylor, Matt Klein, and Vincent Vendramini

Summary

This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver.

Note: In this application note, *transceiver* refers to these types of transceivers:



For the test we use the test system developed by the SYRTE for timing distribution measurement.

- fs measurement capability
- Very high timing stability $10e-16$
- WR switch improvement.
 - Remove of local PLL
- Conditioned room.
- Dedicated measuring apparatus
- Selection of fiber length
- Selection of transceivers

● TIMED

- 3 laboratoires engagé actuellement : LPCC, CENBG, IJCLAB,
 - Autre laboratoire intéressés ?
- Le document en fin écriture.
- Question ouverte sur la partie switch