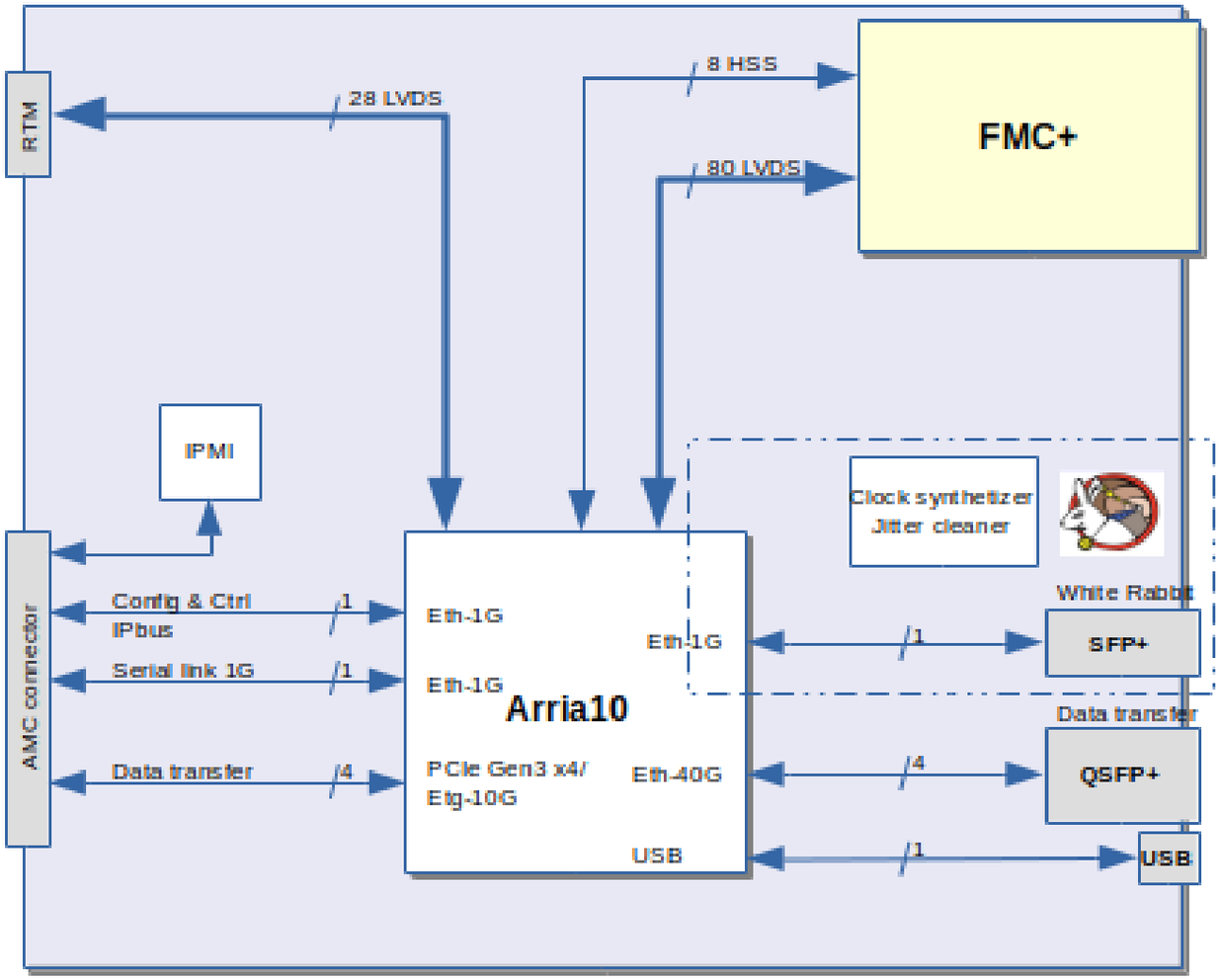
Laboratoire de Physique des 2 infinis Irène Joliot-Curie

IDROGEN

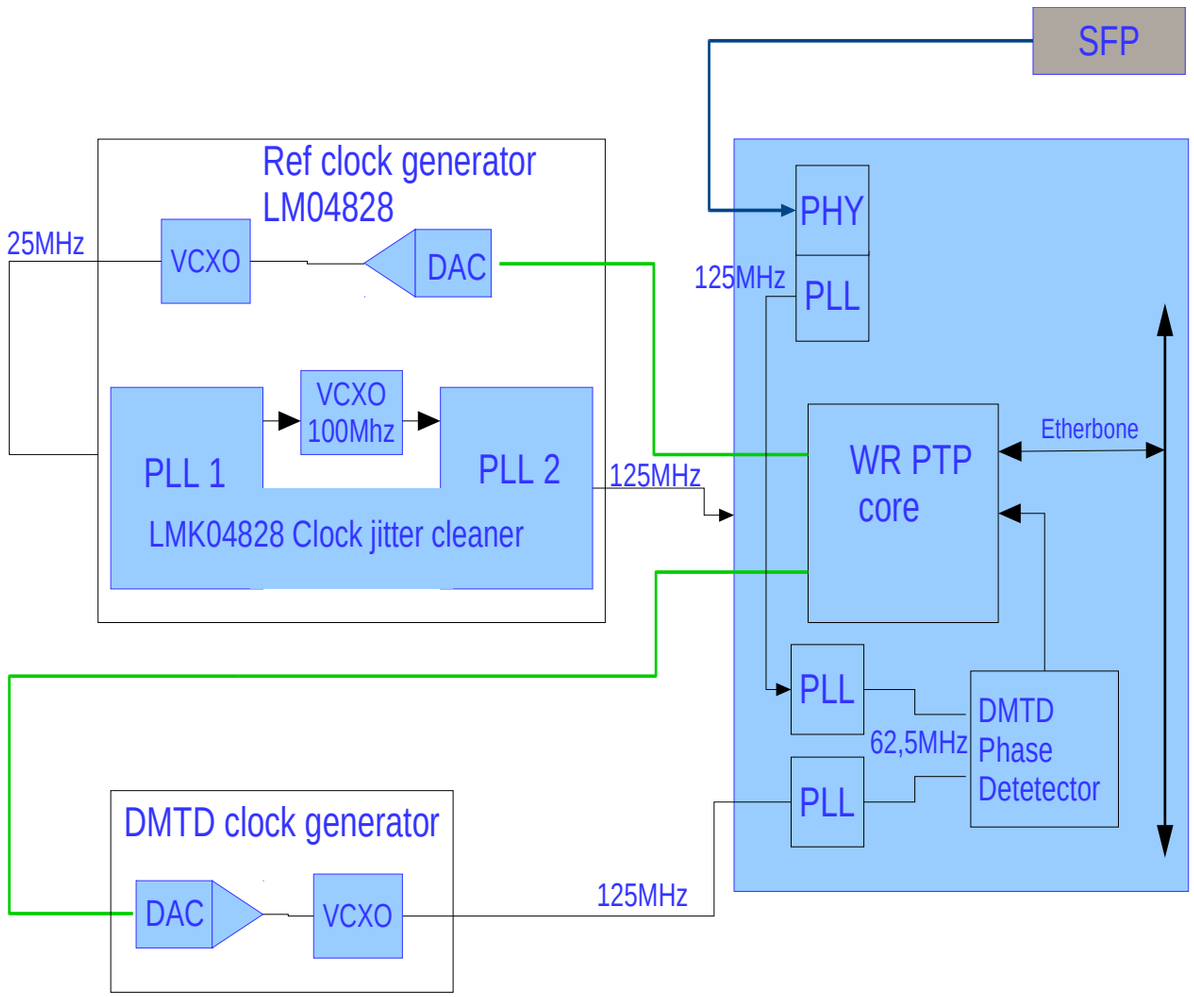
IDROGEN : 13Oct2021

IDROGEN main features



- MTCA 4.0 satndard, doubel width, fullsize AMC.
- Stand-alone mode
- VITA57.1 (FMC slot)
  - 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant.
- Front panel conectivity
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane conectivity
  - 1Gbe IPbus,PCI 4x Gen3,
  - IPMB, CLK & trigger lane.
  - RTM connector : J30

WhiteRabbit : DAQGEN implementation

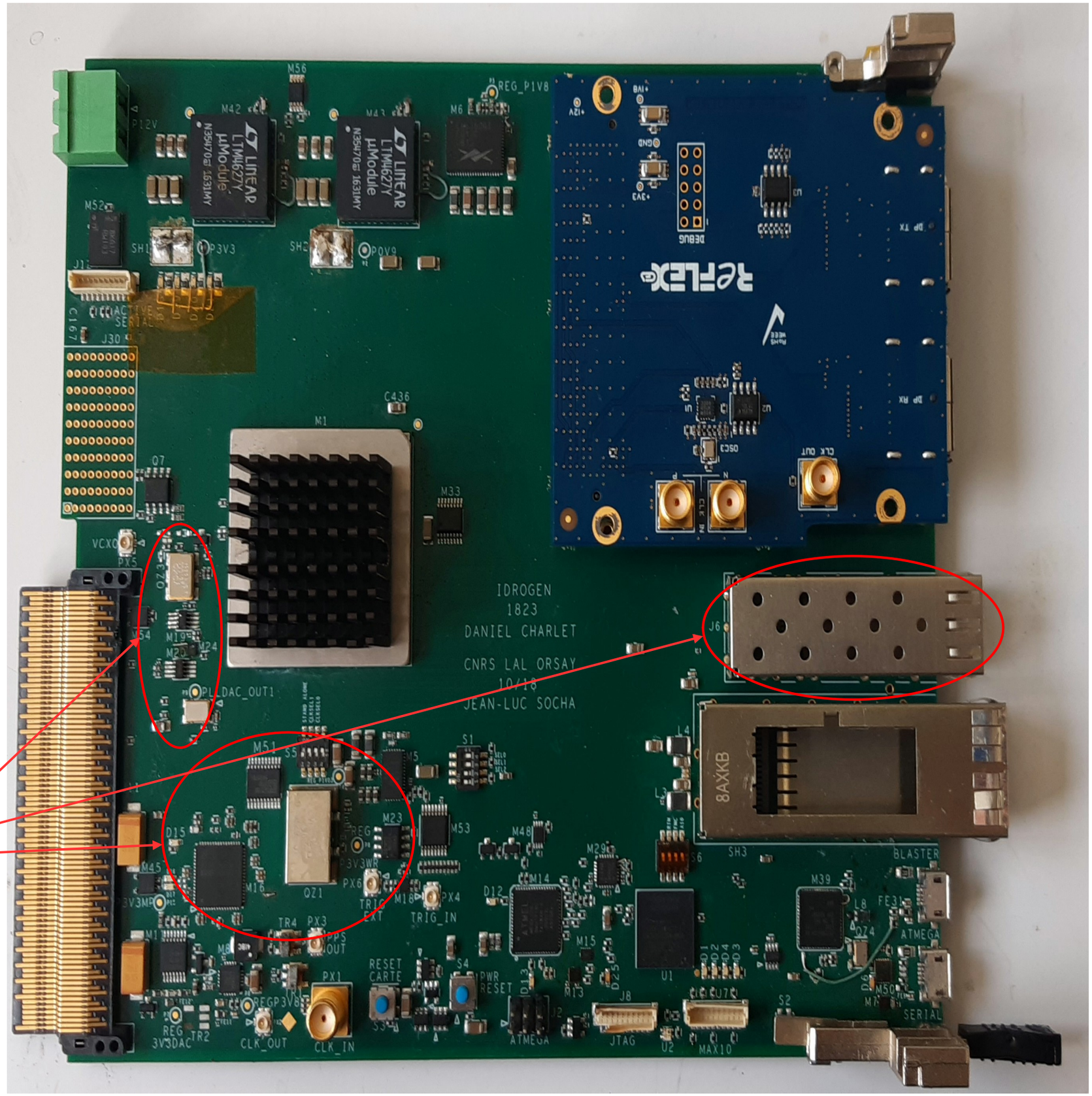


The WhiteRabbit IDROGEN hardware is base on CERN open hardware with Enhancements

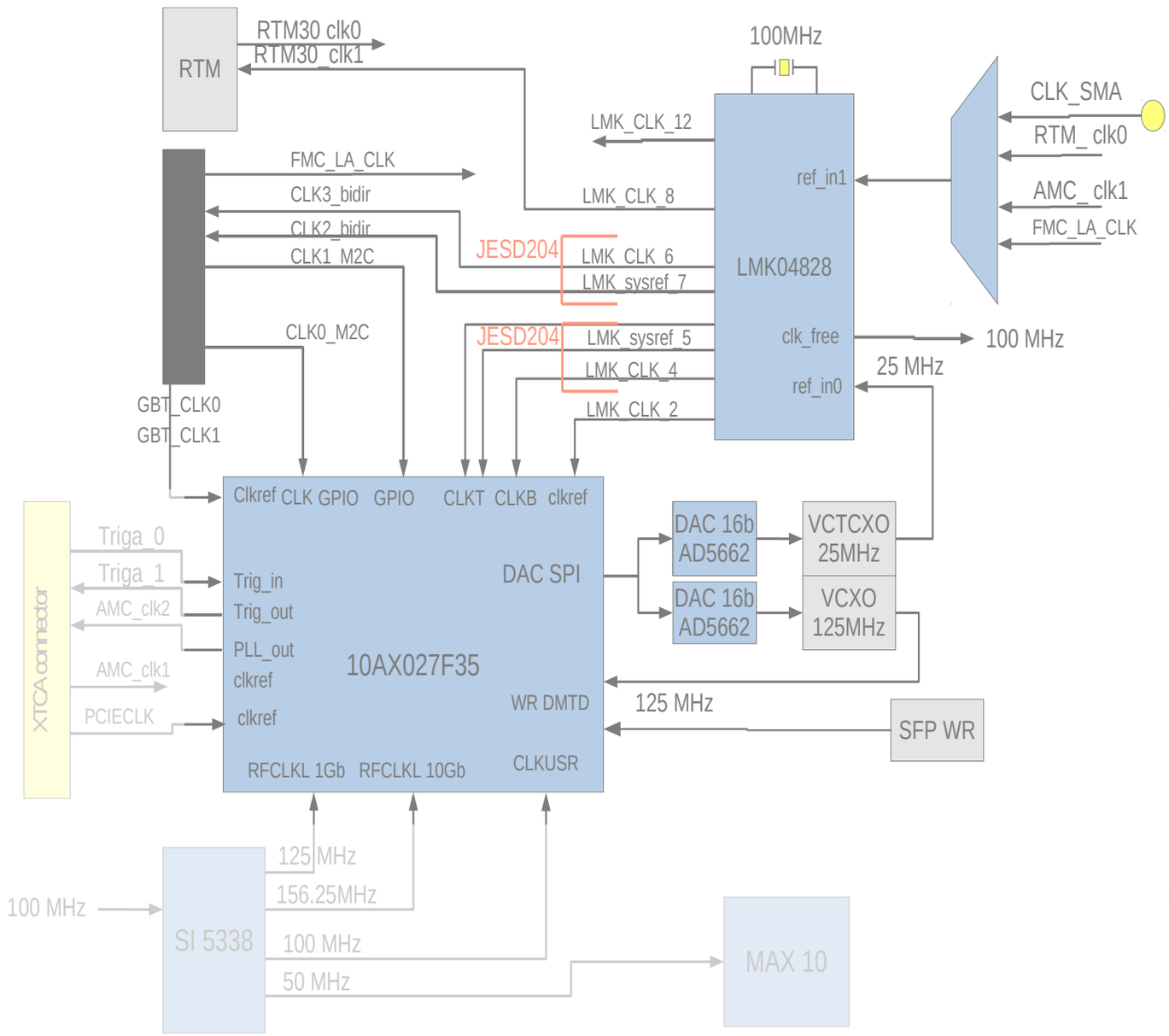
- Based on LMK4828 synthesiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter.
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clock :
  - DDMTD source (comparison between WR master clok from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD
    - remove of internal PLL (future dev.)
  - Tx/Rx routing equalisation

http://www.ohwr.org/projects/white-rabbit/wiki/WRReferenceDesign

IDROGEN board

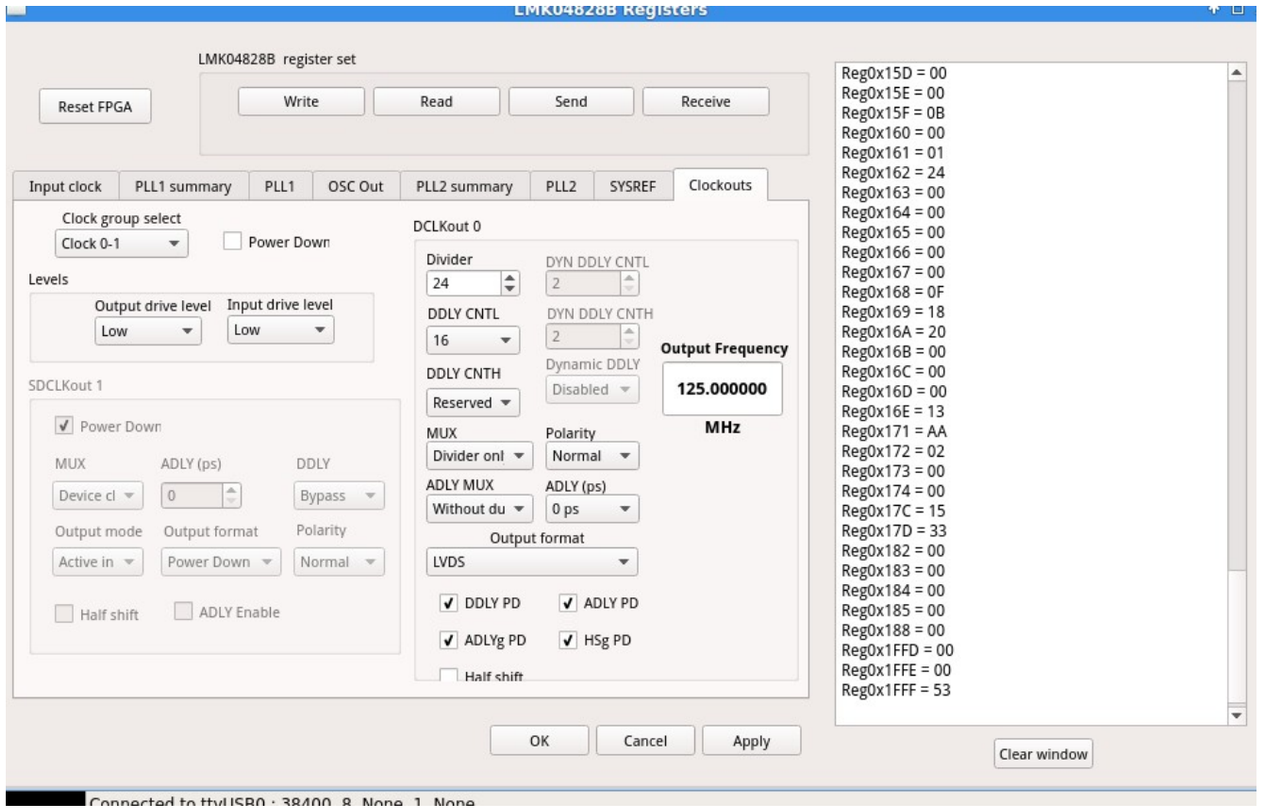


Clock tree: main features 2

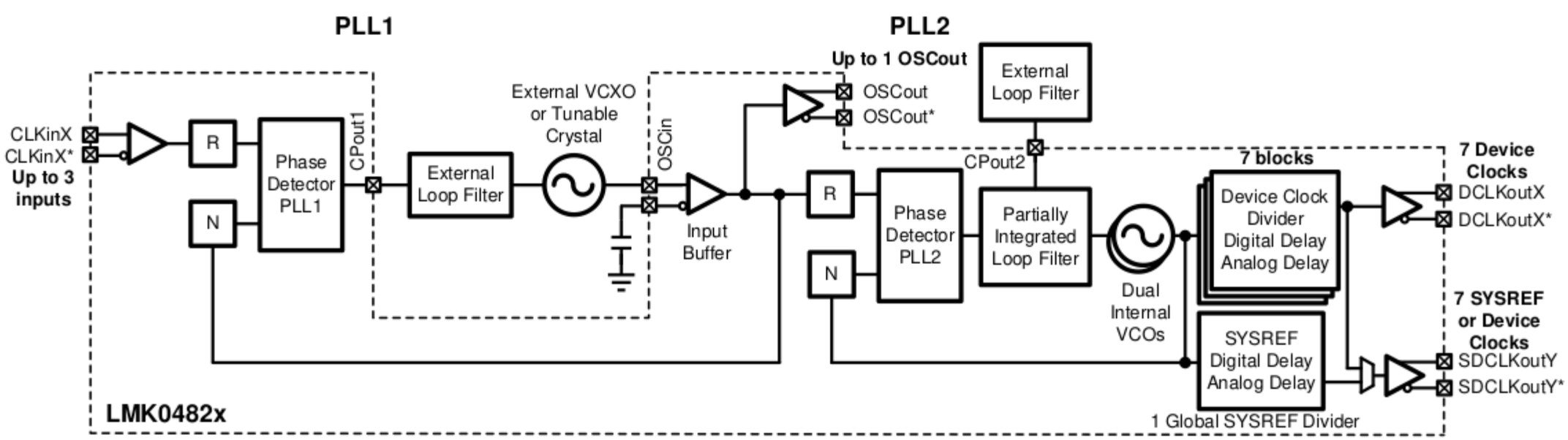


- LMK4828 clock in :
  - White-Rabbit module.
  - SMA connector.
  - RMT30 connector : CLK0.
  - FMC connector : LA_CLK.
  - AMC connector : TCLKB.
  -
- LMK4828 clock out :
  - FMC connector JESD204 compliant : Clk2_bidir, Clk3_bidir .
  - RTM : CLK1
  - FPGA : CLKREF, clk.
  - AMC_CLK2
- FPGA received also direct clocks from different sources :
  - FMC connector
  - AMC connector
  - RTM connector

IDROGEN Clock generator : LMK04828

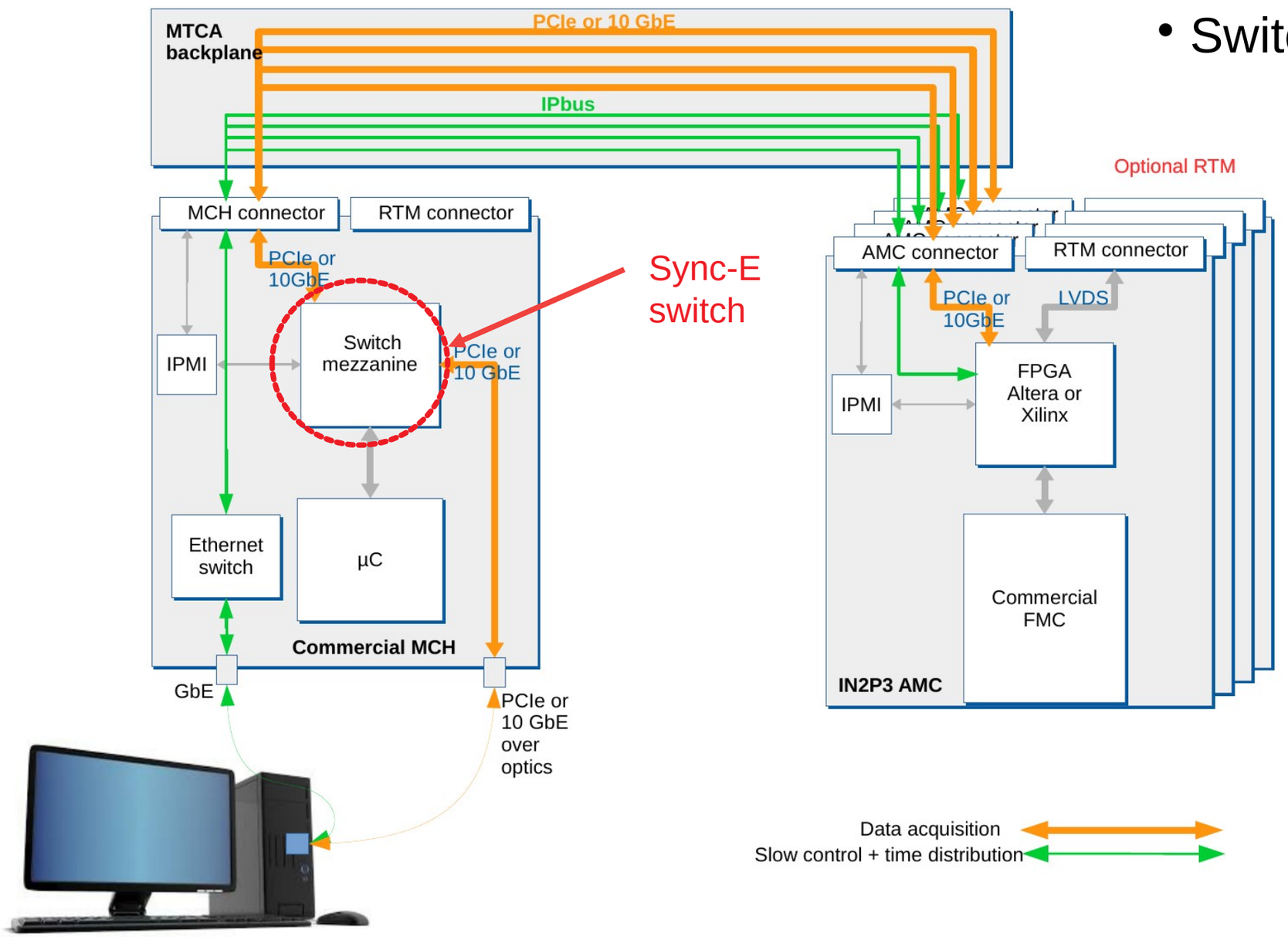


- LMK04828
  - Frequency programmable 11MHz to 3 Ghz
  - Analog delay adjusment by 25ps step
  - ~ 100fs rms jitter
  - JESD20B compatible
  - Free runinng or synchro WR
  - Configure by µP.
  - Re-configuration by USB or Eth
  - Output clk on sma connector

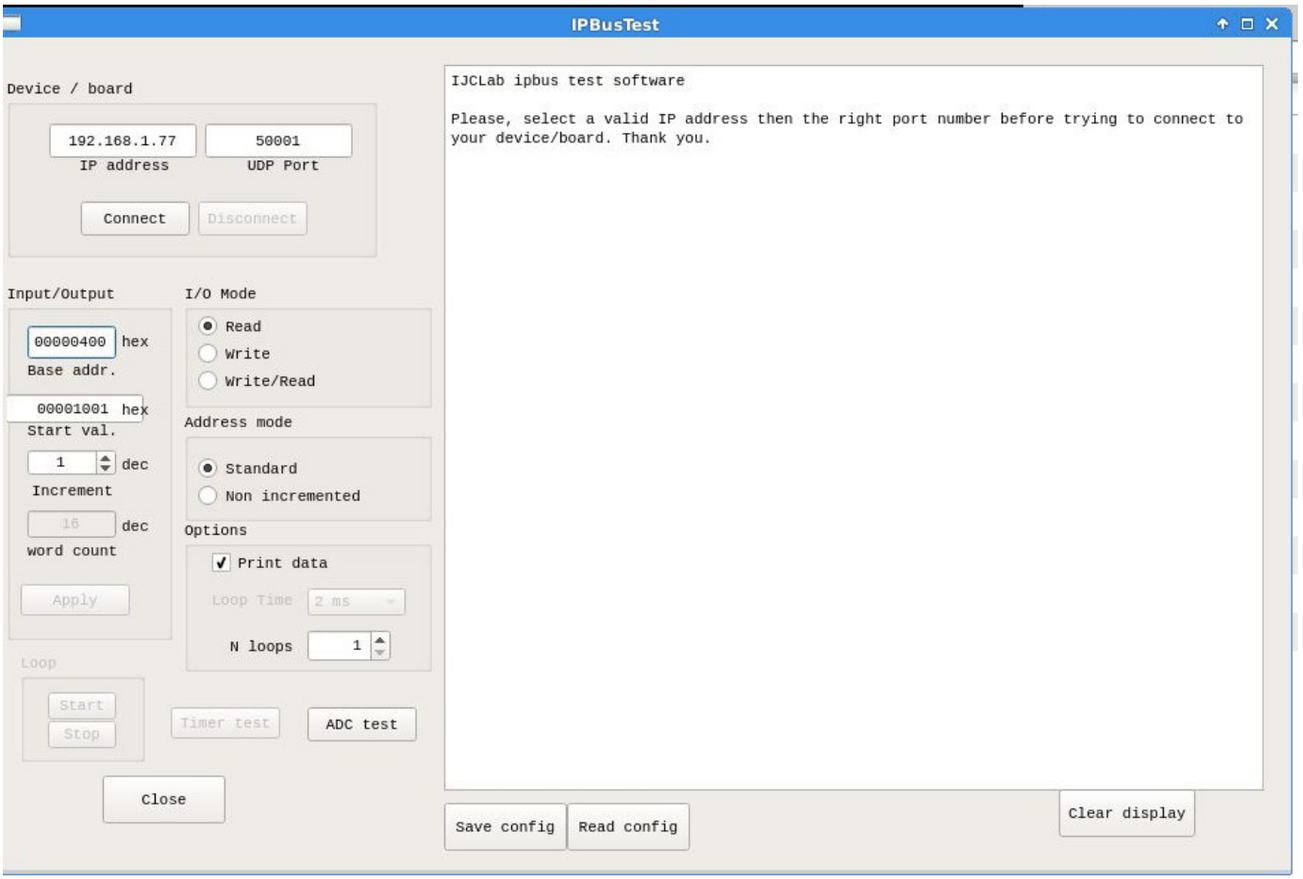


R & T TIMED : WR Crate integration

- Continuation of DAQGEN project
  - Only switch functionality (no GM)
  - Sync-E function on MCH board
    - Test MCH on the shelf product
      - Custom MCH to design
      - Switch function to design

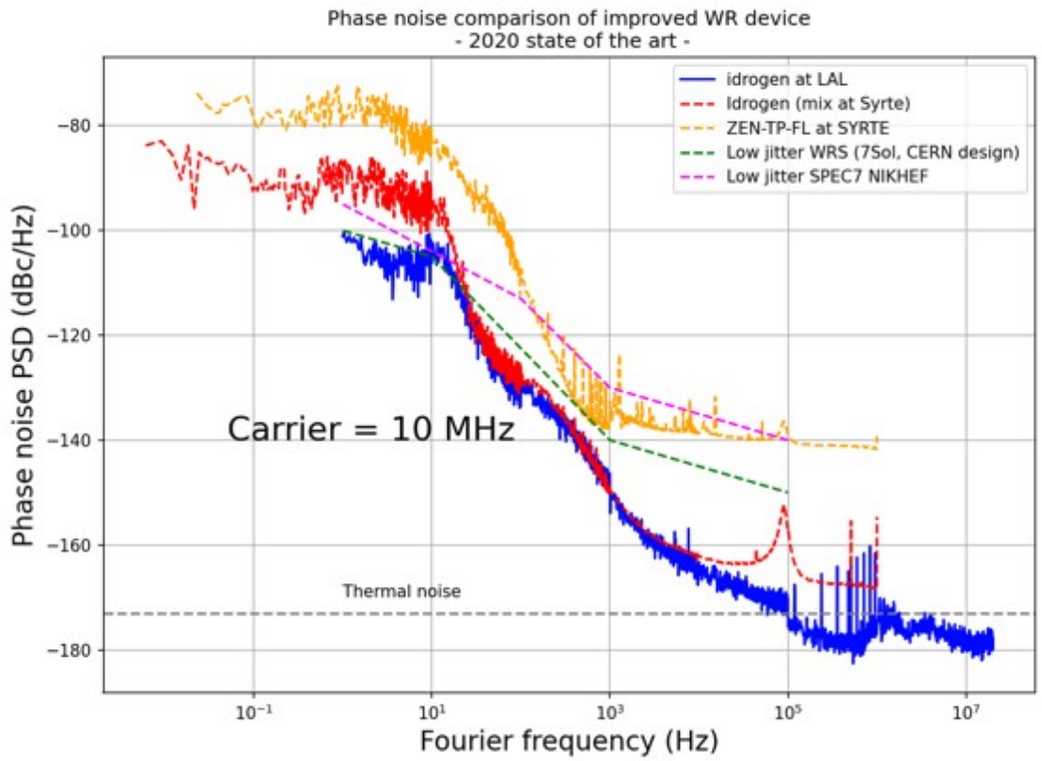


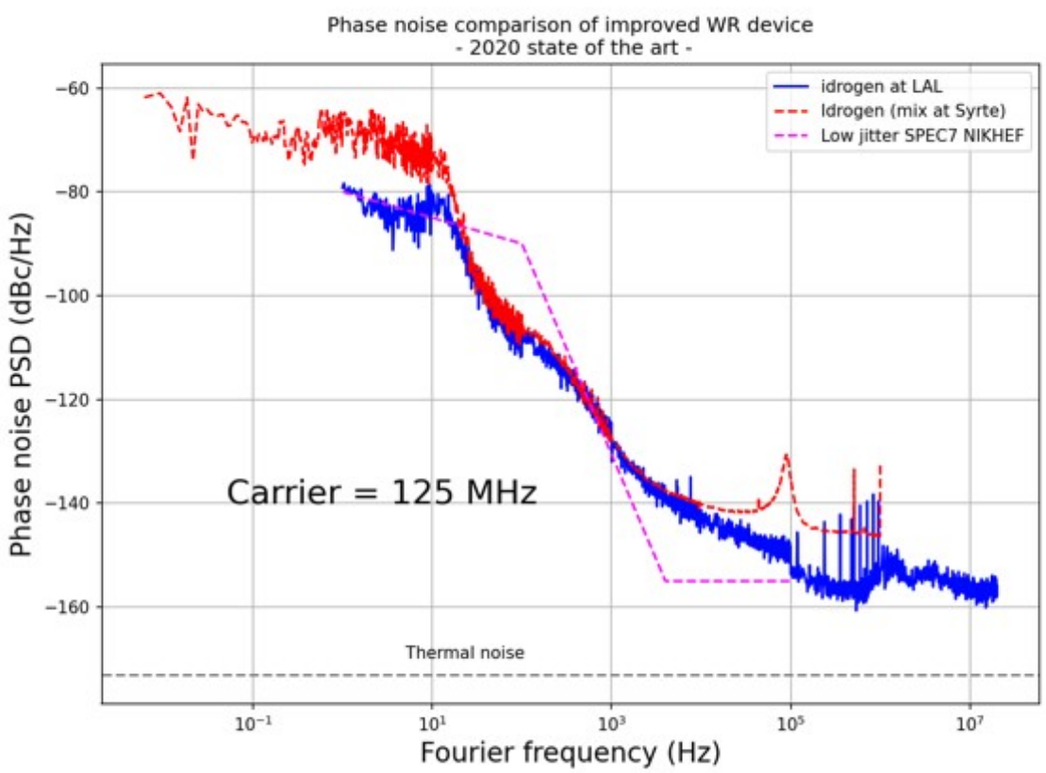
IDROGEN configuration & readout



- IpBus 1G
  - Developed by LPSC for XILINX
  - IntelFPGA version by IJCLA
  - Master QSYS
  - Utility base on QT
- IpBus 10G (in development)
  - Developed by LPSC for Xlinx
  - IntelFPGA version by IJCLA
  - New functionality : Streamer UDP
  - Acquisition software

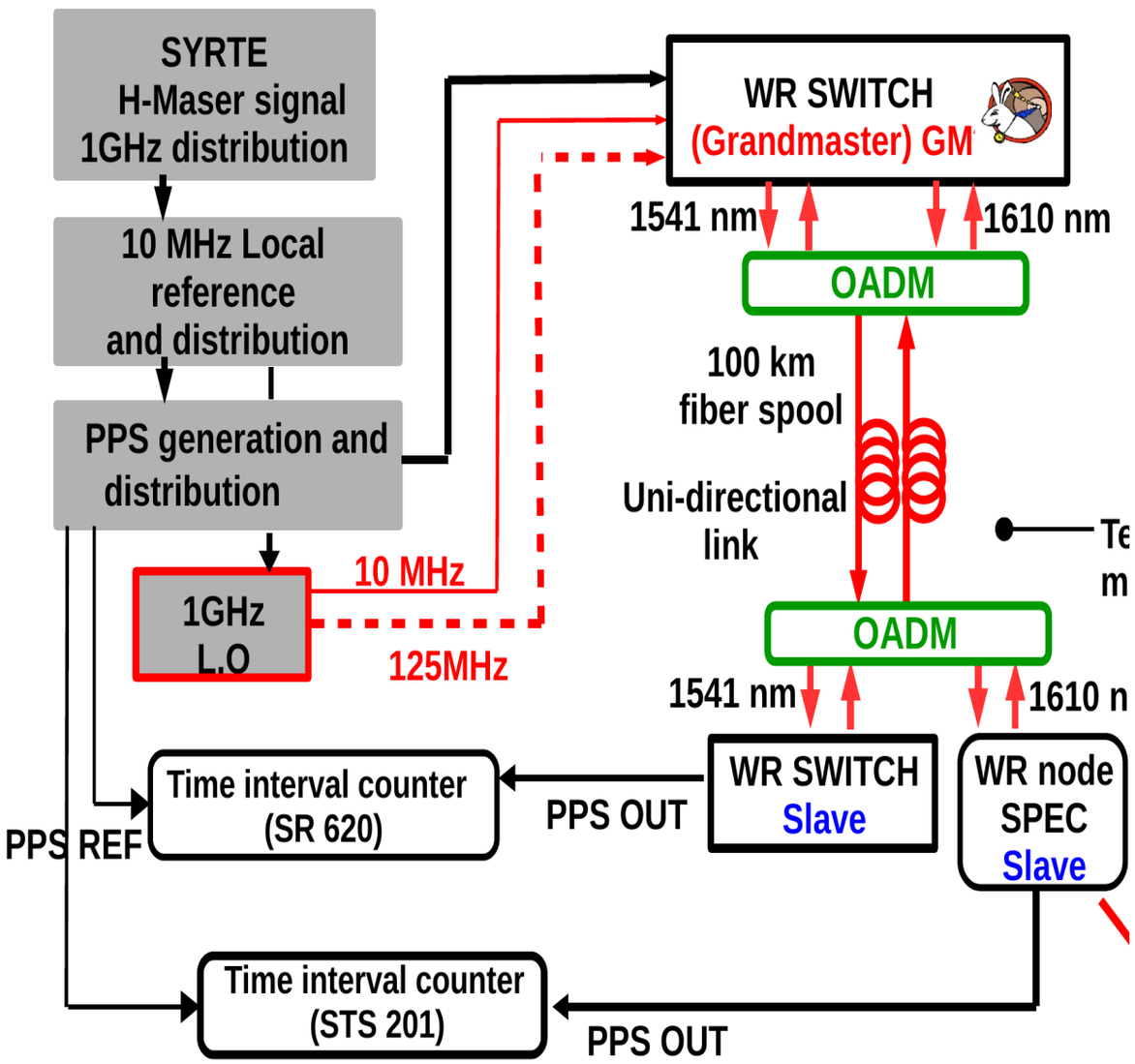
IDROGEN Phase noise measurements





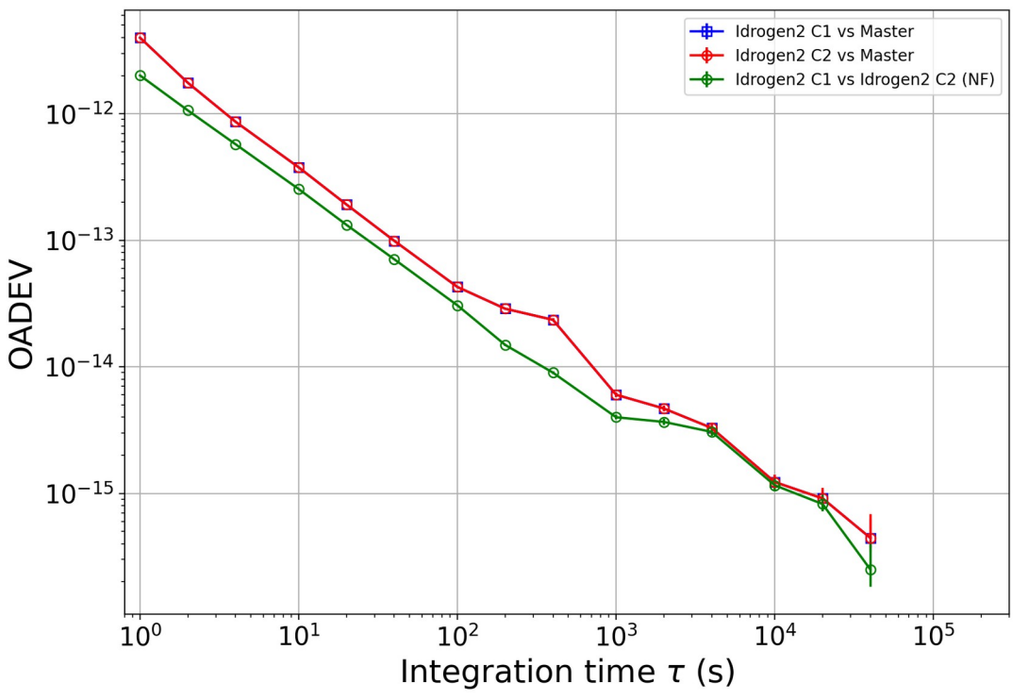
- For the test we measure the phase difference between 2 nodes (IDROGEN board)
  - Best result, one order, than the « challenger »
  - Clock phase jitter
  - PPS time precision 1ps RMS
  - Timing Improvement currently in development

WhiteRabbit, SYRTE test system

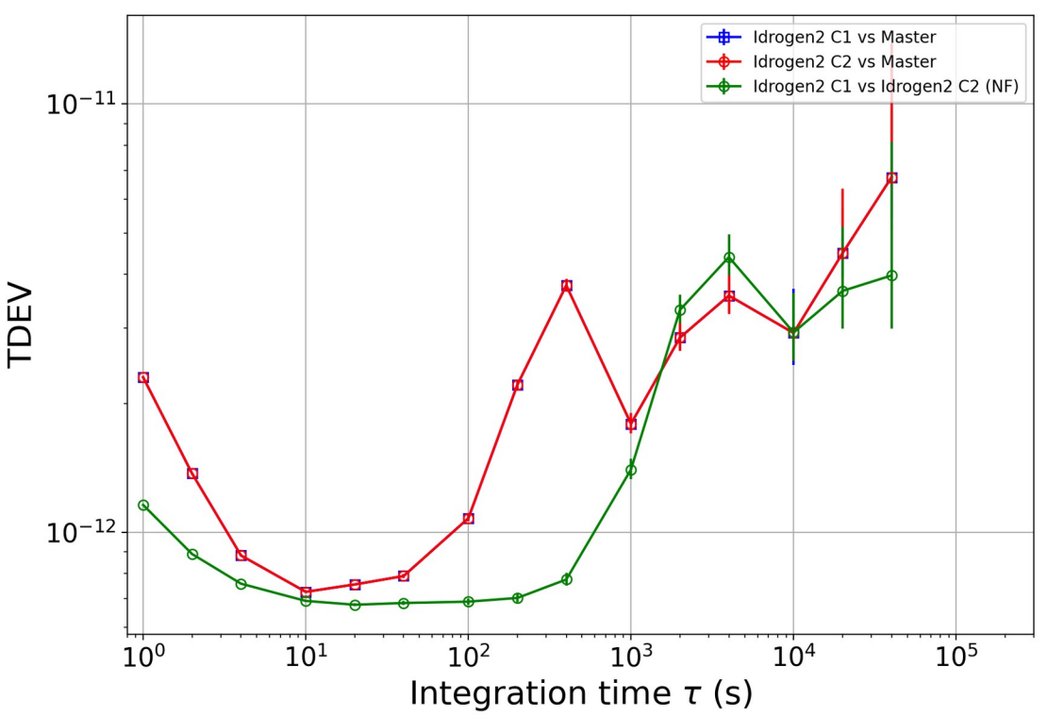


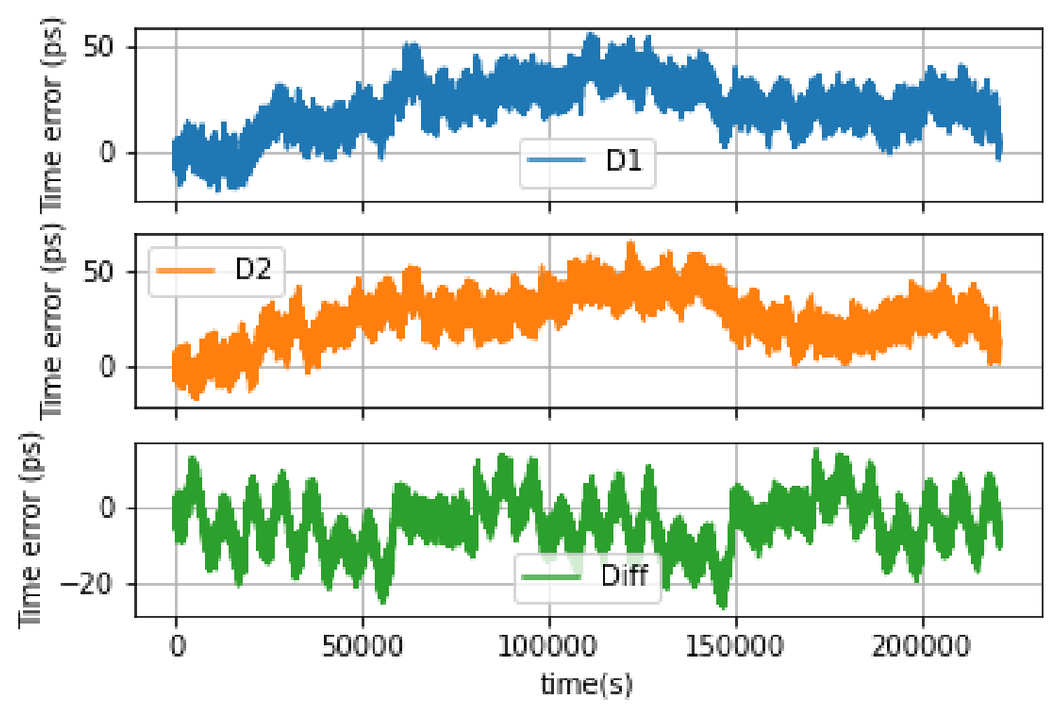
- For the test we use the test system developed by the SYRTE for timing distribution measurement.
  - fs measurement capability
  - Very high timing stability 10e-16
  - WR switch improvement.
    - Remove of local PLL
  - Conditioned room.
  - Dedicated measuring apparatus
  - Selection of fiber length
  - Selection of transceivers

IDROGEN preliminary measurements

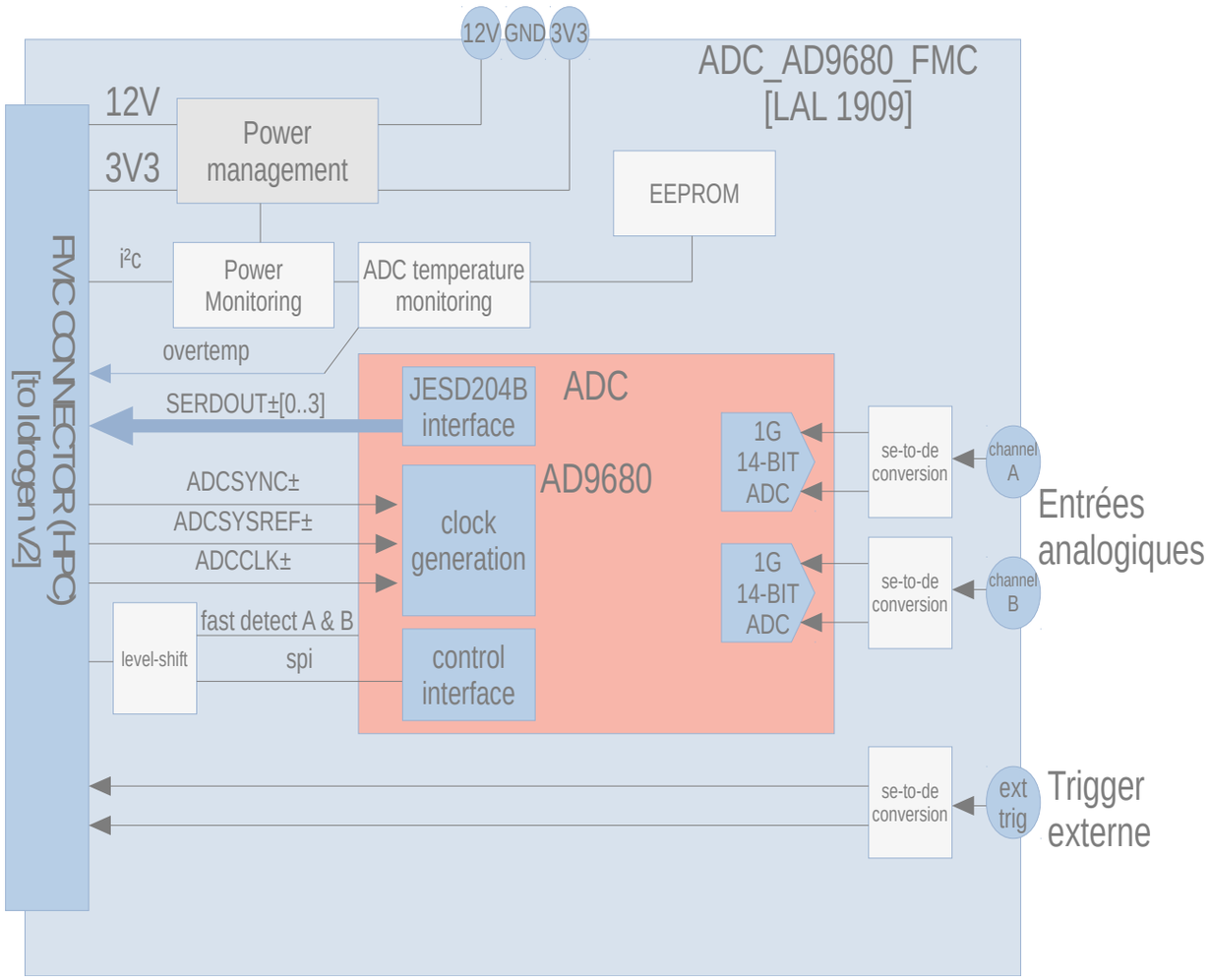


- Pour ces tests on mesures la phase entre 2 nœuds IDROGEN
- Une des cartes partiellement opérationnelles.
- Nouvelle mesure sera faite sur la V3
-



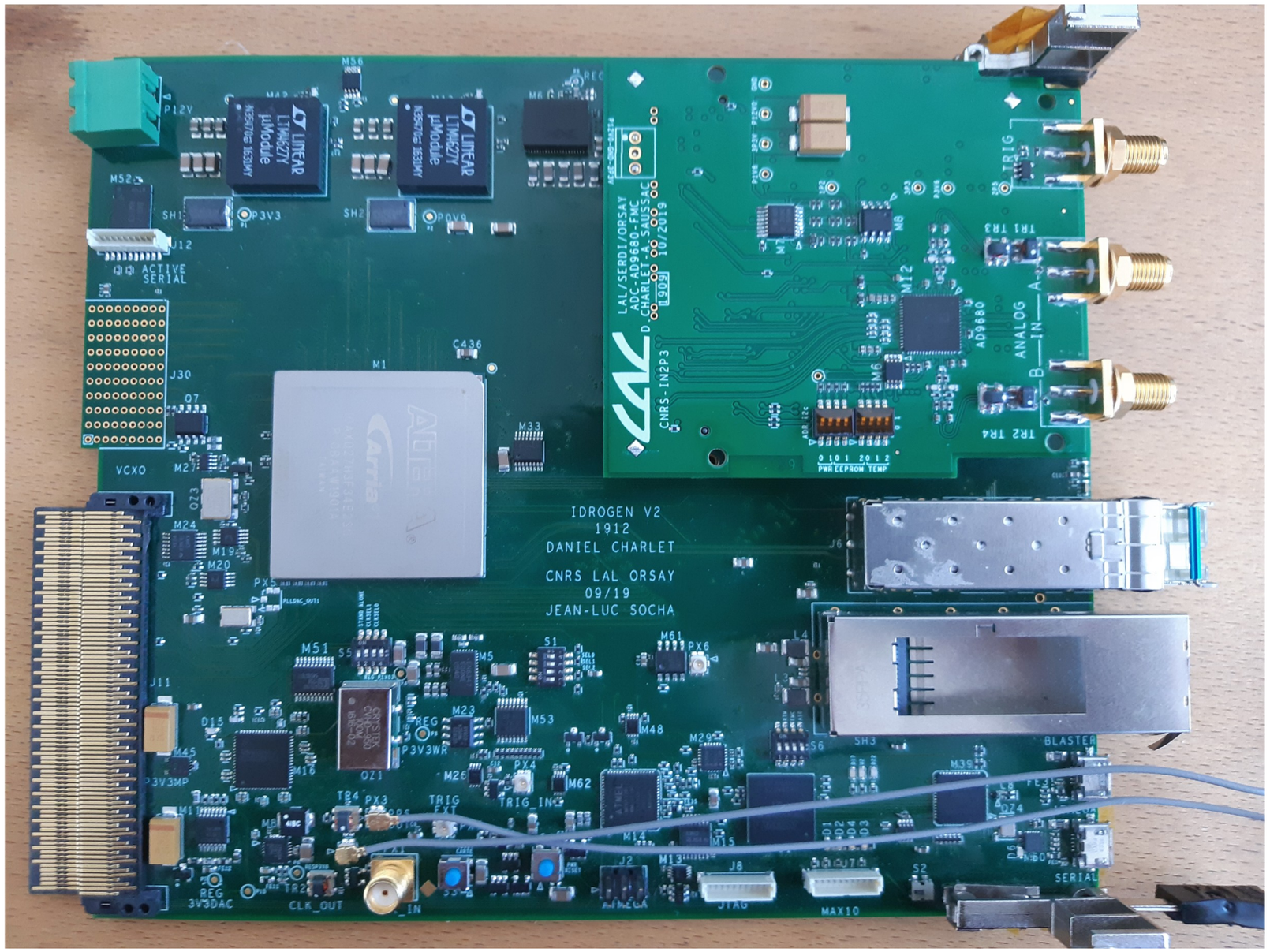


Mezzanine ADC

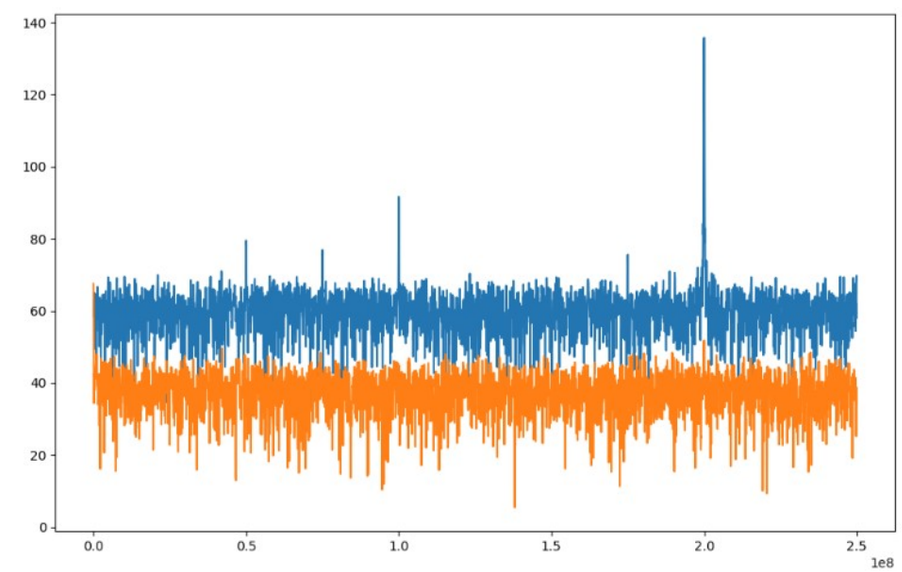


- The motivation of the development of a new mezzanine instead off an on-the-shelf ADC mezzanine :
  - include : its own PLL.
  - ADC clock source : External clock
- Mezzanine main features :
  - VITA57.1 (FMC)
  - ADC 9680
  - 2 channels
  - 14 bits
  - 1.25 GSPS
  - JESD204
  - 2GHz analog bandwidth
  - External trigger in

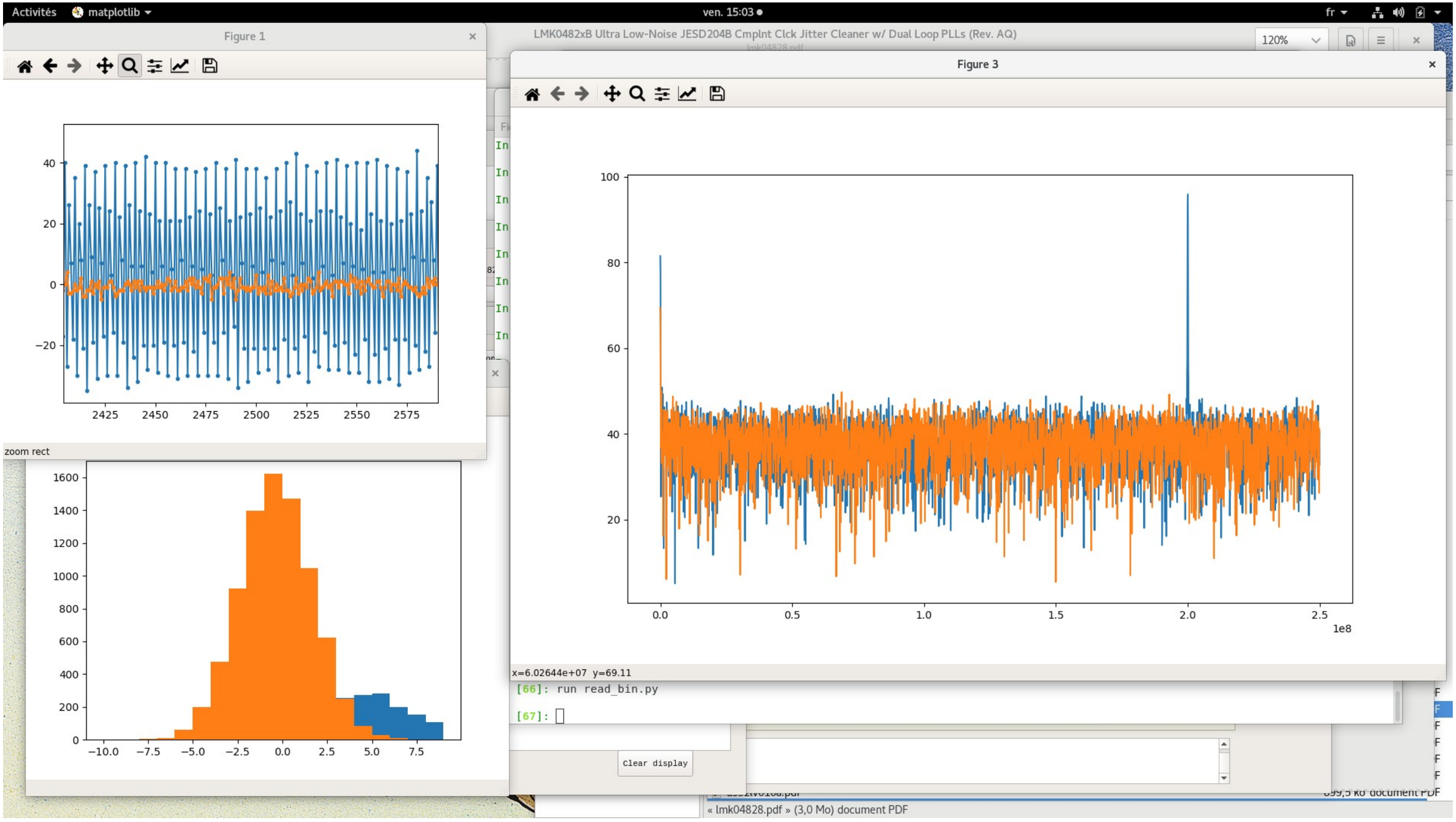
IDROGEN + mezzanine ADC for PAON IV



- Preliminary results
- Bandwtih 500 MHz at 1.5GHz
- WR synchronisation
- JESD204B protocol
- Configuration & readout : IP bus 1G
-



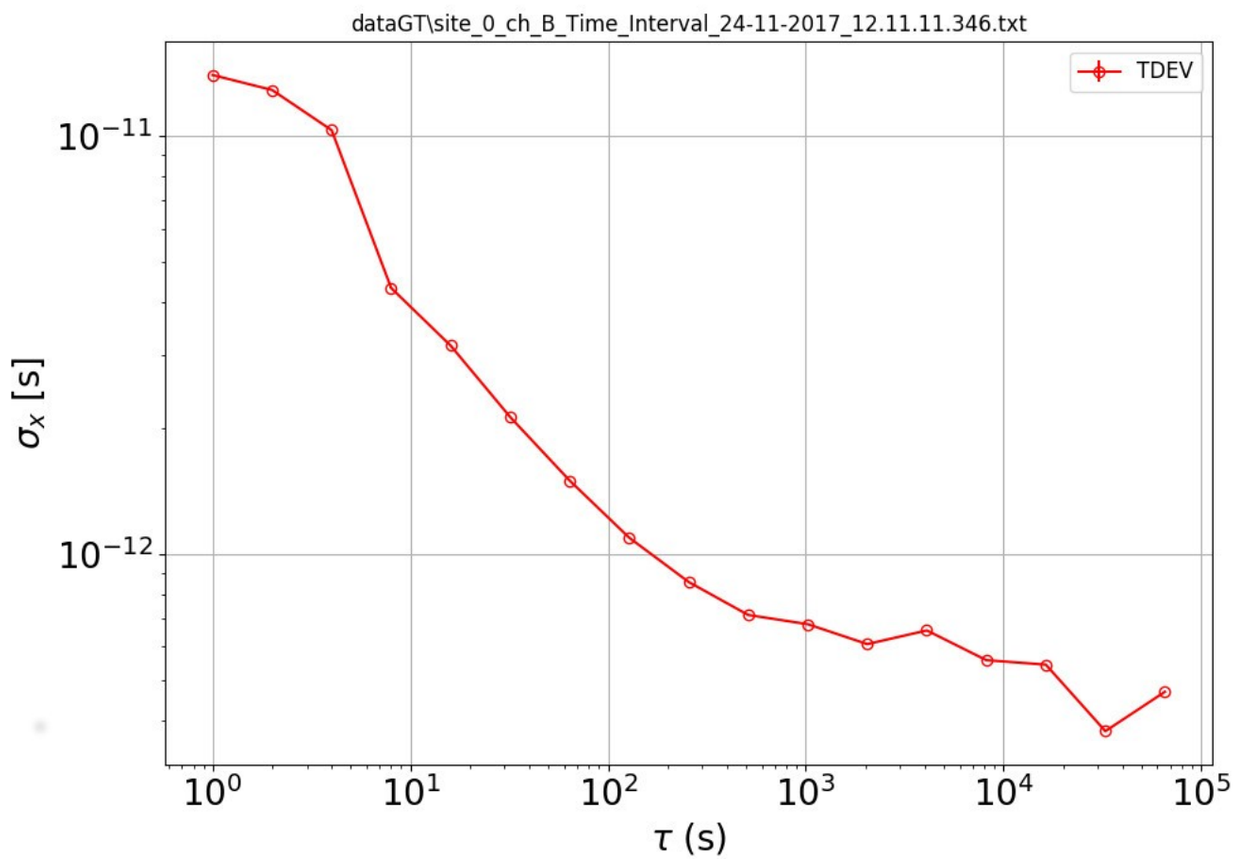
IDROGEN + mezzanine ADC for PAON IV 1.2GHz



Conclusion

- IDROGEN
  - V3 en cours de fabrication
  - PCB à la fin du mois câblage de 2 cartes dans la foulée
  - Câblage des 15 cartes fin de l’année
  - Firmware :
    - 1GEth Ipbus opérationnelle
    - 10GEth en cours de développement.
    - Lecture ADC en JESD204B opérationnelle.
    - Upgrade firmware WR
    - PCIexpress issue du développement de Belle2
- Les différences de valeurs dans les résultats dépendes principalement de ce qui est mesuré et des conditions :
  - Carte seule versus système (maitre esclave)
  - Longueur de la fibre
  -

NEBULA performance



- IDROGEN version -1
  - 400fs after 1000s & 100m of fibers
  - Same design as IDROGEN
  - IDROGEN system qualificationTest
    - With SYRTE test setup
    - 2 IDROGEN board : Grand master & slave configuration .

SYRTE test setup recently operational again