Journées des Métiers de l'Electronique de l'IN2P3 et de l'IRFU
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Shunt Regulator in TJ180 technology

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Presentation Plan

- **Motivation for serial powering**
- **General architecture and design approach**
- **Characterization results**
- **Irradiation results**
- **Test results with Mini-Malta**
- **Summary**

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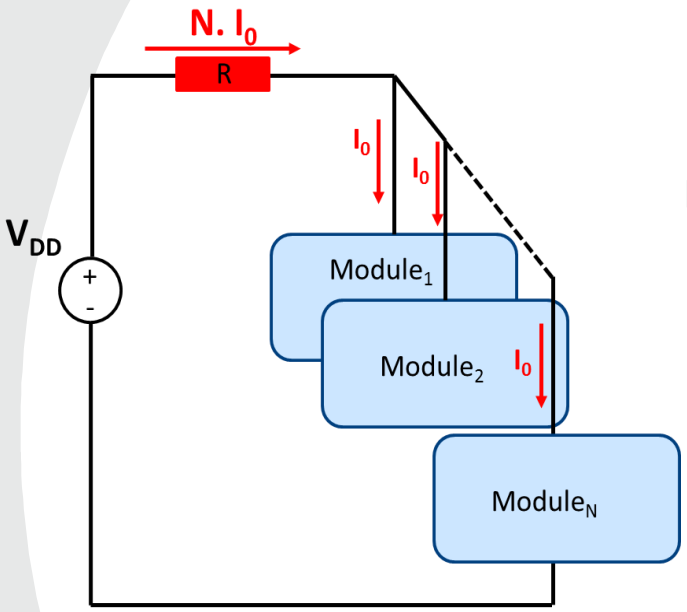
Motivation for serial powering?

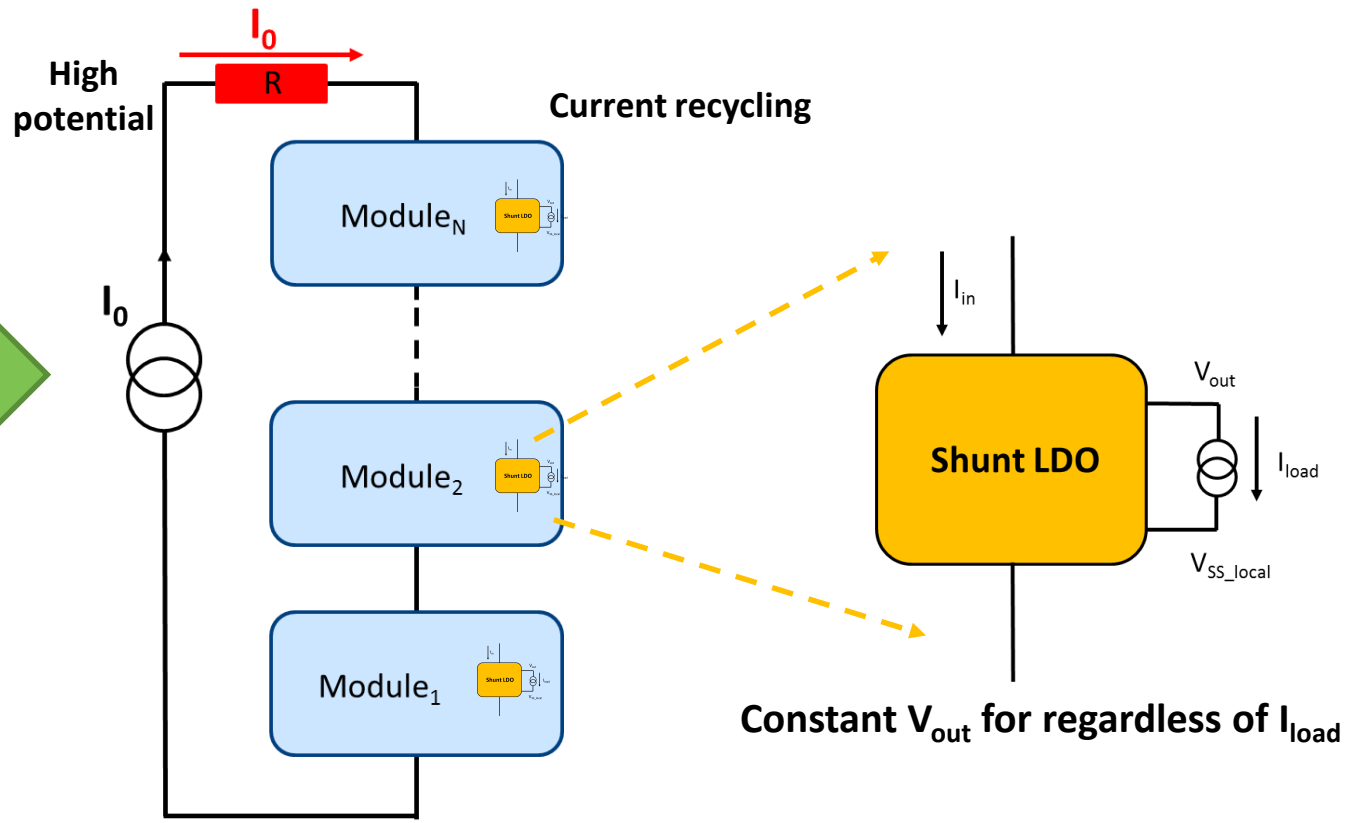
Parallel Powering Scheme



- Relatively high power losses in cables (around 80% losses in the present ATLAS pixel detector [1])
- A need for large cables which goes against material budget reduction

Cable Power losses reduced by N^2

Serial Powering Scheme



- Increases power efficiency and reduces material budget
- As CMOS electronics are designed to work under a constant voltage, a shunt regulator is needed.

[1] L. Gonella *et al.*, "A serial powering scheme for the ATLAS pixel detector at sLHC," *JINST*, vol. 5, 2010.

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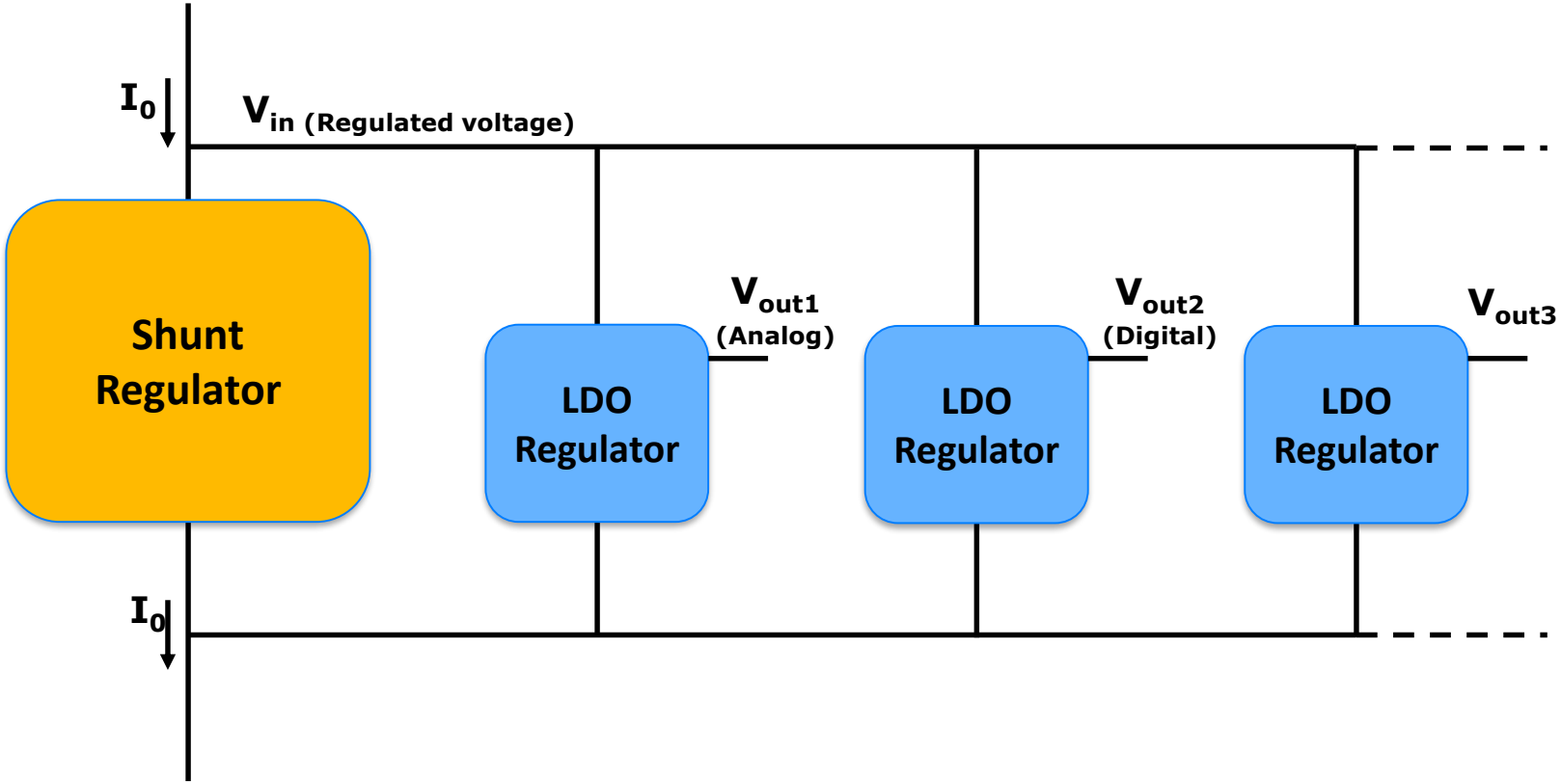
General architecture

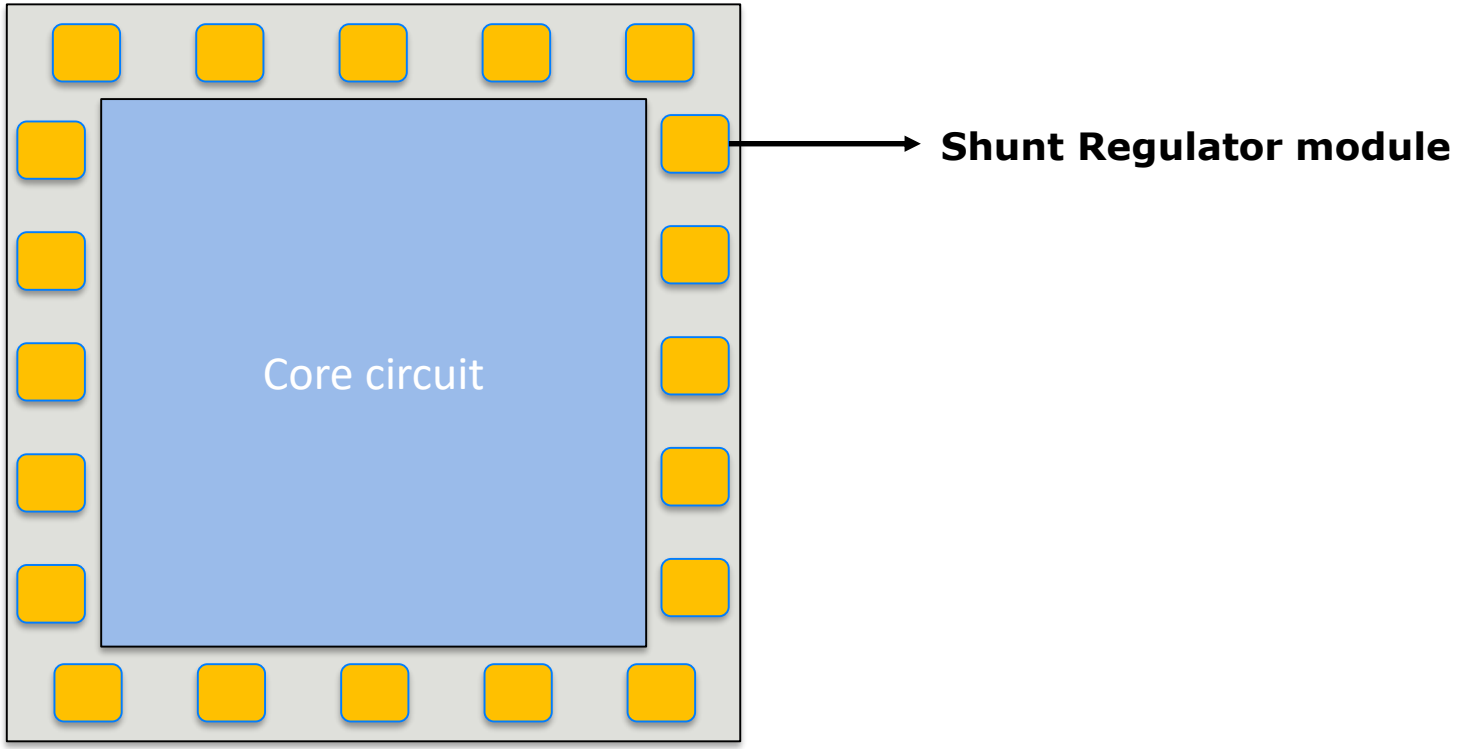


- One common shunt regulator takes in the input current I_0 and produces a regulated input voltage V_{in} (2 V)
- V_{in} is regulated a second round by a voltage LDO regulator
- The regulated output voltages (1.8 V) can be separated in different domains for better noise immunity

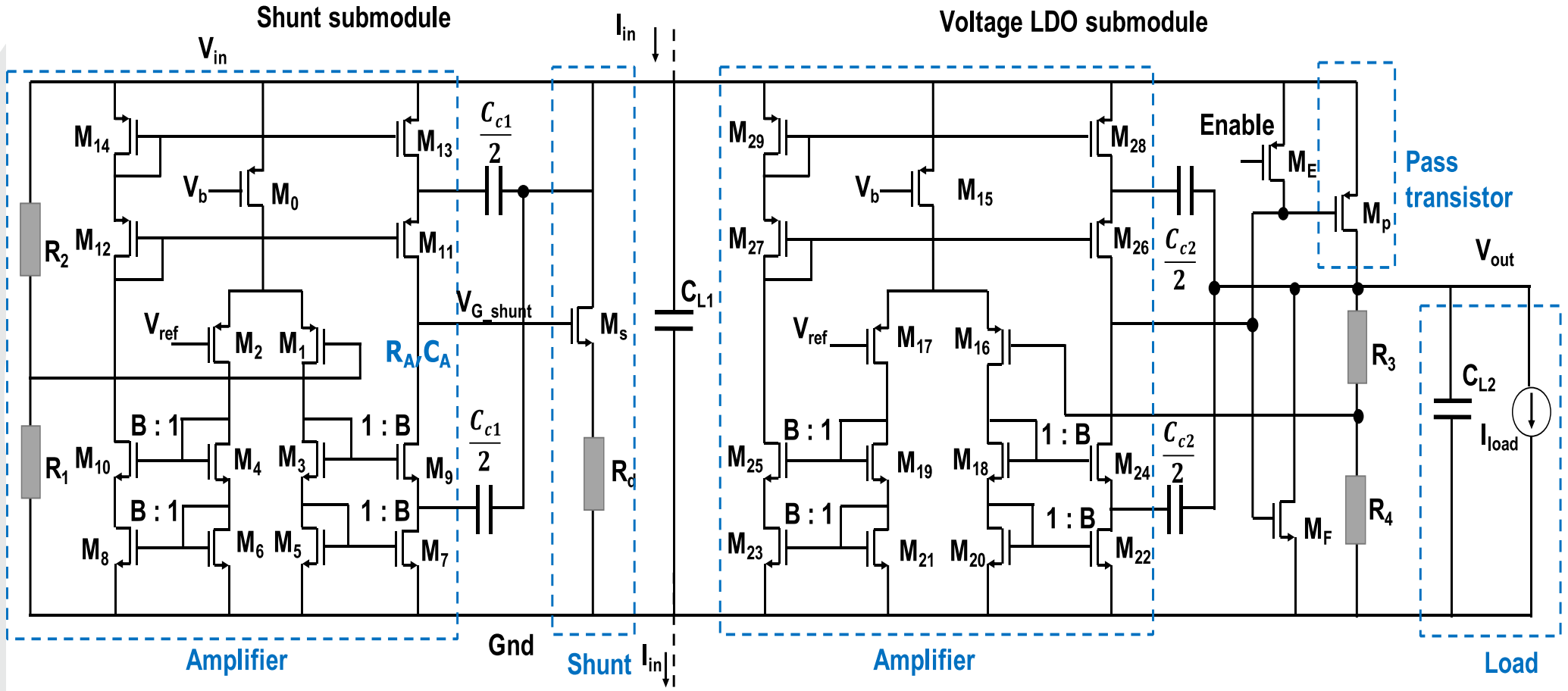
Modular structure

- **It was decided to design the regulator in a modular structure.**
- **Each module can handle a fraction of the input current (10 mA in the present design)**

  - **Better power distribution across a large chip**
  - **Less power density → Easier cooling**
  - **Flexible and scalable design**



Module architecture

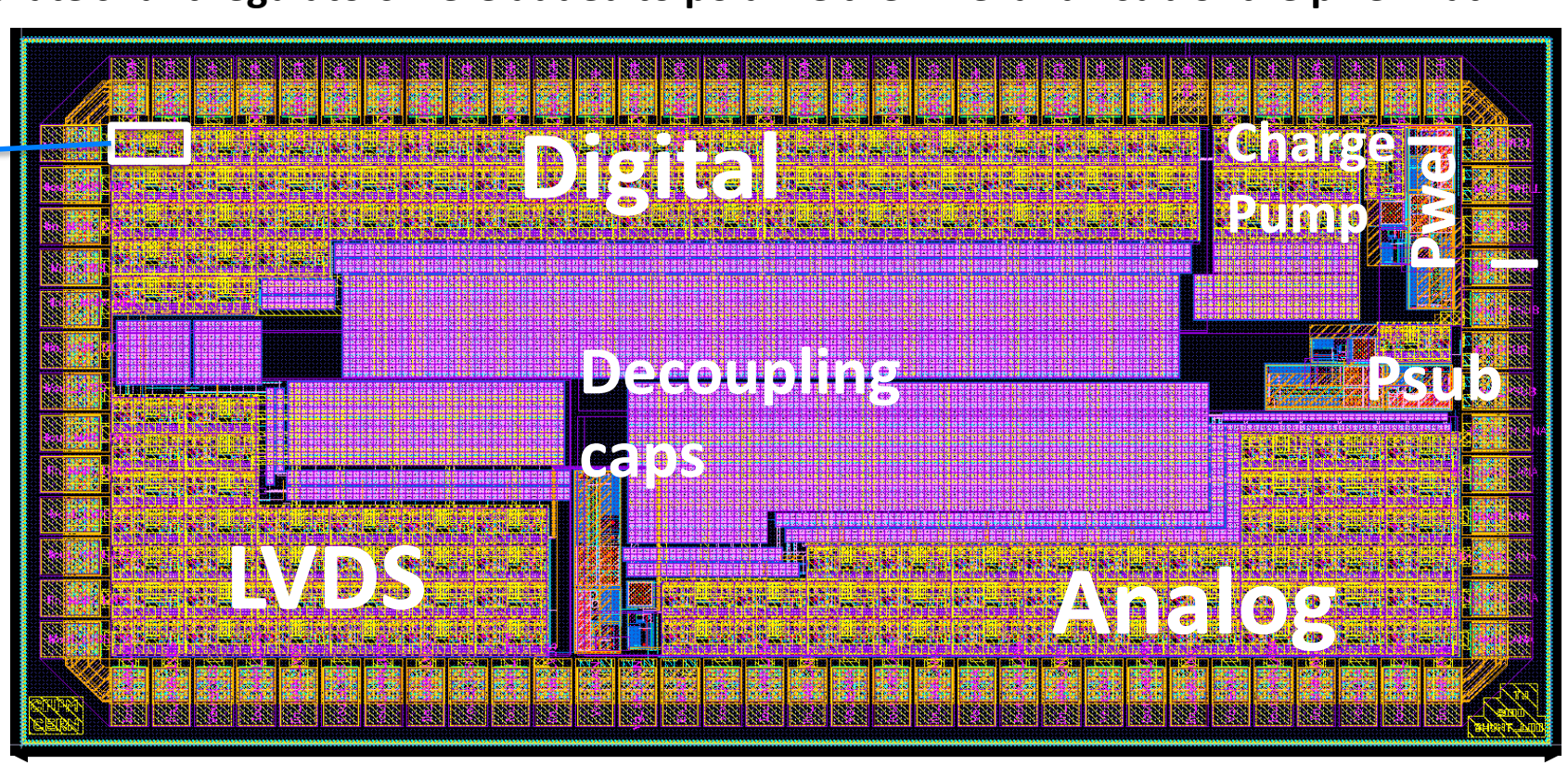


Design was developed with a valuable help from W. Snoeys

Test Chip in TJ180 nm

- Test chip designed to power a chip requiring 1.26 A (Spec estimated for a large monolithic pixel detector)
- The shunt regulator is composed of 126 modules (each handling 10 mA) grouped into separate domains:
  - Analog (40 modules) , Digital (50 modules), LVDS (30 modules), Charge Pump (6 modules)
- Each module is designed to handle an input current of 10mA nominally
- Two separate shunt regulators were added to polarize the Pwel and Psub of the pixel matrix

One module
Iout = 10 mA



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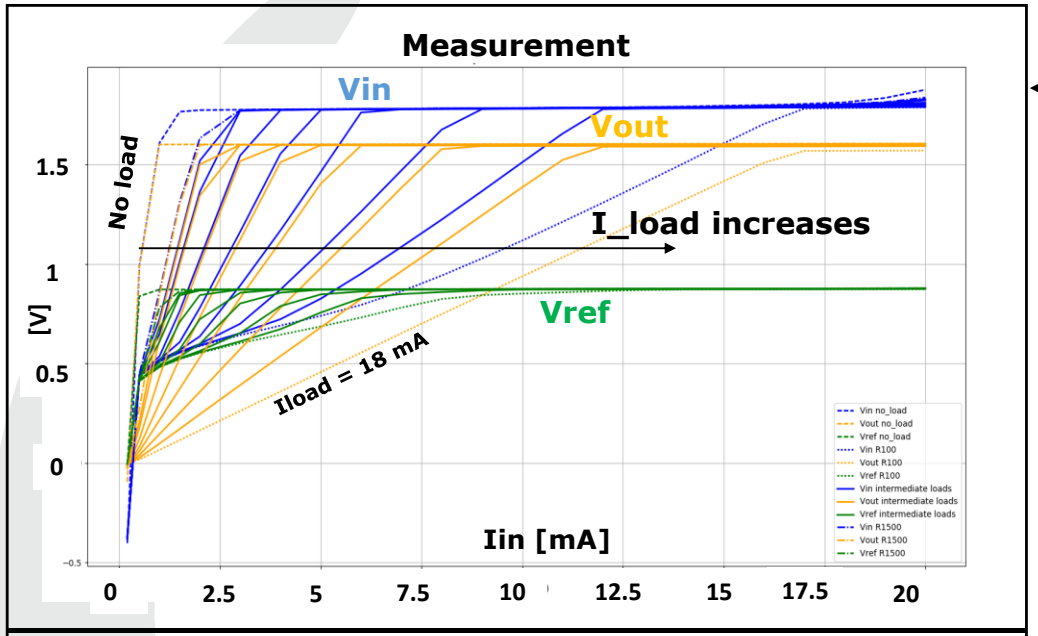
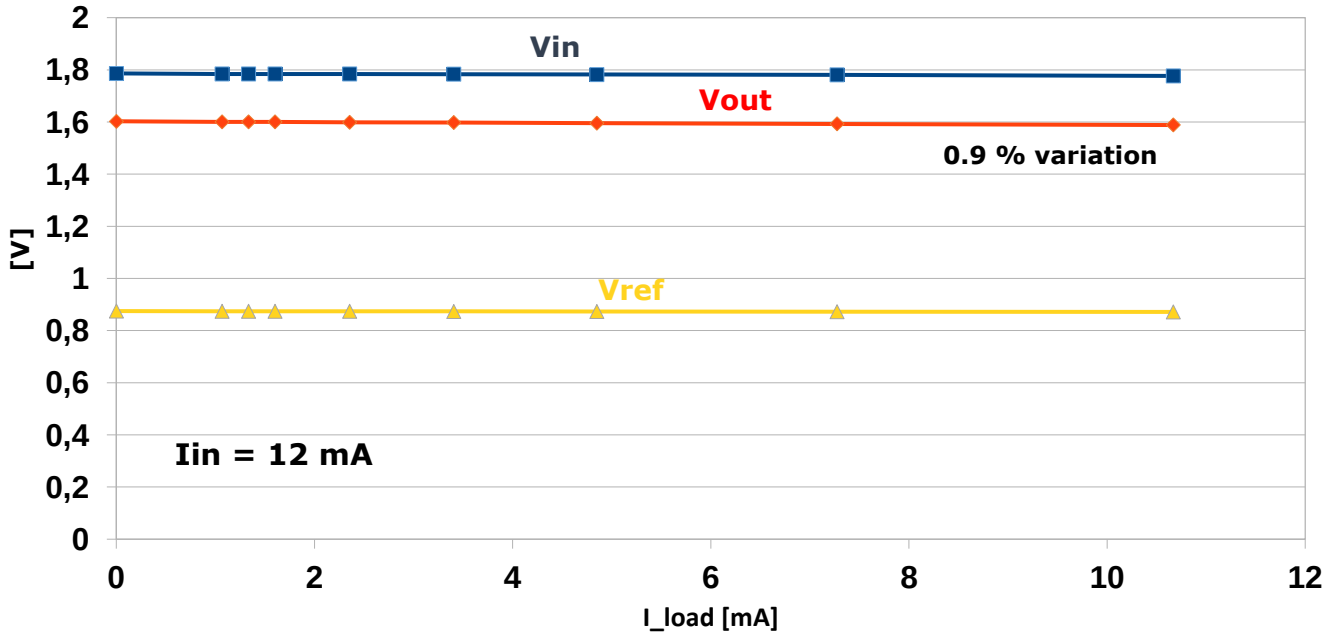
Characterization Results



A single module regulator

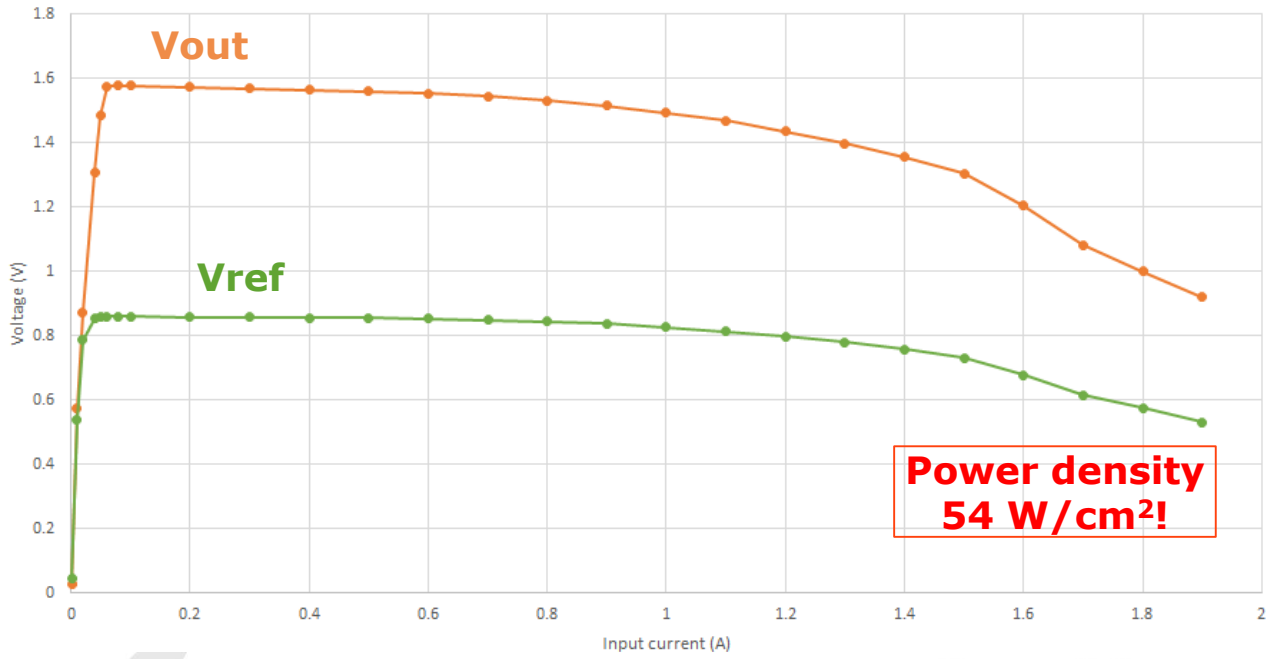
Tests carried out with the help of P. Barrillon and CPPM team



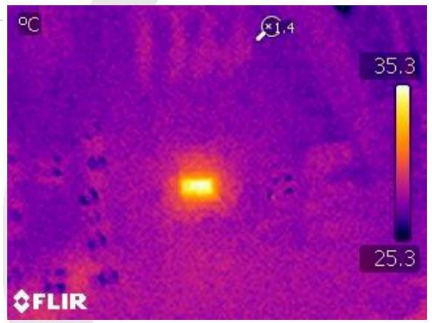
- **Regulation <1% with a constant drop-out of 200 mV**
- **Modules consumption can be adapted to the load**

Main Domain Regulator (126 modules)

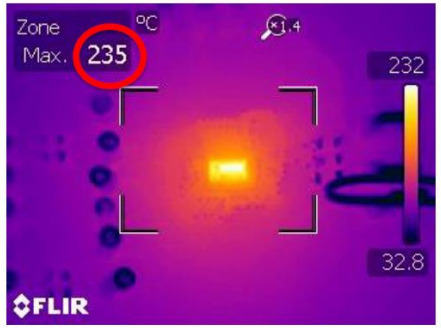
Without cooling



Low current (mA)



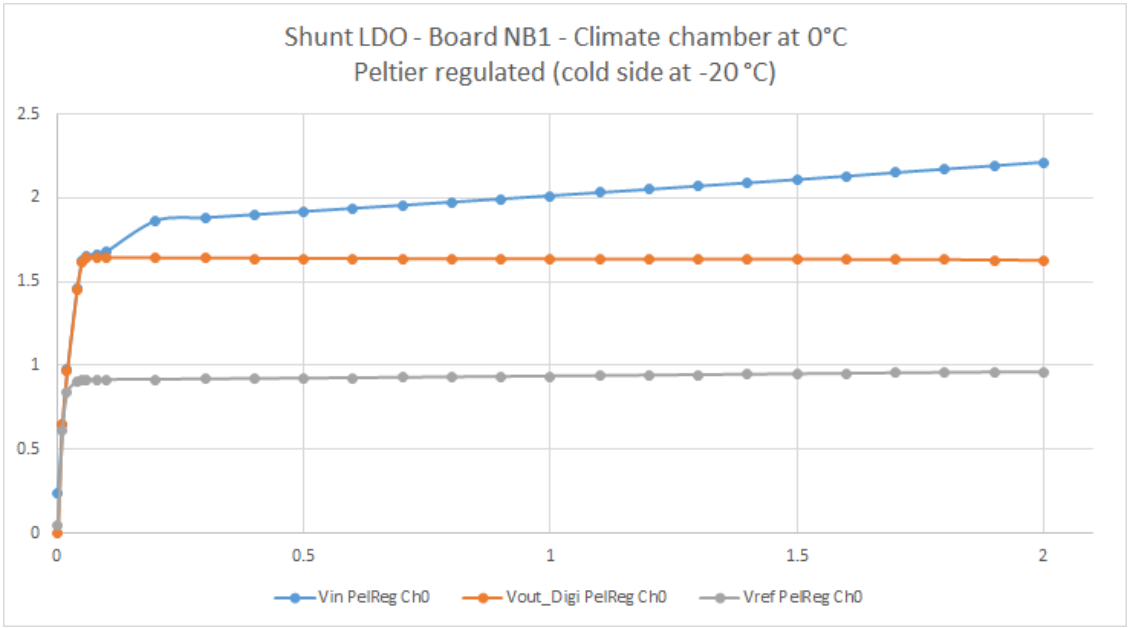
Max current (2 A)

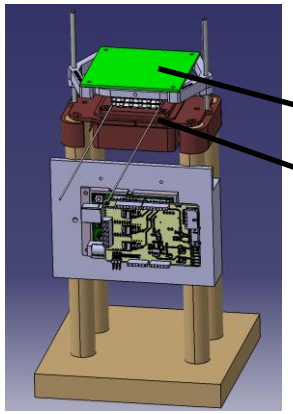


At 2A of input current, the chip consumes 4W. The chip dimension is 3,97 mm x 1,88 mm

➔ Power density = 54 W/cm²

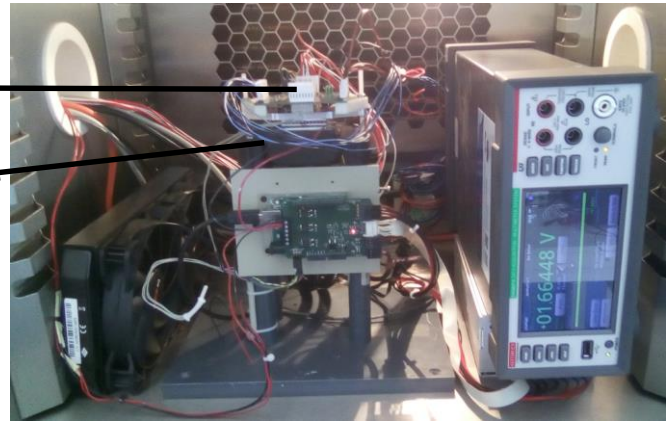
Cooling with Peltier device in a climatic chamber



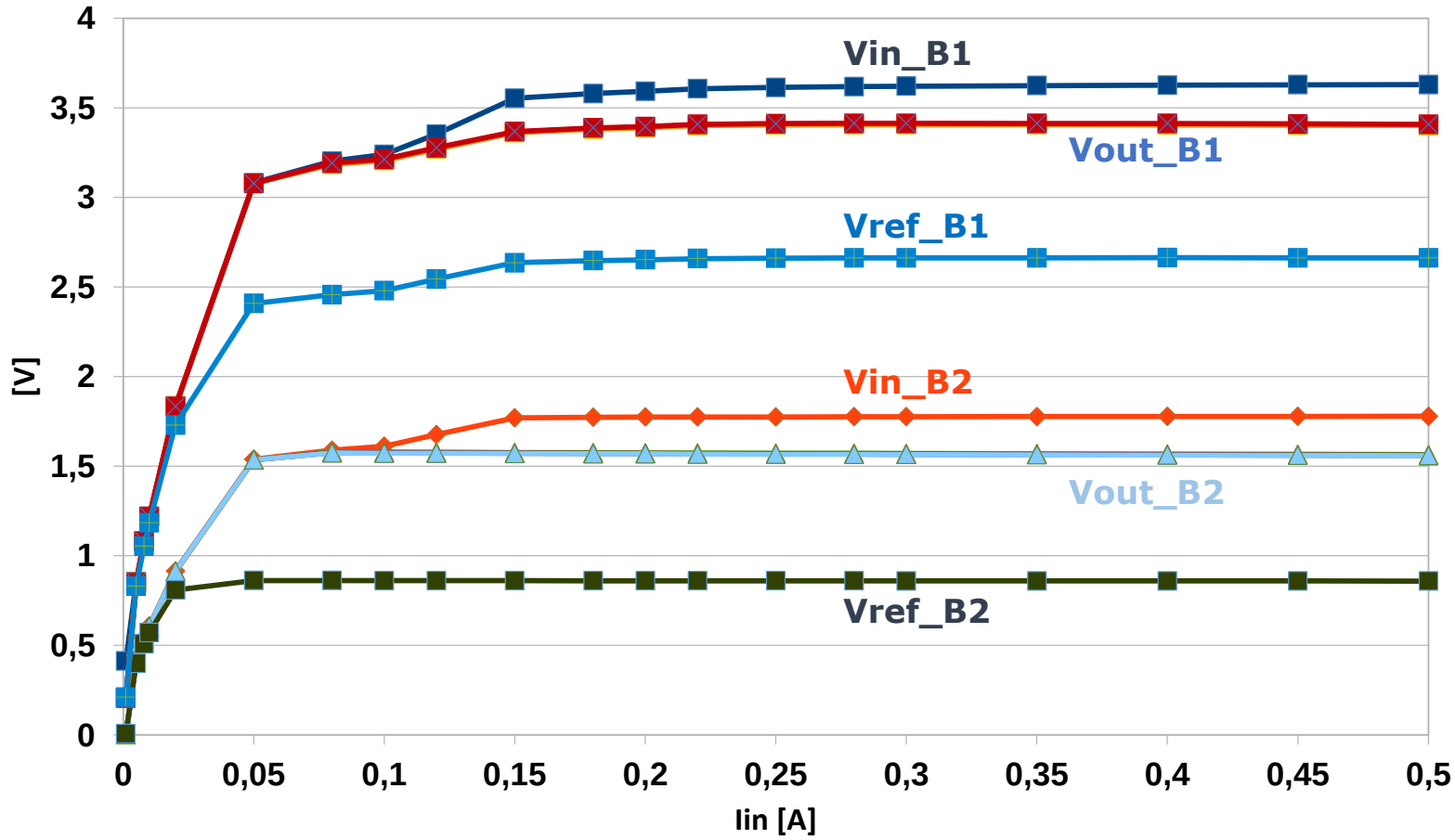


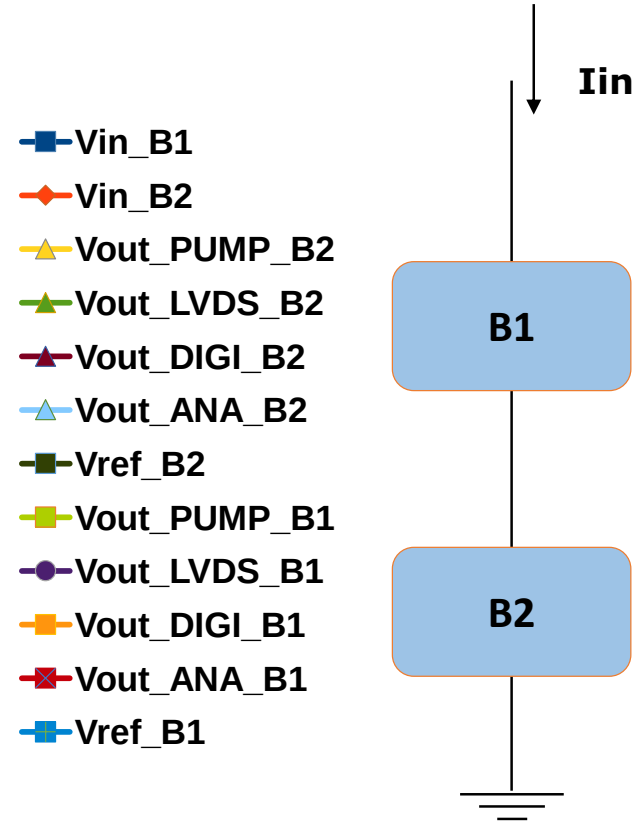
DUT

Peltier



Serial powering
2 boards in series



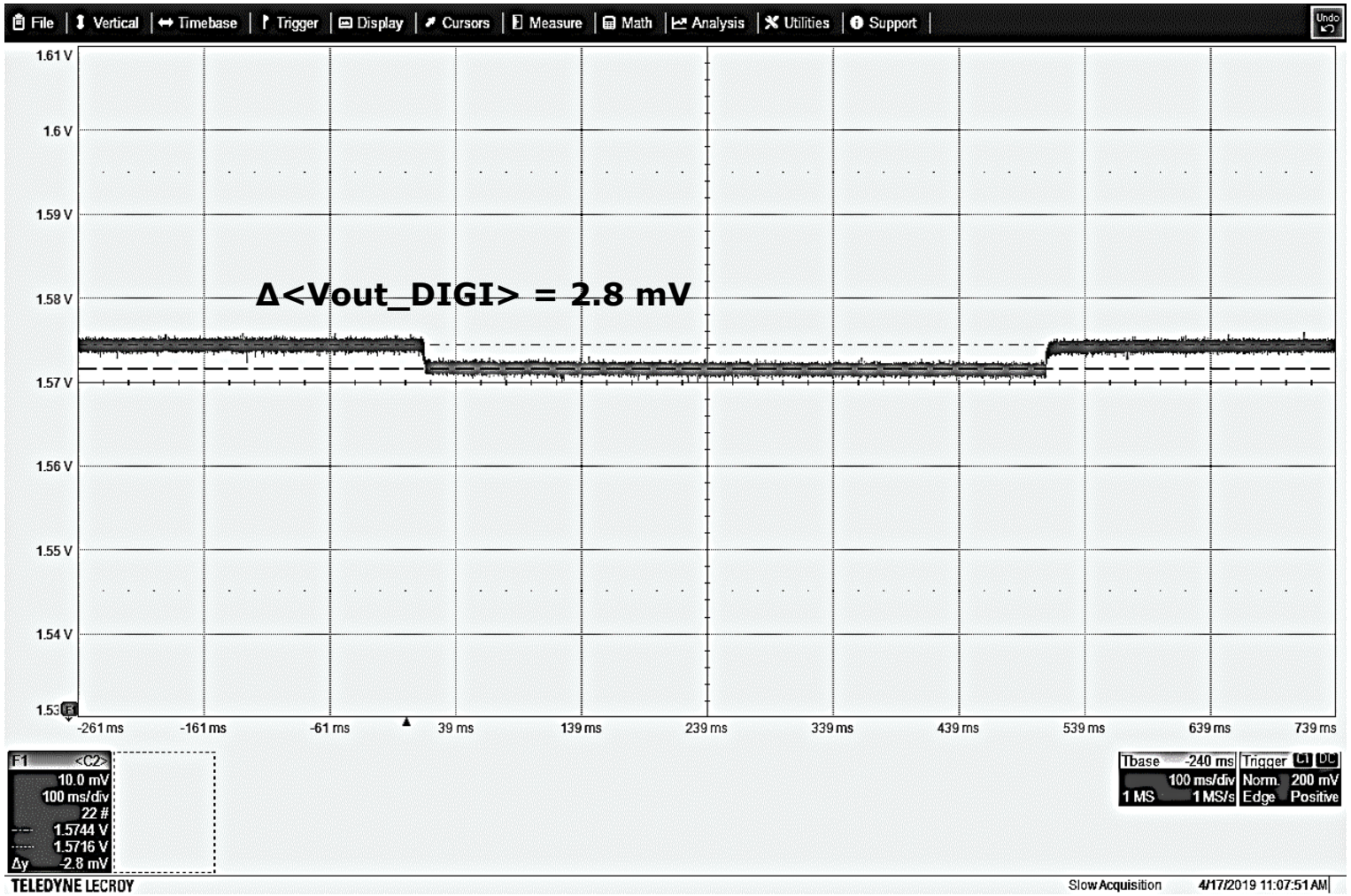


WRT a common ground

*** In lab tests were done without cooling, and current was limited to 0.5 A**

Transient test

A current step of 100 mA was drawn from the digital regulator for 500 ms using an active load
Iin = 400 mA, slew rate (max) = 5 A/µs
Off-chip cap = 10 µF is used for Vin, Vout and Vref



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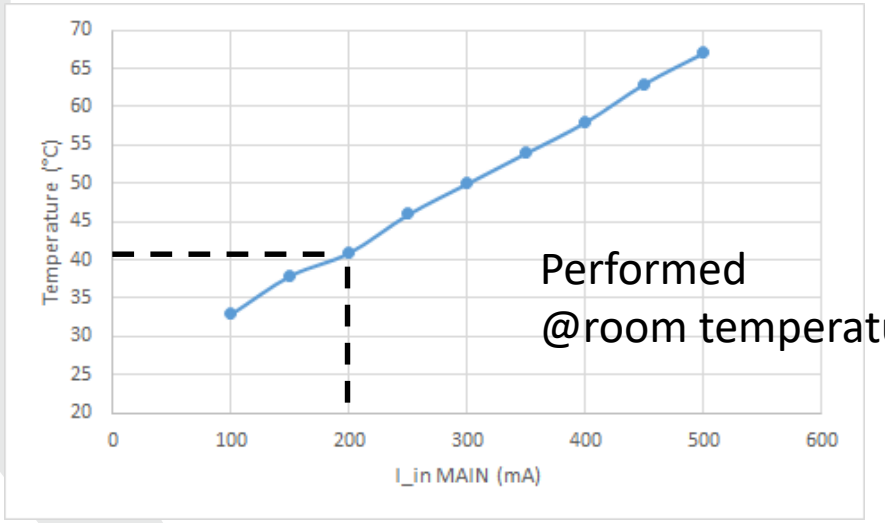
Irradiation Tests

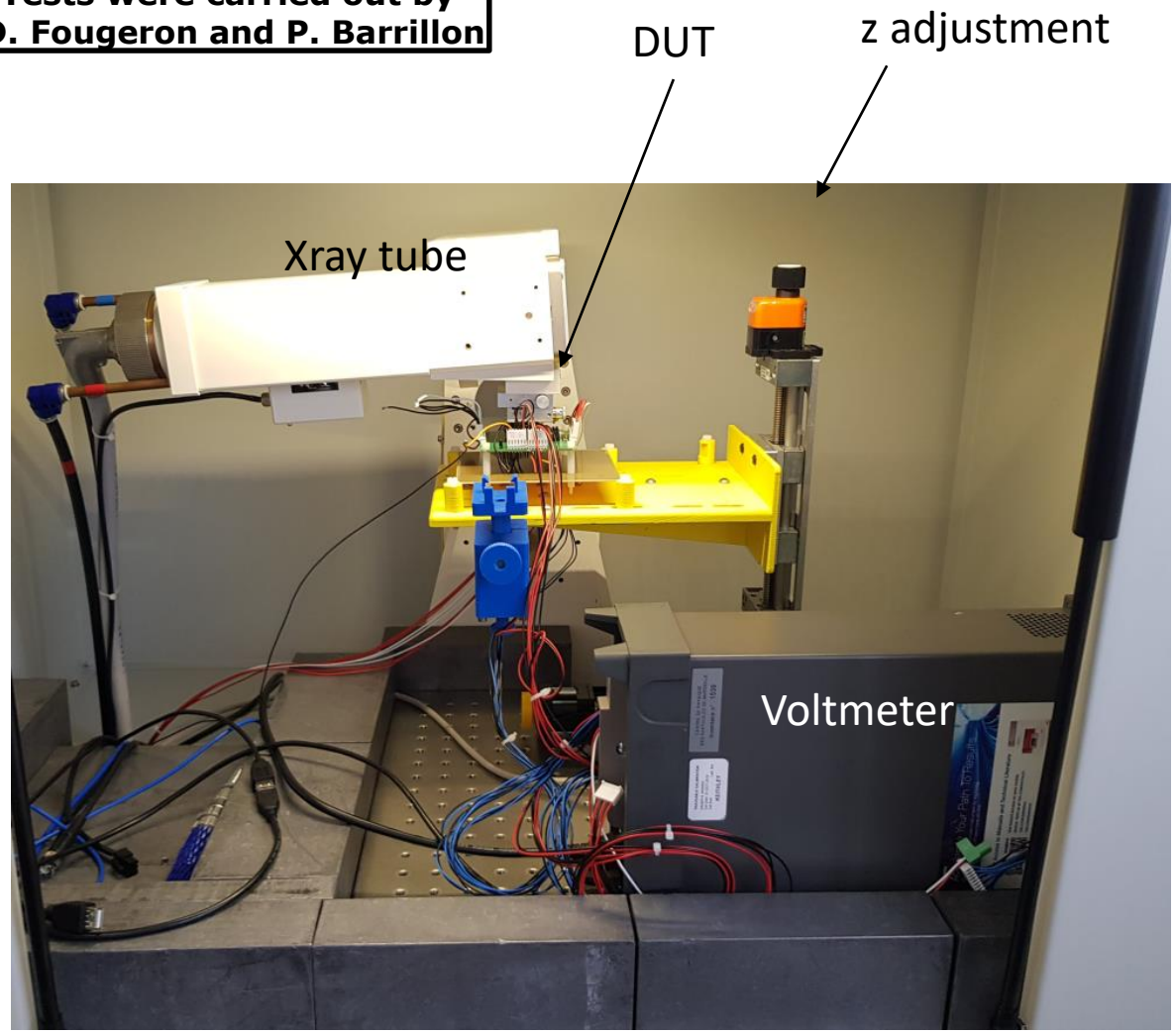
Xray machine at IM2NP
- 20 kV, 20 mA
- Dose rate: 15 krad/min
- Total Dose: 125 Mrad

Chip powered @
- **10 mA (single module)**
- **200 mA (Main Domain)**

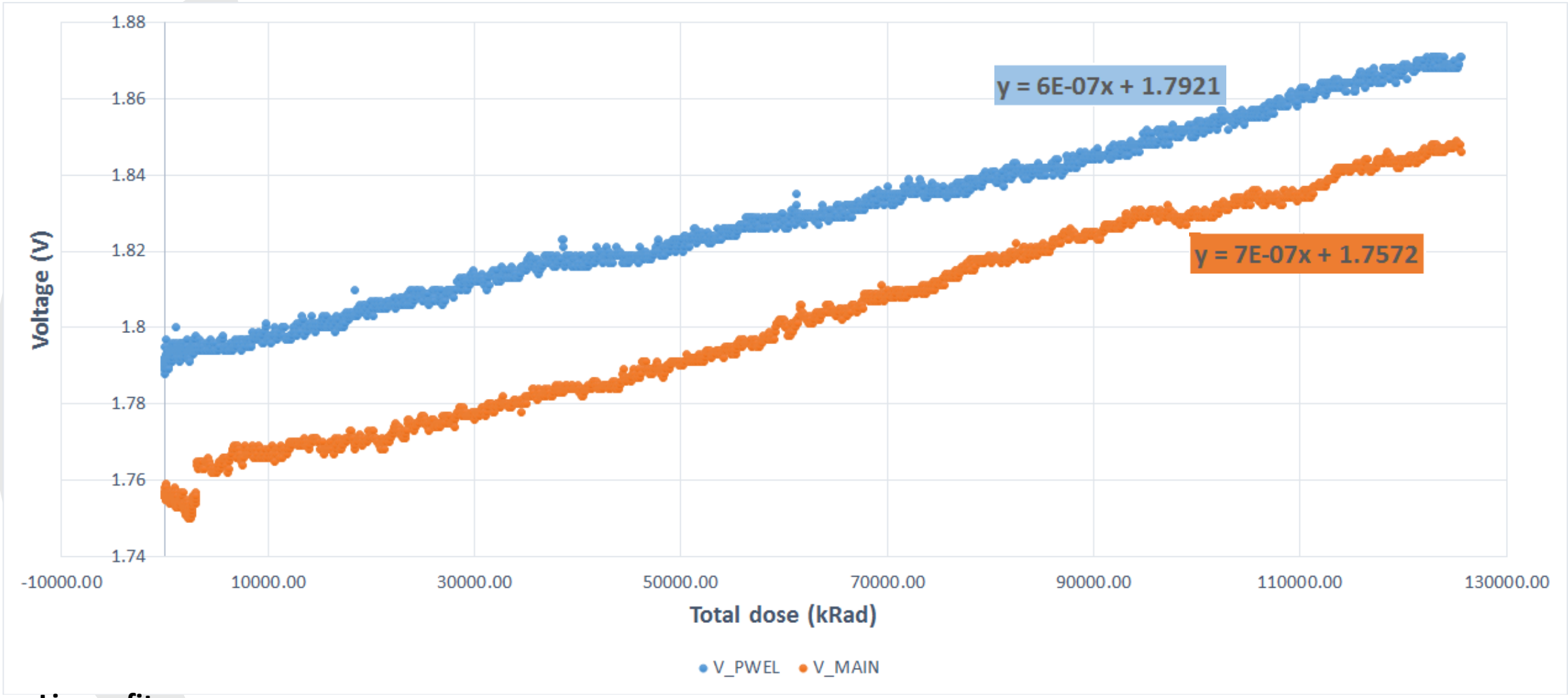
At room temperature



Tests were carried out by
D. Fougeron and P. Barrillon



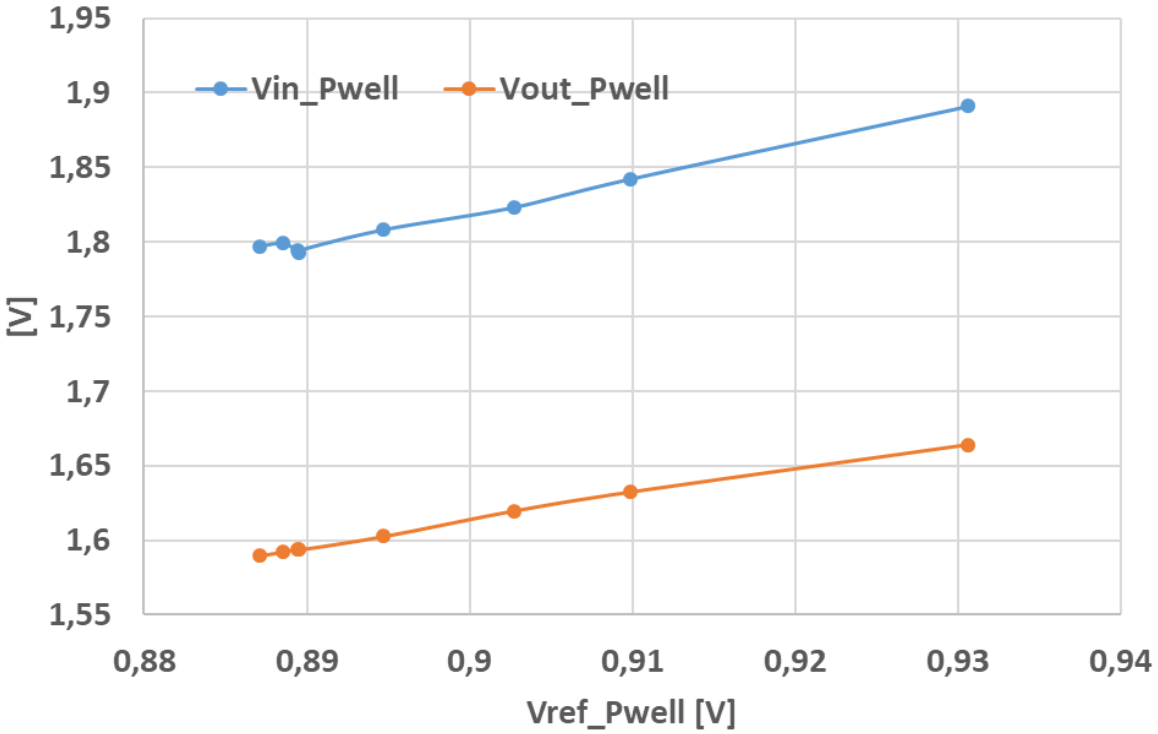
Voltage monitoring

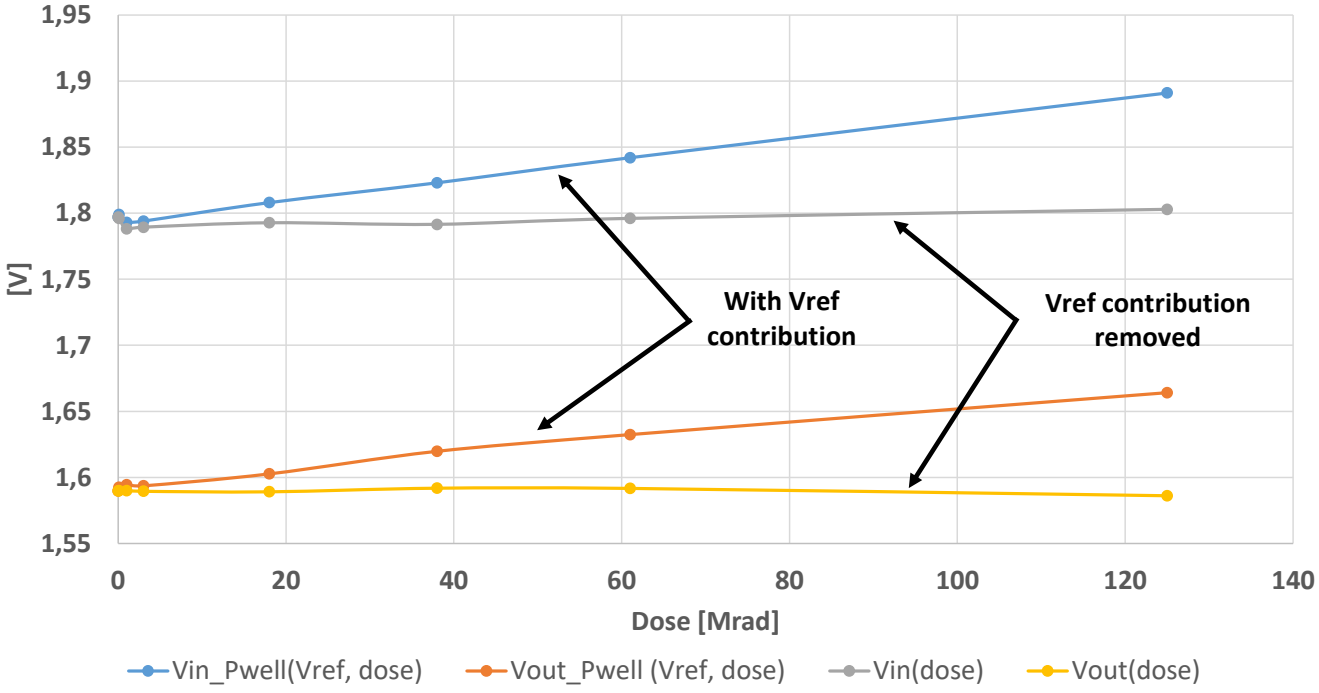


Linear fit:

- Vin_MAIN: 0.7 mV/Mrad
- Vin_PWELL: 0.6 mV/MRad

Bandgap effect





By design ➡ $Vin \propto Vref$

$Vout \propto Vref$

➔ **The output voltage variation is mainly due to the bandgap reference variation**

➔ **Intrinsic variation of the regulator output < 1%**

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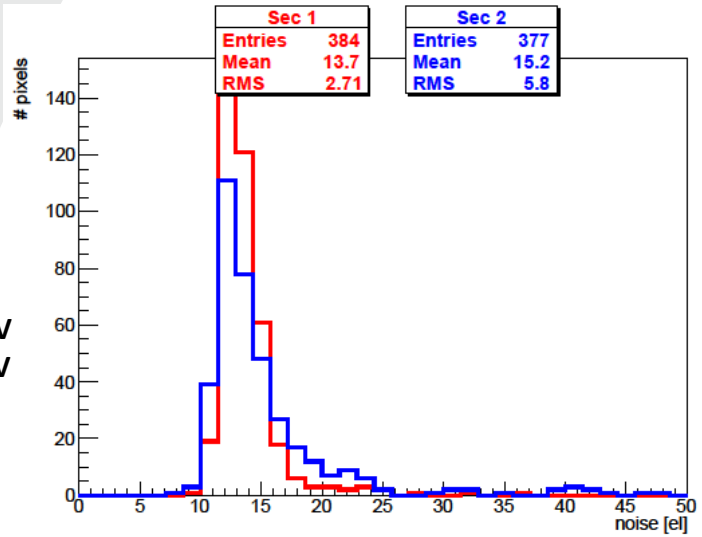
Tests with Mini-MALTA @ CERN

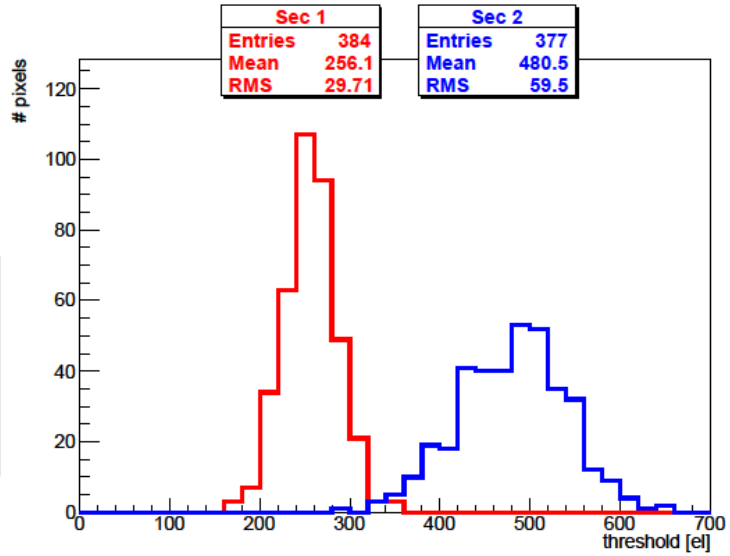
Tests carried out with the help of F. Piro

External:

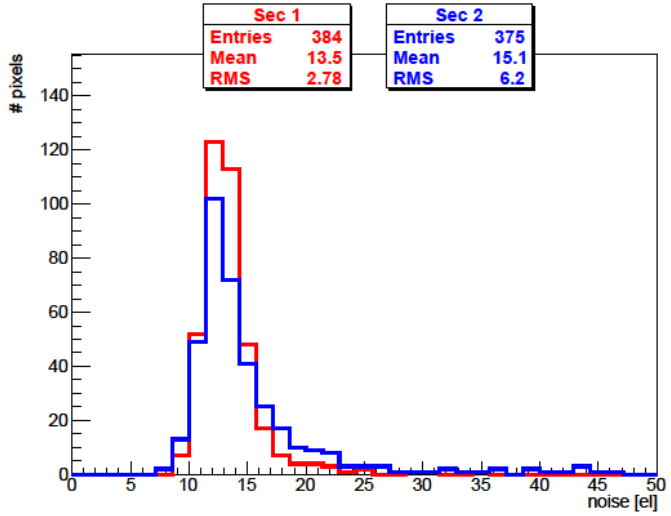
VDD_ANA = 1.8V
VDD_DIGI = 1.8V
Pwell = -2 V
Psub = -6V

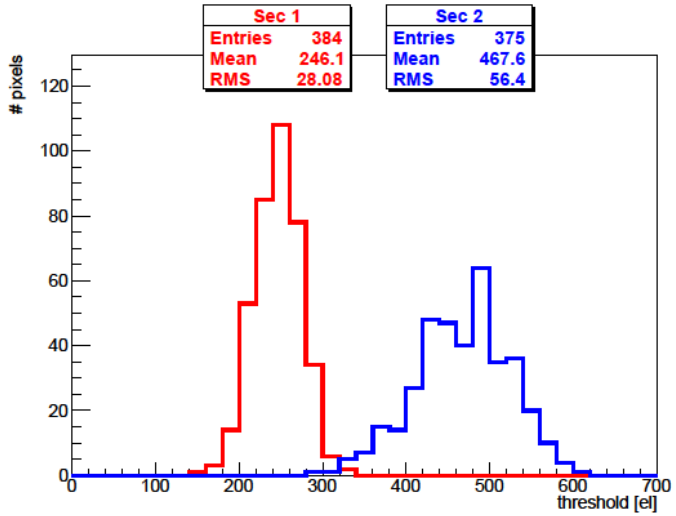
Default Settings





With Shunt Regulator





Noise

Threshold dispersion

Shunt:

VDD_ANA = 1.8V
VDD_DIGI = 1.8V
Pwell = -2 V
Psub = -2

Note:

Pwell and Psub voltages are generated by the same regulator 'Pwell' shifted by -2 V WRT the Main Domain

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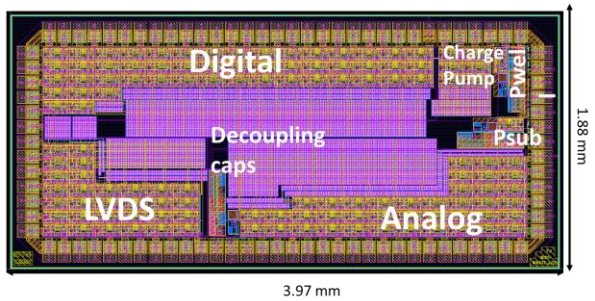
Summary

- **Serial powering increases power efficiency and reduces material budget, an important factor for large detectors such as ATLAS ITK**
- **A shunt regulator was developed in TJ180 technology, in a modular structure that can be arranged in many separate power domains**
- **Electrical characterization measurement shows a response similar to that of simulations with a regulation within 1% for the full range of load values.**
- **The regulator was tested successfully in serial mode.**
- **The test chip was irradiatied up to 125 Mrad, and the results show a deviation of Vin of about 0.6 mV/Mrad which was found to be mainly due to bandgap variation. The regulator intrinsic variation WRT to radiation is <1%**
- **The Mini-Malta chip was operated with the shunt regulator, and measurements show no degradation of noise or threshold dispersion, with respect to the default powering settings.**

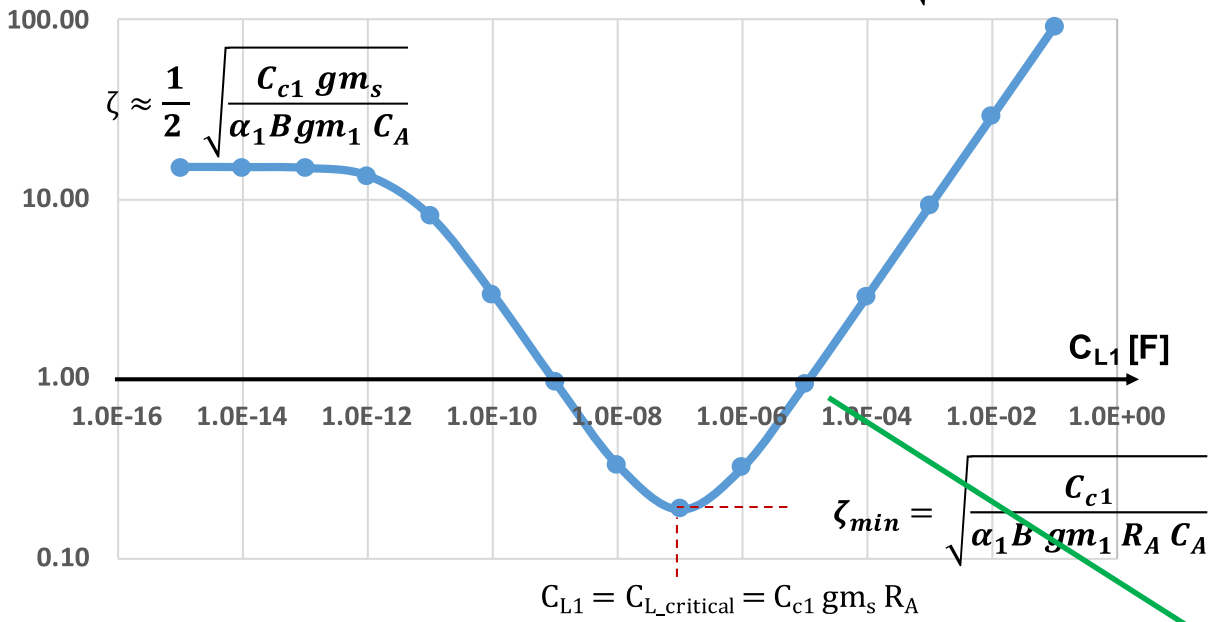


Backup

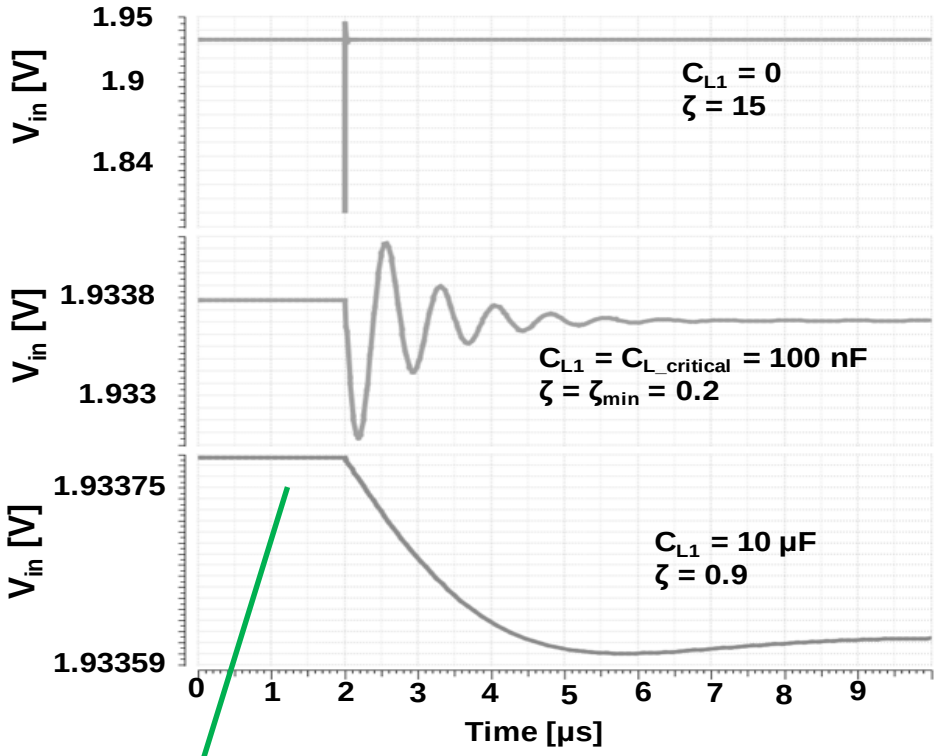
Modeling and simulation

Daming Factor (ζ)

$$\zeta \approx \frac{1}{2\,R_A}\sqrt{\frac{C_{L1}}{\alpha_1\, gm_s\, B\, gm_1\, C_A}}$$



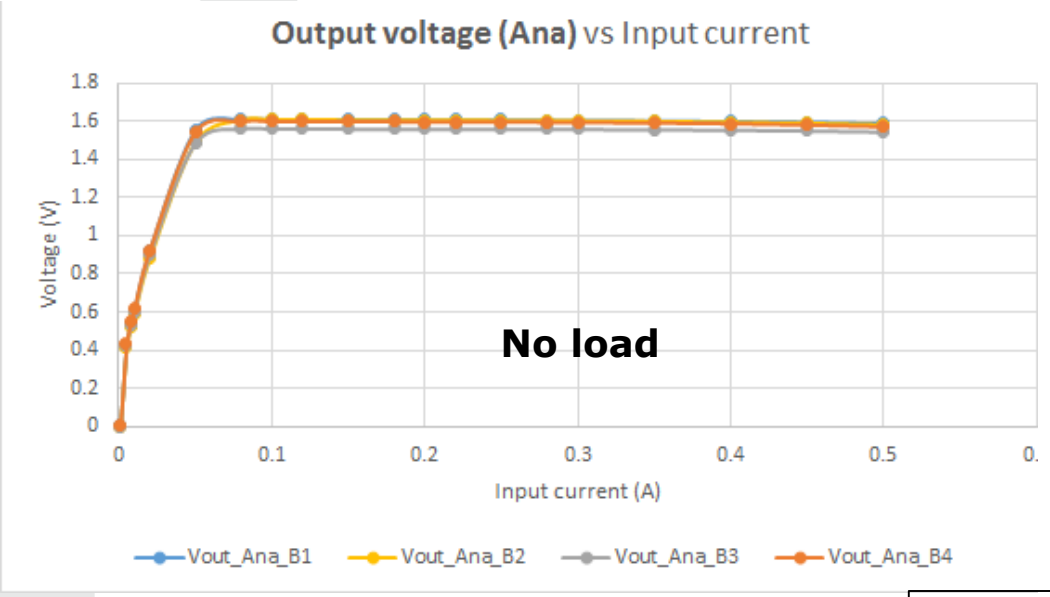
Transient response to a current pulse of 1 mA

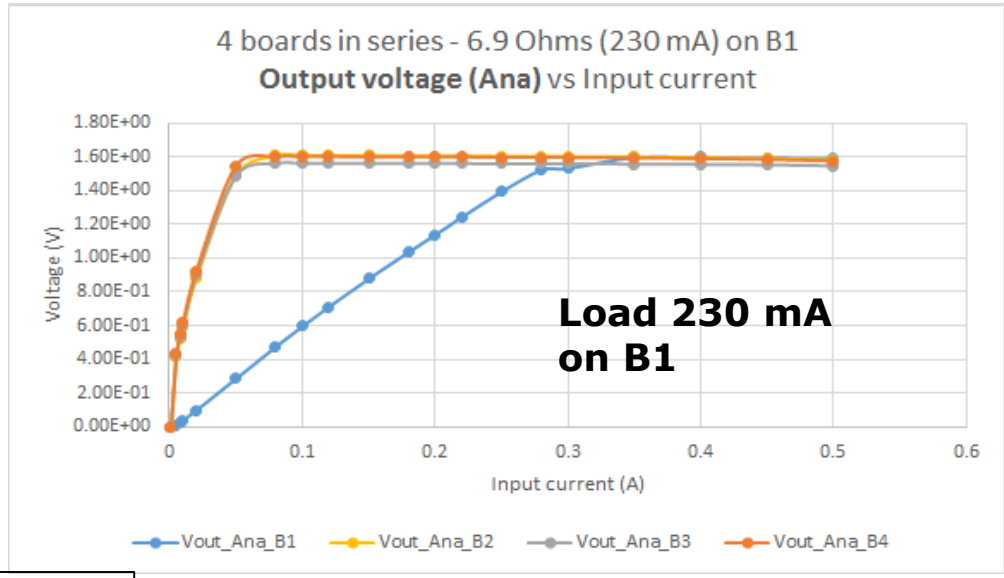


$$\frac{V_{out}}{I_{load}} = -R_0\,\frac{\left[1+\frac{s}{z_1}\right]}{1+\,2\zeta\frac{s}{\omega_0}+\frac{s^2}{\omega_0}}$$

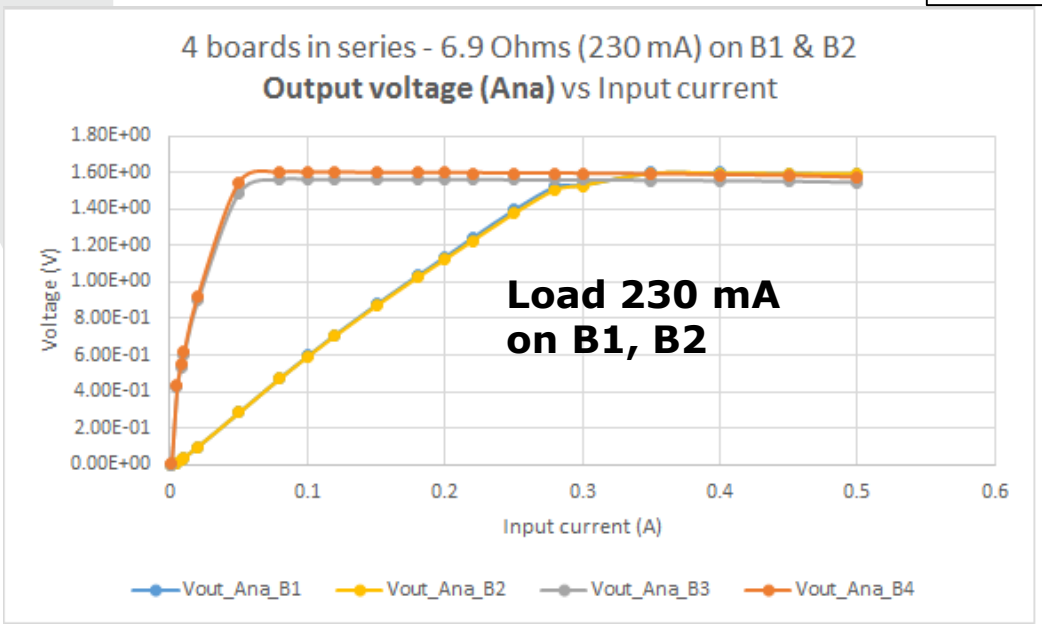
The regulator is designed to be stable for all output capacitance values, but it best operates with an off-chip relatively large capacitor

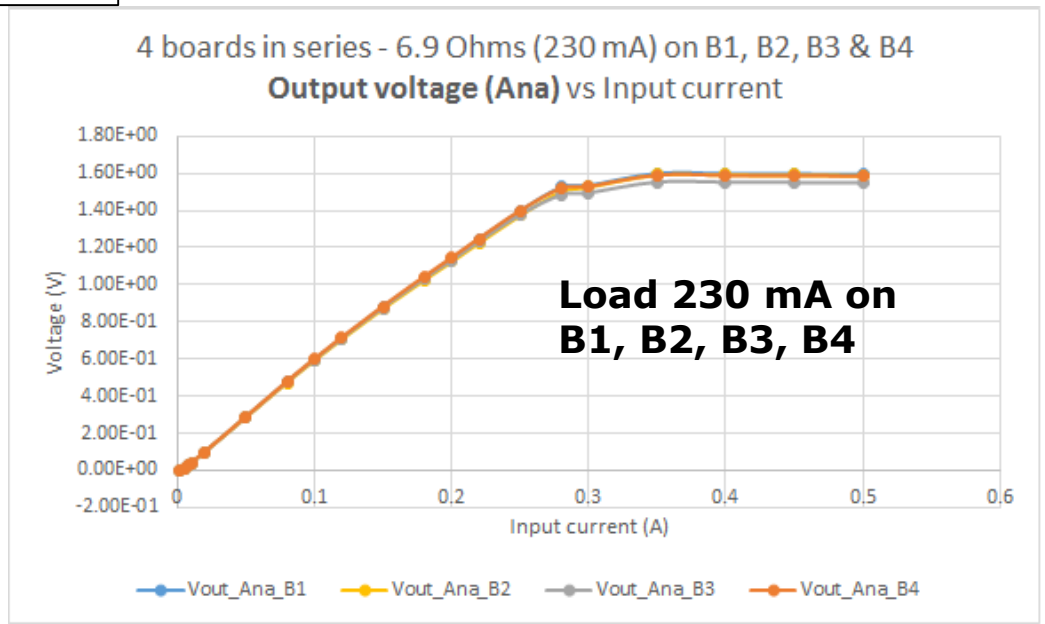
Serial Powering
4 boards in series: B1, B2, B3, B4



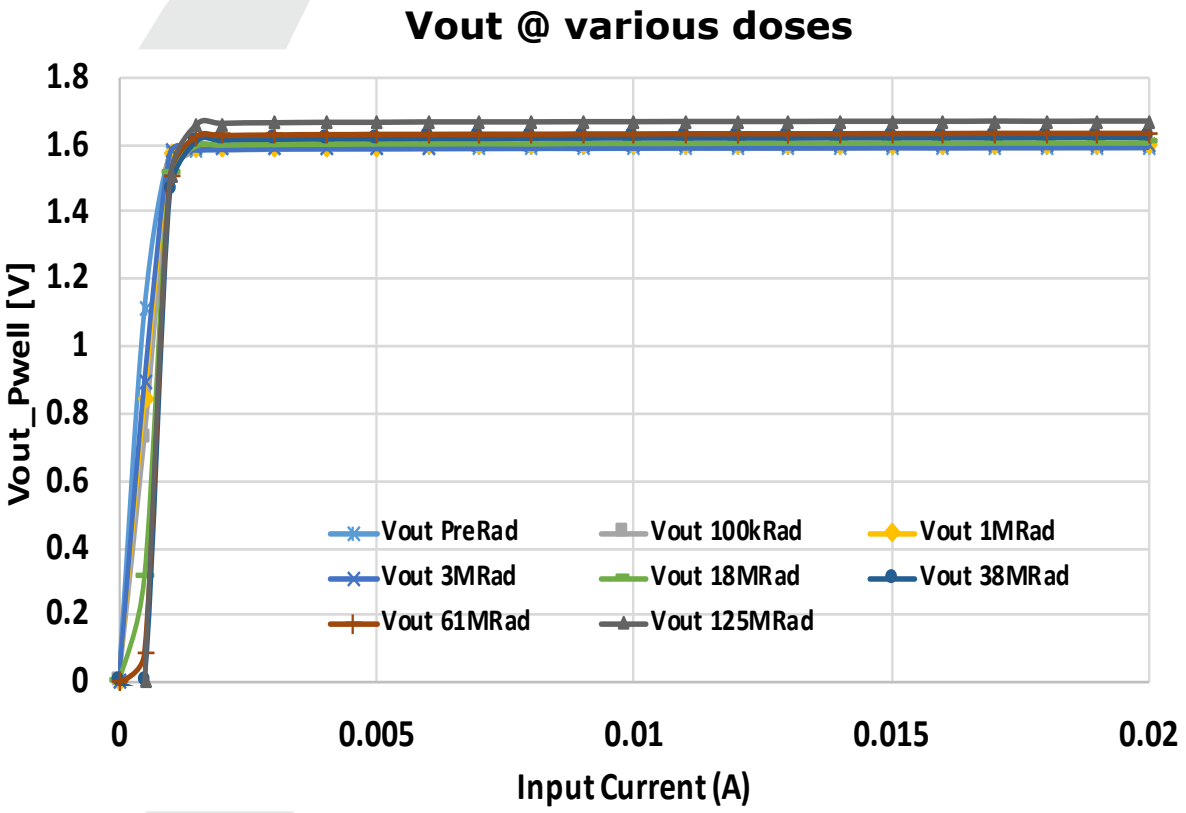


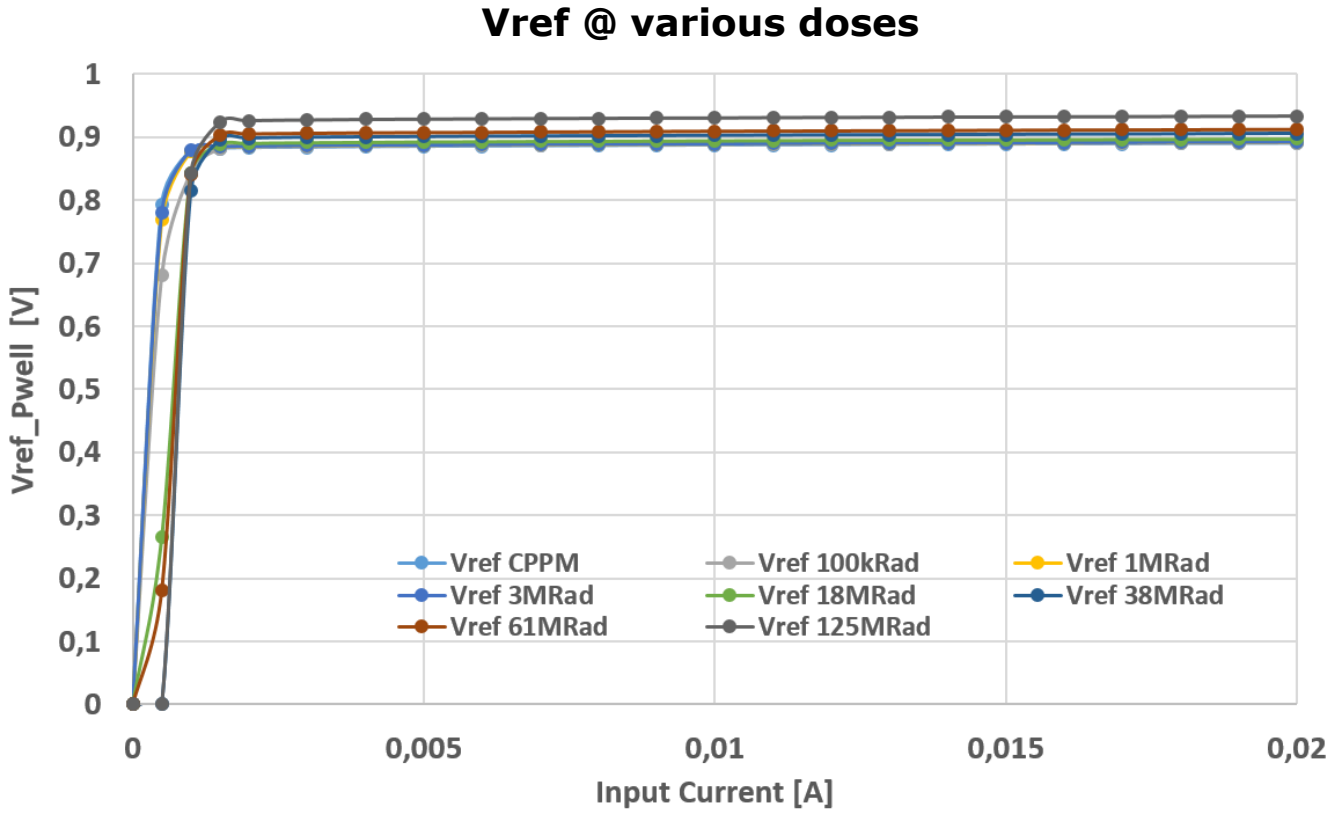
WRT a relative ground



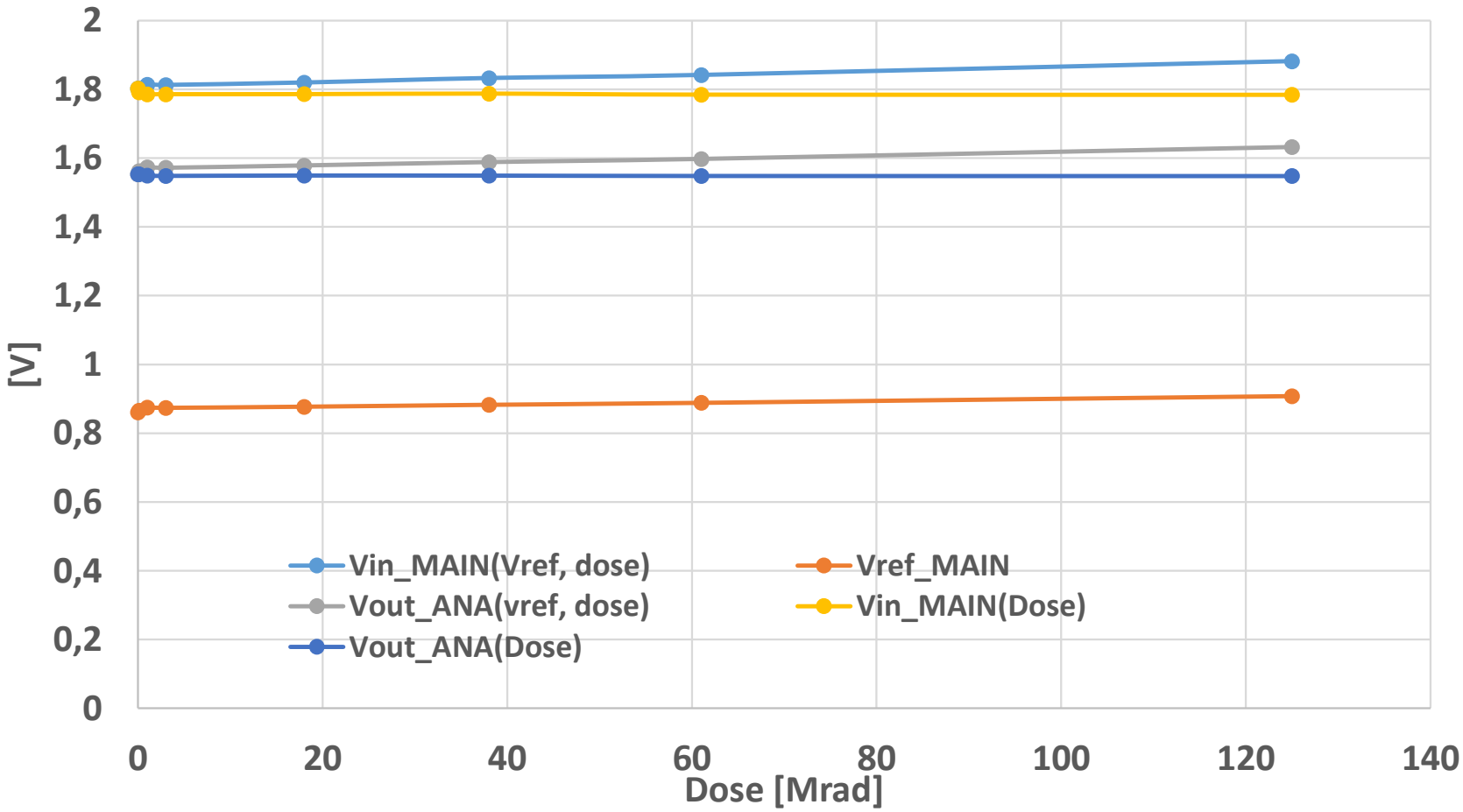


A single module



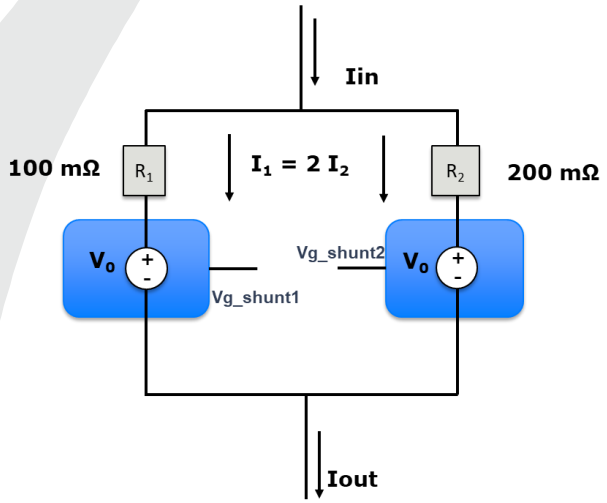


Main domain

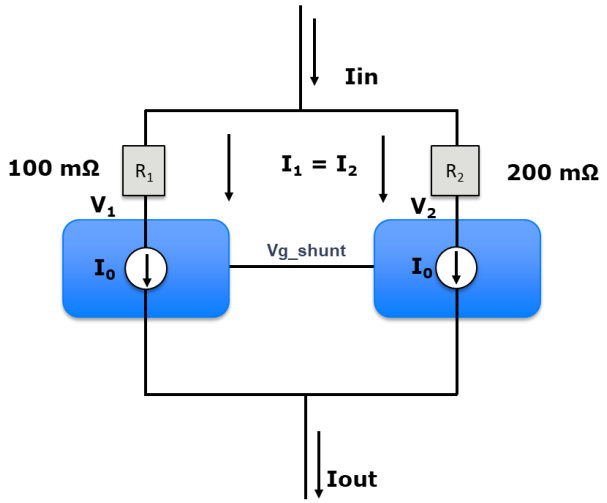

2
1,8
1,6
1,4
1,2
1
0,8
0,6
0,4
0,2
0
[V]
0
20
40
60
80
100
120
140
Dose [Mrad]
Vin_MAIN(Vref, dose)
Vout_ANA(vref, dose)
Vout_ANA(Dose)
Vref_MAIN
Vin_MAIN(Dose)

Regulators in parallel

Vg_shunt separate

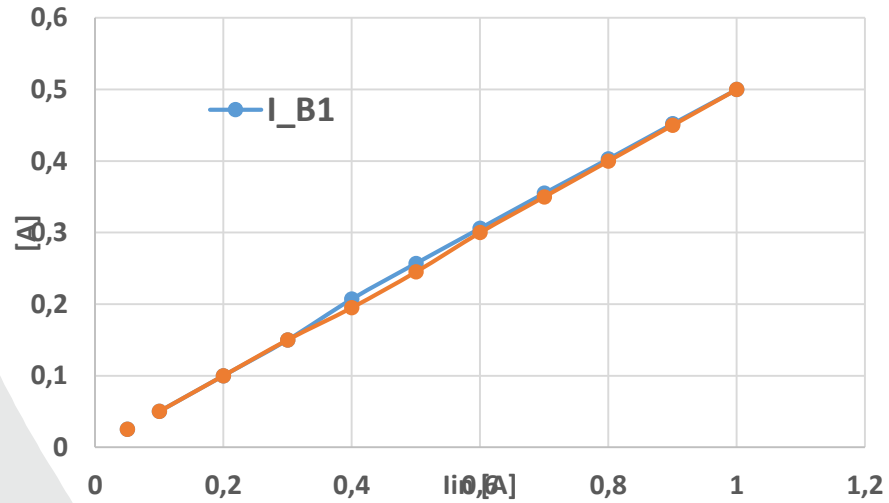


Vg_shunt common

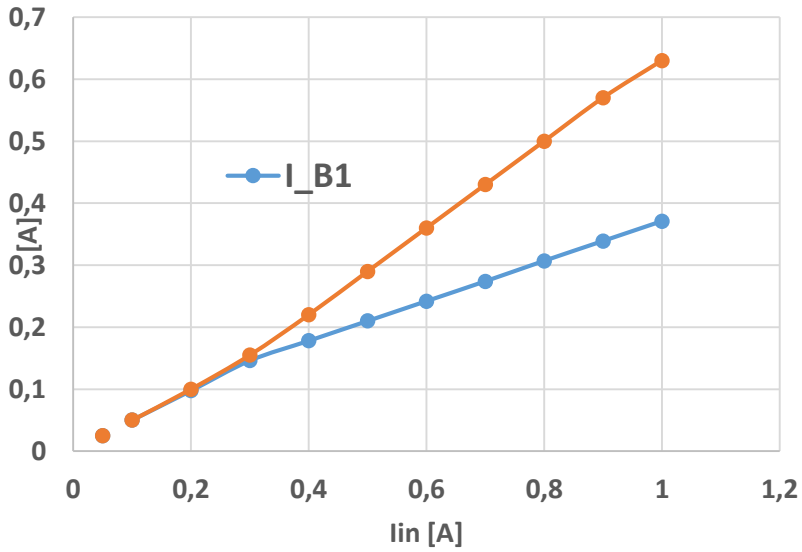


Current distribution is sensitive to setup asymmetries in parallel configuration

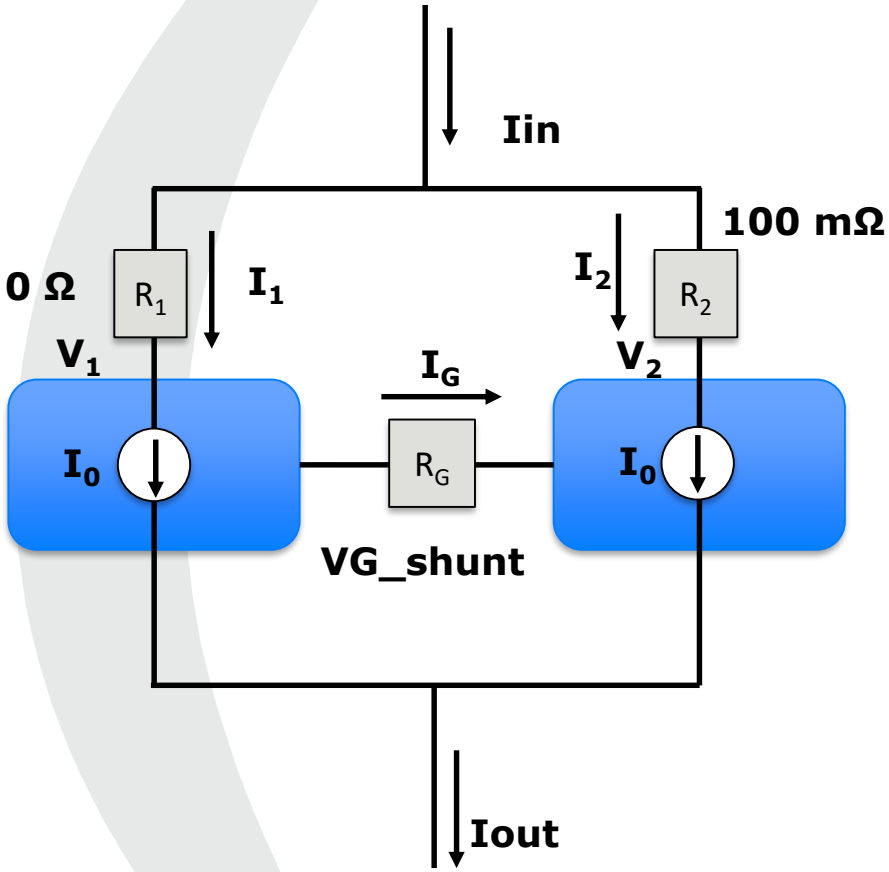
Symmetrical setup

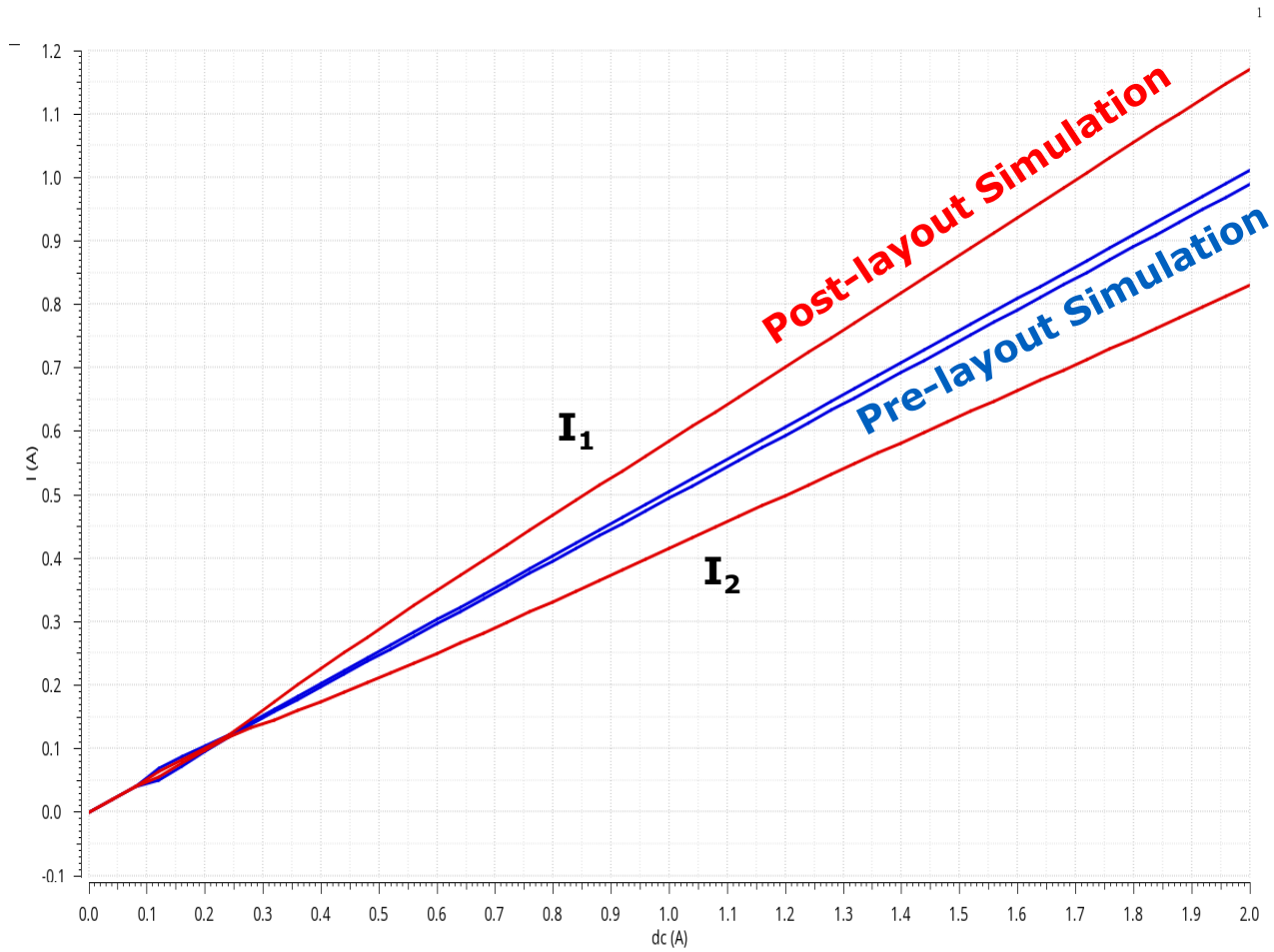


Deliberately introducing a mismatch of 100 mΩ



Parallel powering

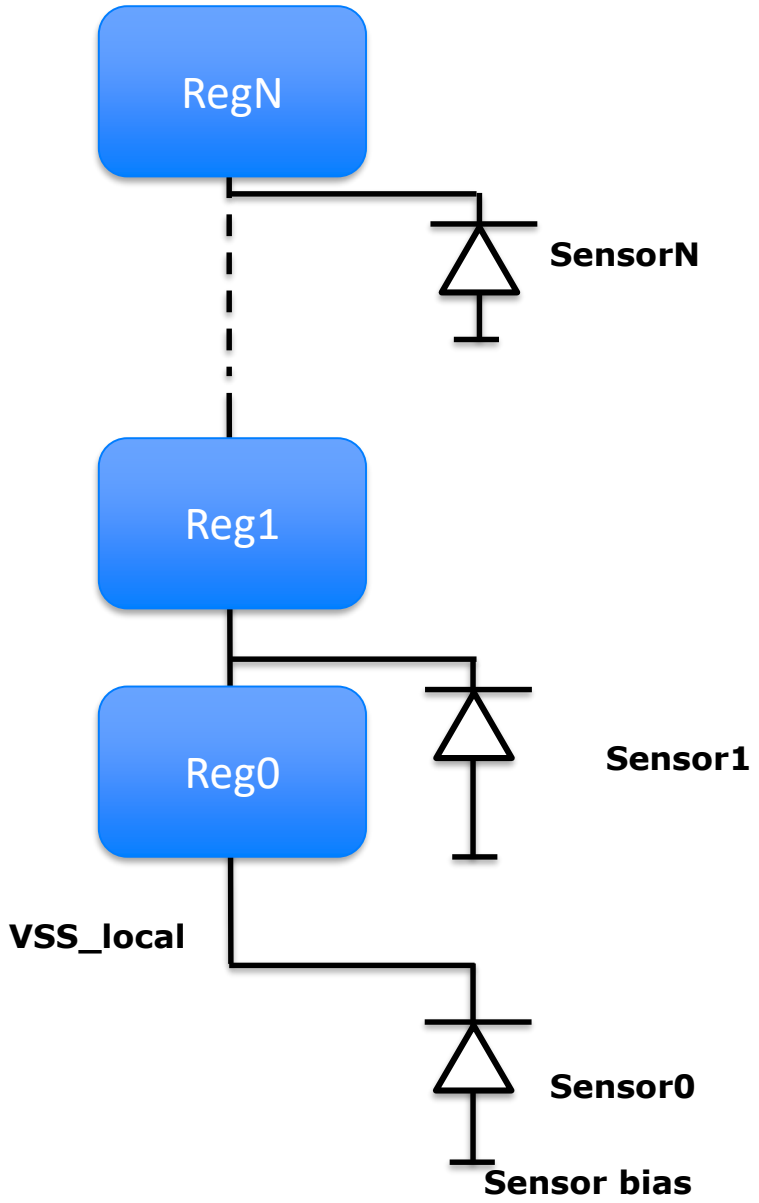


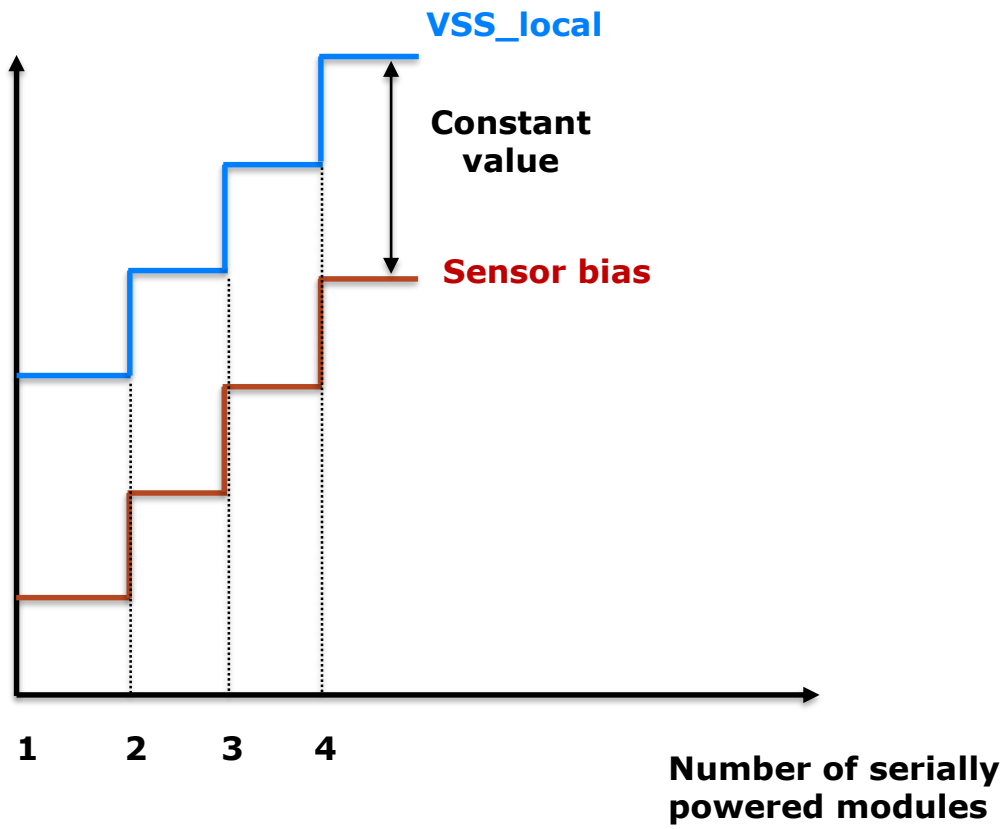


Rg is implemented with a thin metal layer
0.5 µm wide; Resistivity = 80 mΩ/□
Module = 100µm x 200 µm
Rg ≈ 10 Ω/module

Initial simulations show that a decrease by a factor of 10 of Rg should be sufficient
0.5 µm width ➔ 5 µm width

Sensor Bias

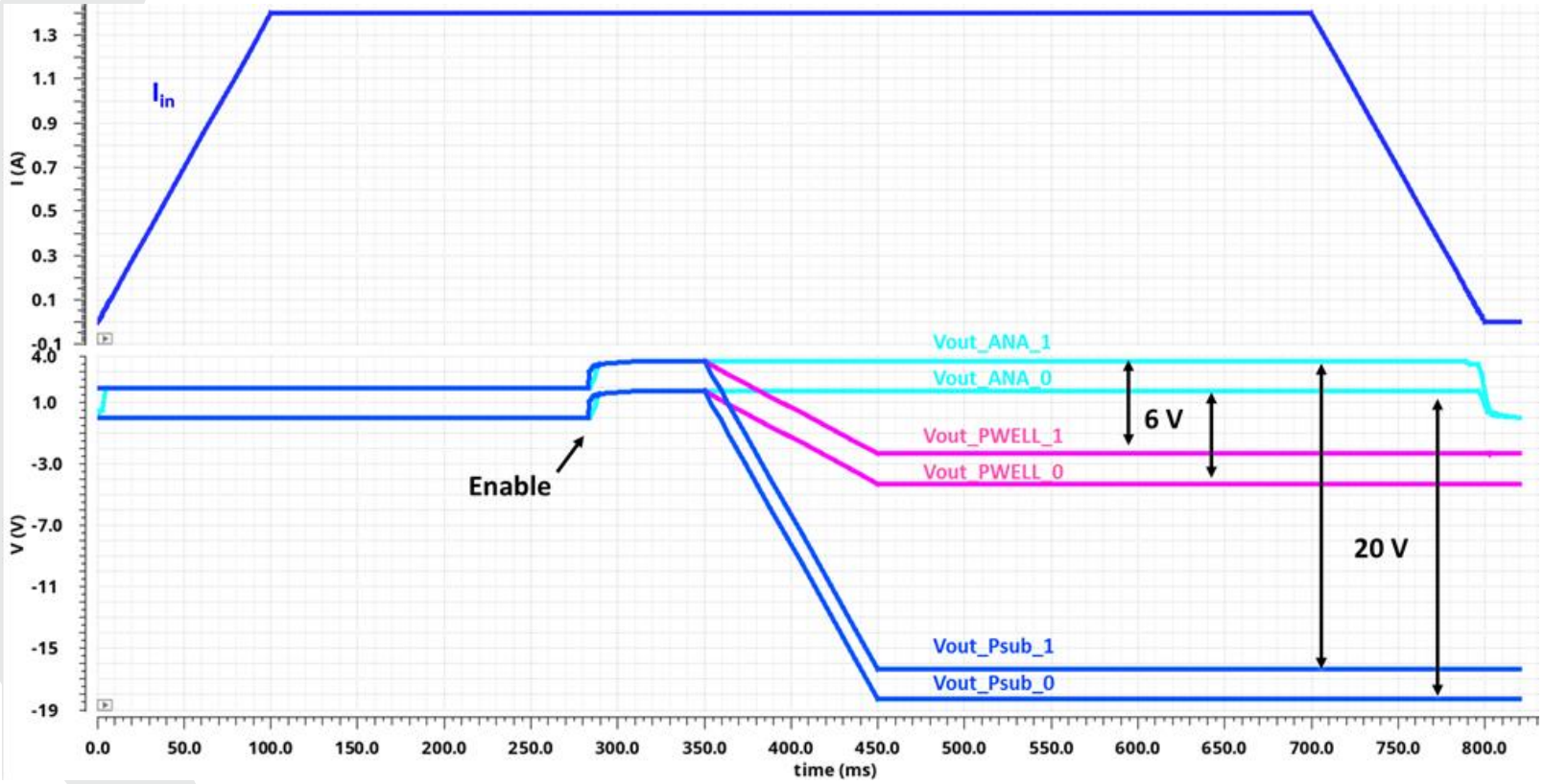


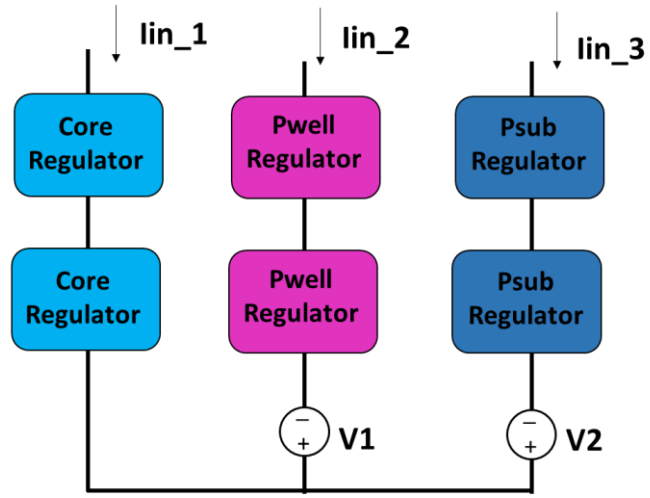


Sensor bias cannot be a contact voltage. It remain constant with respect to the module's relative ground

Shifted Regulators

- **Idea: shifting the floating ground of Pwell and Psub regulators with respect to Module regulator**





Analytic study to remove Vref contribution

$$dV_{in}(V_{ref}, Dose) = \frac{\partial V_{in}}{\partial V_{ref}} dV_{ref} + \frac{\partial V_{in}}{\partial Dose} dDose$$

→ ce qu'on cherche

$$\frac{\partial V_{in}}{\partial Dose} dDose = dV_{in} - \frac{\partial V_{in}}{\partial V_{ref}} dV_{ref}$$

$$\frac{\partial V_{in}}{\partial Dose} = \frac{dV_{in}}{dDose} - \frac{\partial V_{in}}{\partial V_{ref}} \frac{dV_{ref}}{dDose}$$

$$\alpha = \frac{R_1}{R_1+R_2} = \frac{V_{in}}{V_{ref}}\Big|_{Dose=0}$$

$$\frac{\partial V_{in}}{\partial Dose} = \frac{dV_{in}}{dDose} - \alpha \frac{dV_{ref}}{dDose}$$

$$\frac{\partial V_{in}}{\partial Dose} = \frac{d(V_{in} - \alpha V_{ref})}{dDose} = \frac{d(V_{in}')}{dDose}$$

$$\boxed{V_{in}' = V_{in} - \alpha V_{ref}}$$

$$V_{in}(Dose) = V_{in}(Dose=0) + \frac{\partial V_{in}}{\partial Dose} dDose$$

$$= V_{in_0} + \frac{dV_{in}'}{dDose} dDose$$

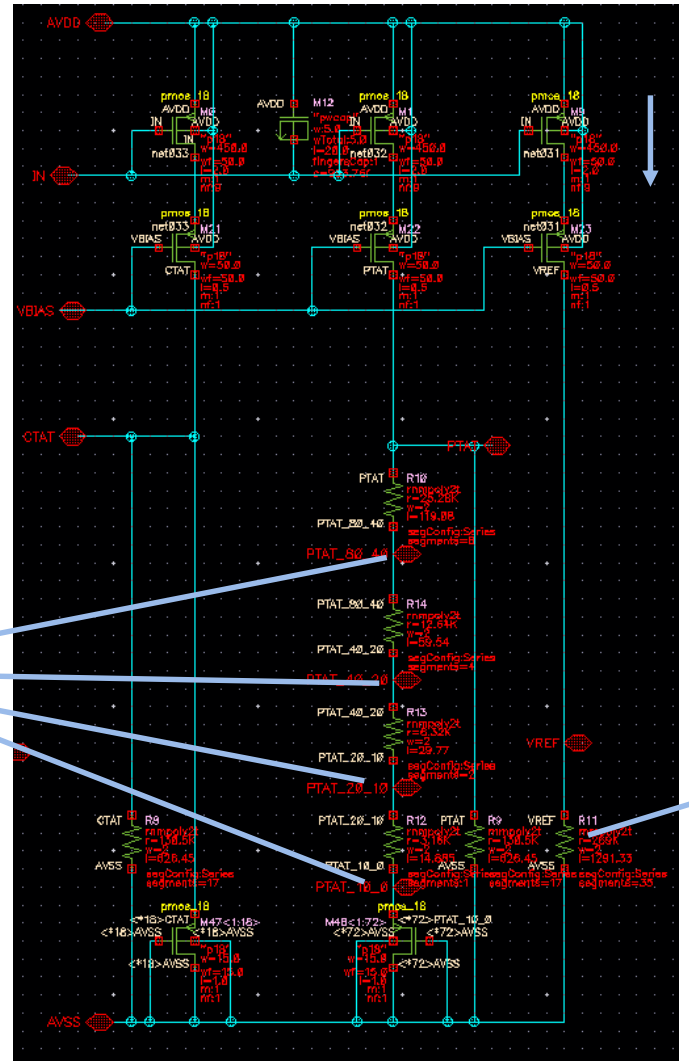
$$\boxed{V_{in}(Dose) = V_{in_0} + dV_{in}'}$$

Bandgap

Bandgap was designed to have a nominal value of 1 V and a few calibration points for voltage adjustments.

Measurements show that

- **Nominal voltage= 858 mV**
- **When all points of calibration shorted → Vout = 953 mV**



Iout = 3.6 µA

Calibration points

Rout = 270 kΩ