RD53 chip progress

Pierre Barrillon, Denis Fougeron, Eva Joly, Mohsine Menouni, Thomas Strebler

CPPM - Aix-Marseille Univ, France

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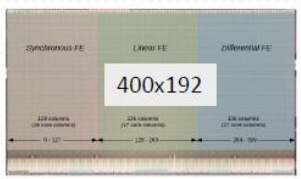
Outline

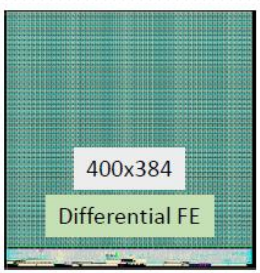
- RD53 project
- RD53 chip architecture
- RD53B-ATLAS testing
- **Radiation hardness**
  - TID testing
  - SEU strategy and testing
- Summary and Conclusion

RD53 project

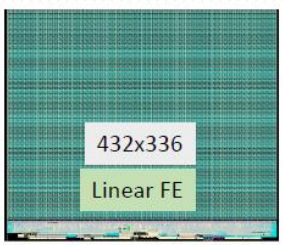
- 24 collaborating institutes - ~20 designers
- Design and develop pixel chips for **ATLAS/CMS phase 2 upgrades**
- Extremely challenging requirements for HL-LHC
  - Hit rates: 3 GHz/cm², Small pixels: 50 x 50 µm²
  - Radiation : **500 Mrad** - 10^{16} neq/cm² over 5 years
- Technology : **65nm CMOS**



RD53A
Size: 20 x 11.5 mm²
submitted in August 2017



RD53B-ATLAS (ITkPix_V1)
size: 20 x 21 mm²
submitted in March 2020

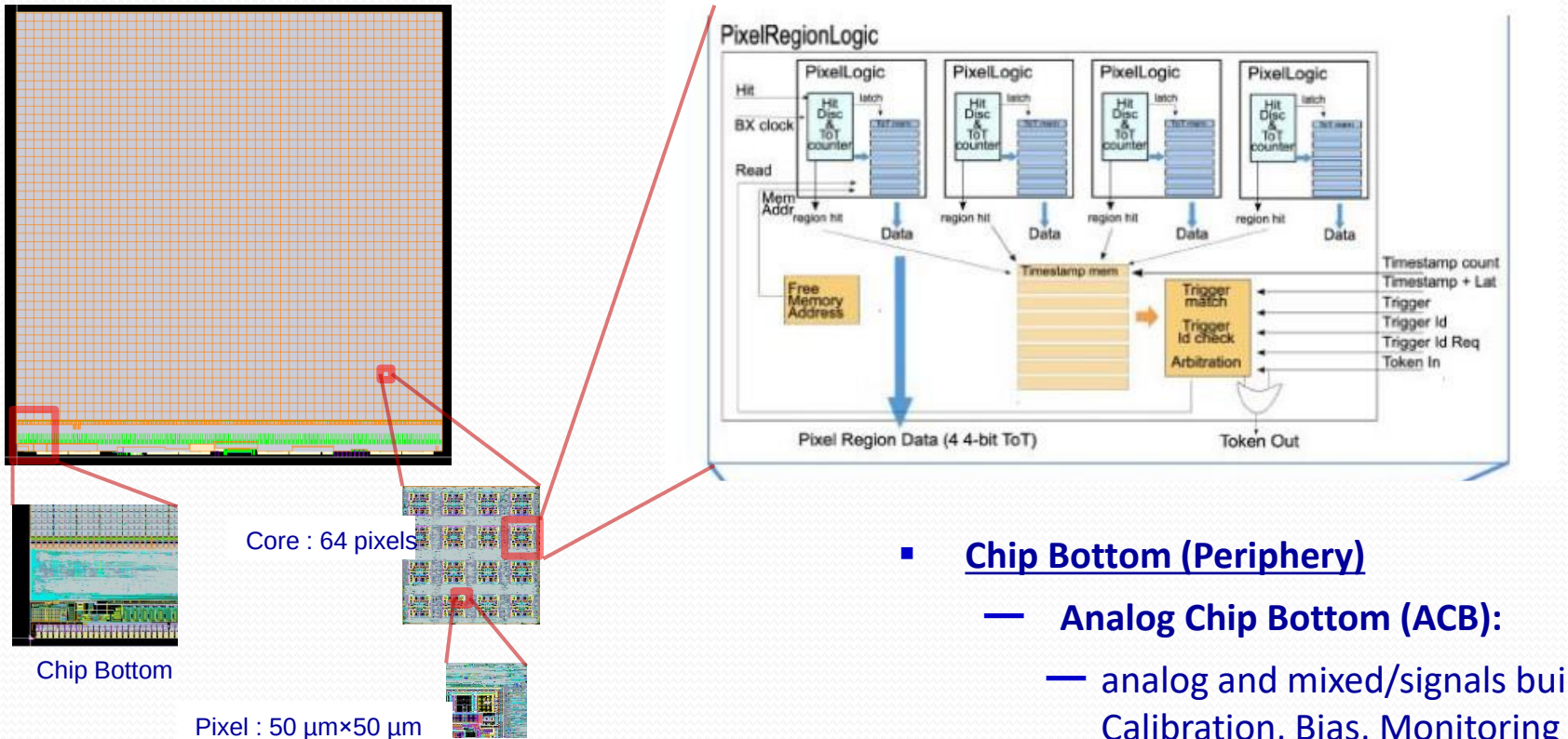


RD53B-CMS (CROC_V1)
size: 21.6 x 18.6 mm²
Submitted in May 2021

ITkPixV1 test board

- **RD53A chip**
  - Large scale demonstrator
  - Submitted in August 2017
  - Tested in an intense way
- **RD53B chip**
  - ITkPixV1 (ATLAS chip) submitted March 2020 and received June 2020
    - High digital current because of an issue in the ToT (Time Over Threshold) latches
    - All the tested functionalities are working as expected
    - The issue was solved by a patch in metal layers : ITkPixV1.1
  - CROC_V1 (CMS chip) received from the foundry the end of August 2021
    - Diced chips will be available soon for testing

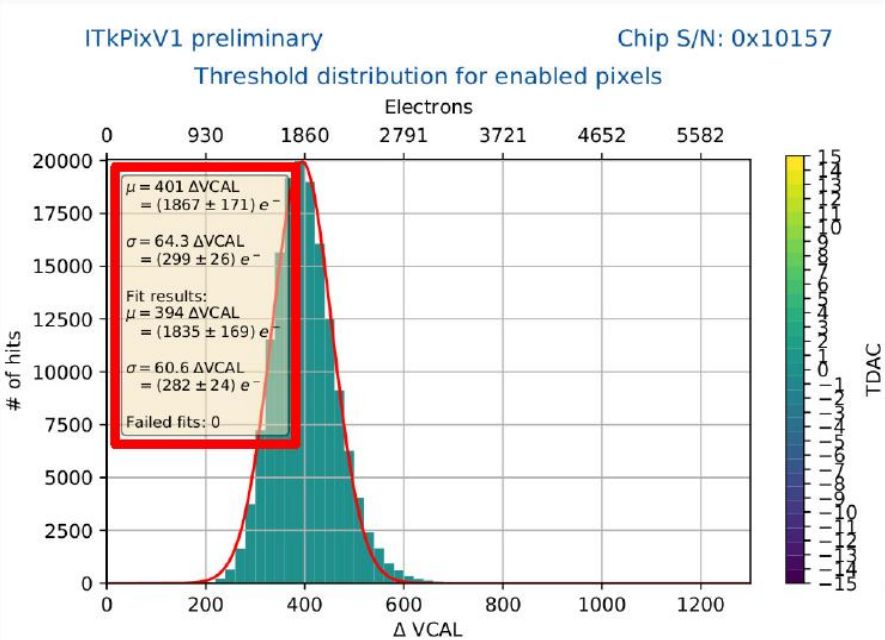
RD53B Floorplan

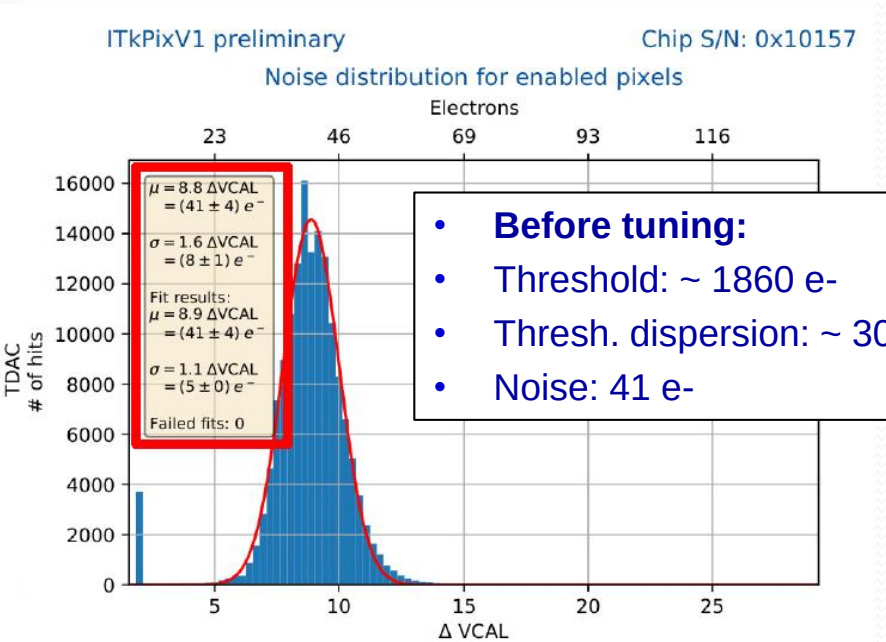


- **Pixel array**
  - 384 x 400 pixels of 50 x 50 µm²
  - 153 600 pixels organized in 2400 identical cores
  - 1 core → 16 analog islands
  - 4 fronts ends per island
  - Analog FE are embedded in a flat digital synthesized “sea”
  - Time Over Threshold (ToT) digitization
  - Shared Pixel Region buffer : Hit storage during Trigger latency

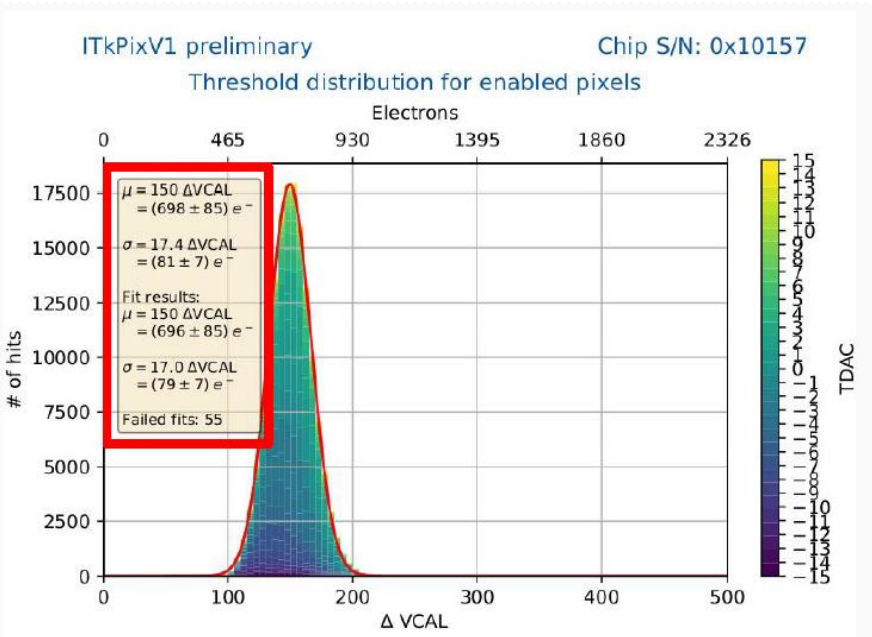
- **Chip Bottom (Periphery)**
  - **Analog Chip Bottom (ACB):**
    - analog and mixed/signals building block for Calibration, Bias, Monitoring and Clock/Data Recovery (CDR)
  - **Digital Chip Bottom (DCB):**
    - synthesized digital logic
  - **Pad frame**
    - I/O blocks with ESD protections, ShuntLDO for serial powering
    - Readout via serial links (1-4 x1.28Gbit/s) using Aurora64/66 encoding

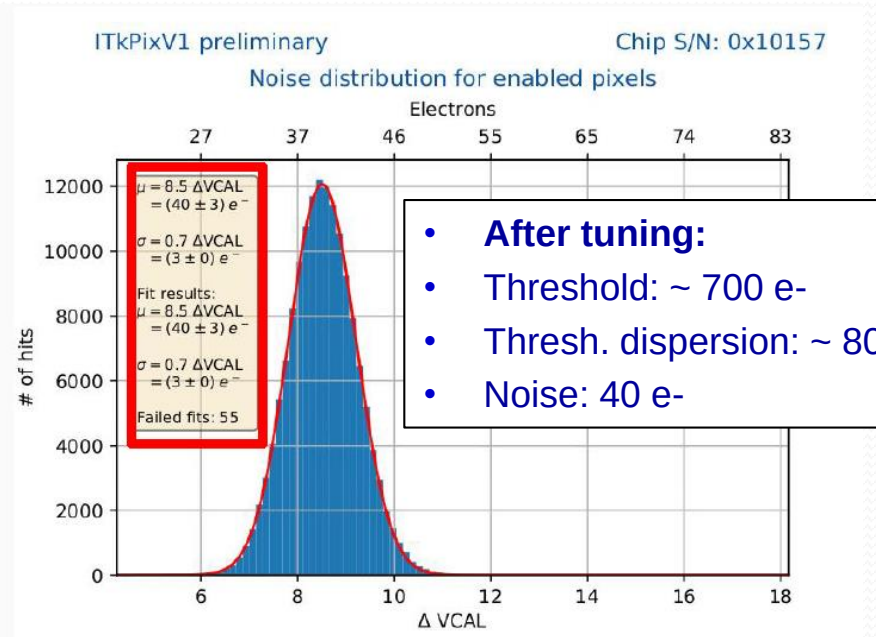
RD53B-ATLAS test results





- **Before tuning:**
- Threshold: ~ 1860 e-
- Thresh. dispersion: ~ 300 e-
- Noise: 41 e-





- **After tuning:**
- Threshold: ~ 700 e-
- Thresh. dispersion: ~ 80 e-
- Noise: 40 e-

Radiation Hardness

RD53 TID test activities

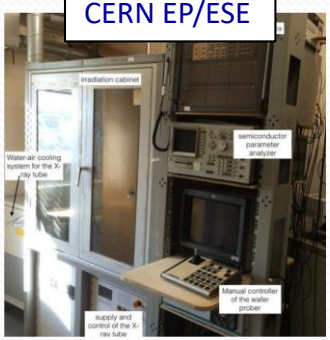
- Extensive radiation campaigns (since 2015) have been carried out to test and qualify :
  - CM0S 65 nm devices, Prototypes of IPs and Front-ends , DRAD test chip to study TID effects on standard cells
- Rules followed in RD53 chip
  - Avoid minimum size digital cells and use large area devices for the analog
  - RD53 chips are designed to meet specifications at 500 Mrad when operating at low temperature (-15 °C)
  - The chip should be maintained powered off during shut down (room temperature)
- RD53 collaboration treats radiation damage as one of the IC design corners
  - 100 Mrad, 200 Mrad and 500 Mrad simulation @ -30°C, 0°C, 25°C models were used to simulate the TID effect on analog and digital designs
- Multiple irradiation campaigns for the RD53A/B chip were done at low temperature (-10 to -20 °C)
  - X-ray machine for high and low dose rate irradiation
  - 60 Co for low dose rate irradiation
  - Kr-85 sources for low dose rate irradiation at -15°C (550 Mrad reached in almost 3 years)

CERN ATLAS

Bonn

Oxford

CERN EP/ESE



Marseille

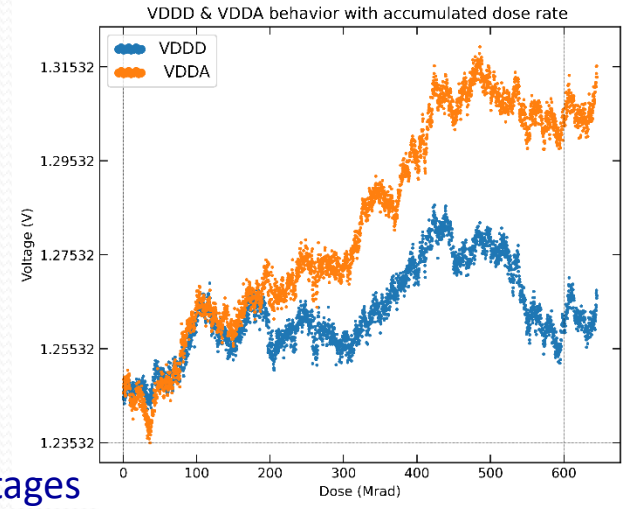
LBL

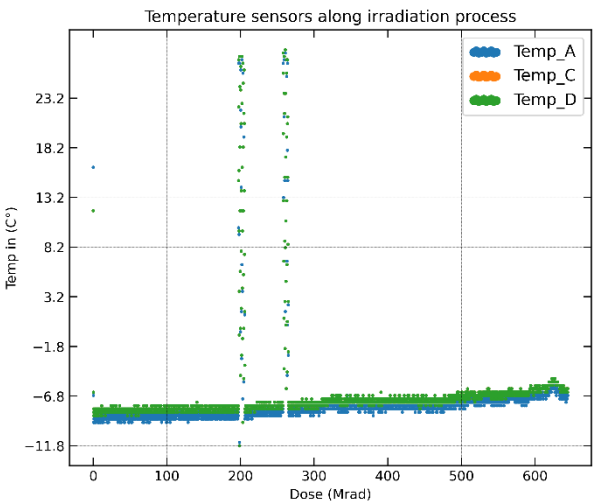
- IJCLab-CPPM collaboration for the ITkPixV1 TID testing at low temperature
  - Xray machine
  - High dose rate and low temperature
  - Voltage monitoring variation and effects on the ring oscillators delay

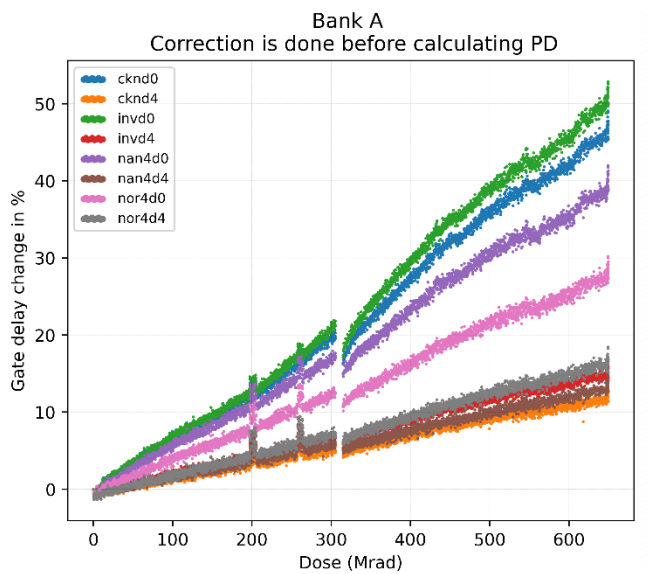
Denis Fougeron presentation in this meeting

TID test results

- The TID tests were conducted in strong collaboration IJCLab/CPPM
  - The temperature is well controlled and stable around -8°C
  - The chip ITkPixV1 in LDO mode
    - VDDD and VDDA generated inside the chip
  - Dose rate of 1.2 Mrad/hour
  - Tested up to 650 Mrad
  - Drift of VDDD/VDDA due to the reference voltages VREFA/VFEFD shift
- **On chip Ring Oscillators**
  - Designed by IJCLab and used intensively for dose monitoring
  - Absolute VDDD correction applied using Freq vs VDDD slopes
  - **Increase for strength 0 gates up to 45%**
    - **Not used in the chip**
  - **Increase for strength 4 up to 28%**
- The results obtained are compatible with those obtained by other institutes







Ring Oscillator	650 Mrad
cknd 0	42 %
cknd 4	12 %
invd 0	45 %
invd 4	16 %
nand4d0	36 %
nand4d4	15 %
nor4d0	28%
nor4d4	18 %

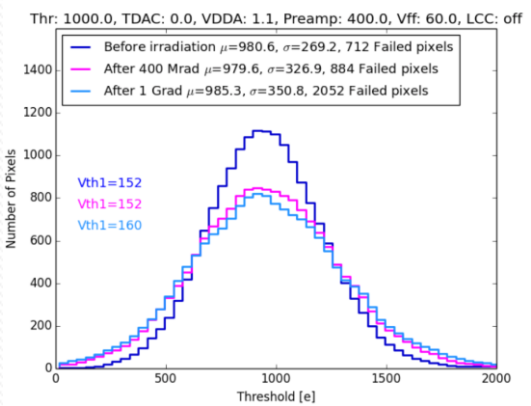
Yahya Khwaira (IJCLab) : RD53 test meeting

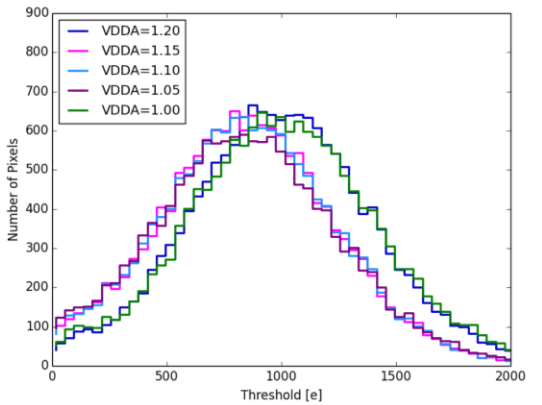
Denis Fougeron presentation in this meeting

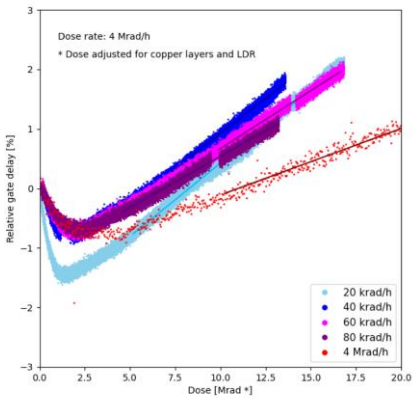
TID test results

Maria Mironova from Oxford institute : RD53 collaboration meeting

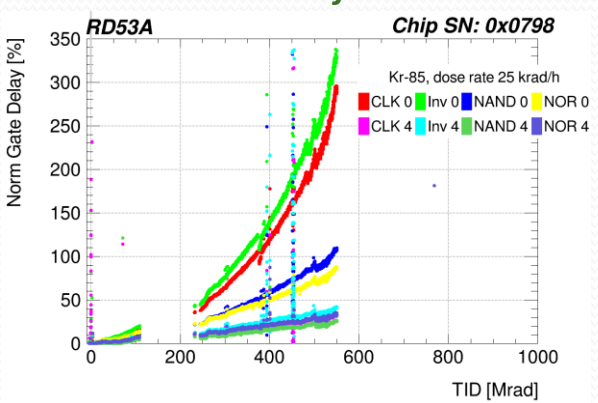
- Analog FE irradiation
  - ITkPixV1 is operational up to 1 Grad even for VDDA=1.0 V
  - Number of failed pixels <5% for most parameter settings
- **Low Dose Rate effect**
  - Impact of low dose rate effects studied for low total doses in X-ray setups
  - Assuming optimistic extrapolation effect
    - **Damage increases for low dose rate by a factor 2-3**
  - Additional low dose rate effects observed in LDR irradiations using Kr-85 at high total doses Longest running
    - **RD53A chip: 3 years!**
    - Results of low dose rate irradiation up to **550 Mrad**
    - The **extrapolation** from high dose rate to low dose is **not obvious**







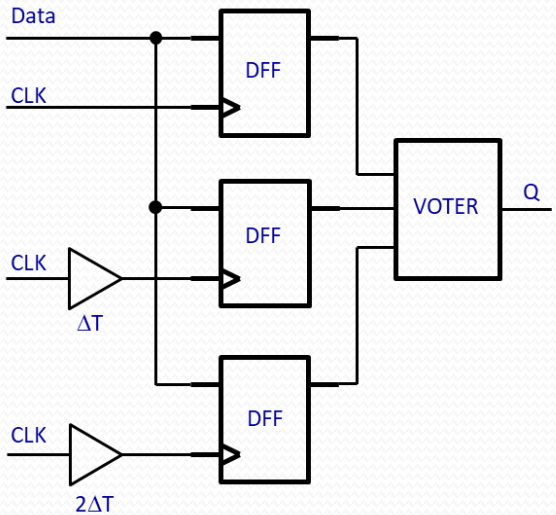
Aleksandra Dimitrievska from LBL institute : RD53 collaboration meeting



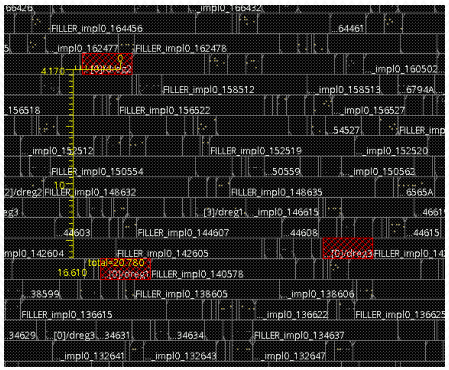
Ring Oscillator	550 Mrad
CLK 4	32%
CLK 0	290%
INV 4	41%
INV 0	328%
NAND 4	25%
NAND 0	108%
NOR 4	34%
NOR 0	86%

SEU mitigation in the RD53B chip

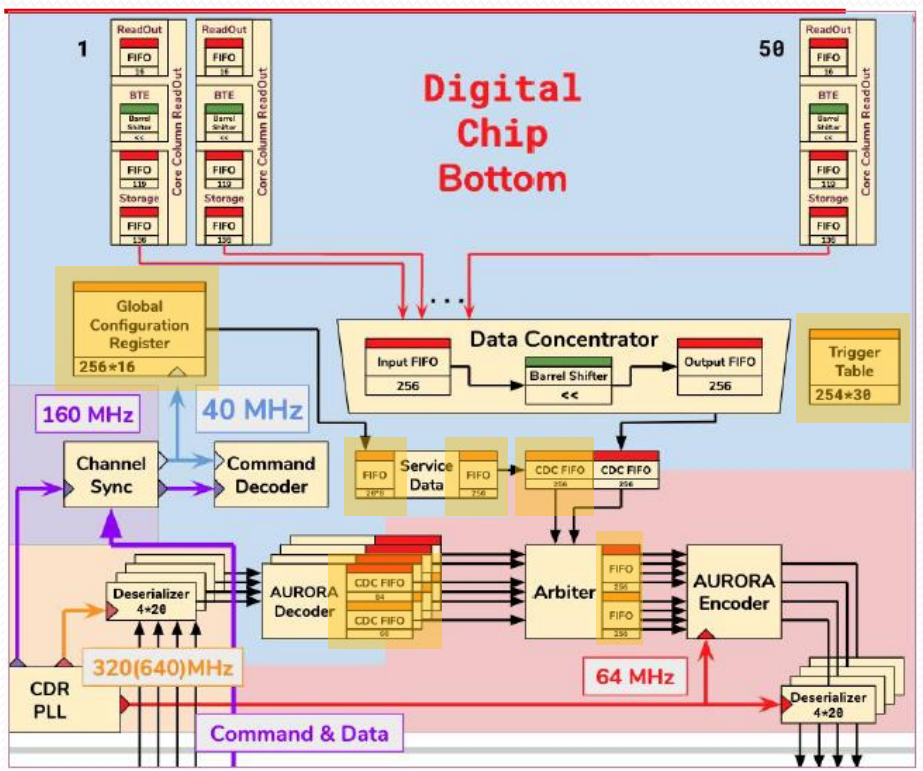
- **Single Event Effects (SEE)** are a major challenge for the RD53B chip design:
  - Should work reliably in an extremely hostile radiation environment
- **Triple Modular Redundancy** (TMR) associated to the **SET mitigation with clock spread** is used in the **Digital Chip Bottom** to reduce the SEU rate in the RD53B
  - Area and power consumption increase
  - Not compatible with the required small pixel size and the power dissipation constraints
- **Mitigation of SEU** concerns only **the critical parts** as the configuration memories, state machines, FiFo pointers …
- Data Paths are not protected
- **50% of the DFFs** in the chip bottom are protected
- All the reset signals are synchronous (avoid a global glitch effects caused by SET)
- **TMR is implemented during synthesis**
  - Simple FF replacement with TMR version
  - TMR flip-flops are constrained to be placed with **15 µm distance**



TMR+SET mitigation with clock spread



Cells Spacing in the same TMR latch



SEU Tests campaigns

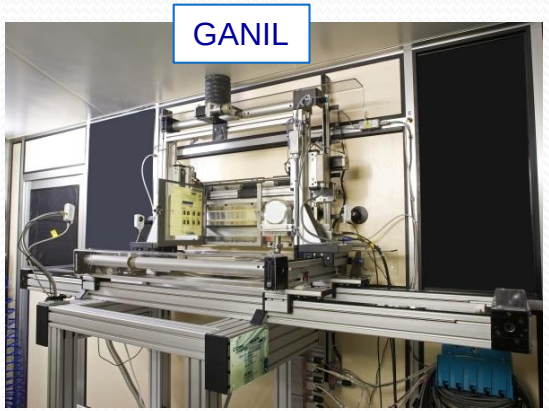
- **Centre de Ressources du Cyclotron (CRC) – Louvain la Neuve**
  - Two SEU test beam campaigns: October 8, 2020 and November 17, 2020
  - The chip irradiated in vacuum with several heavy ions flavours (1.3 to 62.5 MeV.cm²/mg)
- **TRIUMF facility**
  - SEU tests campaign done remotely December 19-20 2020
  - 480 MeV proton beam
  - The chip tested under a proton flux of 1.5 10^9 p/cm²/s similar to the hadron flux in the HL-LHC
- **GANIL – Caen**
  - SEU campaign in April 2021 and dedicated for CDR/PLL
  - Test done with only 1 ion : ^{129}Xe : LET = 30 MeV.cm²/mg
- **KU Leuven-Campus Geel (PULSCAN)**
  - Laser SEU testing October 5, 2021
  - 2 photon absorption
  - Backside pulse injection
  - Pulse energy applied: 1 nJ
  - Pulse frequency: 1 KHz

CRC – Louvain la Neuve

TRIUMF

The flux = 1.5 10^9 p/cm²/s

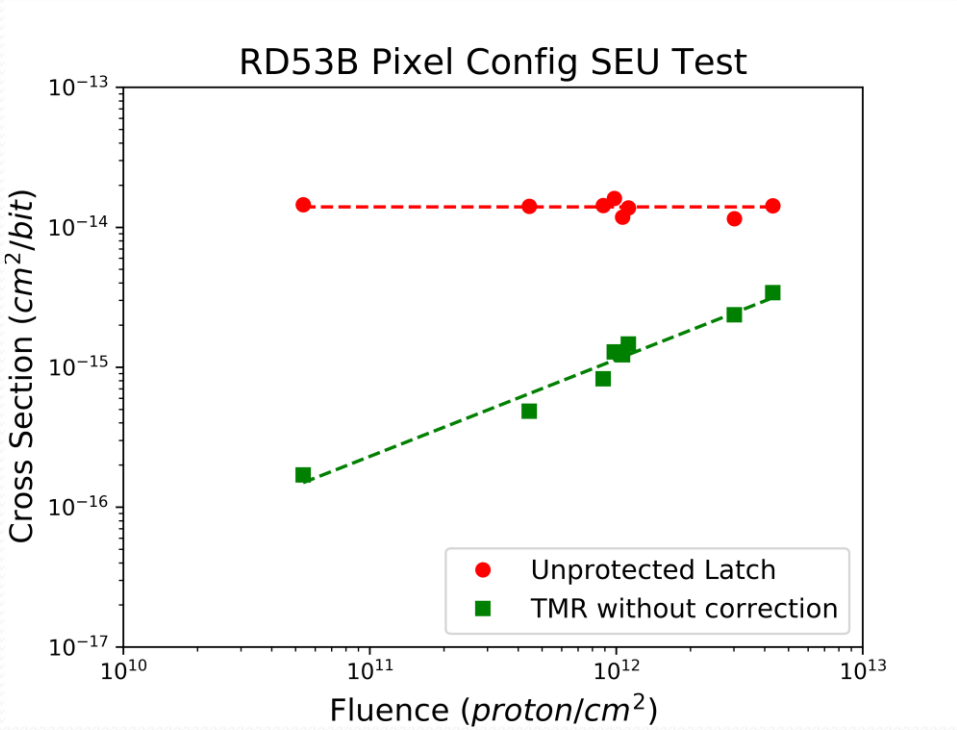
GANIL



PULSCAN - Leuven

Configuration memories tests

- **Pixel memory size** : 8 bits per pixel -> 1.28 Mbit per FE chip
  - Unprotected latch used for 2 bits
  - TMR without correction used for 6 bits
- **Unprotected latch** cross section $\sigma = 1.5 \times 10^{-14}$ cm²
- **Pixel TMR latch** cross section increases with the fluence because of errors accumulation
  - **The TMR is 100 times** tolerant than the unprotected latch for low proton fluence (~5×10^{10} p/cm²) ,
  - **TMR is only 10 times** tolerant than the unprotected latch for moderate proton fluence (~1.0×10^{12} p/cm²)
  - TMR without correction is useful when considering a **regular external re-configuration**
- **Global configuration** : ~3 Kbit in total where a half is reserved only for tests
  - TMR with correction
  - $\sigma = 3.6 \times 10^{-17}$ cm²
  - The tolerance is **improved** by a **factor 400**



- Tests were done with
  - **CDR mode** : serializer and command clocks are provided by on-chip CDR
  - **Bypass mode** : both clocks are provided externally
- In PLL mode, **synchronization issues** with the BDAQ readout system have been identified

HL-LHC SEU rate estimation

Table 1. HL-LHC environment : Atlas pixel detector SEU error rate estimation.

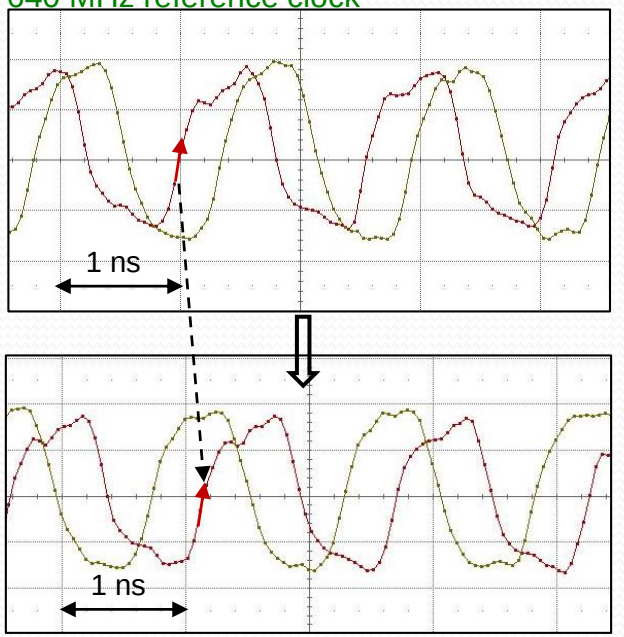
					Pixel Conf.	Pixel Conf.	Global Conf.
Layer	Location	R (cm)	Z (cm)	SEE-Flux ($cm^{-2}.s^{-1}$)	Unpr. latch (flip/FE)	TMR latch* (flip/FE)	TMR w/corr (flip/FE/hour)
0	L0 rings	3.6	114	1.0×10^{9}	230	7	0.2
2	L2 rings	15.6	286	0.82×10^{8}	19	0.095	1.7×10^{-2}
4	Outer Endcap	274.6	286	0.35×10^{8}	8	0.022	7.2×10^{-3}

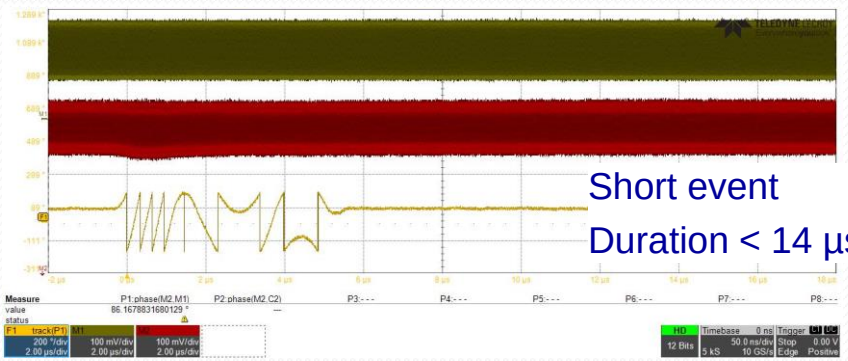
*Based on external re-configuration time interval of 50 seconds

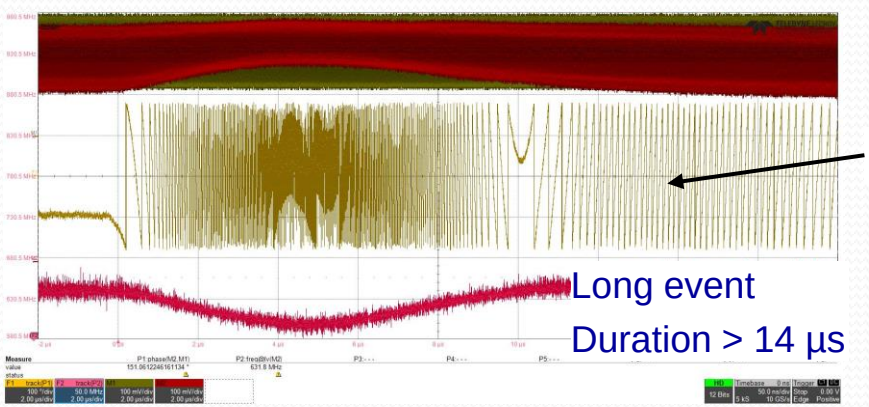
CDR testing at GANIL

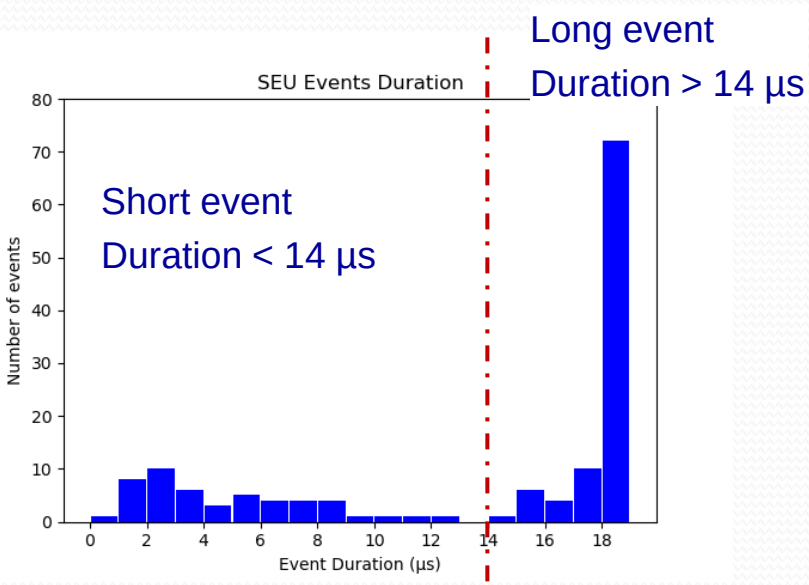
- Scope trigger : CDR clock rising edge “moves” from the low level of the ref clock to the high level
- Short event (<14µs) : already
- Long events (>14µs) showing a shift of phase and frequency
  - Not observed when testing the CDR prototype

640 MHz CDR clock
640 MHz reference clock

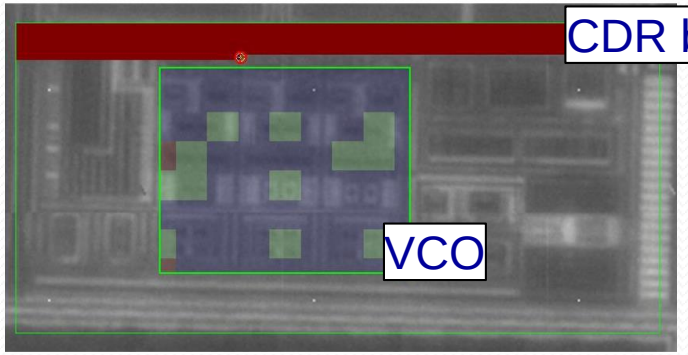


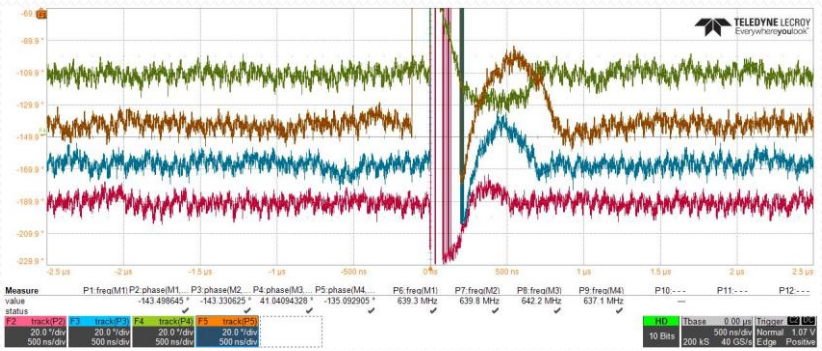




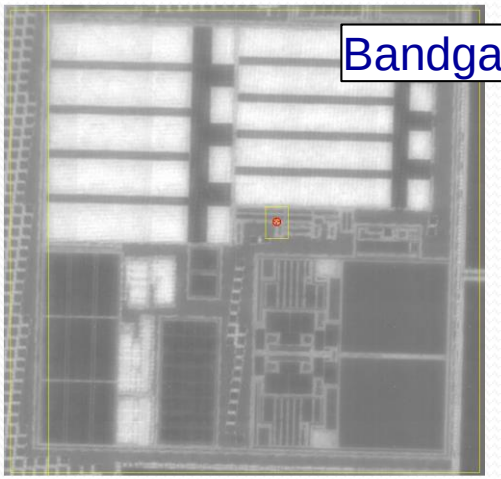


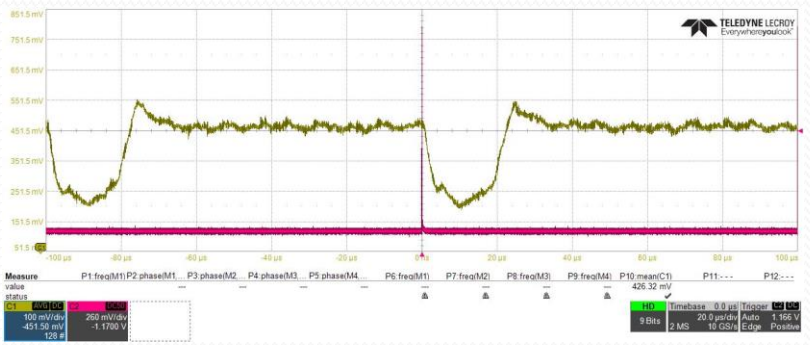
Laser SEU testing





- Laser energy: 1 nJ
- Only short events were observed when shooting in the CDR or VCO blocks
- Shooting green bordered area in VCO stages caused just small phase shifts of the serializer clock
- **Compatible** with the group of **short events** seen in GANIL





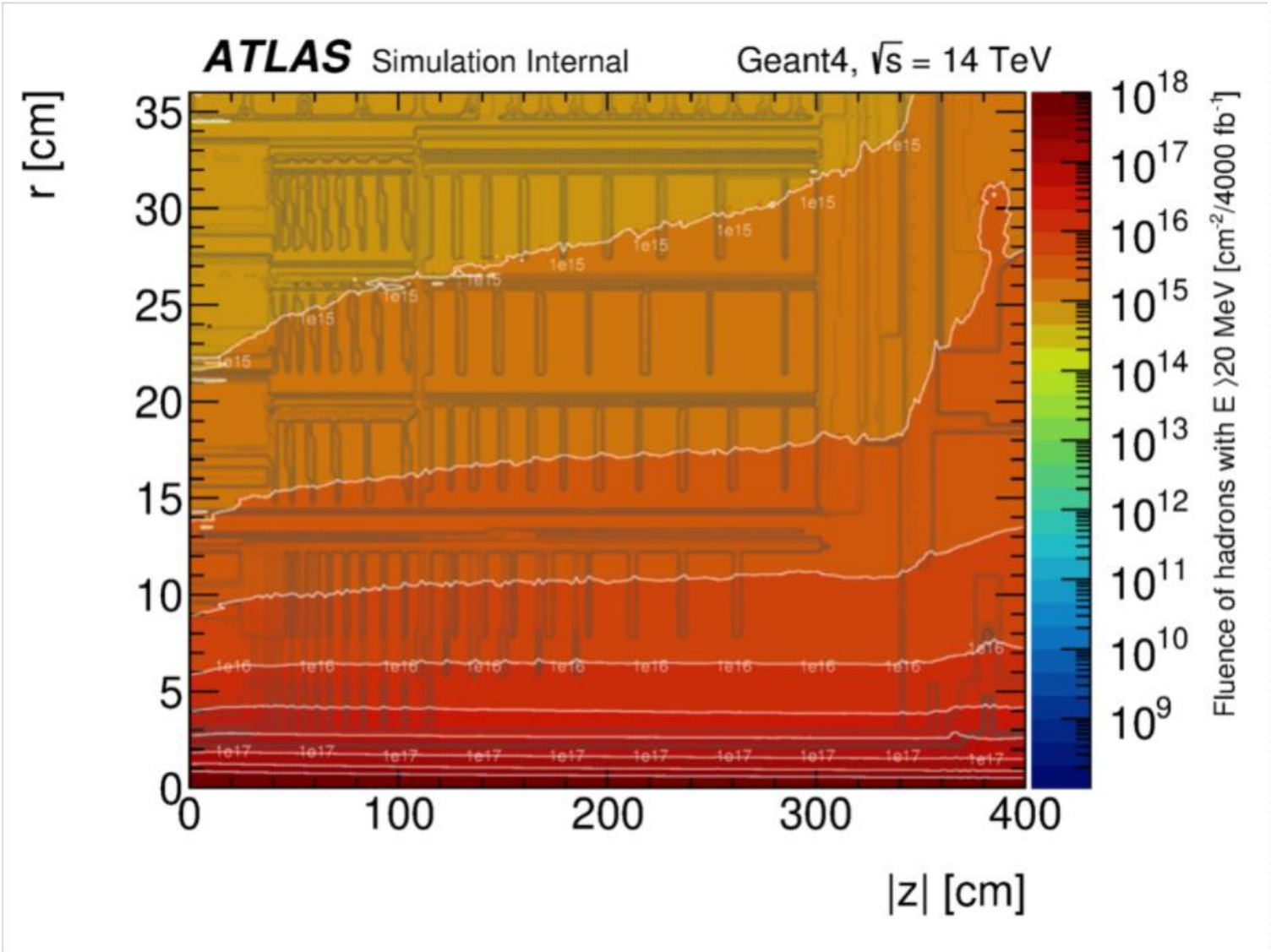
- Laser energy: 1 nJ
- Shooting in core bandgap and monitoring VREF_A
- Shooting some specific transistors showed sensitive behavior
- VREF_A jumps in range of [20 us, 30 us]
  - **Explains the long events observed in GANIL**

Summary and Conclusion

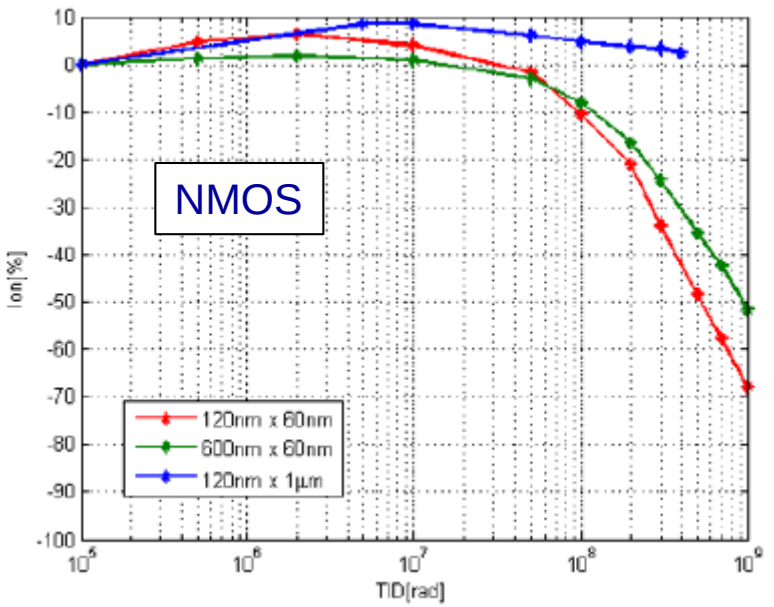
- **RD53 Radiation hardness**
- TID tests done **at low temperature** (-20°C) and **high dose rate** show that the RD53B chip is operating correctly up to **1 Grad**
- Tests at **low dose rate** are in progress
- SEU tests were done with high LET ions and 480 MeV proton beam
  - The chip is working correctly without need of resetting or power cycling
  - No issue observed with the state machines and critical paths and No latch-up or chip-stuck observed
  - The global memory based in TMR with correction is quite tolerant to SEU
  - The pixel memory needs to be refreshed at regular intervals
- Future tests
  - Tests in a real working conditions, **high trigger rate and high hit rate**
  - Test of the communication and the effect of the **CDR SEU** on the whole chip
- **RD53C chip**
- **ITkPixV2 chip** will be submitted March 2022 and the tests finalized the end of 2022
- **CROC_V2 chip** will be submitted June 2022 and the tests finalized the end of Q1-2023
- Fixing of known bugs, verifications and simulations are currently in progress

Backup Slides

Fluence of Hadrons > 20 MeV (4000 fb-1)



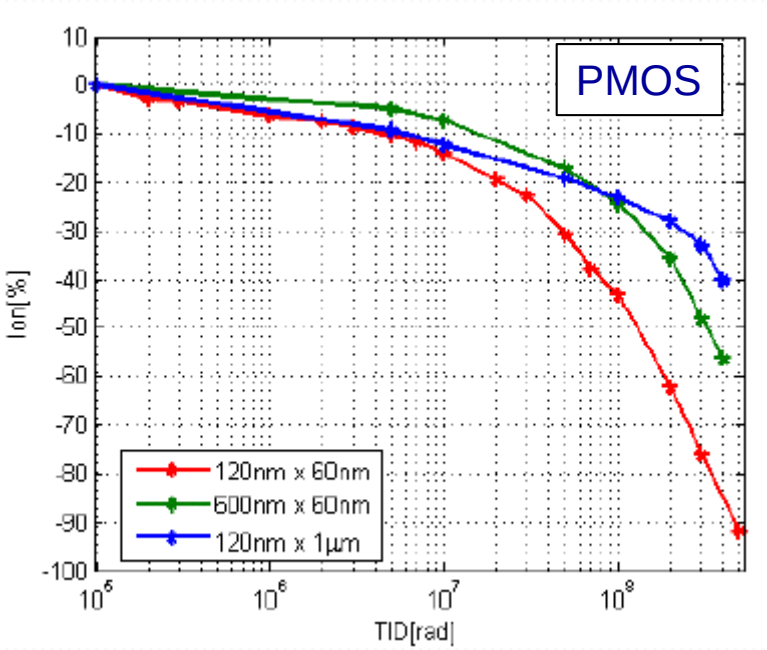
TID effects on the 65 nm CMOS process



Narrow channel

Short channel

Minimum size

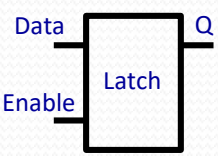


- Irradiation damage depends on several parameters : device geometry, bias, temperature, dose rate …
- All these parameters must be taken into account in the design to ensure correct operation in the HL-LHC environment.
- Size : Short and Narrow transistors are affected by RISCE and RINCE. Strong degradation of “Digital” devices
- Temperature : Strongly depends on temperature during irradiation and bias conditions of the devices
  - Less damage for the NMOS and PMOS device when Irradiation is done at low temperature (-20 °C)
- Bias : More damage for the worst case bias : VGS=VDS=1.2 V (diode connected)
- Leakage current : For this 65nm process, the increase of the leakage current is very limited
  - In general, the enclosed layout is not needed

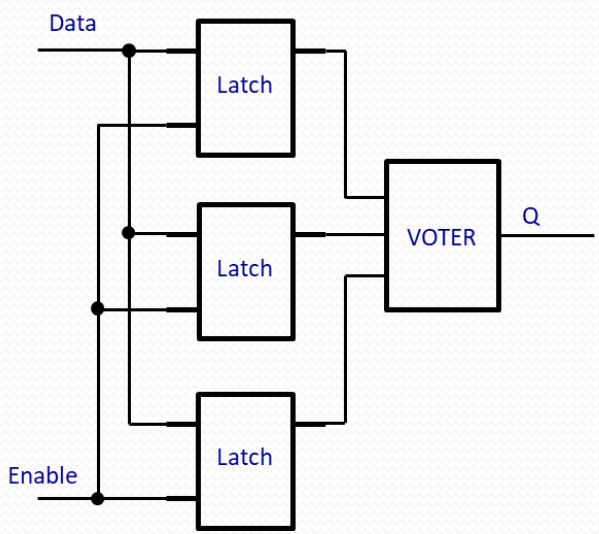
SEU mitigation in the RD53B chip

Chip Configuration

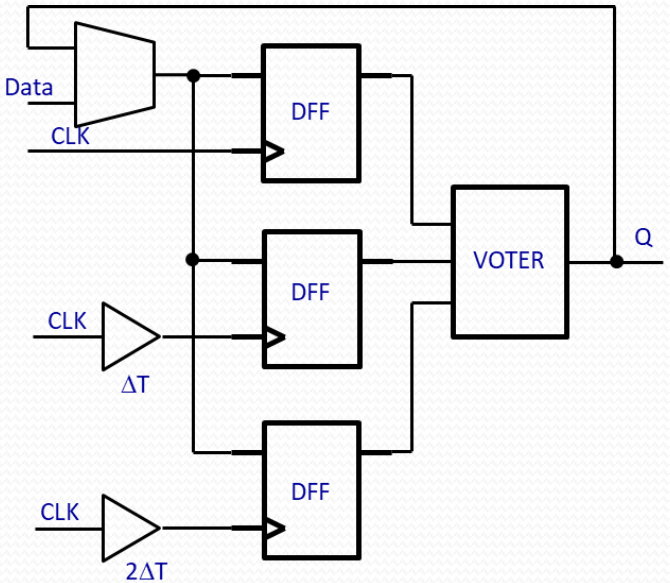
- **Pixel configuration**
  - Memory size : **8 bits per pixel** -> 1.28 Mbit per FE chip
  - **Unprotected latch (single latch)** used for 2 bits
  - **TMR latch without error** correction implemented for 6 bits
  - The small pixel area does not allow to implement the auto correction
- **Global configuration**
  - Memory size : 1.6 Kbit
  - Located in the Digital Chip Bottom
  - **TMR with clock skew and error correction**
- The configuration registers (global and pixel) **do not have a reset**
  - A re-configuration step is necessary to put them in a right state



Unprotected single latch



TMR latch without correction

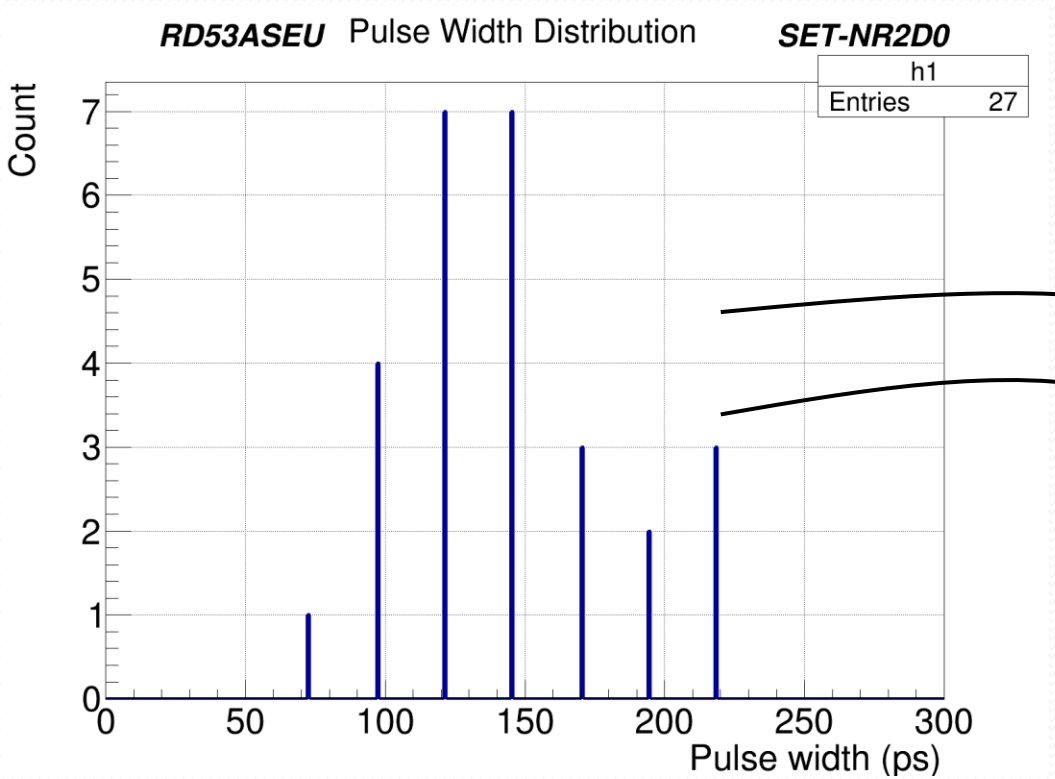


TMR with correction

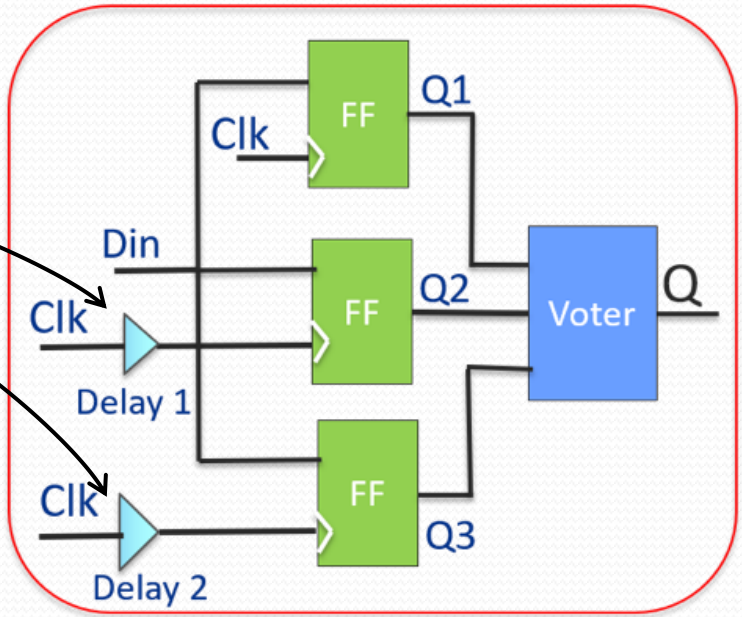
TMR with clock skew

- **ΔT is set to 200 ps**
- Filter SET glitches **shorter than 200 ps**
- **Implementation Challenges** :
  - Triplicated clock skews made by clock tree synthesis
  - Timing closure (hold time)
  - Delay variation with process, power supply, temperature and TID

SET Analysis



SEU tolerant design with temporal Mitigation



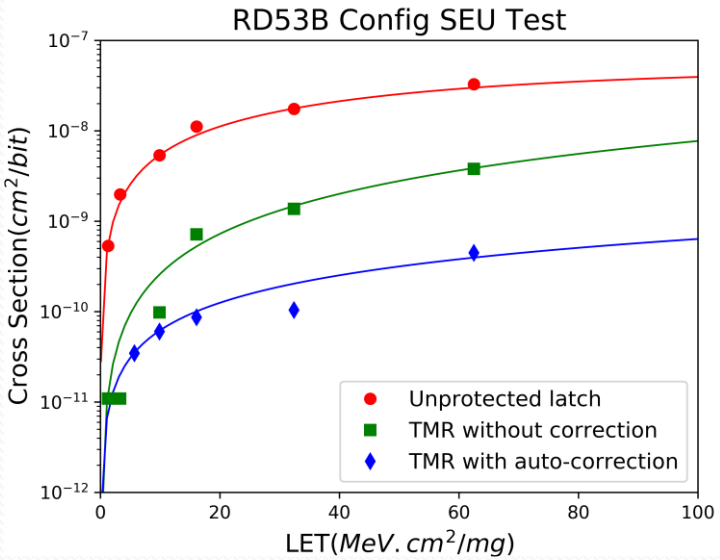
- SET test structures implemented in the chip
  - Measurement of pulse width > 70 ps with a resolution of 30 ps
- NOR gate: SET pulse width ： **70 ps < PW < 220 ps**
- RD53B chip
  - The structure using temporal mitigation is implemented in RD53B
  - This work helped to set the optimal value for the delay

Pixel Configuration

Bits	Name	Description
[0]	Enable	Include the pixel in the DAQ data path
[1]	Cal Enable	Turn on charge injection (*)
[2]	HitOr Enable	Add the pixel to its wired OR core col. hit line
[3:6]	TDAC value	Value for in-pixel theshold trim DAC
[7]	TDAC sign	Selects differential branch set to TDAC value

Configuration memories tests

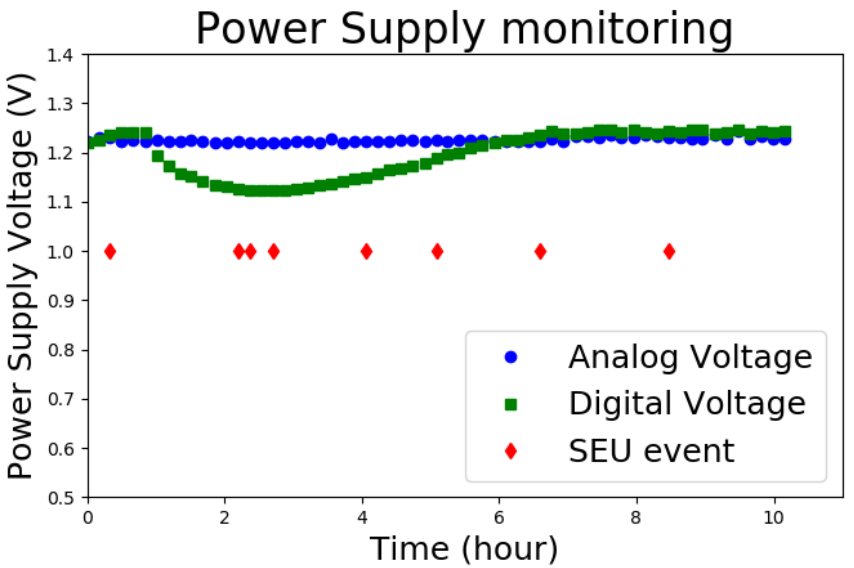
- **Pixel memory size :** 8 bits per pixel -> 1.28 Mbit per FE chip
  - TMR without error correction implemented for 6 bits
  - Unprotected latch used for 2 bits
- **Global memory size :** ~3 Kbit in total (209 global registers)
  - TMR with correction
- Unprotected latch :
  - **Saturation cross section :** $\sigma_{SAT} = 6.0 \times 10^{-8}$ **cm²**
  - **Threshold LET** $LET_{th} < 1$ **MeV.cm²/mg**
- TMR latch (no correction)
  - For a particle fluence of **2.0×10^5 p/cm²**, the saturation cross section is improved **by a factor 10**
  - **The TMR w/o correction is very efficient for mitigation** for low error rate
  - The cross section increases with fluence because **of errors accumulation**
- Tests were done with:
  - **PLL mode** : serializer and command clocks are provided by on-chip CDR
  - **Bypass mode** : both clocks are provided externally
- In PLL mode, **synchronization issues** with the BDAQ readout system have been identified



	Unprotected latch cross section (cm²)	Global Register cross section (cm²)
calculation for 200 MeV proton based on heavy ion testing	8.6×10^{-15}	7.9×10^{-17}
Experimental value 480 MeV proton test	**1.5×10^{-14}**	**3.6×10^{-17}**

Global configuration results

- Long duration global register run
  - Duration : 10h30 , Total fluency : 7.2×10^{13} p/cm²
  - SEU number : 8
- Slow increase of V_{IND} from 1.7 V to 2 V
- The internal V_{DDD} decrease limited to 8% (1.2 V to 1.1V)
- The run Stopped because of a power supply issue
  - Supply was placed inside the beam area
- **The TMR with correction show a gain of ~ 400 regarding the unprotected latch**
- Global Registers seem to be very tolerant to SEU
- Results are compatible with what expected from heavy ion testing



	Unprotected latch cross section (cm²)	Global Register cross section (cm²)
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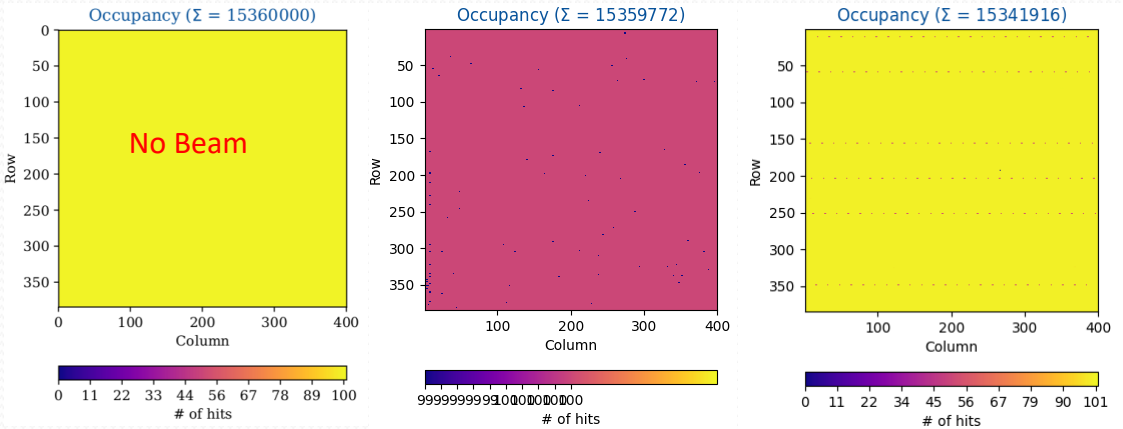
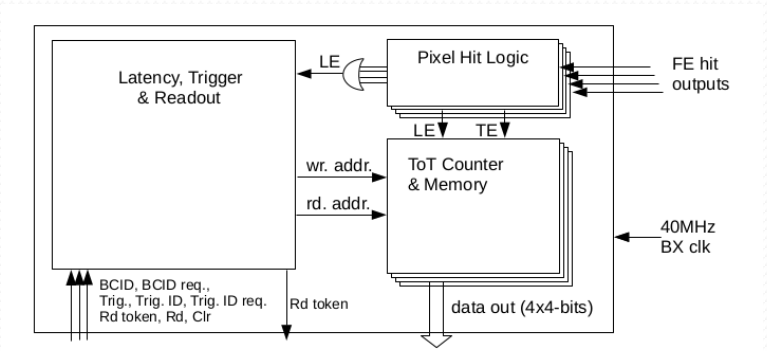
Layer	Location	R (cm)	Z(cm)	SEE-Fluence (cm^{-2}) Hadrons> 20 MeV	SEE-Flux ($cm^{-2}.s^{-1}$) Hadrons> 20 MeV	Pixel configuration Unprotected latch	Global Configuration Mean time between errors (per FE chip)
0	L0 rings	3.6	114	3.26×10^{16}	**1.0×10^{9}**	4.6 SEU/sec	**5 hours**
2	L2 rings	15.6	286	2.66×10^{15}	0.82×10^{8}	0.38 SEU/sec	58 hours
4	Outer Endcap	274.6	286	1.14×10^{15}	0.35×10^{8}	0.16 SEU/sec	138 hours

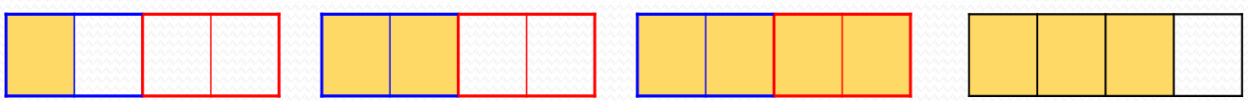
Digital scan

- **Standard procedure of digital scan:**
  - 100 digital injections per pixel
- **For the digital scan test, Individual pixels can show bigger/lower amount of hits**
- This concern **clusters of 4 pixels**
  - It is due to **SEU** in the **digital part of the pixel**
  - This is explained by the **digital architecture organized by regions of 4 pixels**
  - Fired pixels in the same cluster varies between 1 and 4
  - SET or SEU on the common logic to these 4 pixels results as if 1,2,3 or 4 pixels were touched at the same time



More/less hits are received (100 is injected)





1 SEU affecting individual pixel (Pixel Hit logic)

1 SEU affecting 2 neighboring pixels (LTR block)

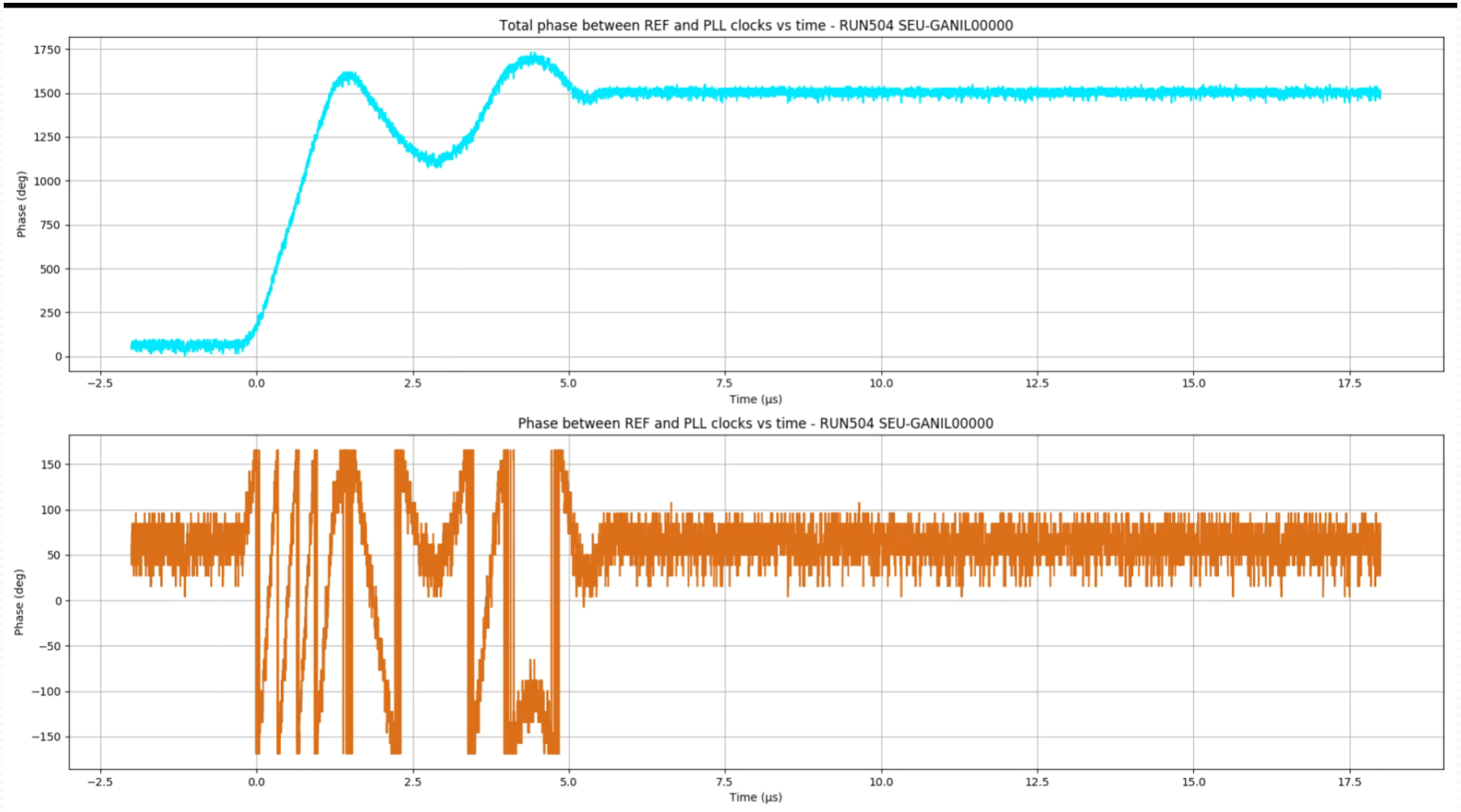
2 independent SEUs (LTR block)

This case is not present in any of the scans, but would be counted as 2 SEUs

- Tests were done with:
  - **PLL mode** : serializer and command clocks are provided by on-chip CDR
  - **Bypass mode** : both clocks are provided externally
- In PLL mode, **synchronization issues** with the BDAQ readout system have been identified
  - Map where missing hits are not random
- SEU tests of the **CDR/PLL block** of the RD53B chip are in progress

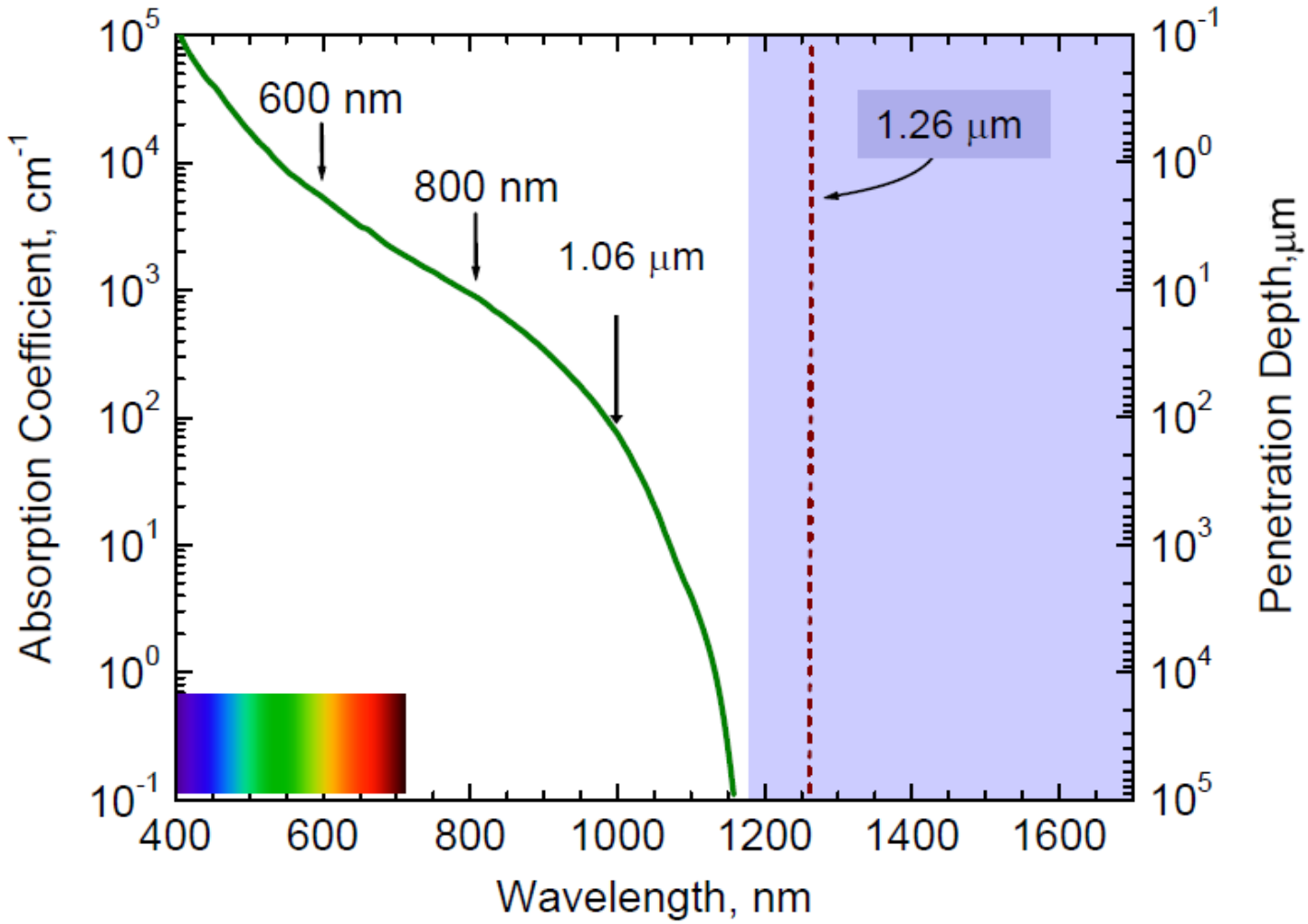
(Injection and readout is always done separately in pixels border with blue and read)

Example of phase shift

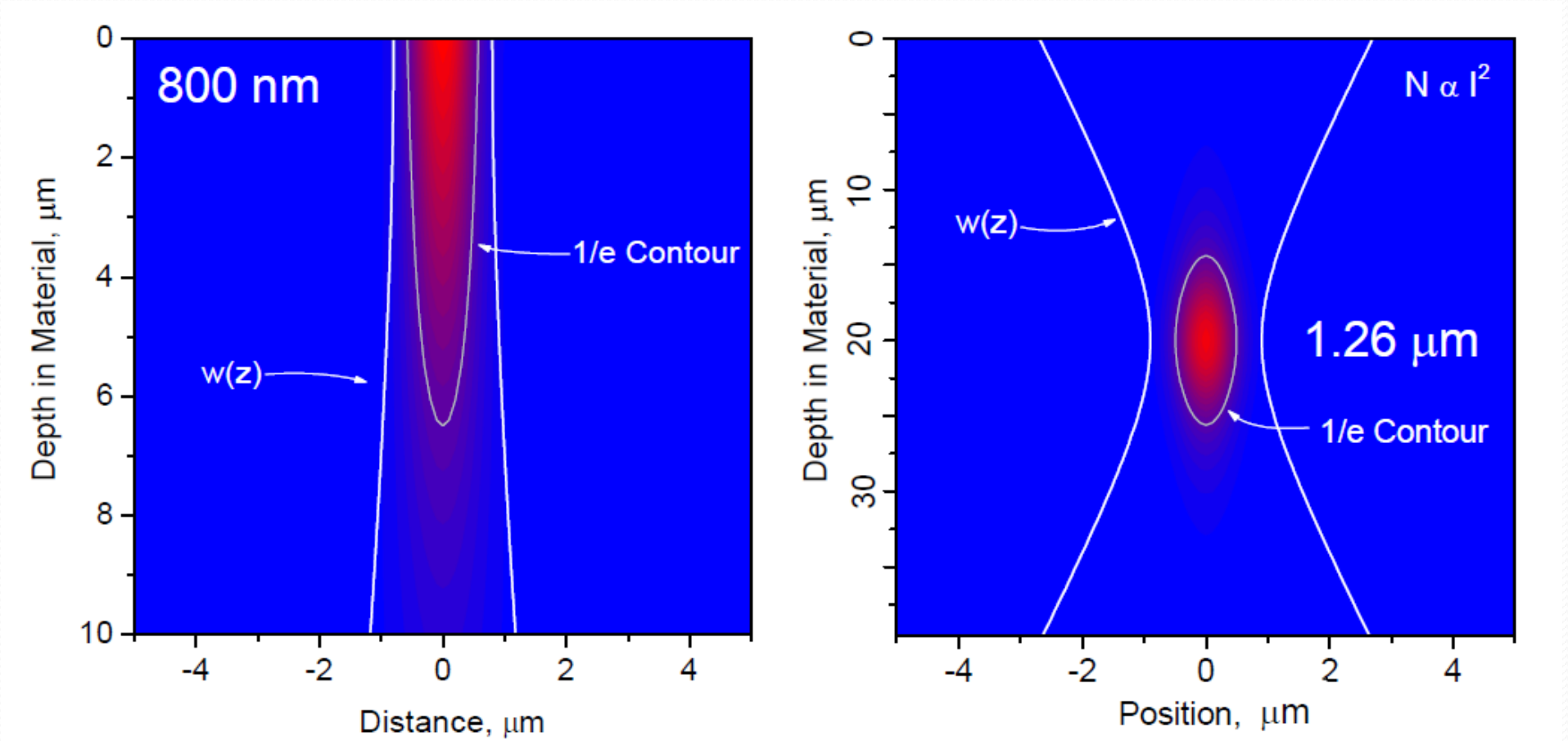


mp4 video showing an example of a saved SEU Event - Duration = 20 µs

Two photon optical absorption

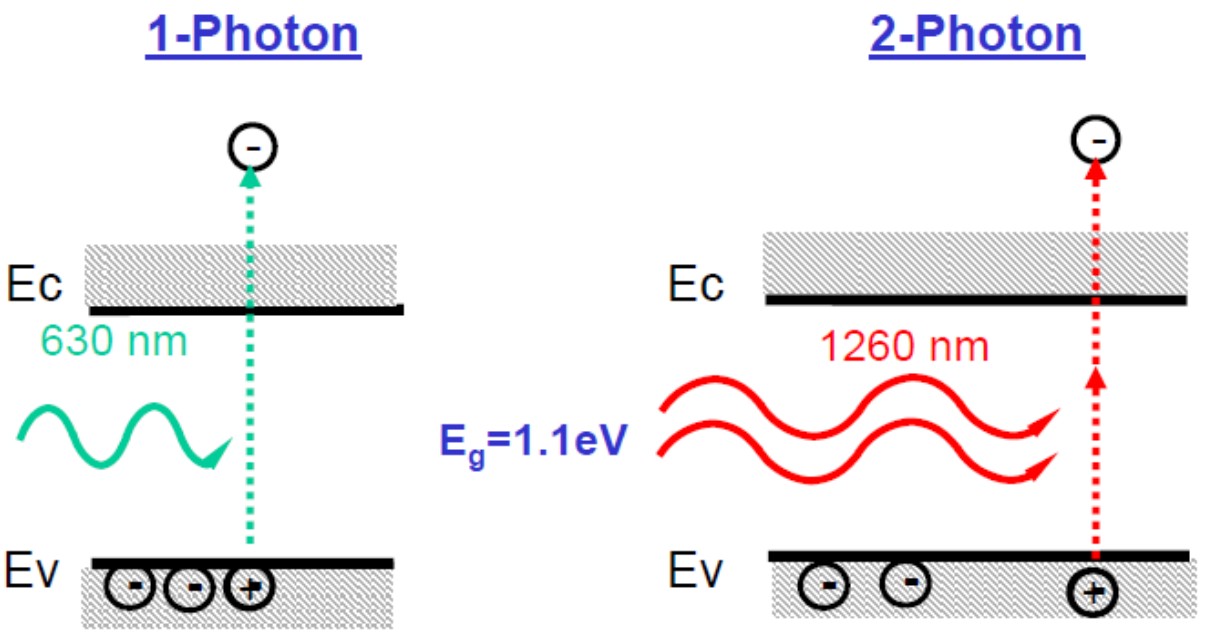


Charge density distribution



- Carriers are highly concentrated in the ***high irradiance region*** near the focus of the beam
- Carriers can be ***injected at any depth*** in the semiconductor material
- ***backside illumination***

Two photon Silicon excitation



- *Single photon absorbed*
- *By the material (silicon)*
- *Creates a single e-h pair*

- *Two photons absorbed*
- *By the material (silicon)*
- *Simultaneously*
- *Creates a single e-h pair*

RD53B data flow

- Data flow architecture
  - Hits are stored as Time-over-Threshold, associated to a time stamp
  - 6-bitToT counter, but only 4 bits are stored and read-out
  - Each pixel has 8x4-bit ToT memories
  - Support of 6-to-4 ToT mapping (dual slope)
  - Selectable counting clock: 40 MHz or 80 MHz
  - The time stamp memories shared among 4 pixels of the same 4x1 Pixel Region
  - Token-based readout of hits, organized in Core Columns
- Multiple levels of data processing, event building, buffering and formatting before final readout via serial links
- Command, control and timing are provided by a single 160Mbit/s differential control link, driving up to 15 chips (4 bit addressing)
- CDR/PLL recovers Data and Clock
- Readout via serial links (1-4 x1.28Gbit/s) using Aurora64/66 encoding
- Multi-Chip Data Merging available for low-rate outer pixel layers: one chip of the module can be configured as “primary” to aggregate serial data from one or more other “secondary” chips and merge them with its own output