Institute of Research into the Fundamental Laws of the Universe
DEDIP

Novel Low-Power Multichannel Time-to-Digital Converter for the CMS High Granularity Calorimeter

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with material from HGCAL FE electronics working group and IRFU CMS group

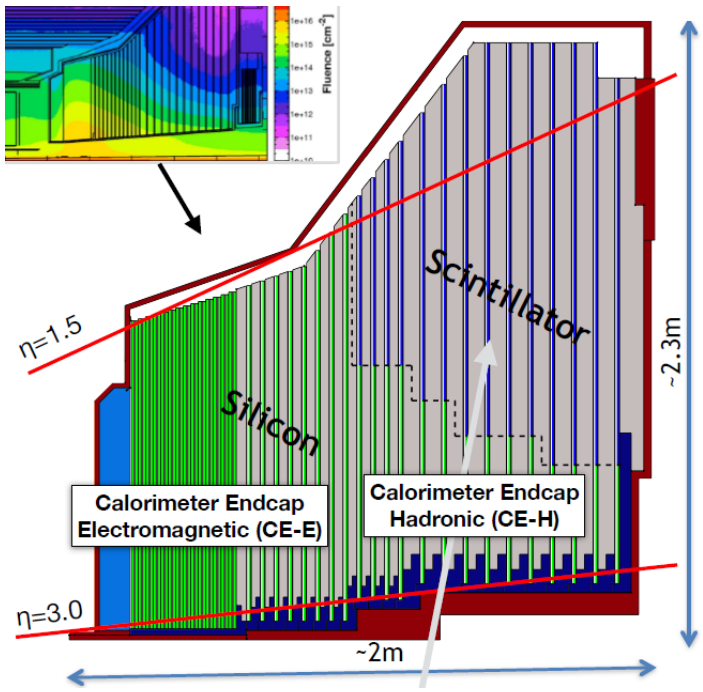
13/10/2021

Journées des Métiers de l'Electronique de l'IN2P3 et de l'IRFU

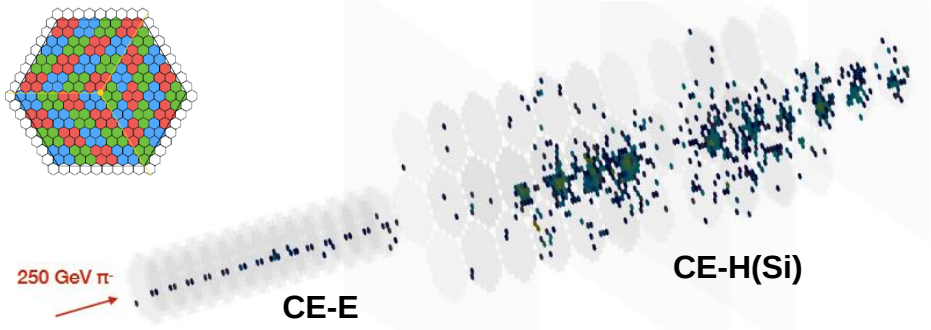
HL-LHC necessitates upgrades to the CMS detector

Experimental challenges	LHC	HL-LHC	General mitigation strategy
• inst. luminosity • detector irradiation • pile-up interactions	2×10^{34} s^{-1} cm^{-2} O(10^{14} neq/cm^2) O(40)	→ up to 7.5×10^{34} s^{-1} cm^{-2} >O(10^{15} neq/cm^2) 140-200	‣ improved trigger & computing ‣ radiation-tolerant sensors & electronics ‣ timing and increased granularity

HGCAL: where highly granular calorimetry comes to life at the energy frontier
- Silicon as sensitive material in high radiation region, scintillator+SiPMs elsewhere.
- 3D energy & time measurement of particle showers.



Hexagonal **silicon sensor** based modules in CE-E and high radiation regions of CE-H.
Scintillating tiles with on-tile SiPM readout in low-radiation regions of the CE-H.
Area : 1000 m^2, 6 M Channels @ -30 ° C



HGCAL = Imaging calorimeter

Thorben Quast (CERN) TIPP 2021 Status and Plans for the CMS High Granularity Calorimeter Upgrade Project

HGCROC3 overview

Overall chip divided in two symmetrical parts
• 1 half is made of:
– 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
– Bandgap, voltage reference close to the edge
– Bias, ADC reference, Master TDC in the middle
– Main digital block and 3 differential outputs (2x Trigger, 1x Data)

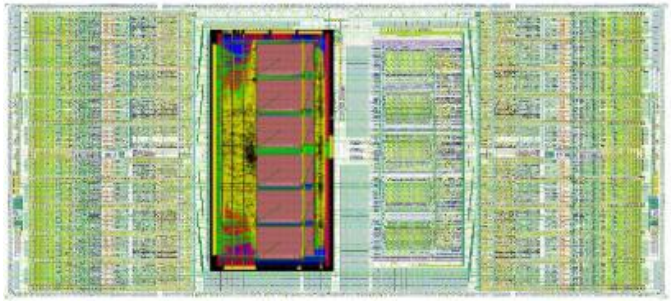
Measurements High dynamic range : 0.2 fC -10 pC (Si) or 300 pC (SiPM)
• Charge
– ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
– TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
– ADC: 0.2 fC resolution. TOT: 2.5 fC resolution
• **Time**
– TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

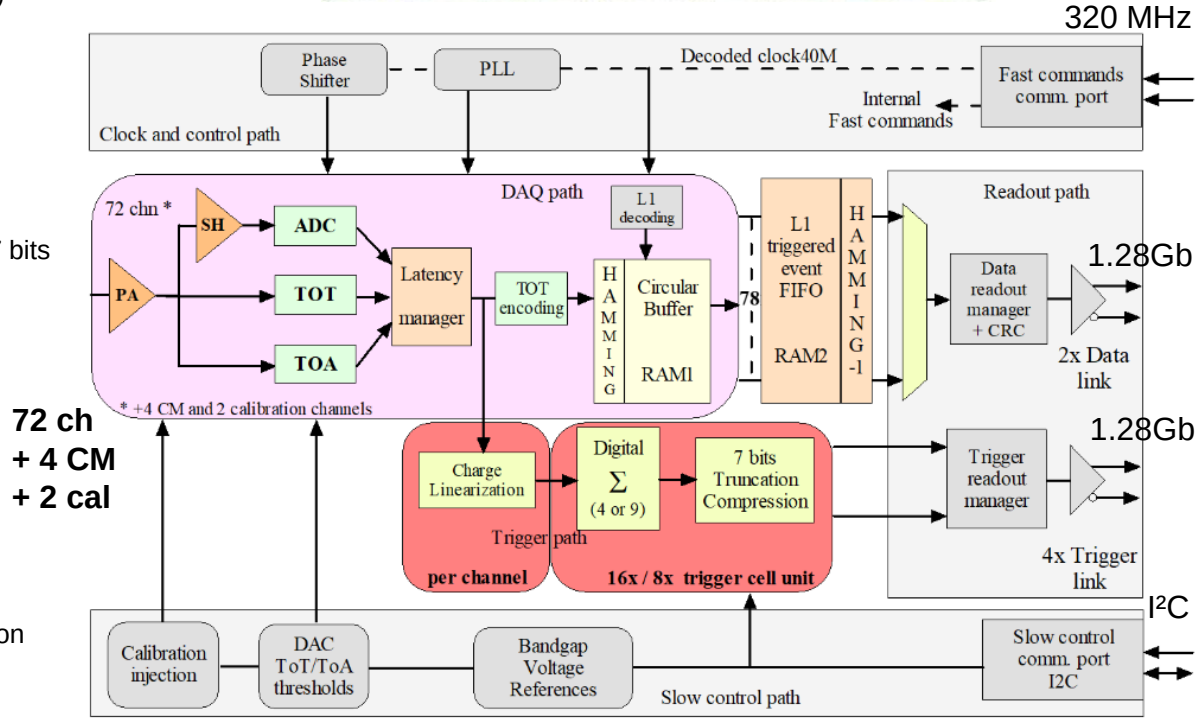
Two data flows
• DAQ path
– 512 depth DRAM (CERN), circular buffer
– Store the ADC, TOT and TOA data
– 2 DAQ 1.28 Gbps links
• Trigger path
– Sum of 4 (9) channels, linearization, compression over 7 bits
– 4 Trigger 1.28 Gbps links

Control
• Fast commands
– 320 MHz clock and 320 MHz commands
– A 40 MHz extracted, 5 implemented fast commands
• I2C protocol for slow control

Ancillary blocks
• Bandgap (CERN)
• 10-bits DAC for reference setting
• 11-bits Calibration DAC for characterization and calibration
• PLL (IRFU)
• Adjustable phase for mixed domain

CMOS 130 nm 15x6 mm





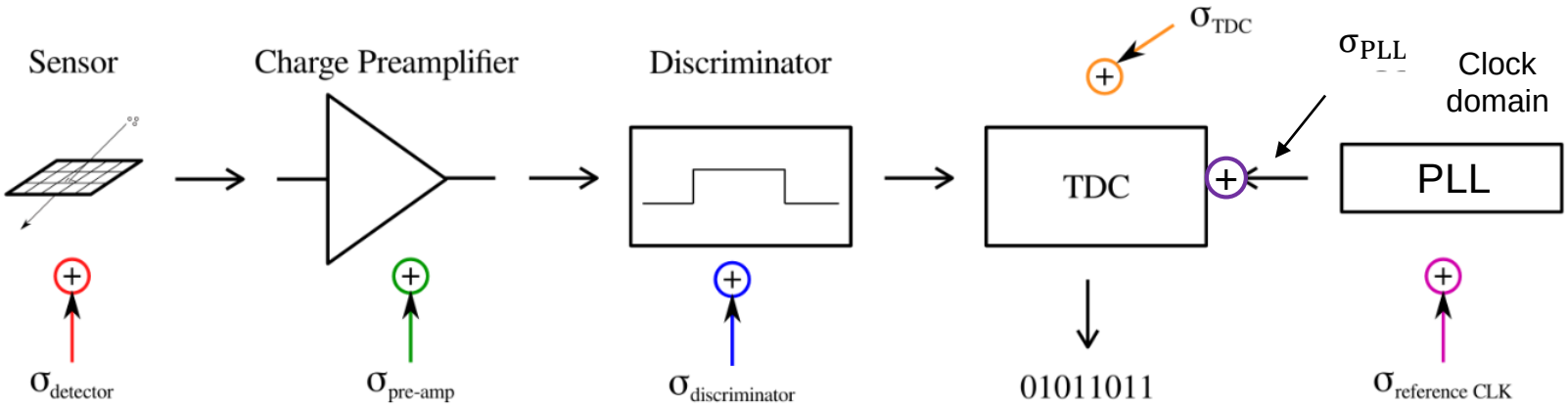
Precision time measurement

high energy showers for pile-up rejection, primary vertex identification

Up to an average of 200 simultaneous proton collisions ➔ imply that timing measurements with resolutions in the 30 ps range will greatly enhance pileup mitigation.

The front-end ASIC (**HGCROC**) provides **time-of-arrival (ToA)** measurement for individual hits with signals above 12 fC (equivalent to 3-10 MIPs), such that clusters with pT>5GeV should have a timing resolution **better than 30 ps**.

The precision of the overall timing measurement depends on the intrinsic performance of the sensor + preamplifier and discriminator, the characteristics of the TDC used for the ToA measurement, and the clock distribution system.

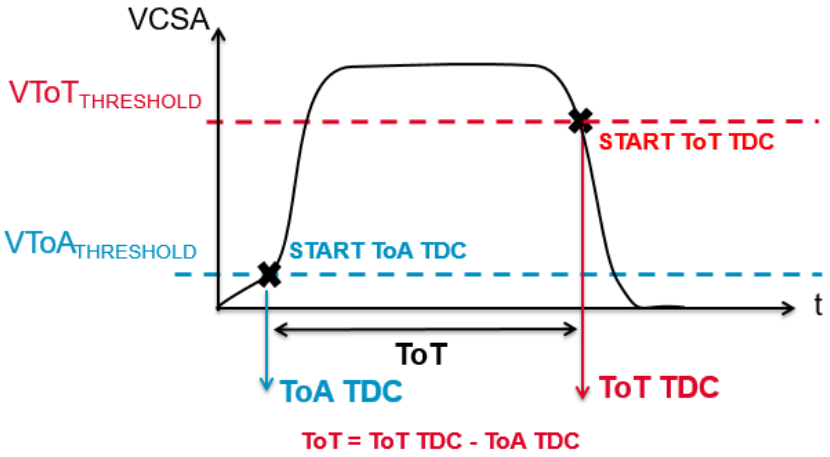


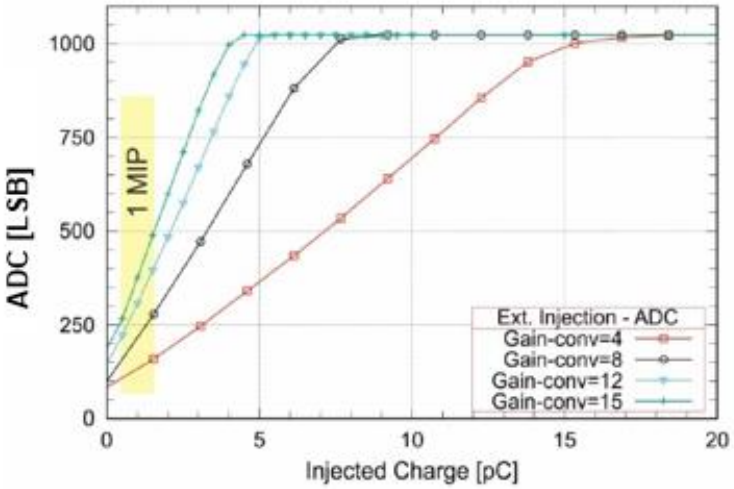
© Time to Digital Converters and results from a new 5ps TDC prototype ASIC1Graz University of Technology / CERNlukas.perktold@cern.chLukas Perktold

Proposed method for energy and time measurements

High dynamic range : 0.2 fC -10 pC (Si) or 300 pC (SiPM)

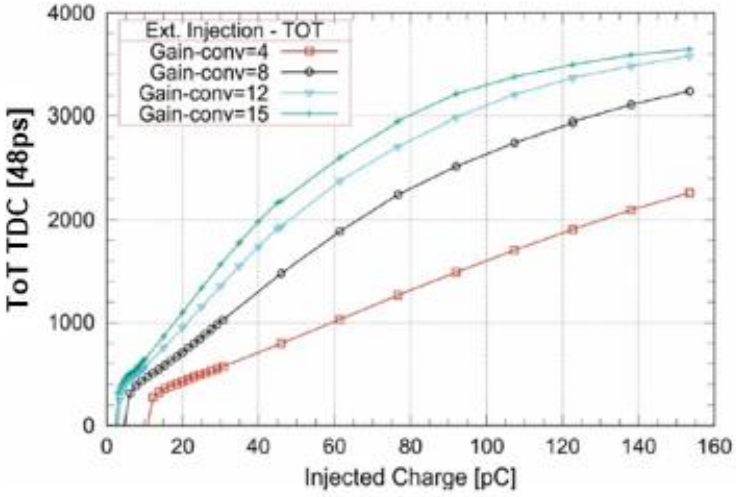
CSA linear regime : the signal goes to a 10-bit SAR-ADC





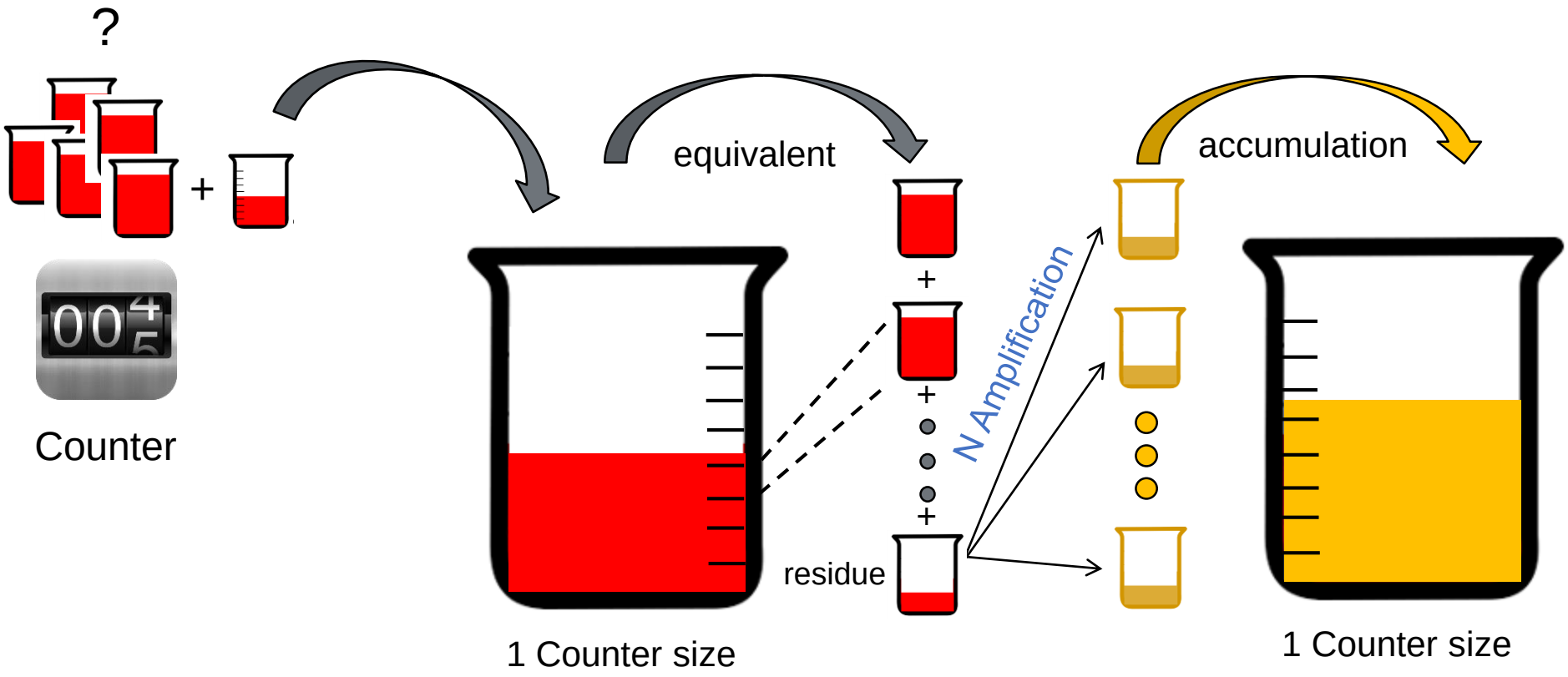
Saturation regime : 12-bit TDC Time-over-Threshold (ToT) with a 50 ps binning up to 200 ns

Fast discriminator associated to a 10-bit TDC provides the ToA with a 25 ps binning in the 25 ns clock preriod

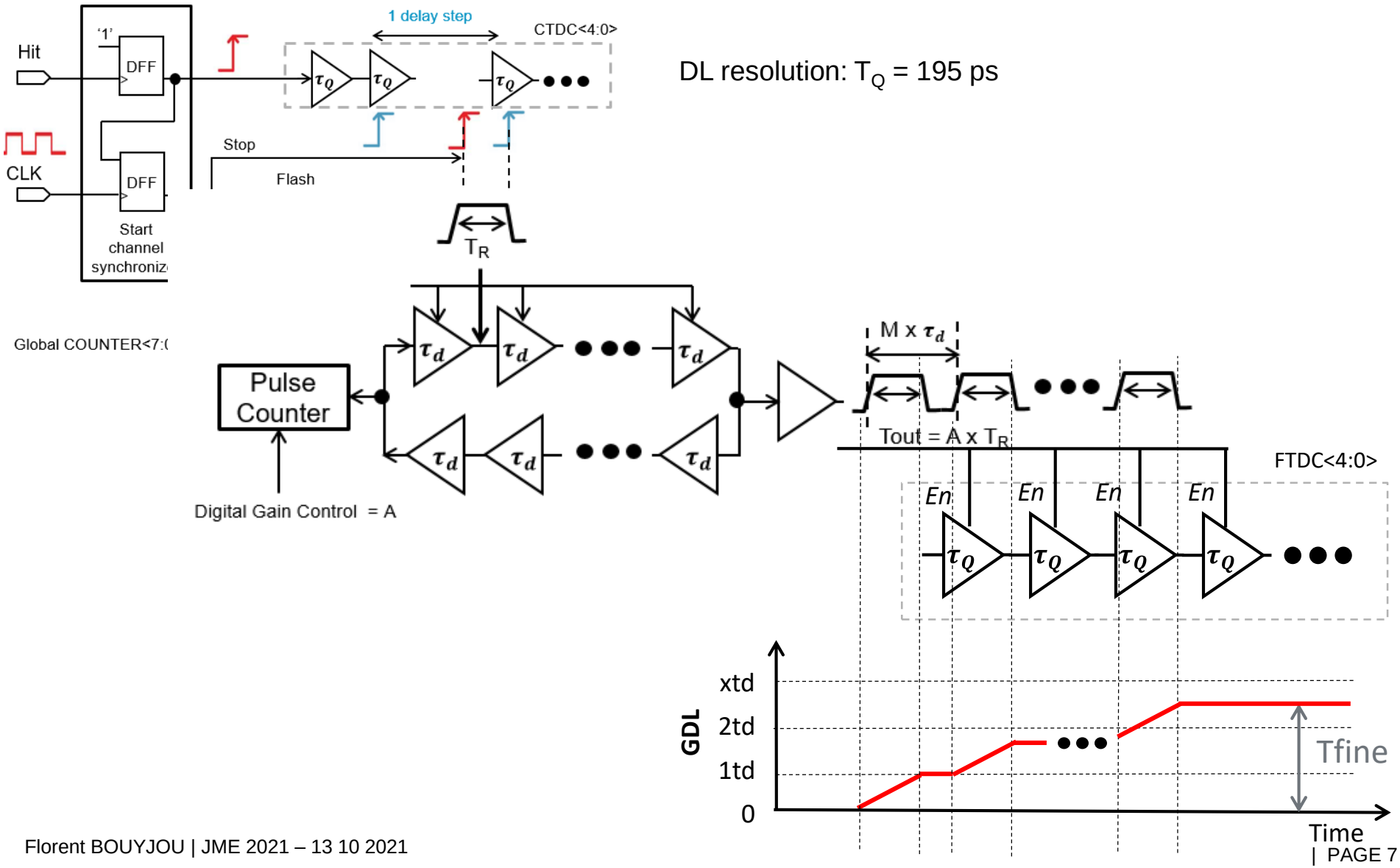


3-steps TDC architecture with Time Amplifier (TA)

3-steps conversion : Introduction to the Pulse-Train Time Amplifier

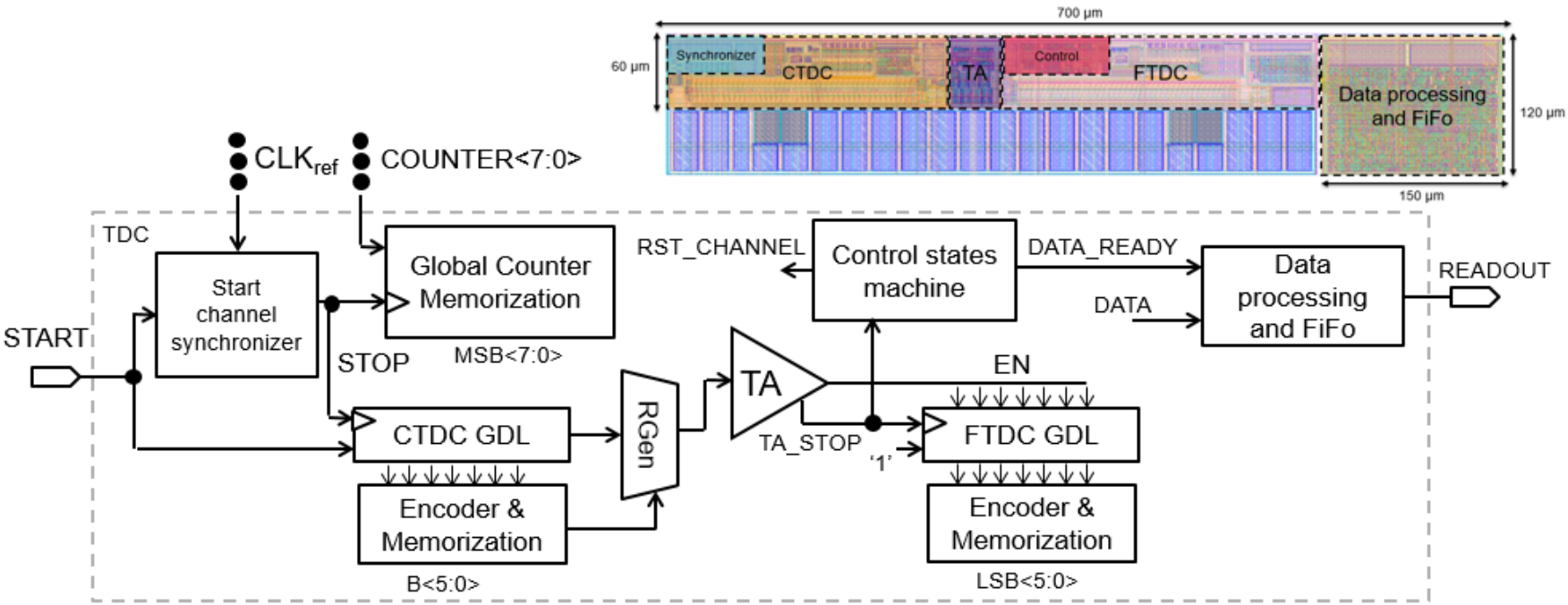


Concept and design of the TA



DL resolution: T_Q = 195 ps

TDC architecture



3-steps TDC architecture :

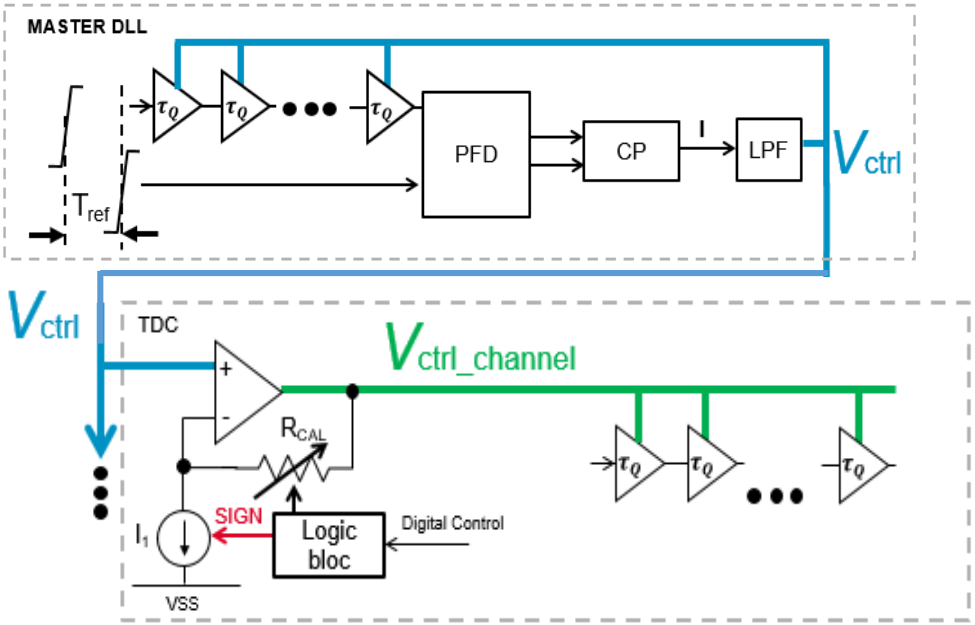
- **PLL 160 MHz** + gray counter 2 bits, LSB_{gray}: 6.25ns
- **Coarse TDC**: 5 bits, LSB_{CTDC}: 195ps
- **Fine TDC**: 3 bits, LSB_{FTDC} : 24.4ps

LSB_{TDC} = 24.4ps ⟹ Optimal σ_t = 7ps

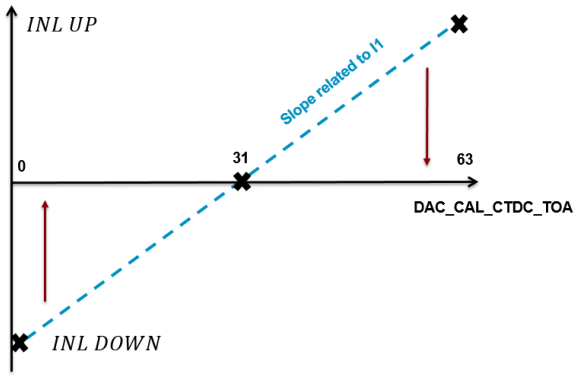
$$D_{out} = D_{counter} \times NA - D_{CTDC} \times A - D_{FTDC}$$

Architectural advantages: high speed conversion (less than 25 ns)
low power consumption (only when an event occurs)

Channel Delay-Line INL gain correction

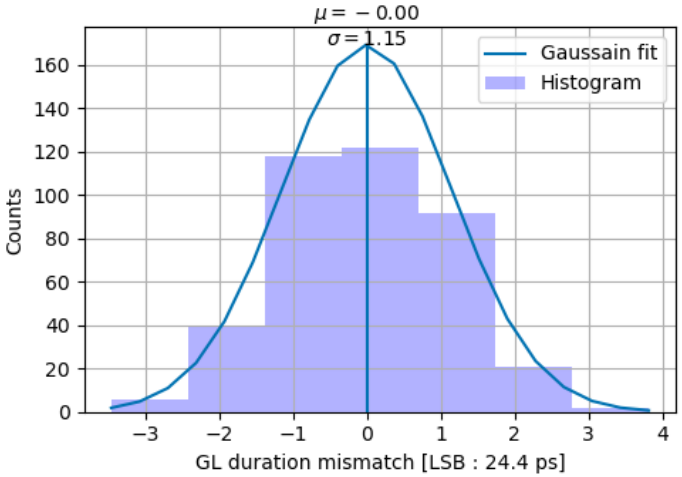


$$V_{ctrl\_channel} = V_{ctrl} + I_1 \boldsymbol{R_{CAL}} + V_{OFF}$$



Effective number of linear bits :

$$N_{linear} = N - log_2(INL + 1)$$



GL Mismatch simulation min max :
-3 LSBs < 0 < 3 LSBs

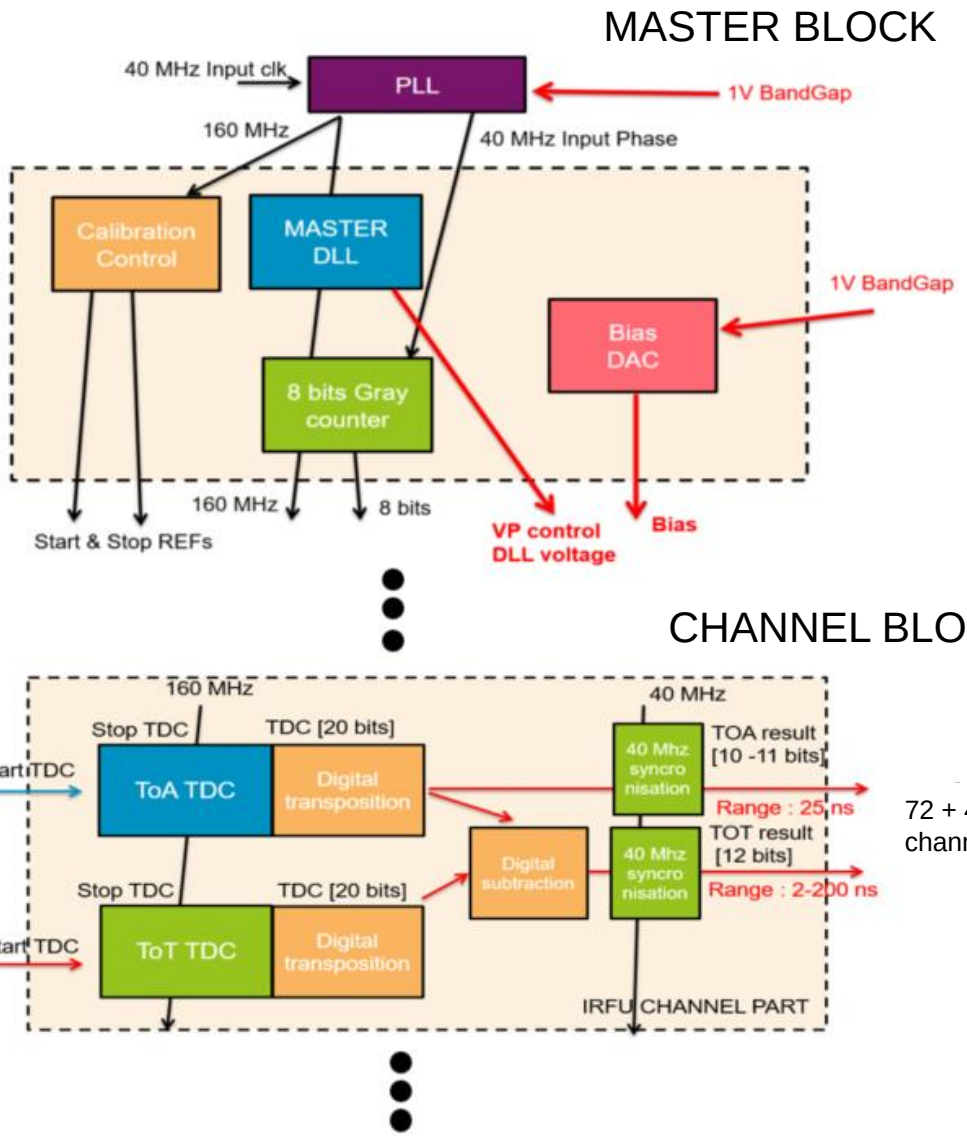
TDC Architectural block diagrams

PLL:

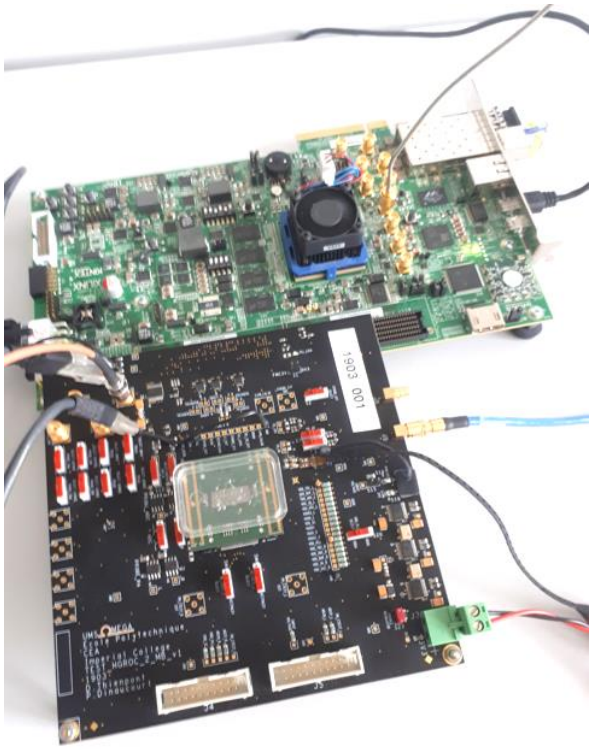
Low jitter so as not to contribute too much to the noise of the TDC.

MASTER DLL :

For a continuous channels calibration
keep channels performance under **temperature and process variations**
Large time range by **adding a counter**



HGCROC2 Test Setup



Code density test :

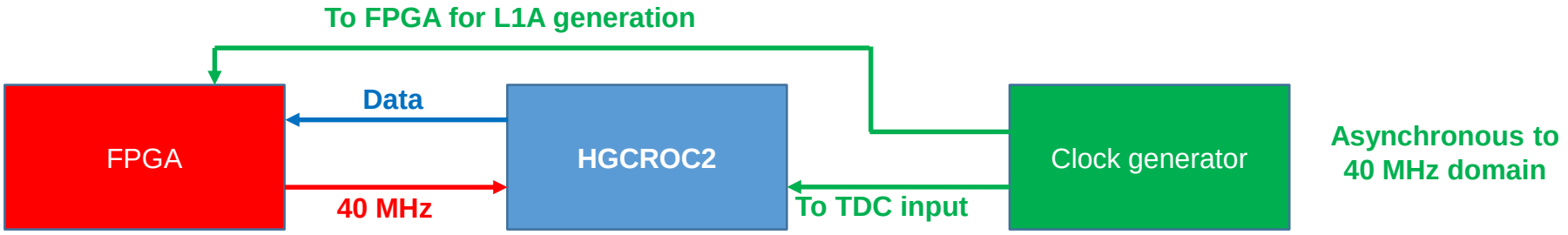
Uniformly distributed events across clock cycle (Asynchronous clock domains)

2 external trigger inputs for the 72 channels

Performance evaluated by measuring the Δt between 2 channels:

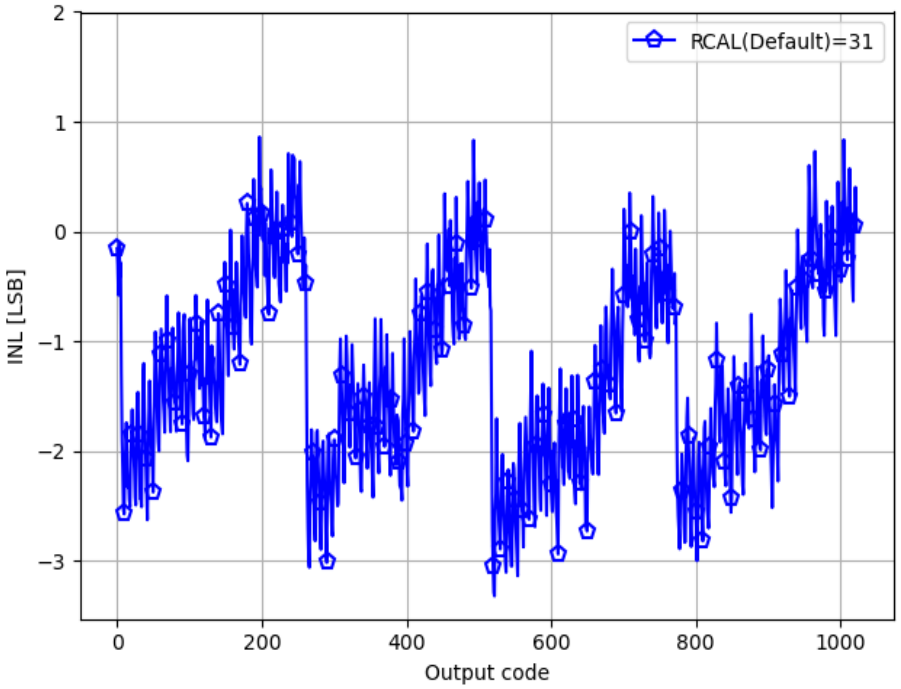
$$\sigma t = \sigma \Delta t / \sqrt{2}$$

External uncorrelated clock as the TDC input



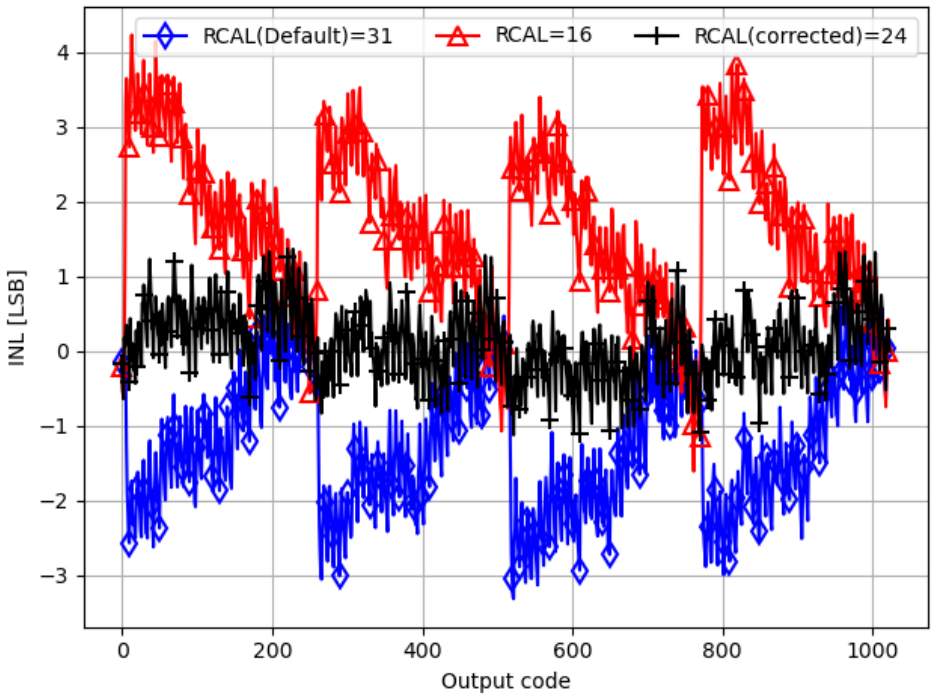
Channel Delay-Line INL gain correction

Integral-Non-Linearity



Maximum INL is 3.4 LSB

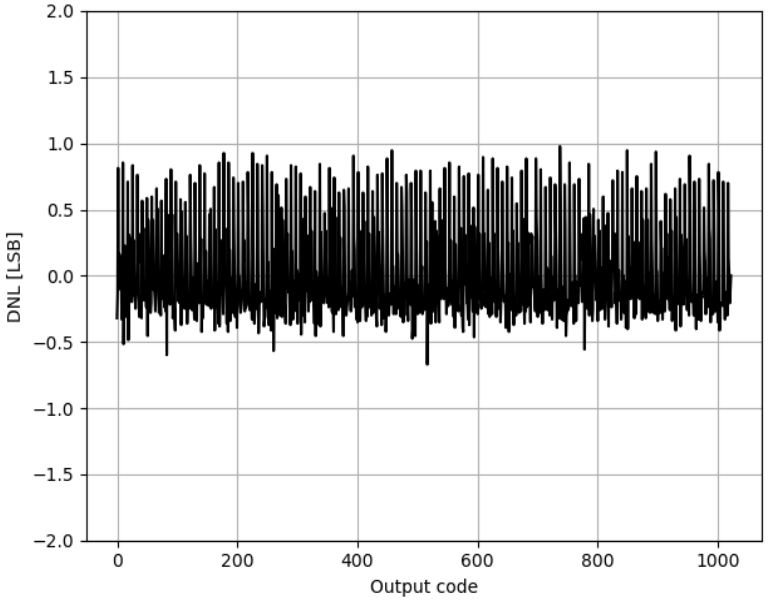
Channel gain fine tunning



Best configuration is the black curve
INL is -1.1/1.4 LSB

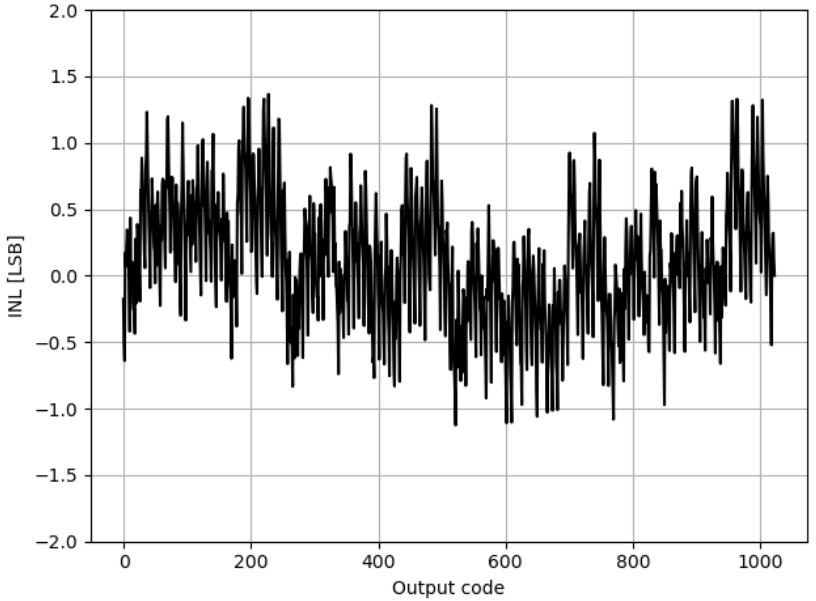
Channel Delay-Line INL gain correction

Differential-Non-Linearity



DNL is -0.7/1 LSB

Integral- Non-Linearity

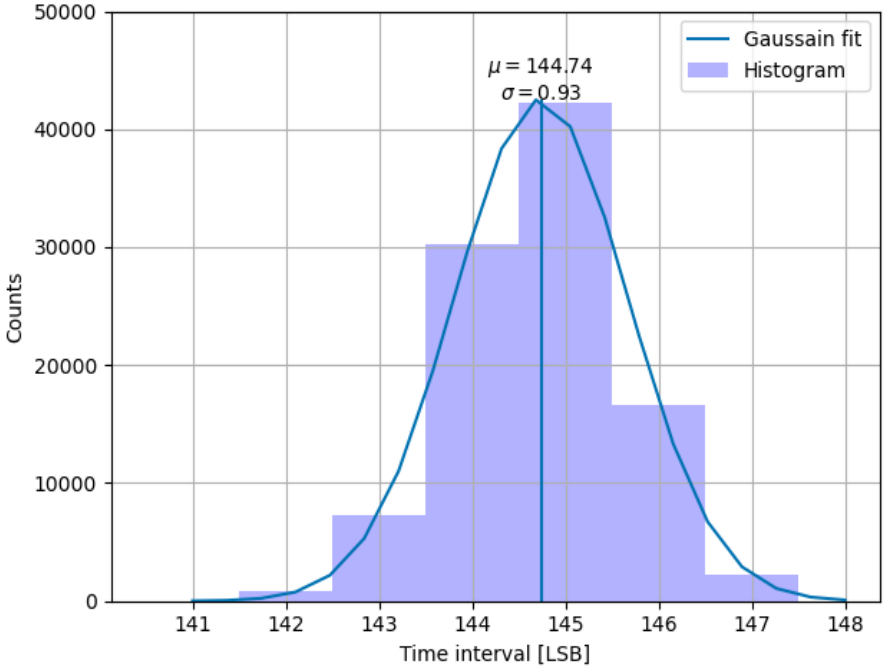


INL is -1.1/1.4 LSB

ToA TDC timing precision

Timing precision looking at Δt between 2 channels with channel 0 as reference
Expressed as σ of the distribution obtained with internal INL correction

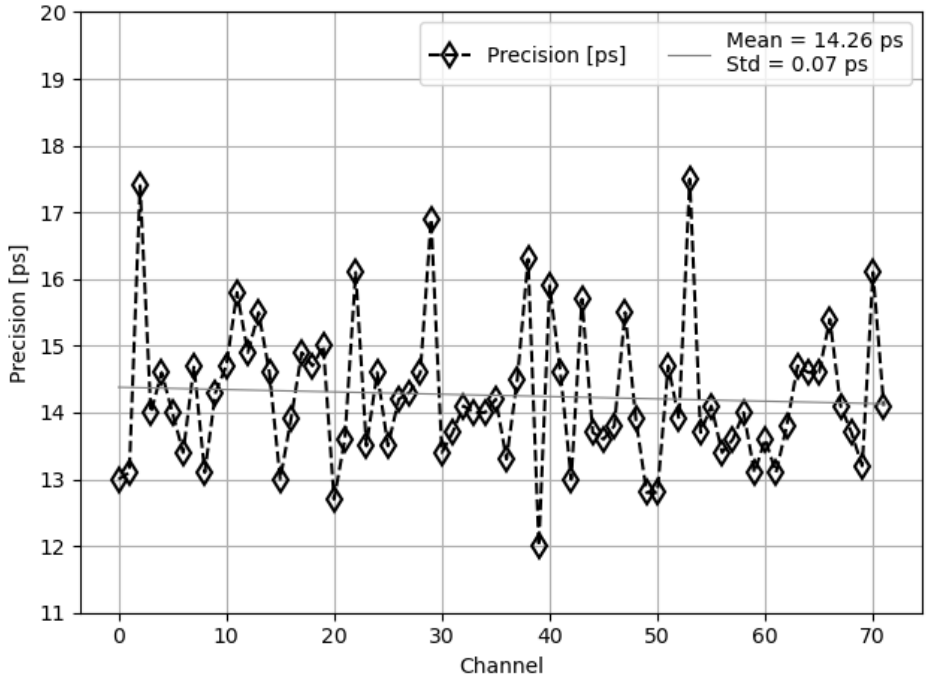
Exp : Channel 40 ➔
delayed by 1.5 m SMA cable



Single Shot Resolution

Sigma x 24.4 ps / √2 = **16 ps RMS**

All channels



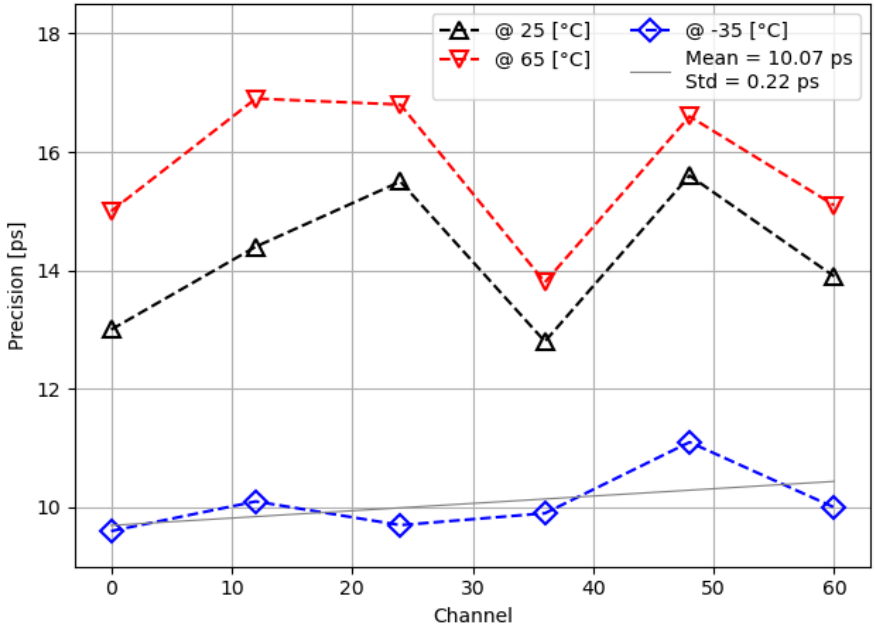
Mean Single Shot Resolution

14.26 ps RMS

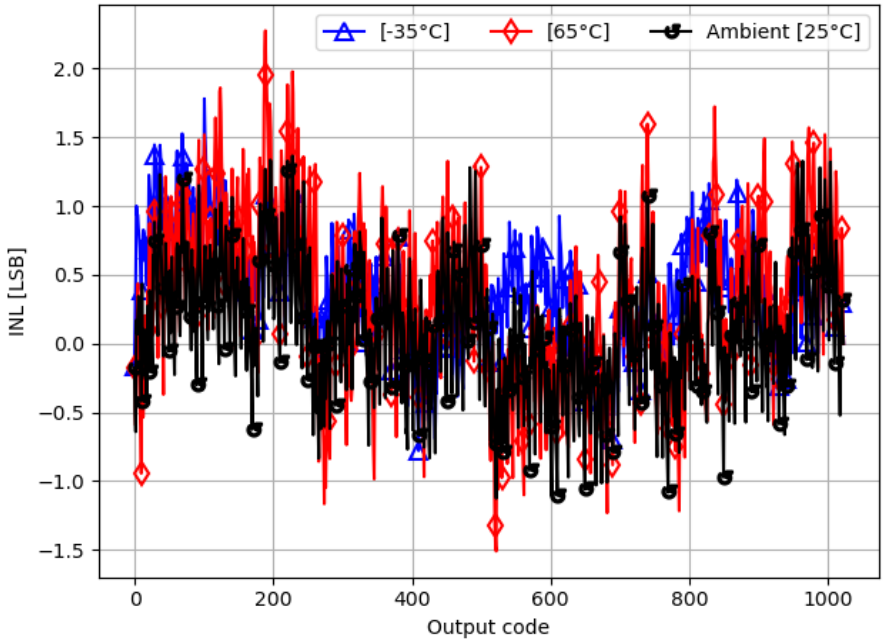
ToA TDC timing precision

Precision and INL through temperature
Ambient temperature calibration 25°C and we observe channel temperature variations temperature range of −35 / 65 °C.

Single Shot Resolution



Integral- Non-Linearity



Mean precision:
10,1 ps at -35°C
14,1 ps at 25°C
15,8 ps at 65°C

Summary and next steps

Multichannel ToA TDC: 10 bits with 25 ns total range is covered with a 14.26 ps precision at ambient temperature
Power consumption is about 2.2 mW at a 40 MHz measurement rate or 100 µW if there is no event.

Master DLL and channel Delay-Line INL gain correction :
- INL is reproducible and stable with time and temperature
- Channel-by-channel fine tuning validates
  INL < 2 LSB achievable

Some TDC channels have issue for some conversion: we can observe outliers corrected in next version **HGCROC3.**

HGCROC3 received in september 2021 with first encouraging measures
- TID and SEU upgrades
- Leakage current optimization
- Calibration modes