

DIAMASIC

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O. Rossetto^a, L. Tribouilloy^a, and CAO LPSC

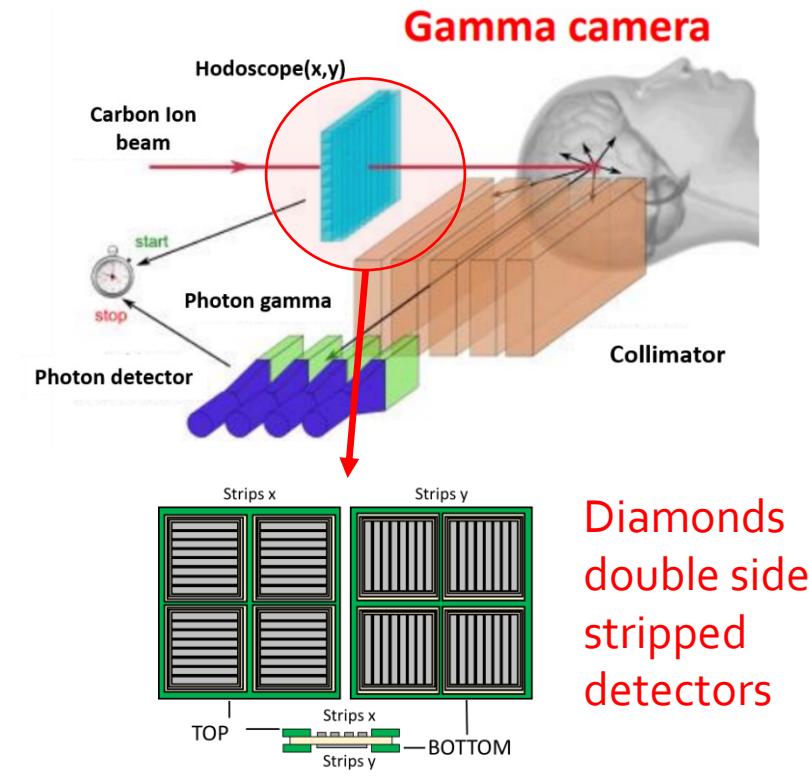
SCHEDULE

- Project overview
- Electronic Design
 - Front-end
 - Time to Digital Converter (TDC) → **L. Leterrier talk**
 - Charge to Digital Converter (QDC)
 - Analog to Digital Converter (ADC)
- Conclusions

PROJECT OVERVIEW

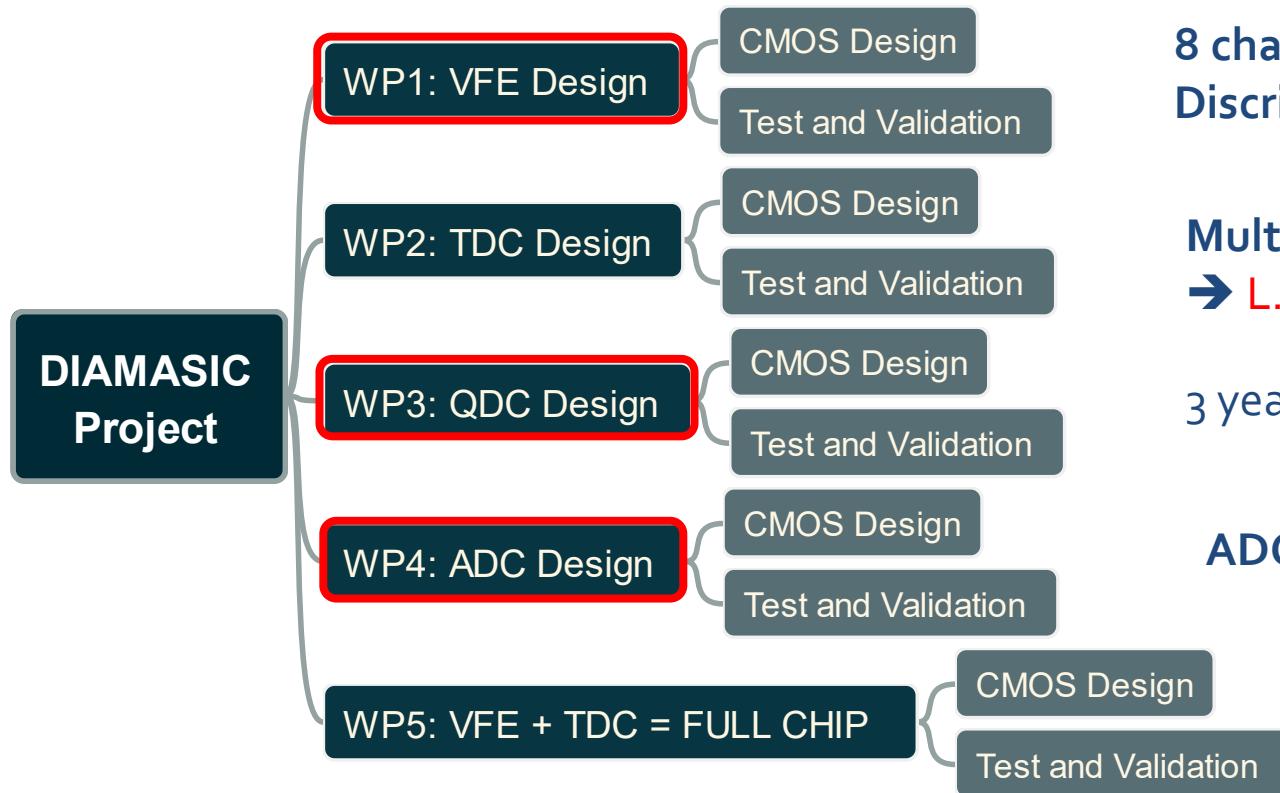
- Medical physics
 - Particle therapy hodoscope: position + time stamp
- Using diamond as detector material:
 - Intrinsic radiation hardness
 - Fast signal risetime enables timing precision of a few tens of ps
 - Low noise
 - Cost
 - Availability of large area
- Beam tagging hodoscope for online ion range verification in hadrontherapy:
 - Time resolution of 100 ps
 - Count rate of 10 MHz/channel
 - Spatial resolution ≈ 1 mm
 - Radiation hard
- Charge measurement
 - ADC with noise shaping principle
 - QDC

Property	Units	Diamond	Silicon
Band Gap E_g	eV	5.47	1.12
Electron mobility μ_e	$\text{cm}^2 / \text{V}\cdot\text{s}$	1700	1420
Hole mobility μ_h	$\text{cm}^2 / \text{V}\cdot\text{s}$	2100	470
Saturation velocity	cm / s	2×10^7	1.4×10^7
Intrinsic carrier density	cm^{-3}	$< 10^3$	1.5×10^{10}
e/h pair energy	eV	13	3.6
Displacement energy	eV	37-47	15-20
Density	g cm^{-3}	3.52	2.33
Rad length X_0	cm	12.2	9.4
Dielectric constant ϵ_r (relative)		5.7	11.9
Breakdown E-Field	V/ μm	1000	30
Resistivity	Ω/cm	$> 10^{15}$	$10^5 - 10^6$



More information:
Talk M.-L. Gallin-Martel
F.R.A.R.E DIAMANT Journée des métiers de l'électronique de l'IN2P3 et de l'IRFU

WP OVERVIEW



Design of multi channel Integrated Circuits:
CMOS 130nm process technology
Radiation tolerant technology
BB130: 1st R&T

8 channel Trans Impedance Amplifier (TIA) + Fast Discriminator: PhD EEATS Grenoble

Multi channel TDC
→ L. Leterrier talk

3 years apprentice engineer (Grenoble INP – PHELMA)

ADC with noise shaping: PhD EEATS Grenoble

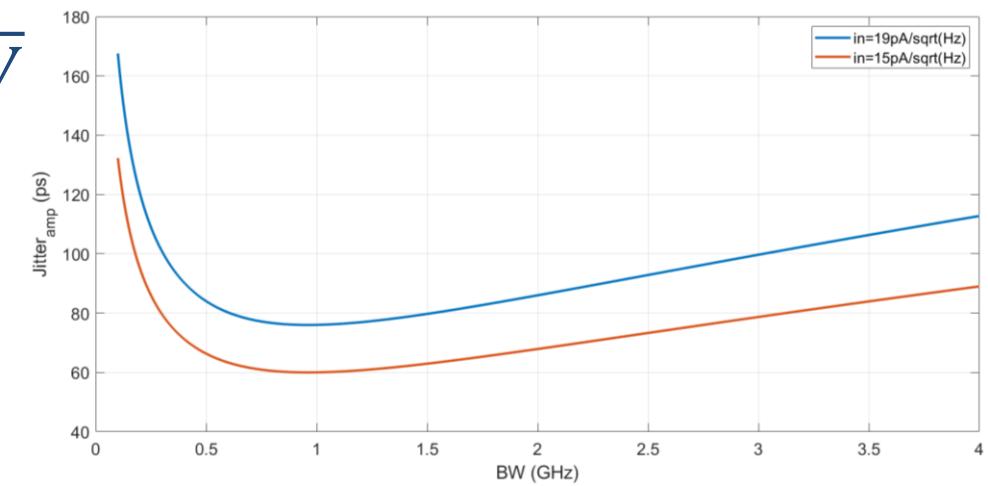
TIMING RESOLUTION

- Part of PhD work
- Timing resolution defined by: $\sigma_t = \sqrt{\sigma_{Jitter}^2 + \sigma_{TimeWalk}^2 + \sigma_{TDC}^2}$
- For fast system, $\sigma_{Jitter} = \frac{T_{rise}}{SNR'}$

$$SNR = \frac{dV}{\sigma_n} \quad \sigma_n = G_{TIA} \times i_n \times \sqrt{\alpha \times BW}$$

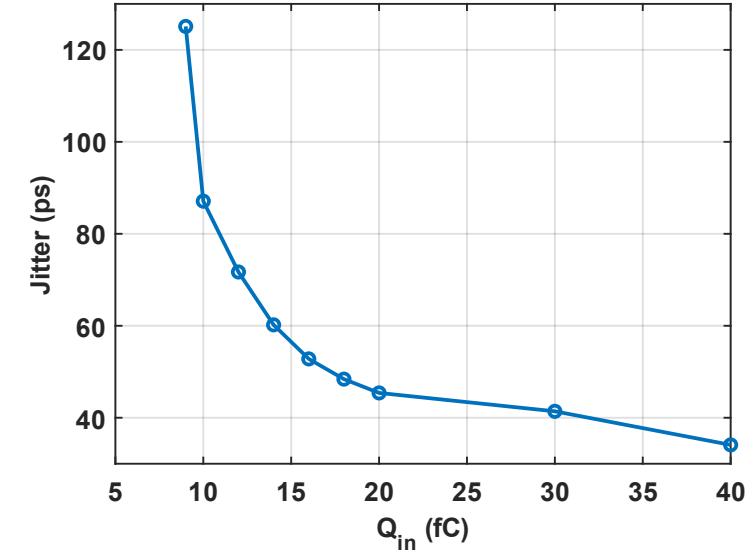
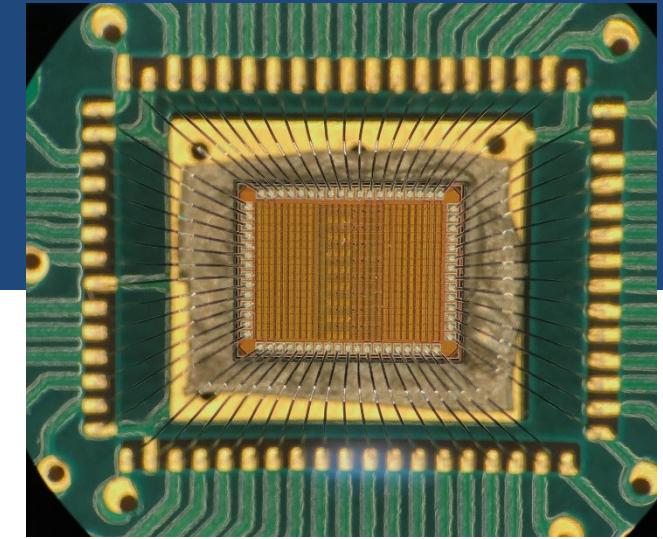
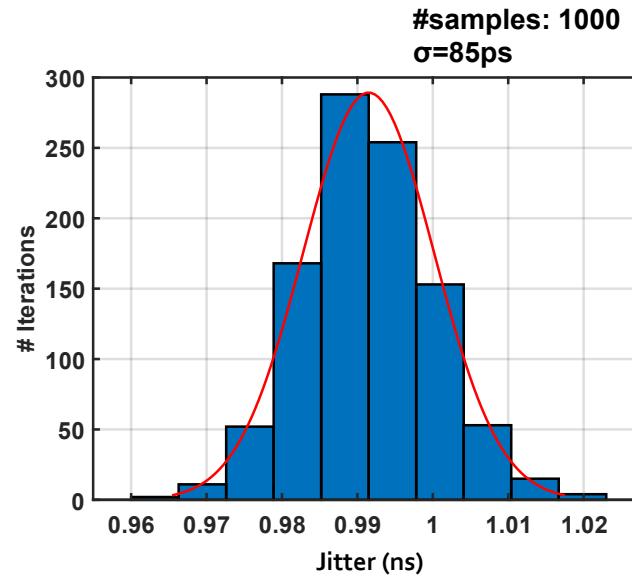
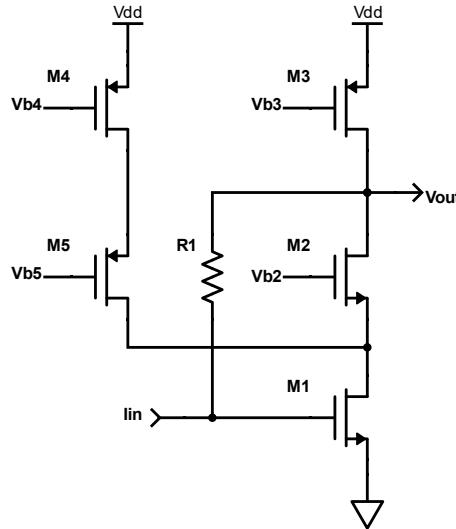
- We define a new expression:

$$\sigma_{Jitter} = \frac{i_n \times \sqrt{\alpha \times BW} \times T_r}{I_{inmax}}$$



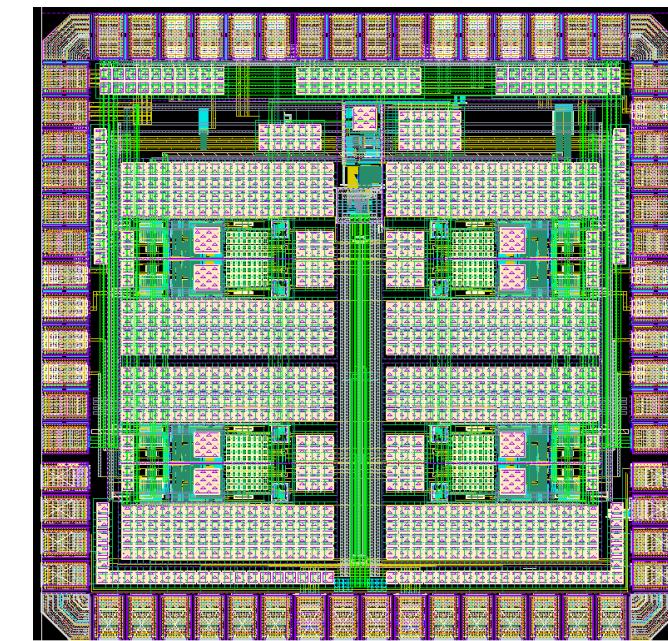
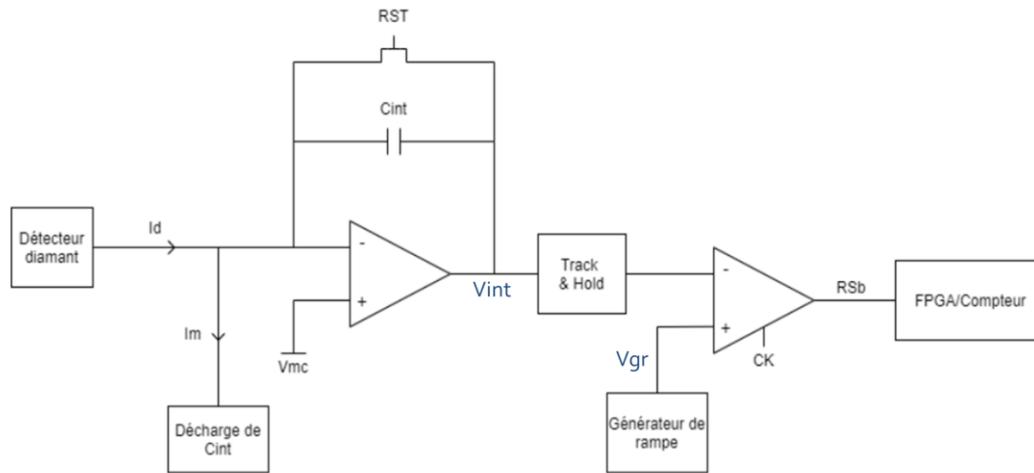
WP1: VFE DESIGN

- Several FE was studied, designed and tested:
 - Common gate stage
 - LNA stage
 - **Resistive feedback TIA**



WP3: QDC DESIGN (1)

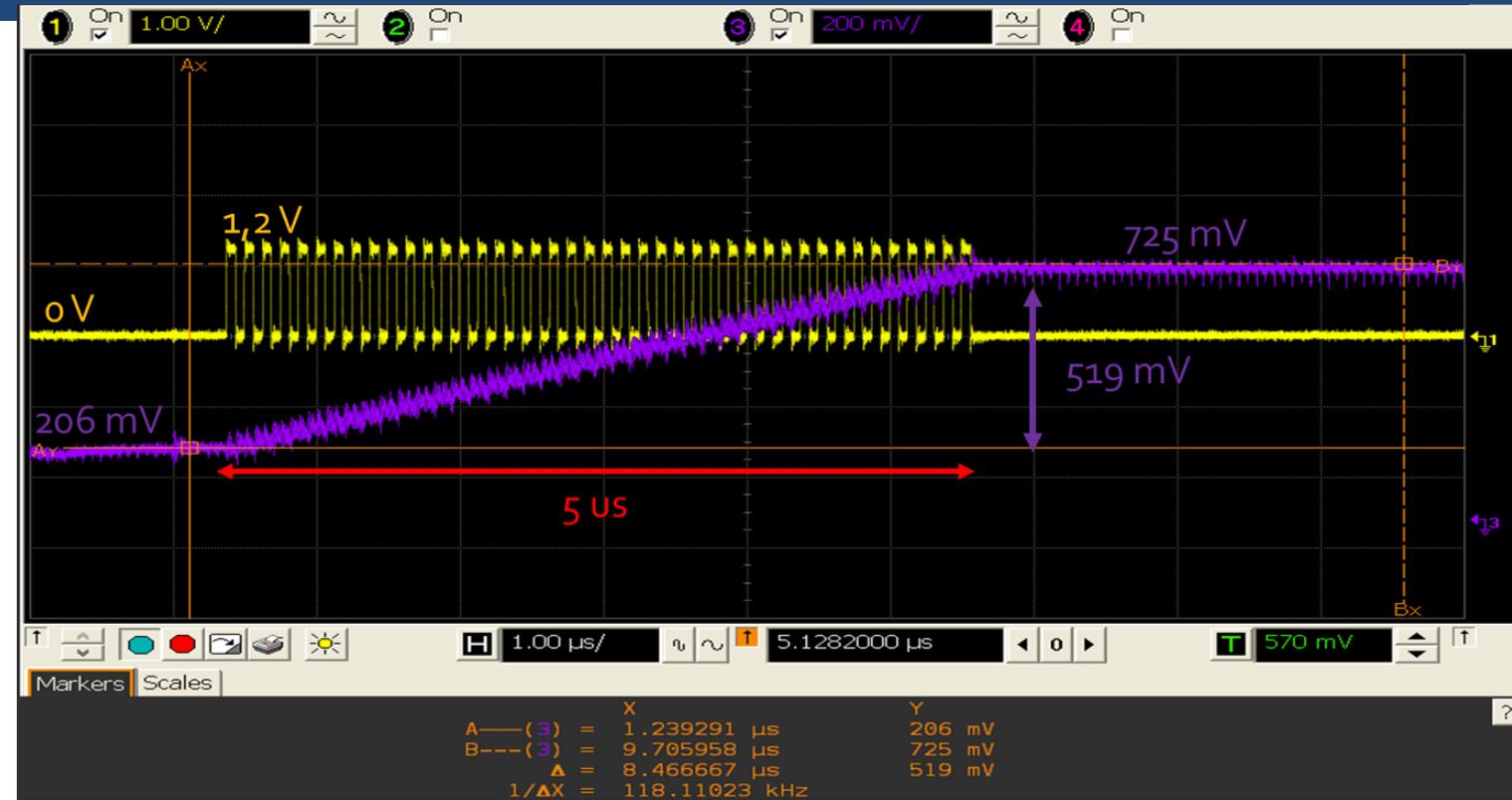
- 3 years apprentice engineer (Grenoble INP – PHELMA)
- Specifications:
 - Input Current range: $10\text{nA} - 100\mu\text{A}$
 - Integration time: 1 ms to 100ms
 - Charge dynamic range of 10^6



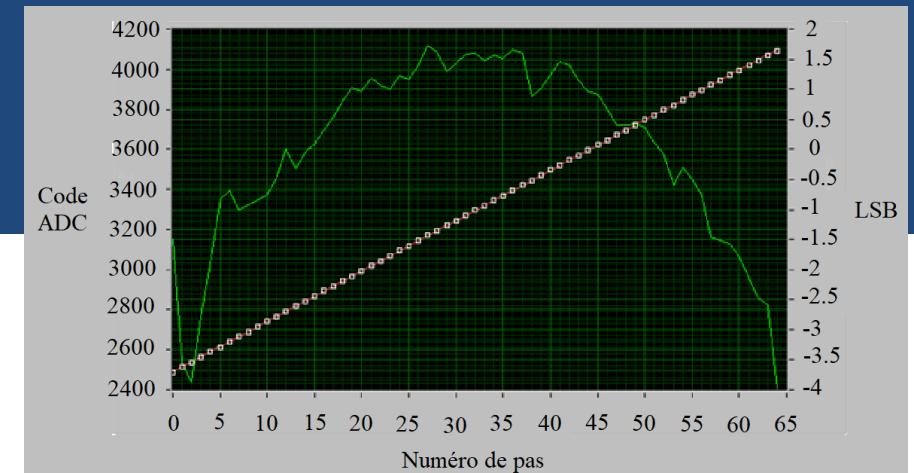
One QDC channel: $523 \mu\text{m} \times 247 \mu\text{m}$

FULL chip:
1.5 mm x 1.5 mm
8 channels
Submitted on May 2021

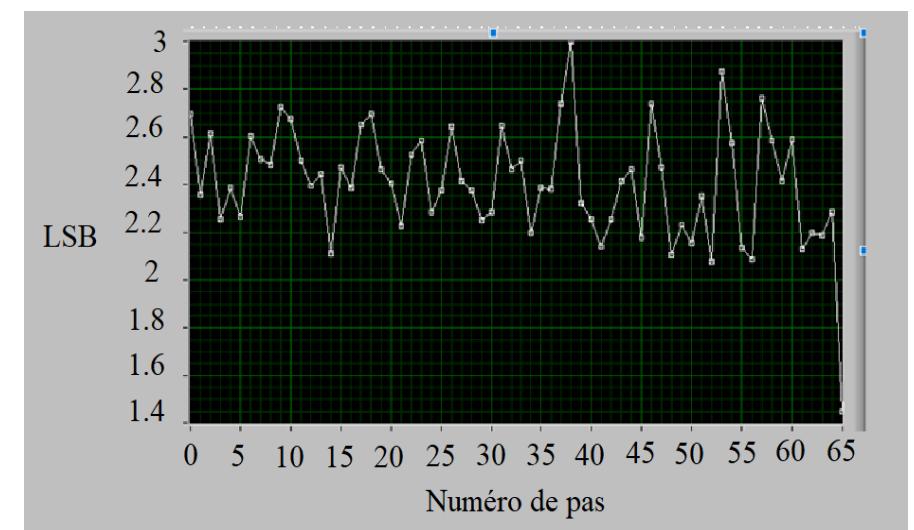
WP3: QDC DESIGN (2)



Testing of the ramp generator with 40 steps



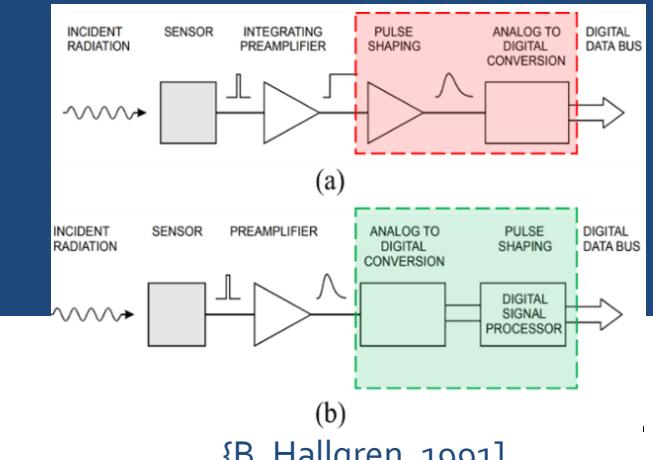
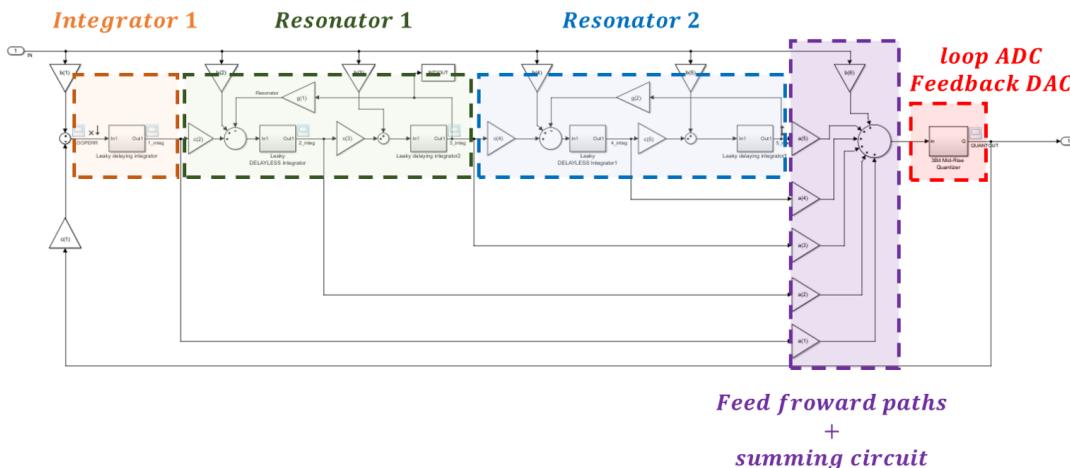
INL: -4 LSB/+2 LSB



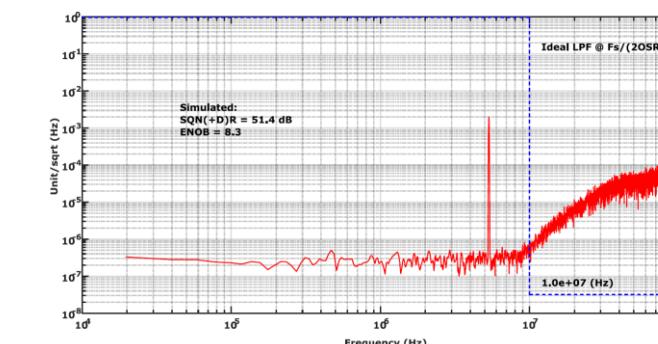
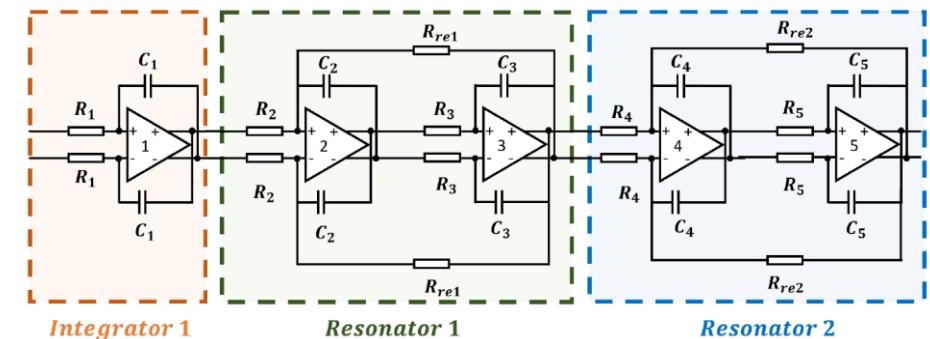
Max noise: 3 LSB

WP4: ADC DESIGN

- PhD EEATS in microelectronics
 - Started in 2018
 - “*Design of a continuous time Delta-Sigma modulator for energy measurement using diamond detectors*”
 - Design Top-Down
 - Will be defended on October, 28th 2021 in Grenoble



{B. Hallgren, 1991}



CONCLUSION

- IN₂P₃ R&T project
 - 2 labs: LPSC and LPC Caen
- Design of several IP blocks available through BB130 project
 - Current/Voltage mode DAC, 5 bits
 - SPI control (32 bits)
 - TIA
 - TDC
- PhD student and 3 years apprentice engineer involved in the project

PUBLICATIONS

Abderrahmane Ghimouz et al. “A Preamplifier-discriminator circuit based on a Common Gate Feedforward TIA for fast time measurements using diamond detectors.” In: 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS). 2018, pp. 281–284. DOI: 10.1109/ICECS.2018.8617950

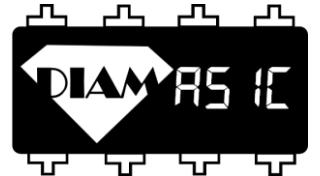
Abderrahmane Ghimouz, et al.. “Systematic high-level design of a fifth order Continuous-Time CRFF Delta Sigma ADC.” In: 2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS). 2021, pp. 1–4. DOI: 10.1109/LASCAS51355.2021.9459156

Abderrahmane Ghimouz et al. “A multichannel front-end electronics ASIC for high-accuracy time measurements using diamond detectors.” In: International Conference on Analog VLSI Circuits 2021.(accepted and will be presented soon)

Abderrahmane Ghimouz, et al.. “DIAMASIC: A multichannel front-end electronics for high-accuracy time measurements for diamond detectors.” In: TWEPP 2021 Topical Workshop on Electronics for Particle Physics. 2021. (Presented and an extended journal paper in under preparation for JINST)

Abderrahmane Ghimouz, et al.. “New Design Approach of Front-End Electronics for high-Accuracy Time Measurement Systems.” In: 2021 28th IEEE International Conference on Electronics, Circuits and Systems (ICECS). 2021 (accepted and will be presented soon)

Abderrahmane Ghimouz, et al.. “Designing Opamp amplifiers for a 5th order CT CRFF DS ADC using Model-based design paradigm and gm/ID methodology.” In: International Conference on Analog VLSI Circuits 2021. (accepted and will be presented soon).



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