



Laboratoire
de Physique
des 2 Infinis

Irène Joliot-Curie

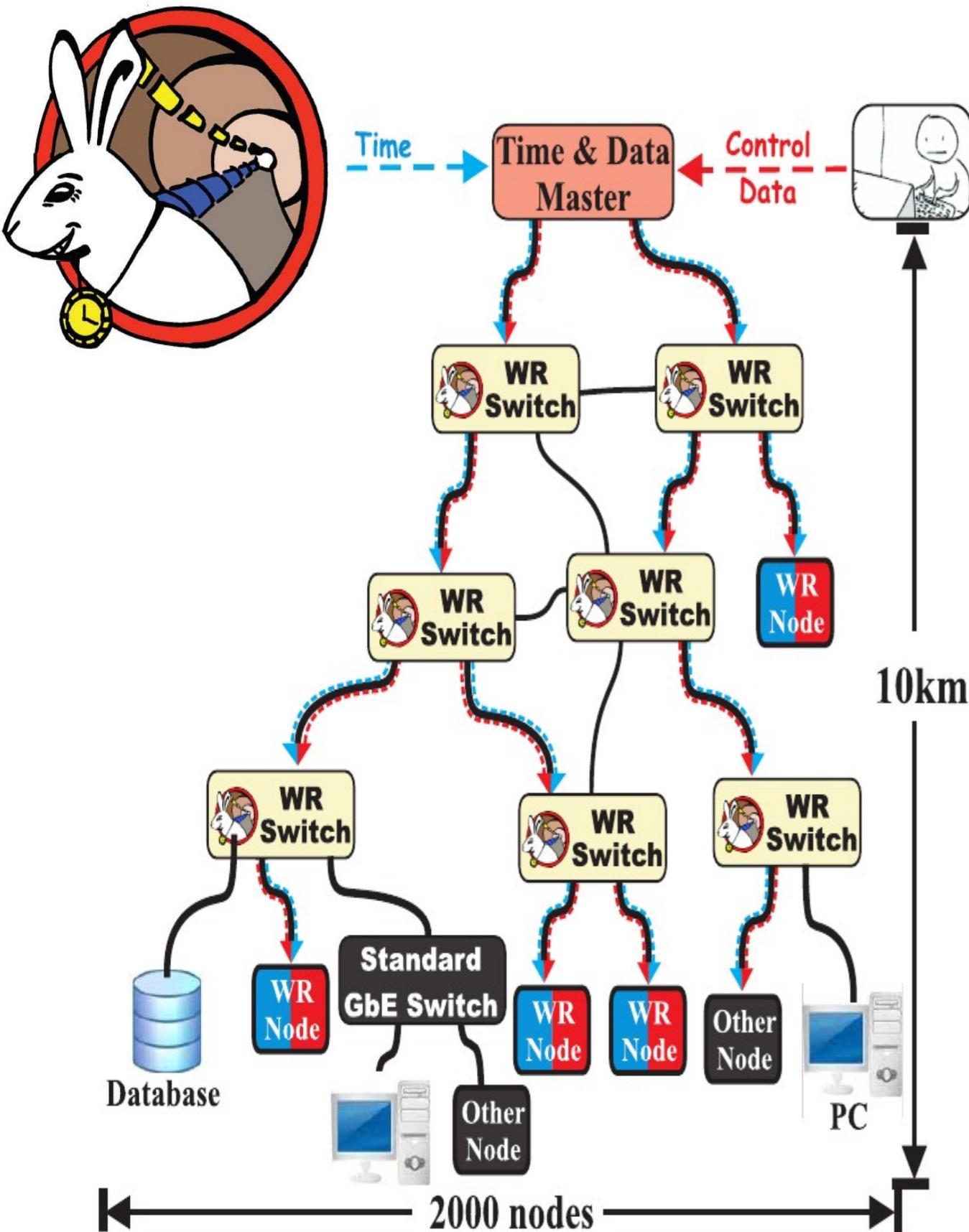
Dissémination du temps et des fréquences avec le WhiteRabbit



Plan

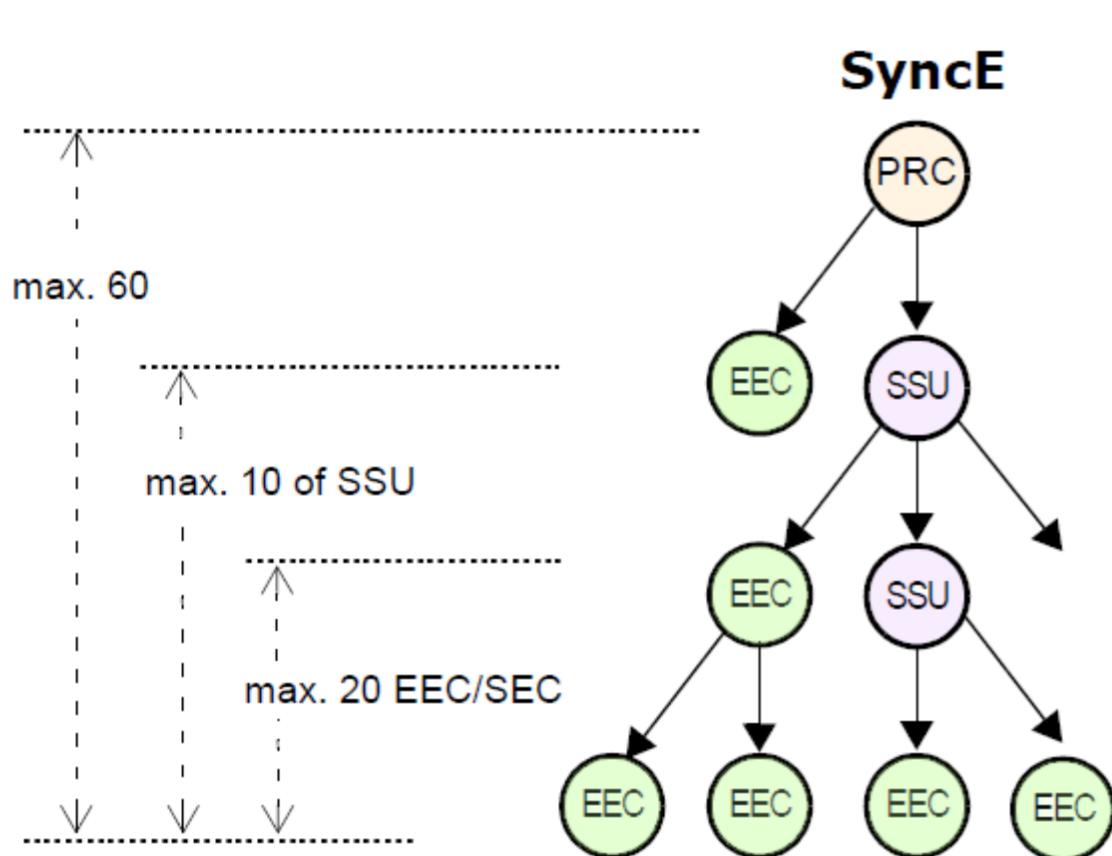
- WhiteRabbit
- IDROGEN board
- R & T TIMED
- T+REFIMEVE

White Rabbit - enhanced Ethernet

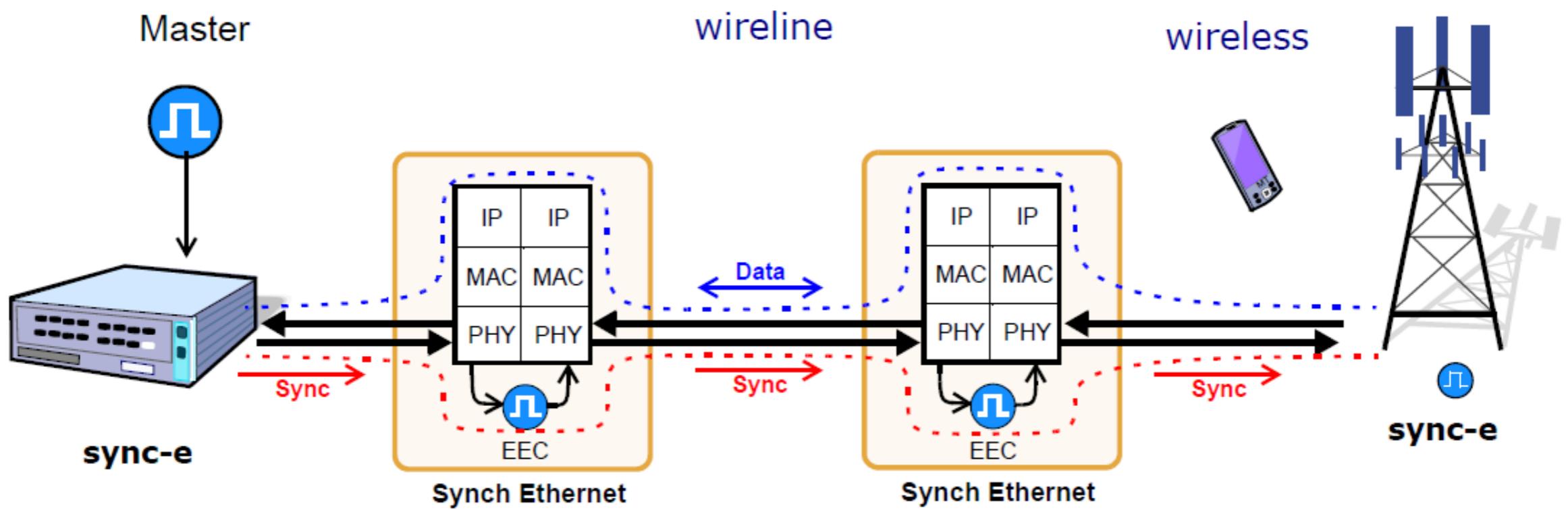


- Two separate services (enhancements to Ethernet) provided by WR
 - High accuracy/ precision synchronisation
 - Deterministic, reliable and low latency Control data delivery
- Sub-ns accuracy and sub-ps precision combination of :
 - Precision Time Protocol (IEEE1588).
 - Synchronous Ethernet.
 - DDMTD phase tracking.
- Low latency
 - 7th Class of service (priority)
- Control data send in control message
 - High Priority HP
- Reliability
 - Forward Error correction

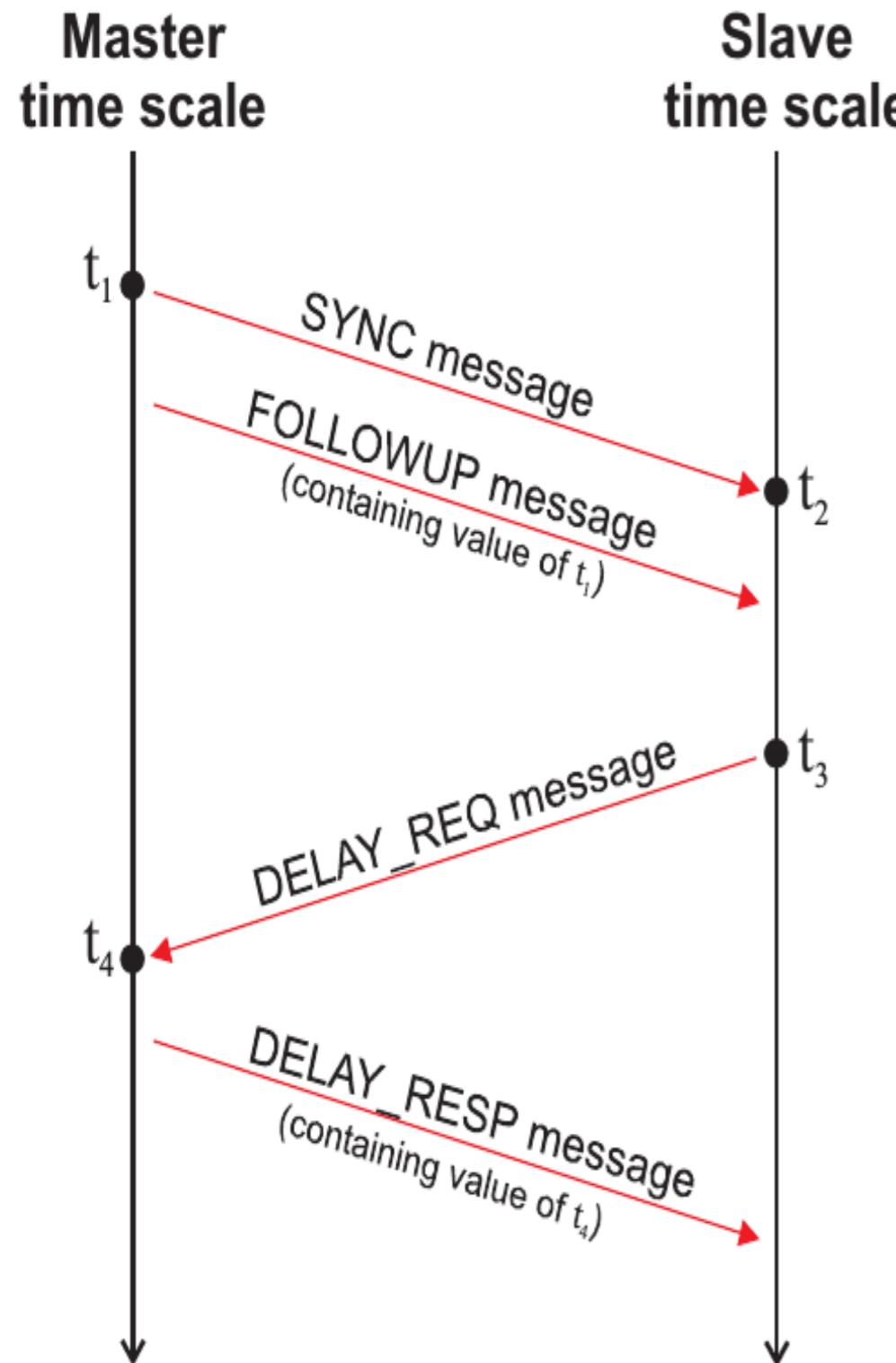
Synchronous Ethernet (Sync-E)



- All network nodes use the same physical layer clock,
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip(PHY)
- A master and unique clock for the whole network
- Synchronous digital hierarchy
- High precision clock definition, 20 better than standard Ethernet clock



Precision Time Protocol (IEEE1588)

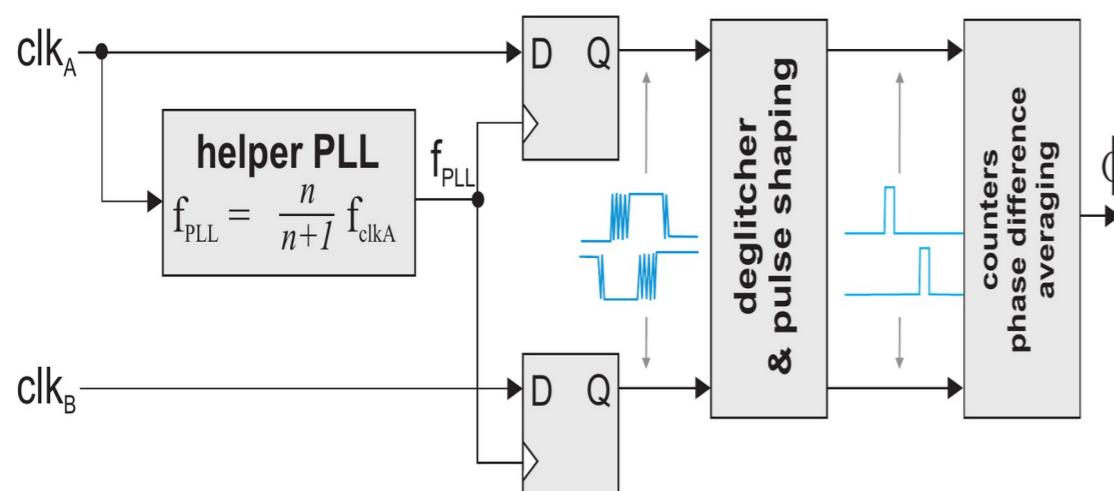


- Packet-based synchronization protocol
- Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.
- Link delay evaluated by measuring and exchanging packets tx/rx timestamps
- PTP is used only for compensation clock offset

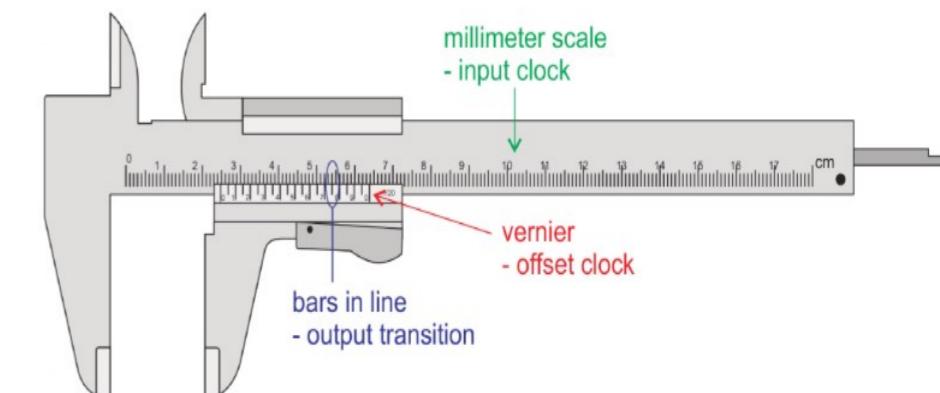
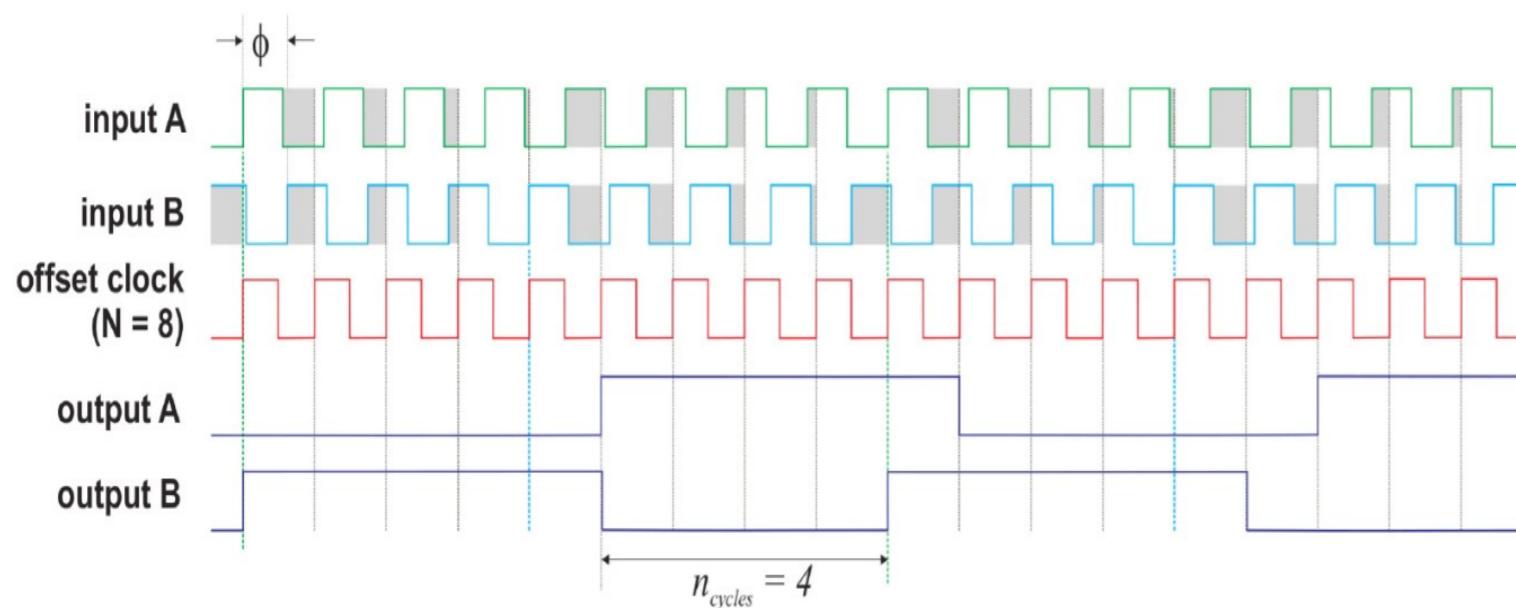
Having values of $t_1 \dots t_4$, slave can:

- calculate one-way link delay:
$$\delta_{ms} = ((t_4 - t_1) - (t_3 - t_2)) / 2$$
- syntonize its clock rate with the master by tracking the value of $t_2 - t_1$
- compute clock offset:
$$\text{offset} = t_2 - t_1 + \delta_{ms}$$

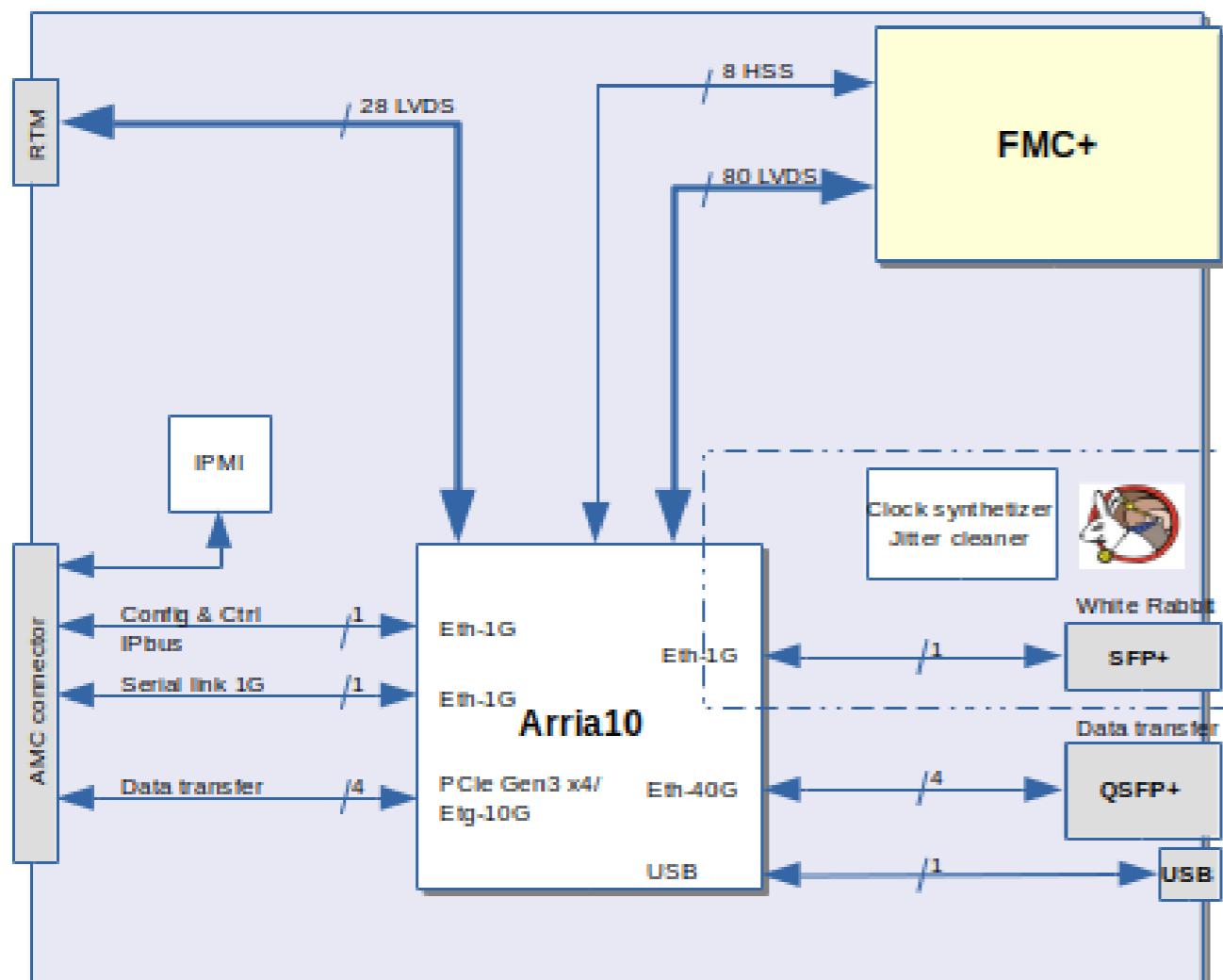
Digital Dual Mixer Time Domain phase detector



- Measure the phase shift between transmit and receive clock on the master side, taking the advantage of Synchronous Ethernet.
- Monitor phase of bounced-back clock continuously.
- Phase-locked loop in the slave follows the phase changes Measured by the master.

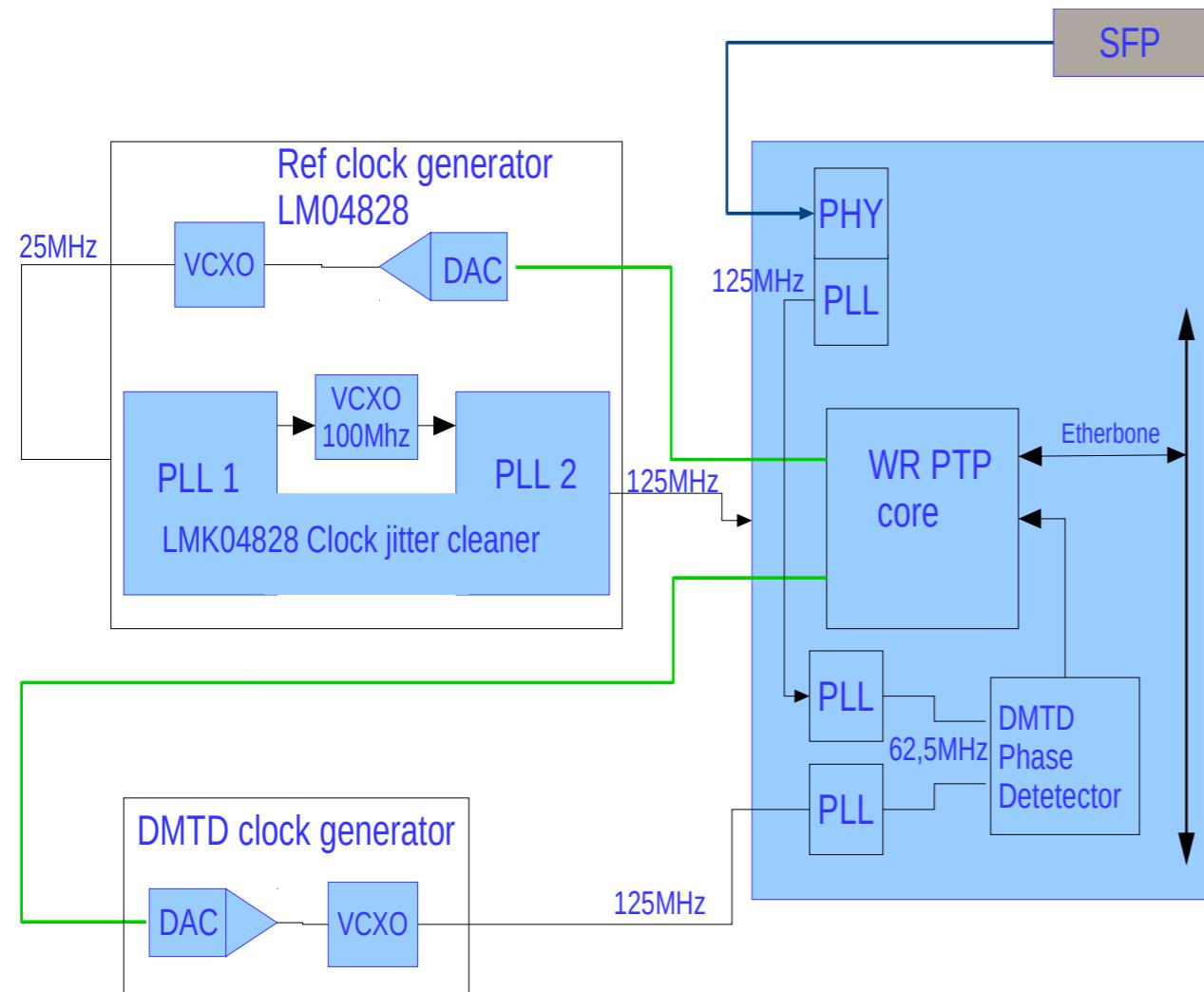


IDROGEN



- MTCA 4.0 standard, double width, fullsize AMC.
- Stand-alone mode
- VITA57.1 (FMC slot)
 - 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant.
- Front panel connectivity
 - WR SFP+
 - QSFP+ 40G, USB
- Backplane connectivity
 - 1Gbe IPbus, PCI 4x Gen3,
 - IPMB, CLK & trigger lane.
 - RTM connector : J30

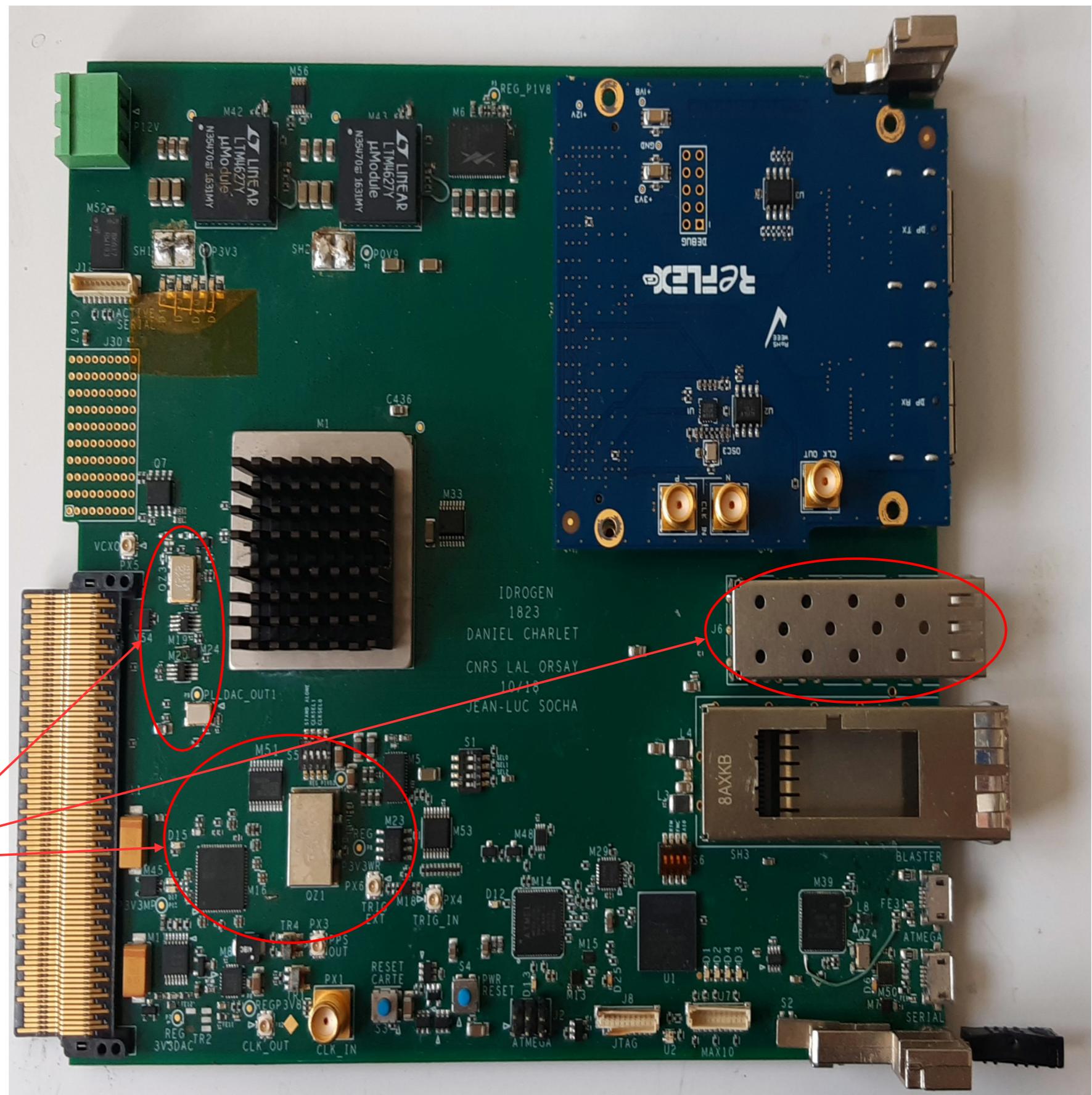
WhiteRabbit : DAQGEN implementation



The WhiteRabbit IDROGEN hardware is base on CERN open hardware with Enhancements

- Based on LMK4828 synthesiser
 - Ultra low noise clock jitter Cleaner with Dual Loop PLL
 - 90fs RMS jitter.
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clock :
 - DDMTD source (comparison between WR master clok from SFP)
 - PLL source with phase adjustment
- **IDROGEN Enhancements**
 - PLL selection
 - VCXO Frequency
 - Input frequency for DDMTD
 - remove of internal PLL (future dev.)
 - Tx/Rx routing equalisation

IDROGEN board

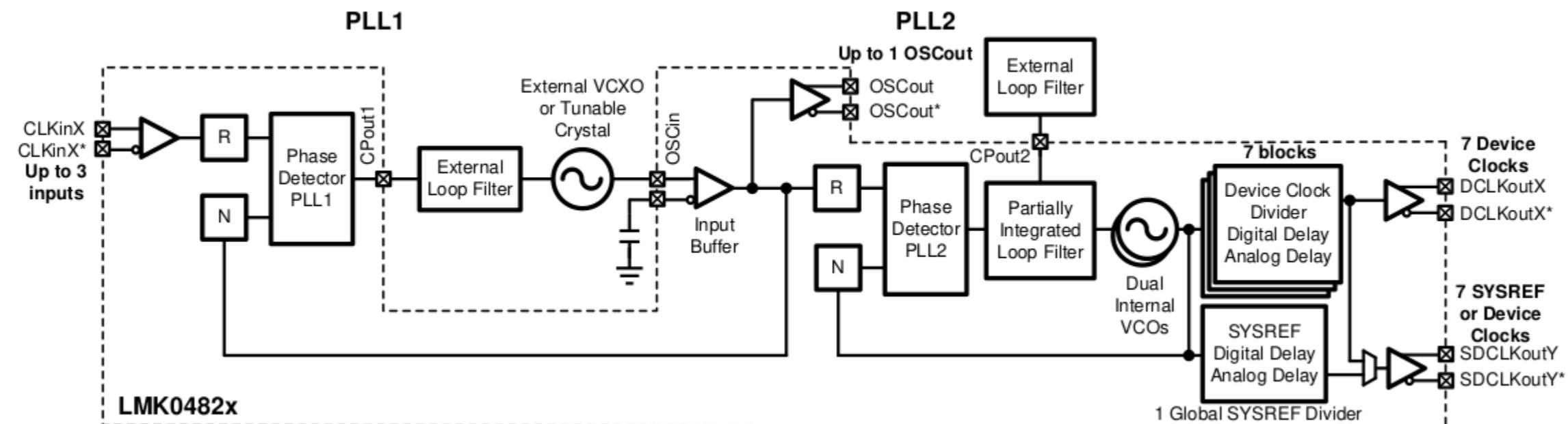
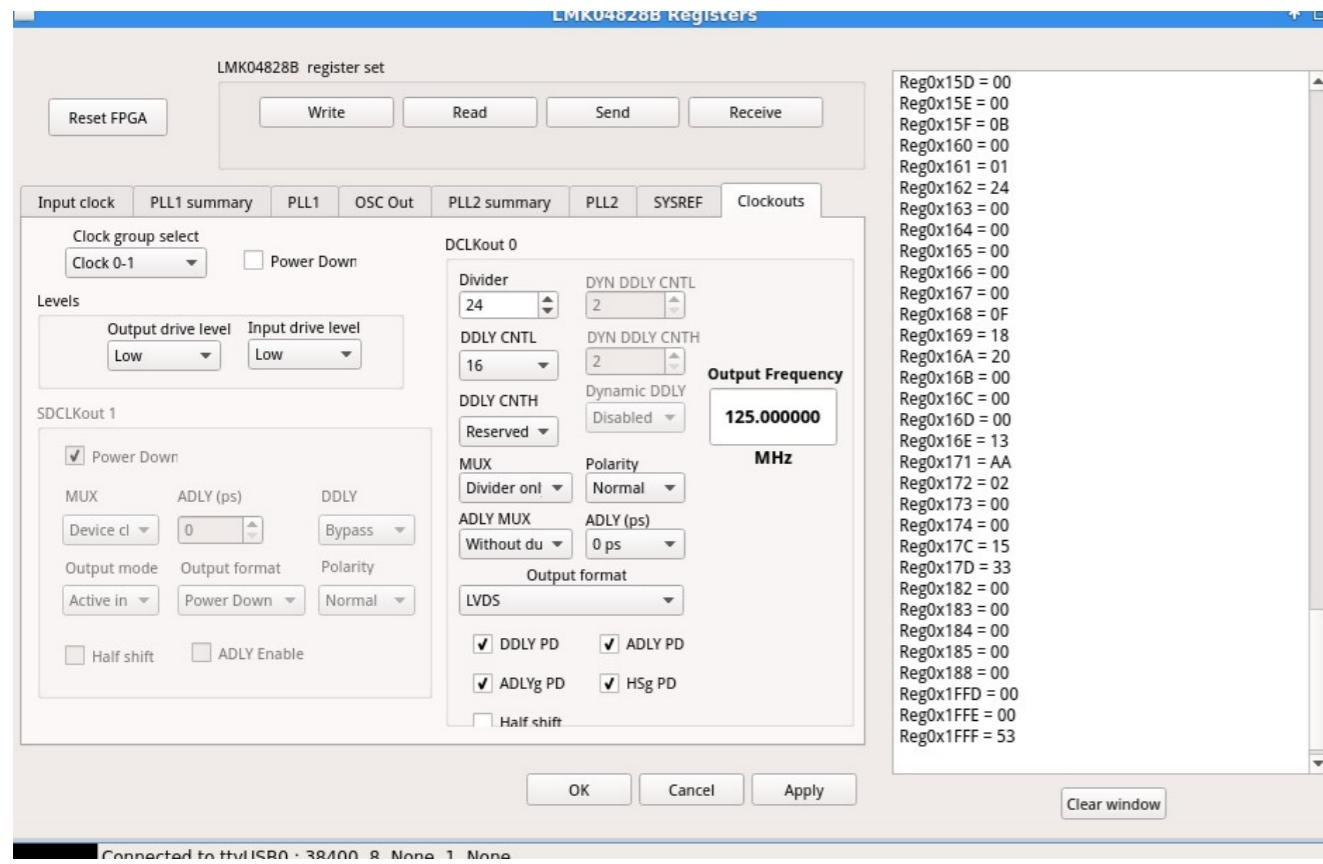


WhiteRabbit
External
components

IDROGEN Clock generator : LMK04828

LMK04828

- Frequency programmable 11MHz to 3 Ghz
- Analog delay adjustment by 25ps step
 - ~ 100fs rms jitter
- JESD20B compatible
- Free runinng or synchro WR
- Configure by μP.
- Re-configuration by USB or Eth
- Output clk on sma connector



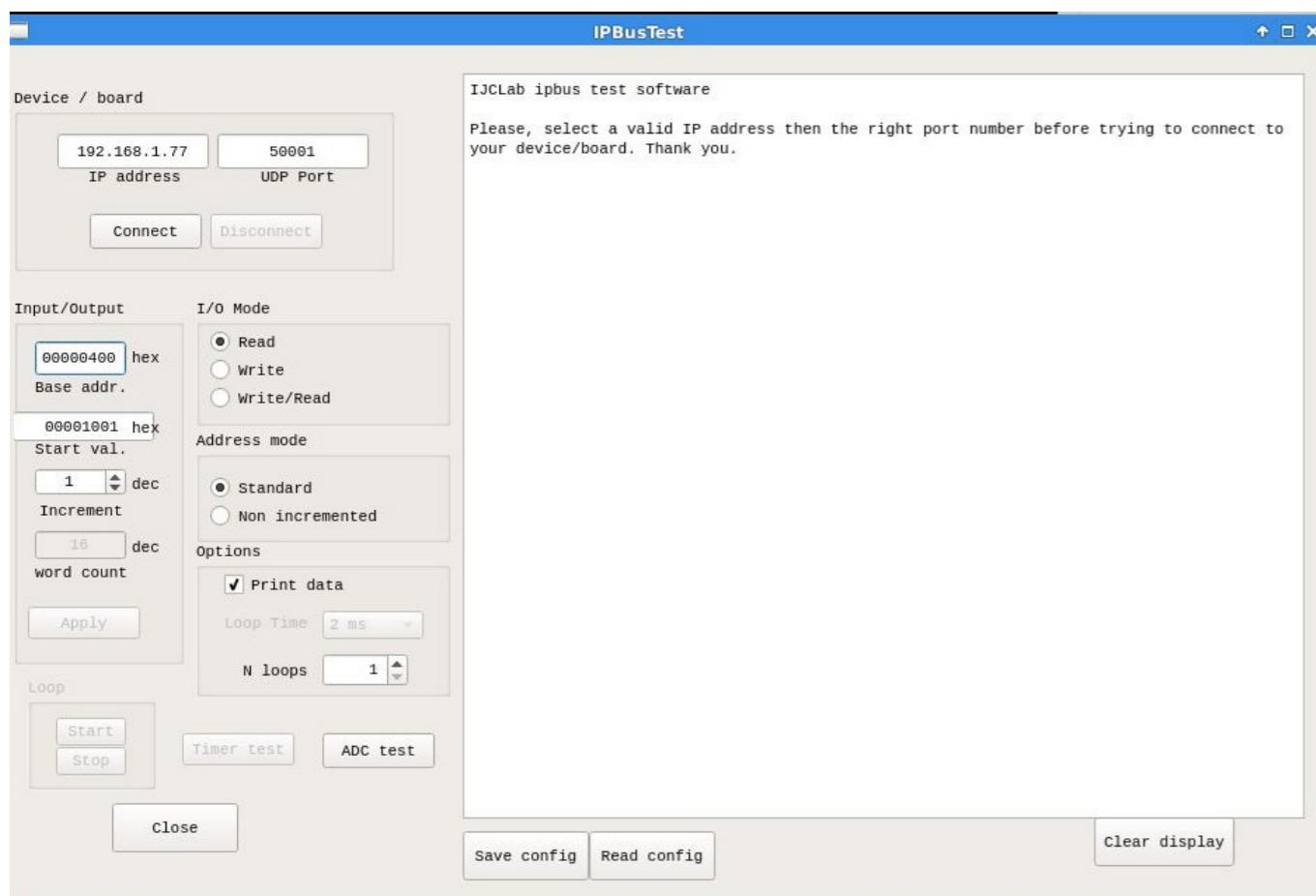
IDROGEN configuration & readout

IpBus 1G

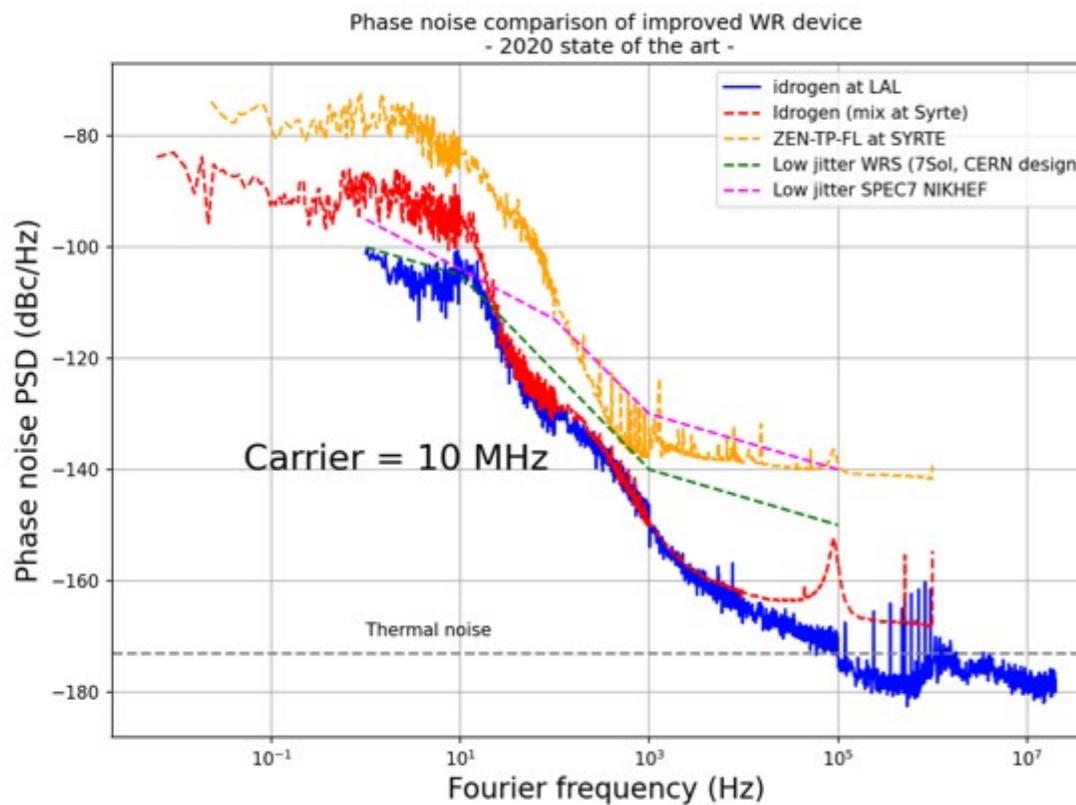
- Developed by LPSC for XILINX
- IntelFPGA version by IJCLA
- Master QSYS
- Utility base on QT

IpBus 10G (in development)

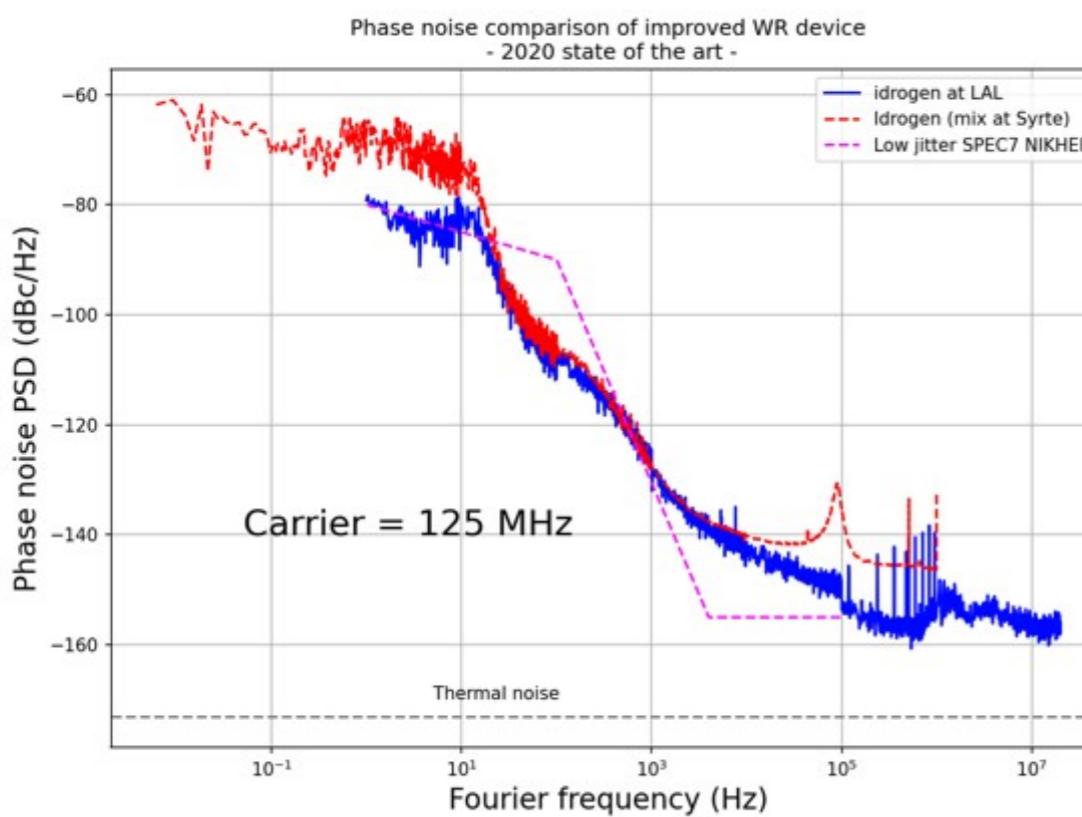
- Developed by LPSC for Xilinx
- IntelFPGA version by IJCLA
- New functionality : Streamer UDP
- Acquisition software



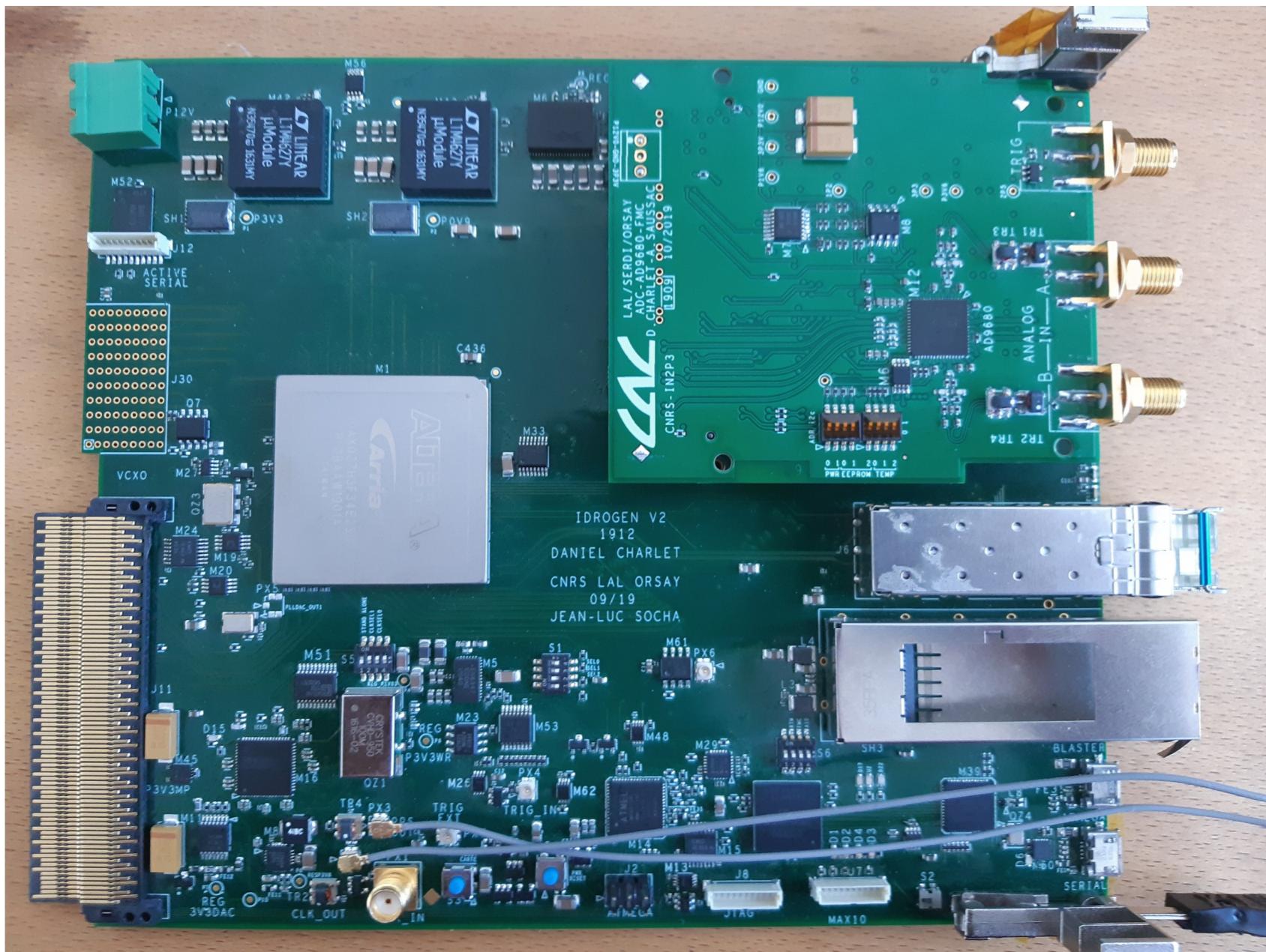
IDROGEN Phase noise measurements



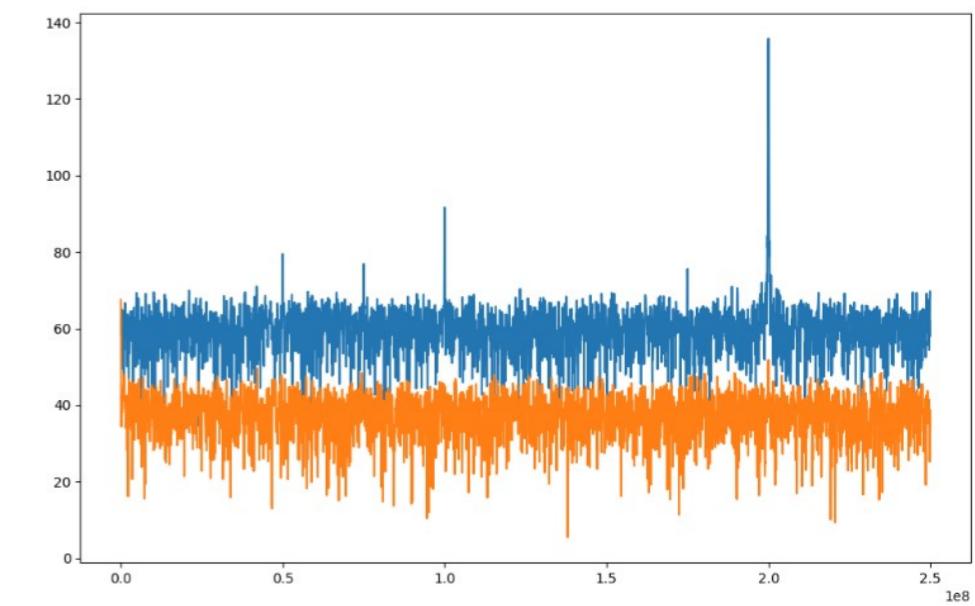
- For the test we measure the phase difference between 2 nodes (IDROGEN board)
 - Best result, one order, than the « challenger »
 - Clock phase jitter
 - PPS time precision 1ps RMS
 - Timing Improvement currently in development



IDROGEN + mezzanine ADC for PAON IV



- Preliminary results
- Bandwidth 500 MHz at 1.5GHz
- WR synchronisation
- JESD204 protocol
- Configuration & readout : IP bus 1G
-

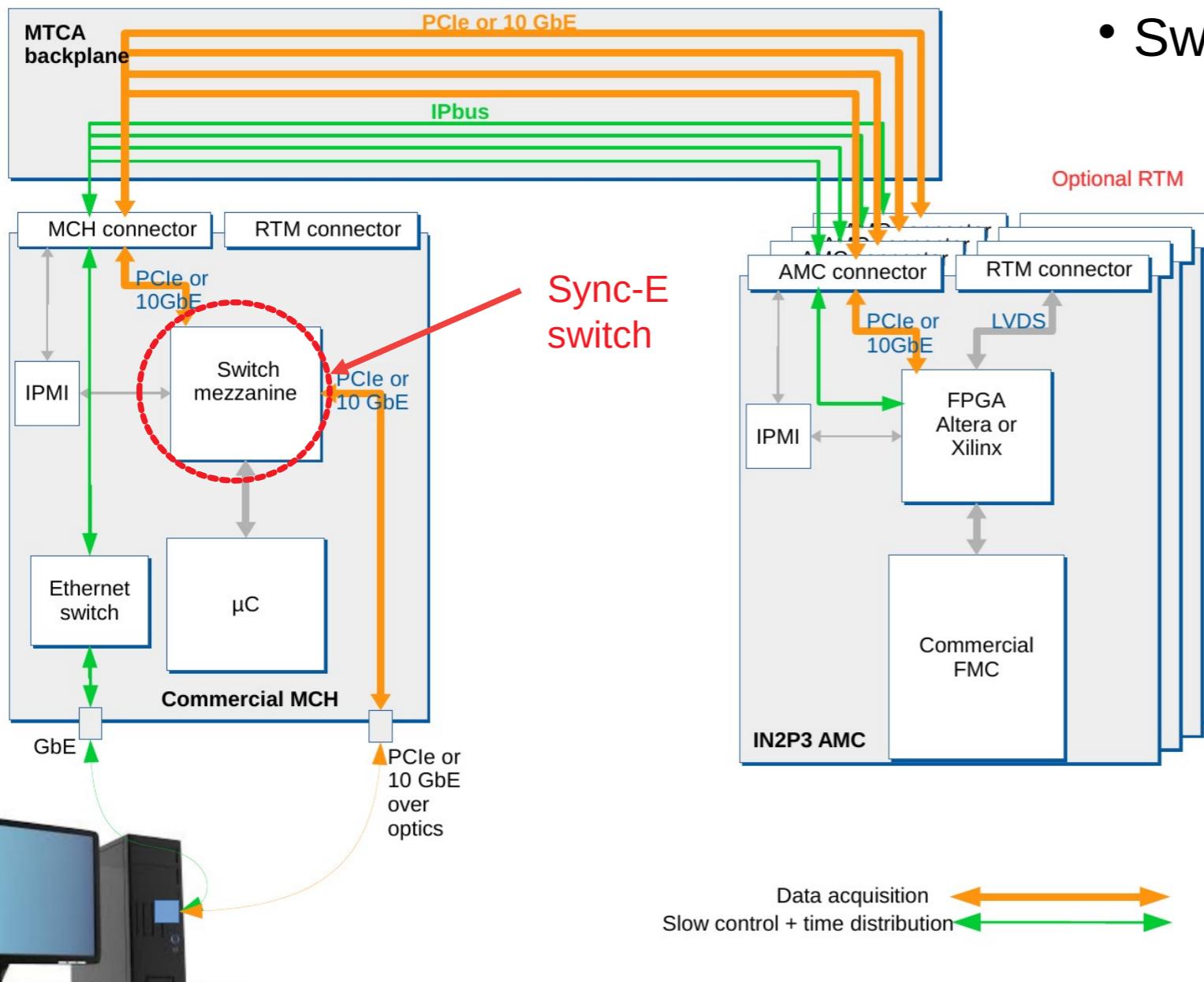


- Integrate WR in μTCA crate
 - Only the WR switch function
 - Sync-E switch in MCH slot frequency transfer.
 - Test on the shelf solution
 - Development of custom board
- Improvement of the WR performance
 - Soft PLL Response time
 - Components upgrading
 - MP replacement
- Integration of WR external component by firmware functions.
 - Integrate PLL
 - Analog VCXO by numeric bloc

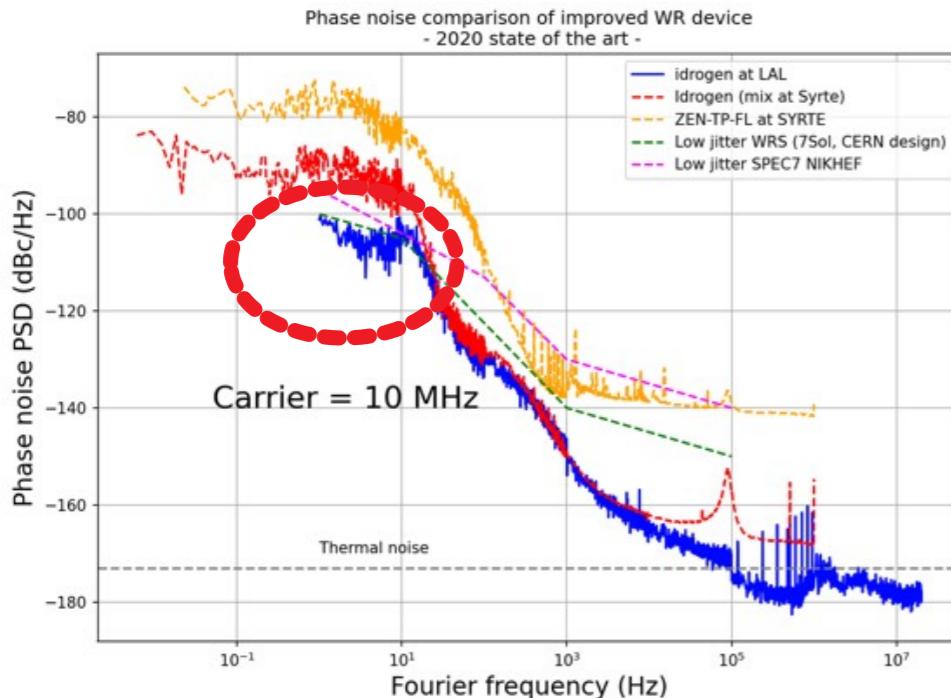
R & T TIMED : WR Crate integration

Continuation of DAQGEN project

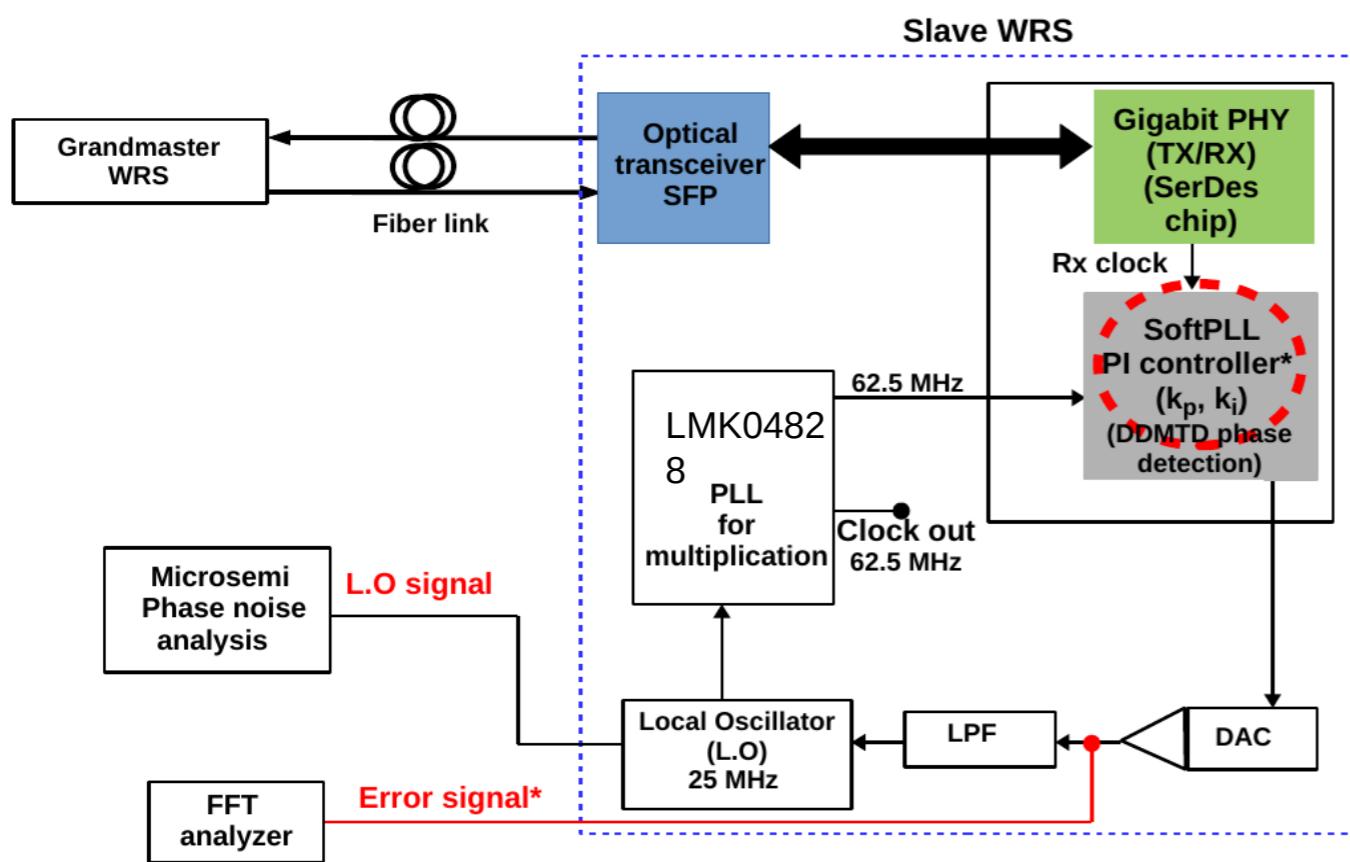
- Only switch functionality (no GM)
- Sync-E function on MCH board
 - Test MCH on the shelf product
 - Custom MCH to design
 - Switch function to design



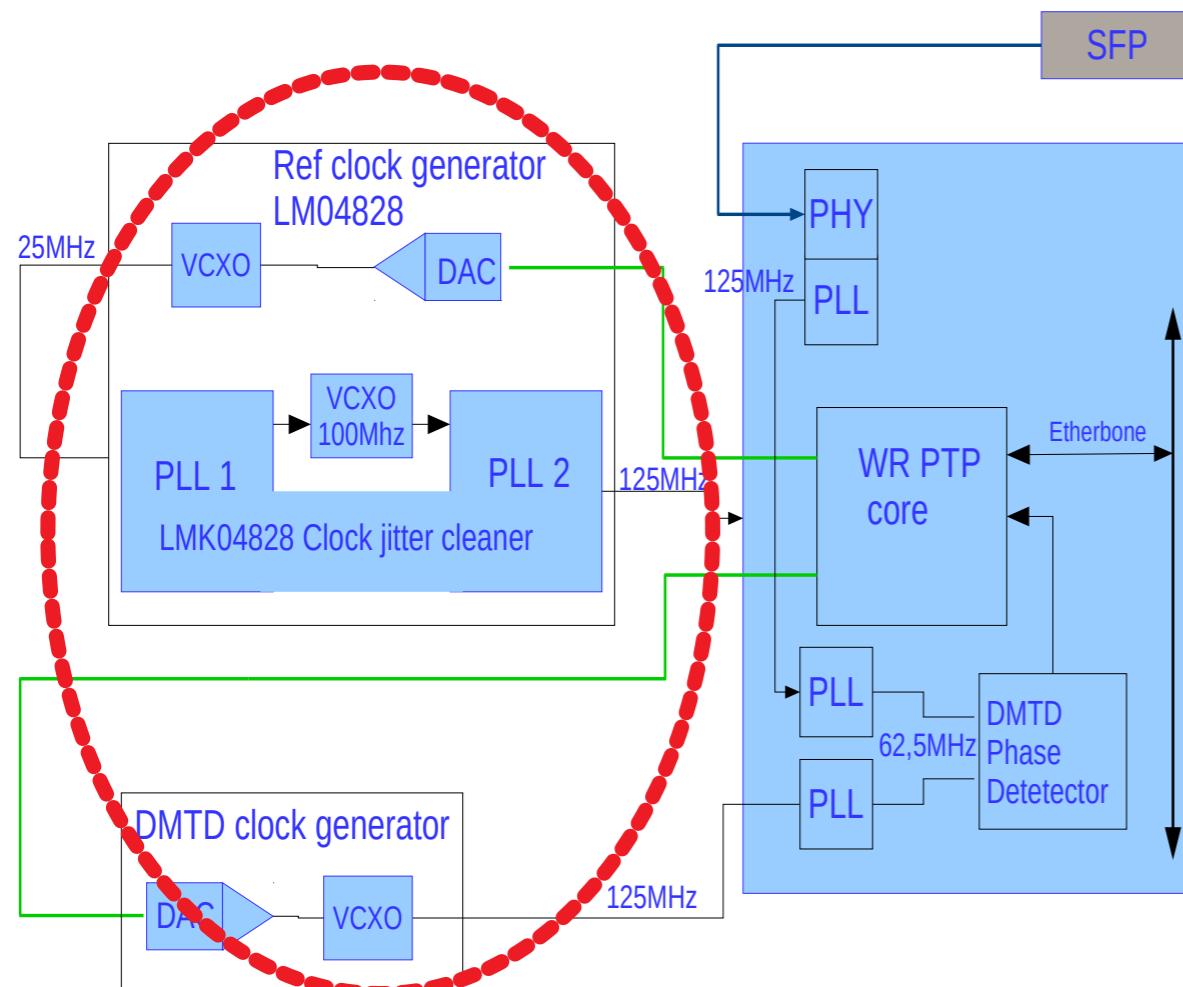
R & T TIMED : Increasing performances



- Collaboration with SYRTE Laboratory
- µP upgrading
 - Replacement of the universal µP base on logic bloc by dedicated µP (NIOS) or hardware µP (SOC)
- Components upgrading
 - VCXO selection
 - Increase Frequency
- Soft PLL modification
 - Decrease the response time
 - Gain integrator optimisation
 - Replacement of the internal µP



R & T TIMED : Firmware integration



- External PLL integration
 - Internal reconfiguration
 - μP Software upgrade
- VCXO intégration
- Derived from video IP
- **FPGA manufacturer dependent**

Application Note: 7 Series FPGAs and Zynq-7000 AP SoCs



XAPP589 (v2.3) April 29, 2015

All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)

Authors: David Taylor, Matt Klein, and Vincent Vendramini

Summary

This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver.

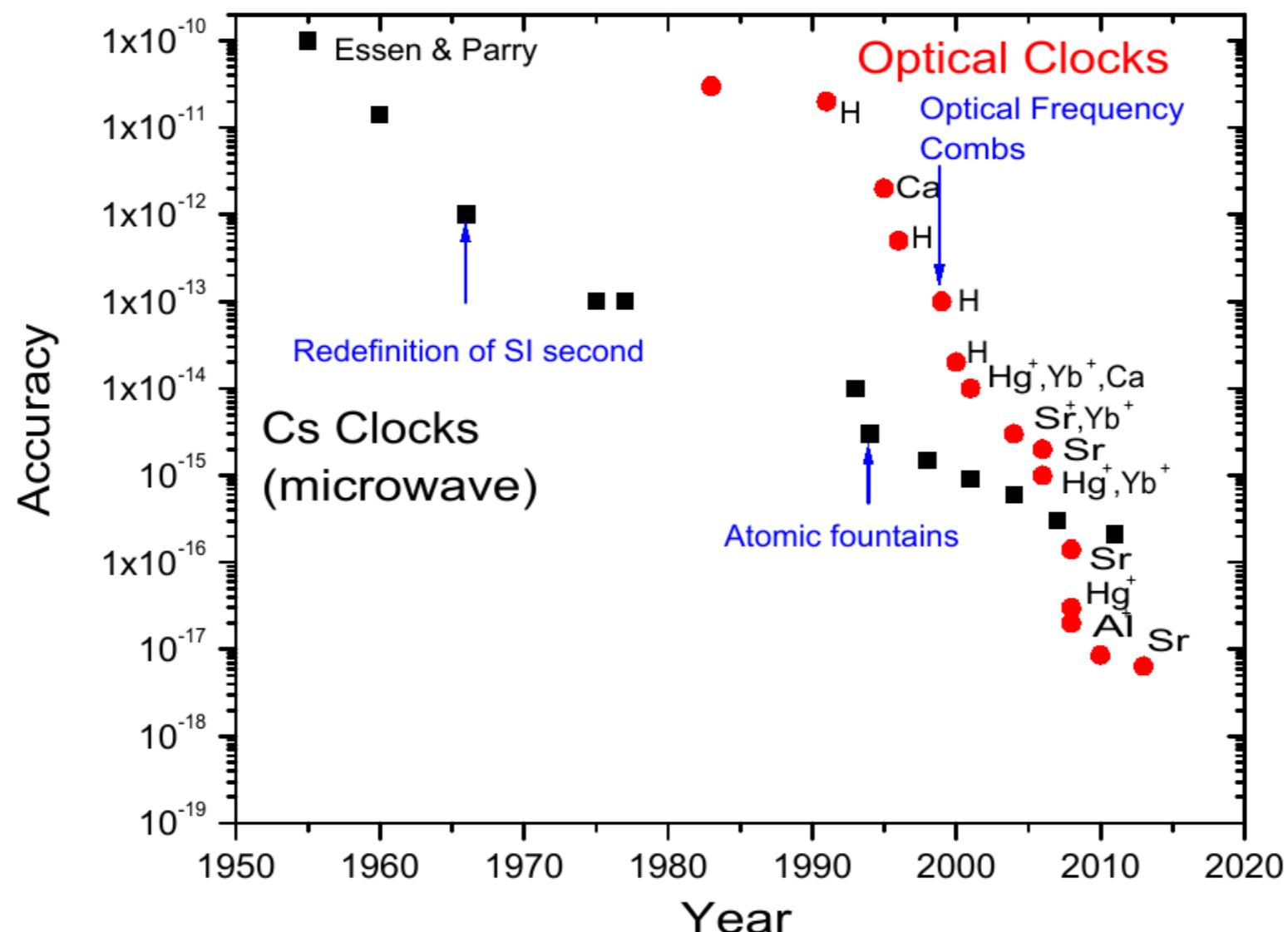
Note: In this application note, *transceiver* refers to these types of transceivers:

T+RFIMEVE

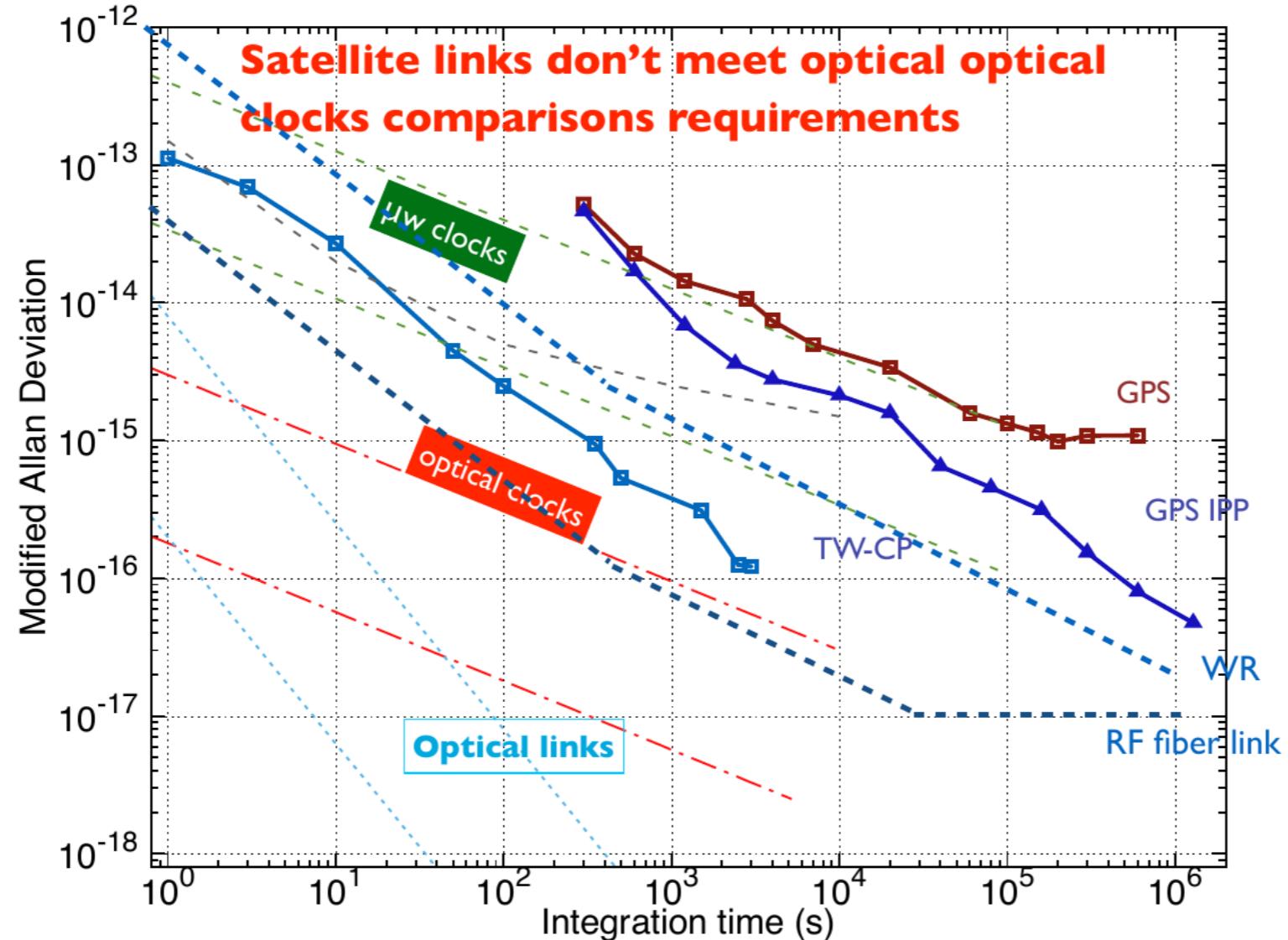
Performance des horloges

Domaine : Métrologie Temps-fréquence

Améliorations spectaculaires des horloges

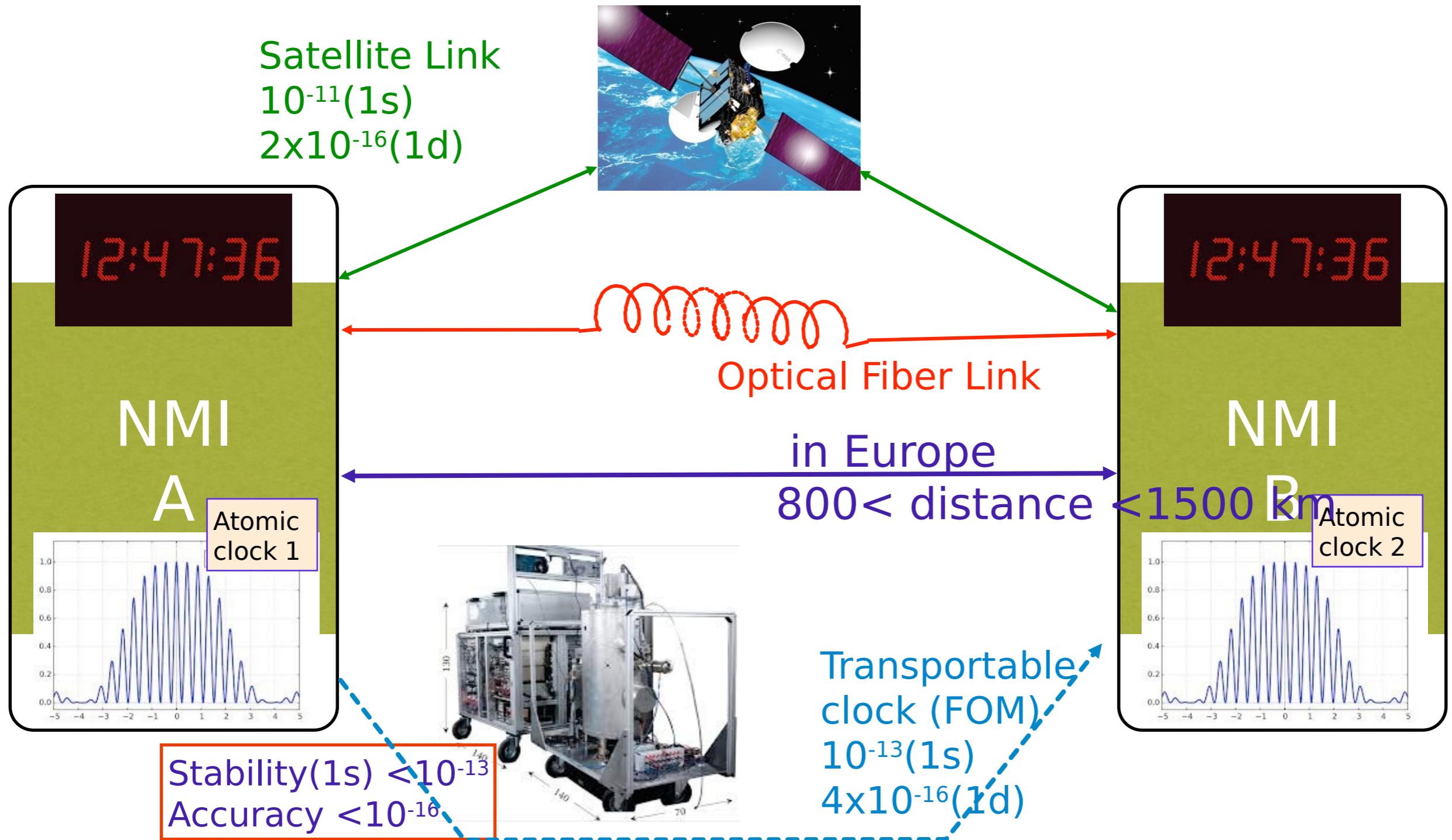


Aperçu des performances de distribution du temps



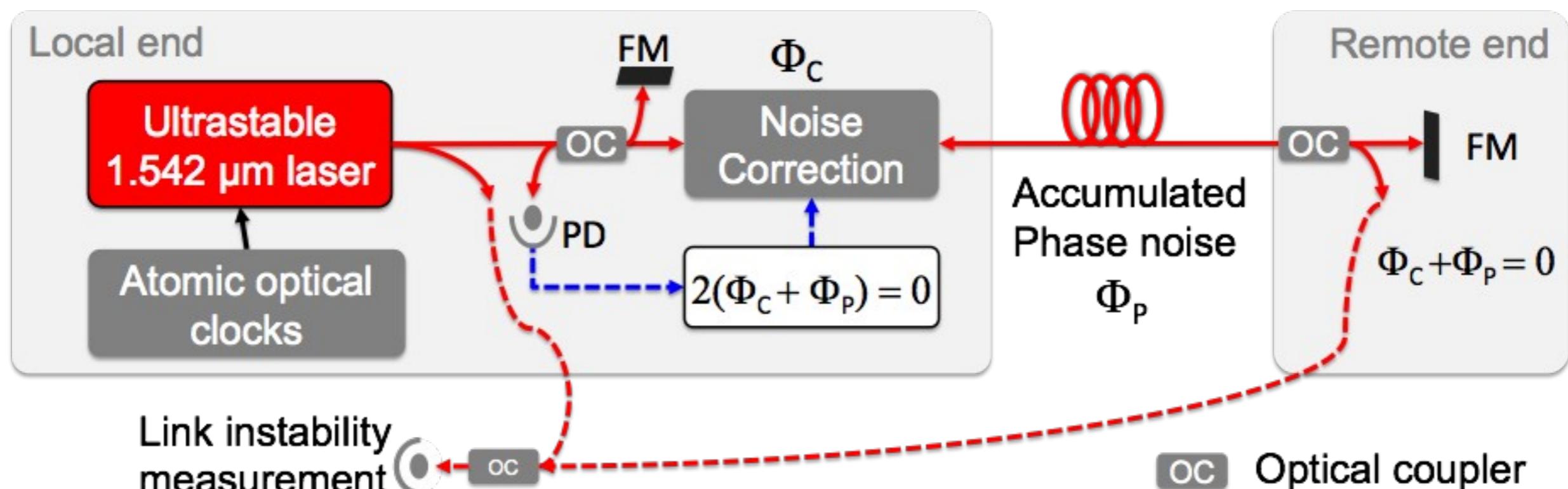
WitteRabbit	Stabilité 1s	Stabilité 1j
Réseau local avec matériel du commerce	1e-11	1e-13
Réseau distant RENATER	1e-12	1e-15
Développement IJCLAB	1e-13	1e-16

Problématique : moyens de comparaison / dissémination



Liens fibrés optique : concepts généraux

- Seminal works: Primas et al, Proc 20th PTTI, 1988, Ma et al., OL 1994
- Active noise compensation after one round-trip
- Strong hypothesis : noises forth and back are the same
- 2 ends at the same place (for link stability measurement)



Exemple pour une méthode « tout optique »

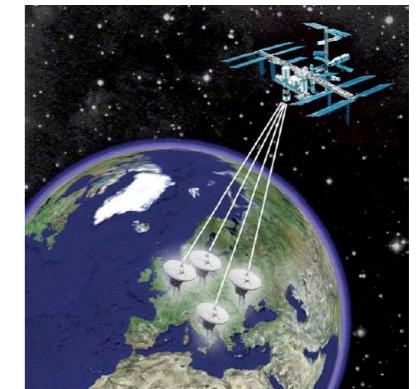
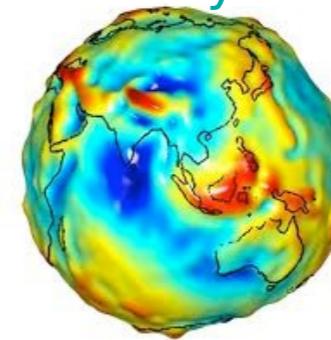
Les besoins en dissémination T/F par fibre

Frequency metrology:

Access to ultra precise reference frequencies for remote user.

Spectroscopy, photonics, quantum sensors, quantum telecom., ...

Geodesy



Applied dimensional measurements:

Traceability of the unit of length for interferometric measurements.

Astronomy:

Phase traceable signals for the synchronization of radio telescopes
VLBI, NOEMA, SKA, LOFAR ...



Broadband communication technology:

Provision of reference signals with low-jitter for synchronization

Large research infrastructures

(ESA, DESY, CERN, GSI):

Time and frequency dissemination in ground stations

Industry : wireless, optical telecom. Galileo GNSS ground segment



REFIMEVE : Réseau Fibre métrologique à vocation européenne

REFIMEVE+ : Equipex du Programme d'investissement d'Avenir (2012)

T-REFIMEVE : Equipex ESR/PIA3 (2020)

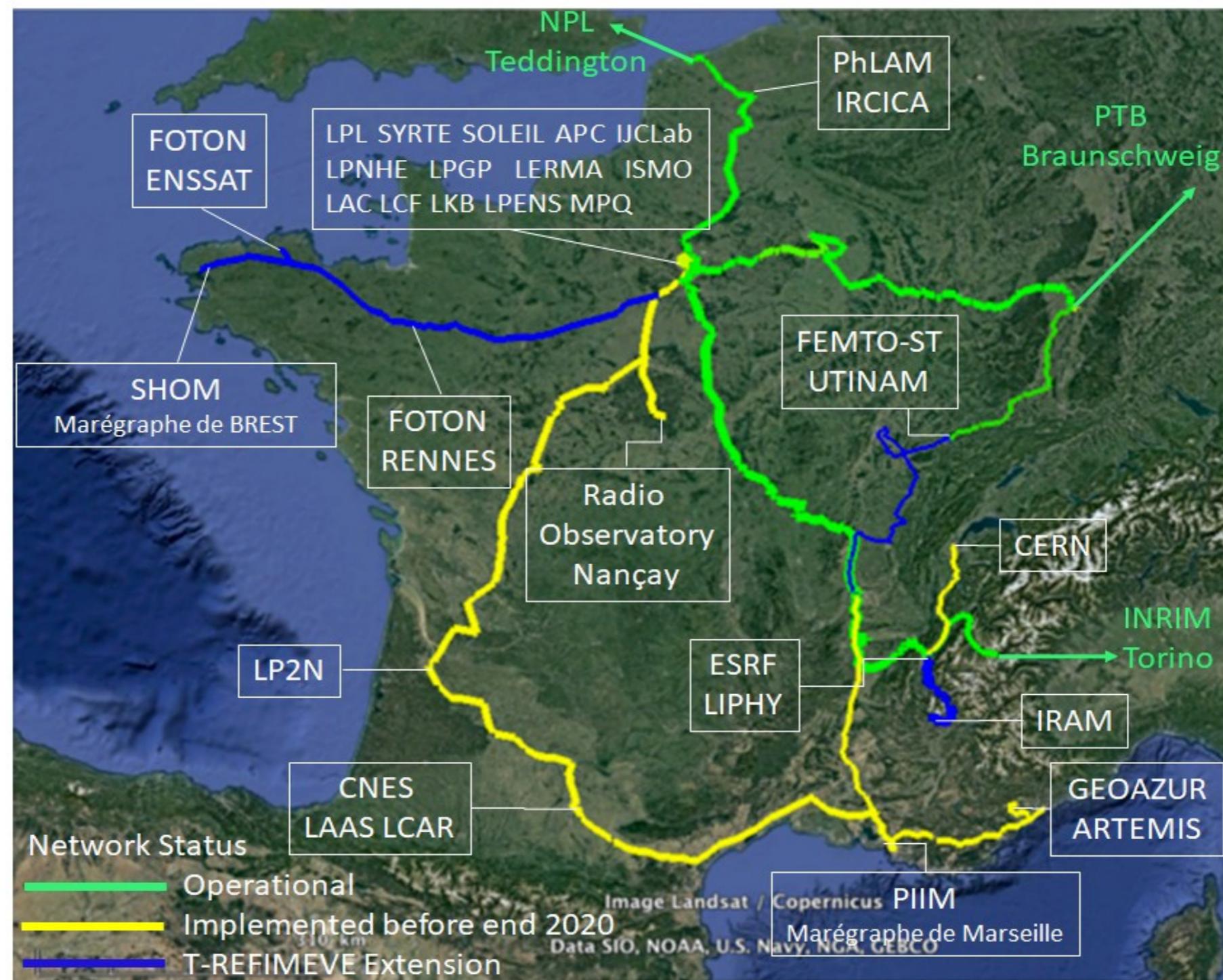
REFIMEVE : infrastructure de recherche

Concept : Dissémination de références temps-fréquence par fibre optique

Partenariat : [SYRTE+LPL+RENATER+Utilisateurs]



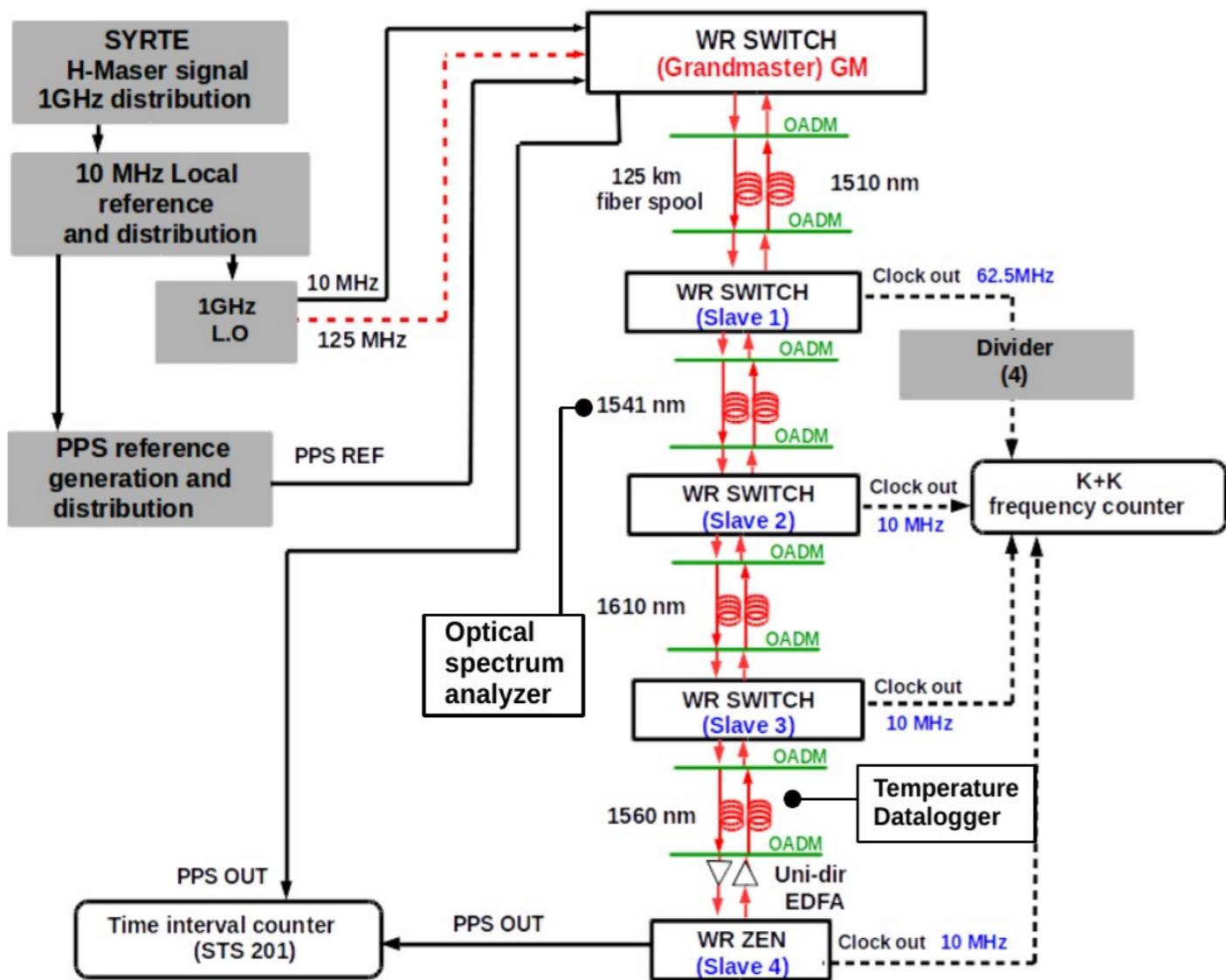
Carte du réseau



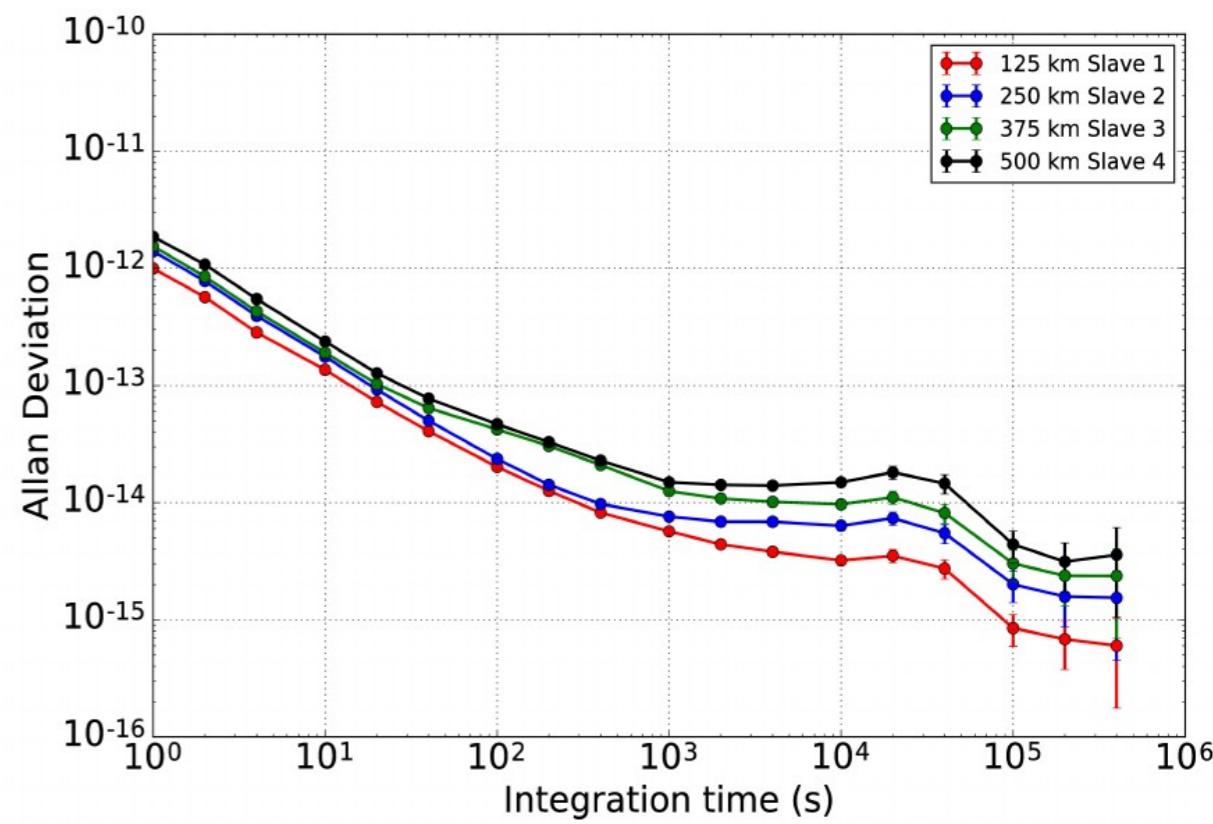
Signaux distribués par T-REFIMEVE

Signal provided by T-REFIMEVE		Stability @1s	Stability @1day	Uncertainty	
				routine	dedicated
Radiofrequency	1 st pillar - 10 MHz (White Rabbit)	10^{-12}	10^{-15}	10^{-14}	10^{-15}
	2 nd pillar - 1 GHz	10^{-13}	3×10^{-16}	10^{-14}	2×10^{-16}
Time	1 st pillar (White Rabbit)	1 ns	1 ns	10 ns	10 ns
	2 nd pillar	20-50 ps	500 ps	10 ns	2ns to 100ps
Optical frequency (194,5 THz - 1542 nm)	Today	10^{-15}	3×10^{-16}	10^{-14}	2×10^{-17}
	Expected progress in 5 years	10^{-16}	2×10^{-17}	10^{-14}	10^{-18}

Distribution du temps test long distance



- Cascade de lien WR
- 500Km de fibre
- Le bruit de la fibre devient dominant
- Disparité système
- Réciprocité du lien



Dissémination du temps : 12 Oct 2021

Conclusion

- Le WR permet ce concevoir de nouvelle architecture du fait de ces caractéristiques (précision, stabilité, distance, nombre de nœud)
- IDROGEN
 - V3 en cours de fabrication
 - 17 cartes de produites : PAON IV, PICMIC, SYRTE, IPHC, LPCC, CCPM
- Engagement important de l' IJCLAB dans T+RFIMEVE
 - Développement de la partie temporelle basésur IDROGEN
 - Plusieurs nœud T+REFIMEVE à l'IN2P3 et 1 au CERN
 - IJCLA,LPNHE,APC
- Nouveaux développement dans le cadre de la R&T et de T+REFIMEVE
 - Amélioration des performances.
 - Integration
 - Upgrade du WR à 10G
 - Test WR 10G sur switch Sync-E 100G

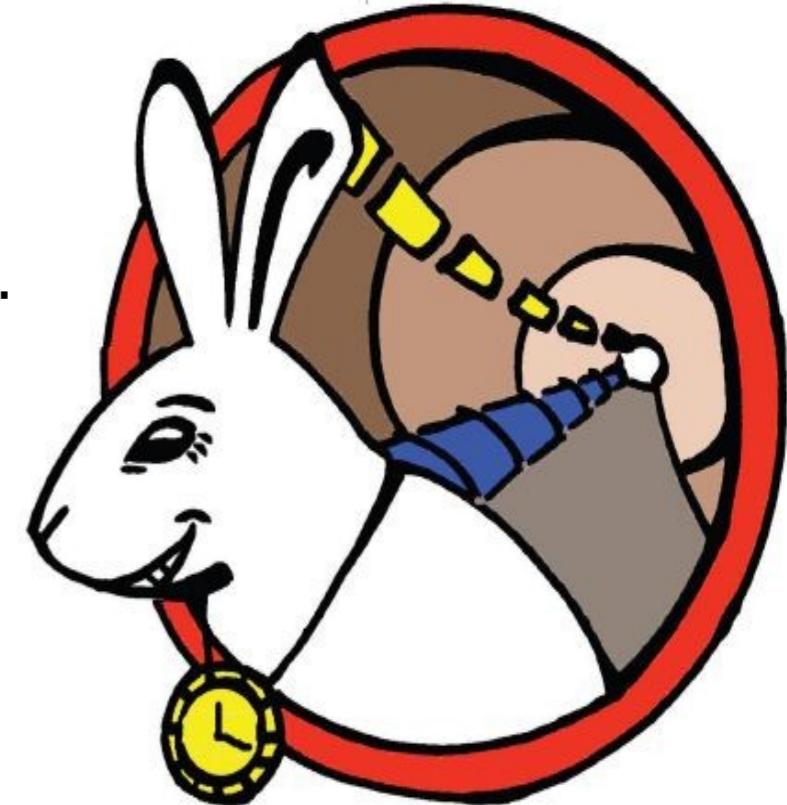
White Rabbit principle: Enhanced Ethernet

● Technology overview

- Precision Time Protocol (IEEE1588)
- Synchronous Ethernet
- DDMTD Phase tracking (Digital Dual Mixer Domain) .

● An extension of Ethernet which provides :

- Synchronous mode (Syn-E) – common clock for physical layer in entire network, allowing for precise time and frequency transfer
- Deterministic routing latency – a guarantee that packet transmission delay between two stations will never exceed a certain boundary.

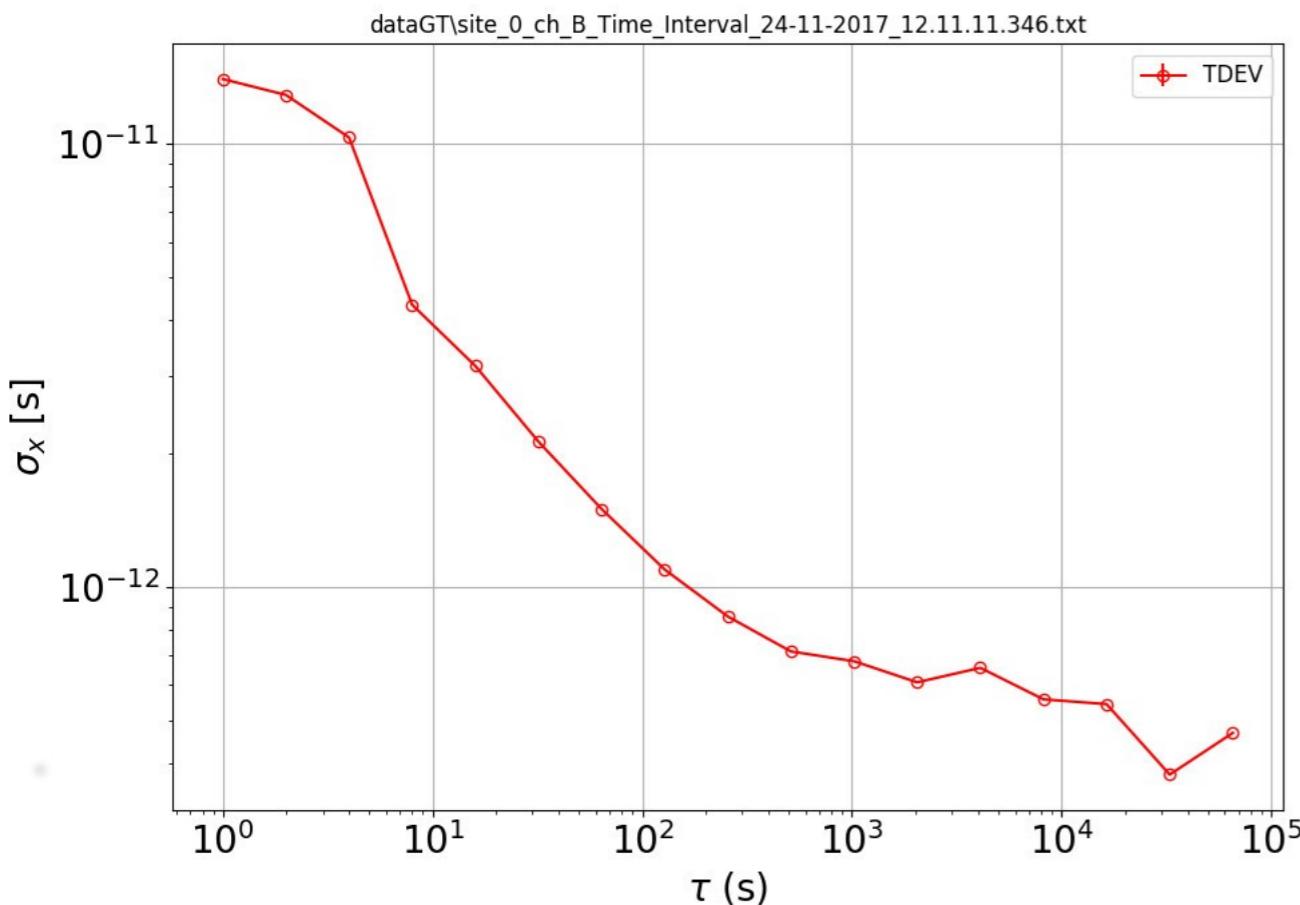


NEBULA performance

• IDROGEN version -1

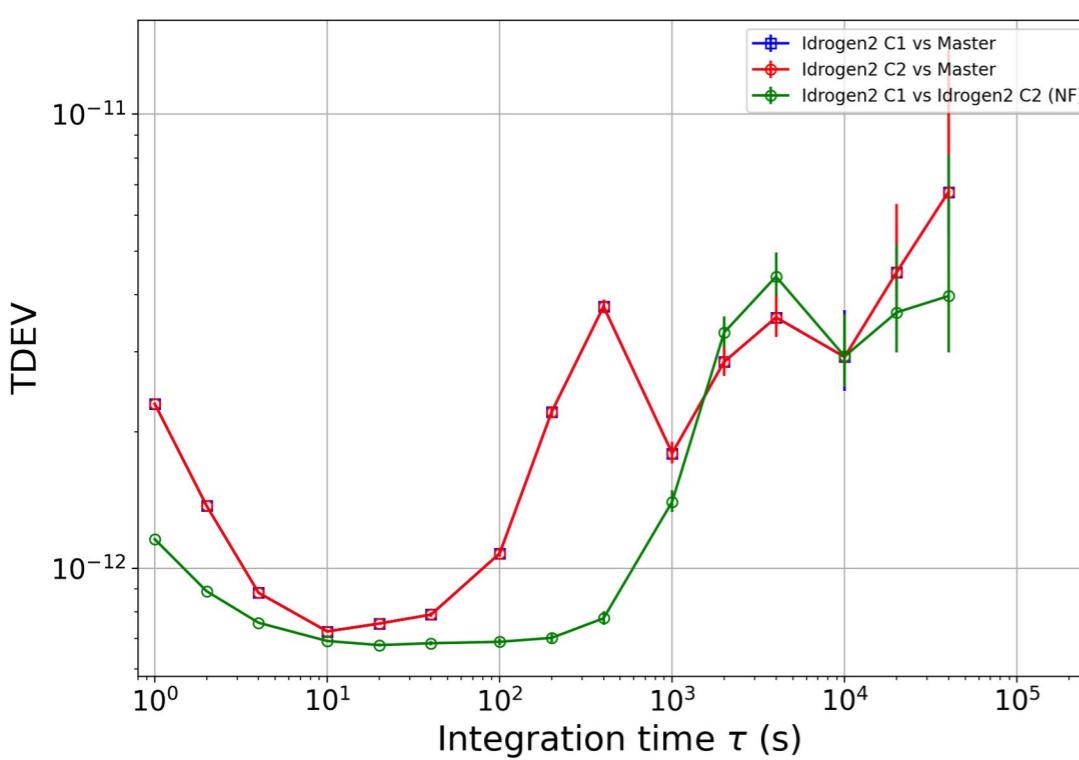
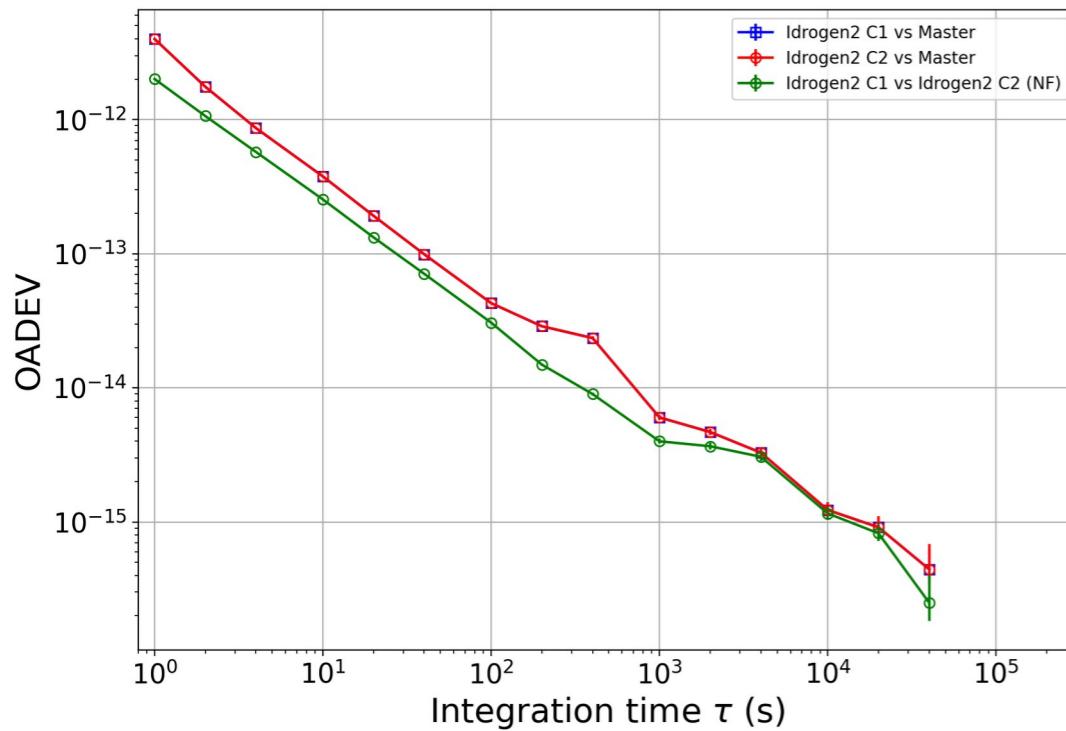
- 400fs after 1000s & 100m of fibers
- Same design as IDROGEN
- IDROGEN system qualificationTest
 - With SYRTE test setup
 - 2 IDROGEN board : Grand master & slave configuration .

SYRTE test setup recently operational again

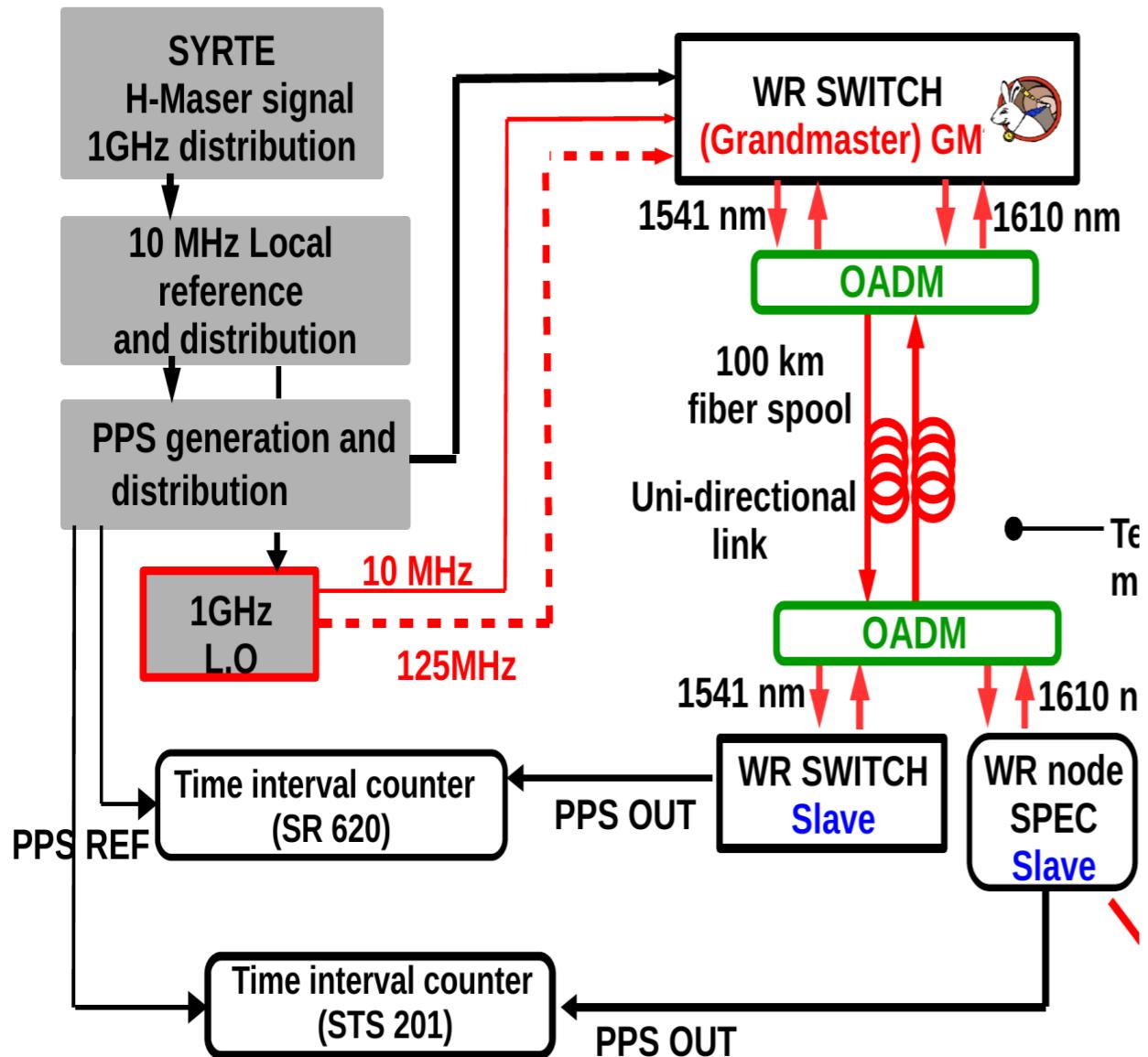


IDROGEN preliminary measurements

- For the test we measure the phase difference between 2 nodes (IDROGEN board)



WhiteRabbit, SYRTE test system



- For the test we use the test system developed by the SYRTE for timing distribution measurement.
 - fs measurement capability
 - Very high timing stability $10e-16$
 - WR switch improvement.
 - Remove of local PLL
 - Conditioned room.
 - Dedicated measuring apparatus
 - Selection of fiber length
 - Selection of transceivers