HGTD ELECTRONICS STATUS

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On behalf of the HGTD project

15th France China Particle Physics Network/Laboratory Workshop
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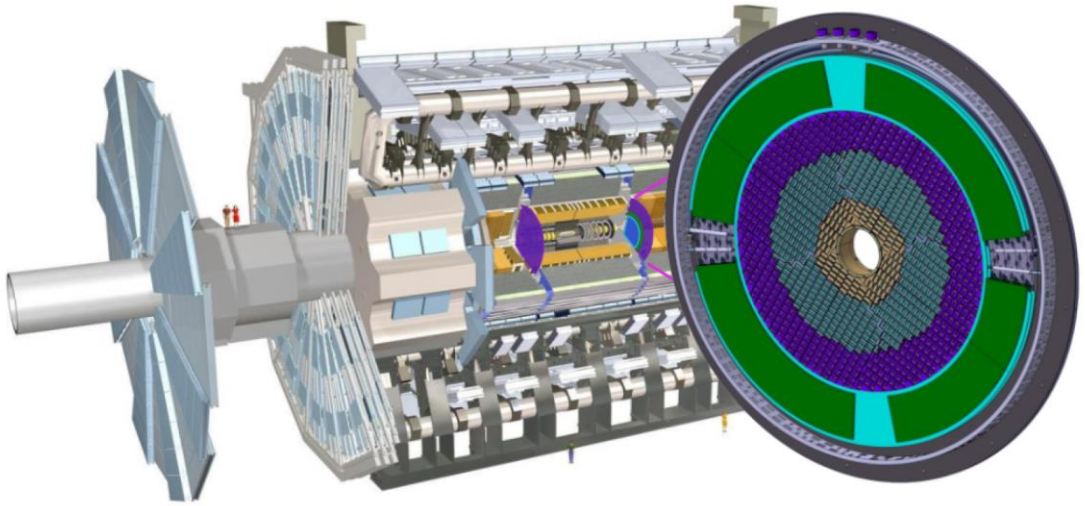
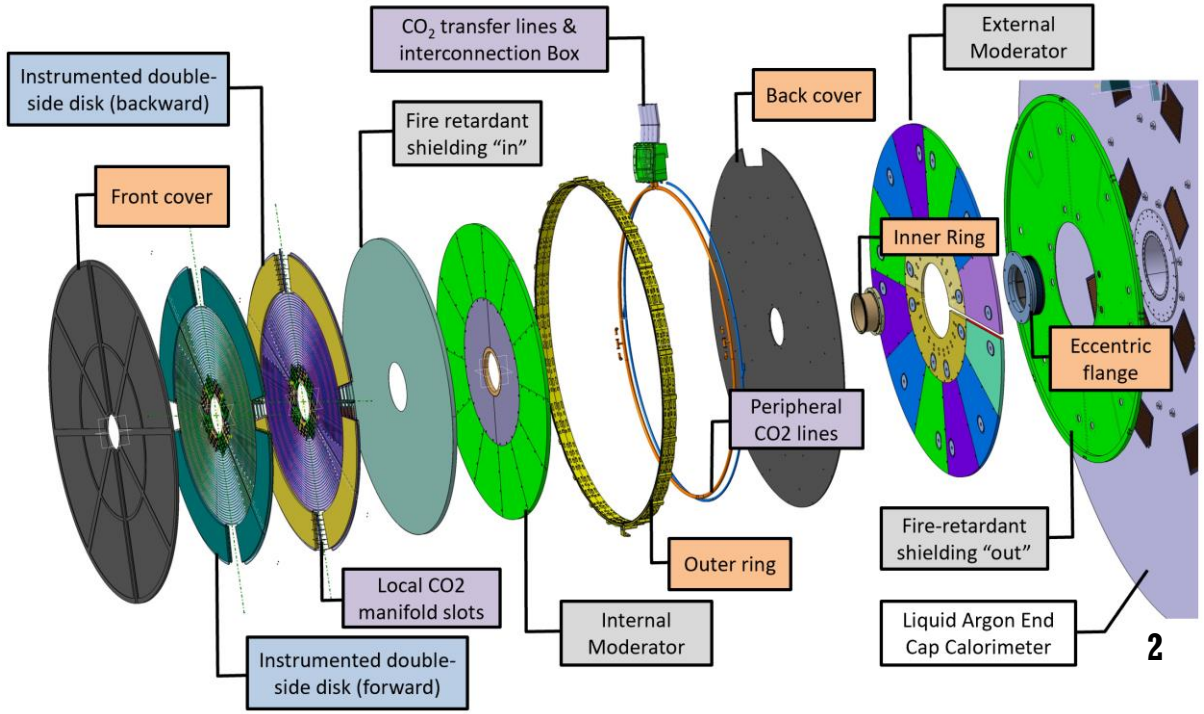
INTRODUCTION

- High Granularity Timing Detector (**HGTD**)
  - Silicon detector with coarse spatial resolution but precise timing
  - ~3.6 million 1.3×1.3 mm^2 pixels with Low-Gain Avalanche Detector (**LGAD**) technology
  - 6.1 m^2 active area
- Pileup rejection
  - Time resolution at the start (end):
    30 (50) ps per track / 35 (70) ps per hit
- Luminosity measurement
  - Goal for HL-LHC: 1% luminosity uncertainty
  - Count number of hits at 40 MHz (bunch-by-bunch)
- Detector structure
  - Two end-caps
    - $z \approx \pm 3.5$ m from the nominal interaction point
    - $110 < r < 1000$ mm
    - Active detector region: $2.4 < |\eta| < 4.0$
  - Each end-cap
    - Two instrumented disks, rotated by 15°

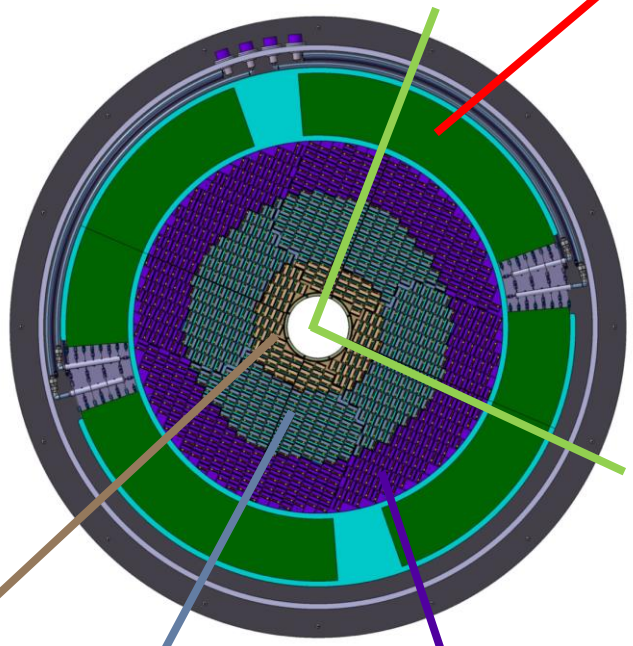
Global view of the HGTD

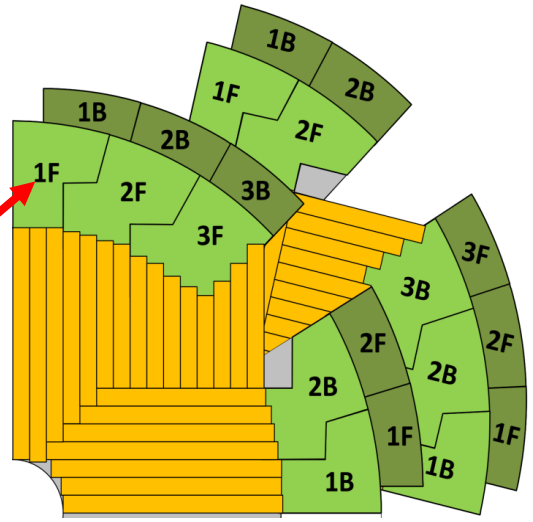




INTRODUCTION

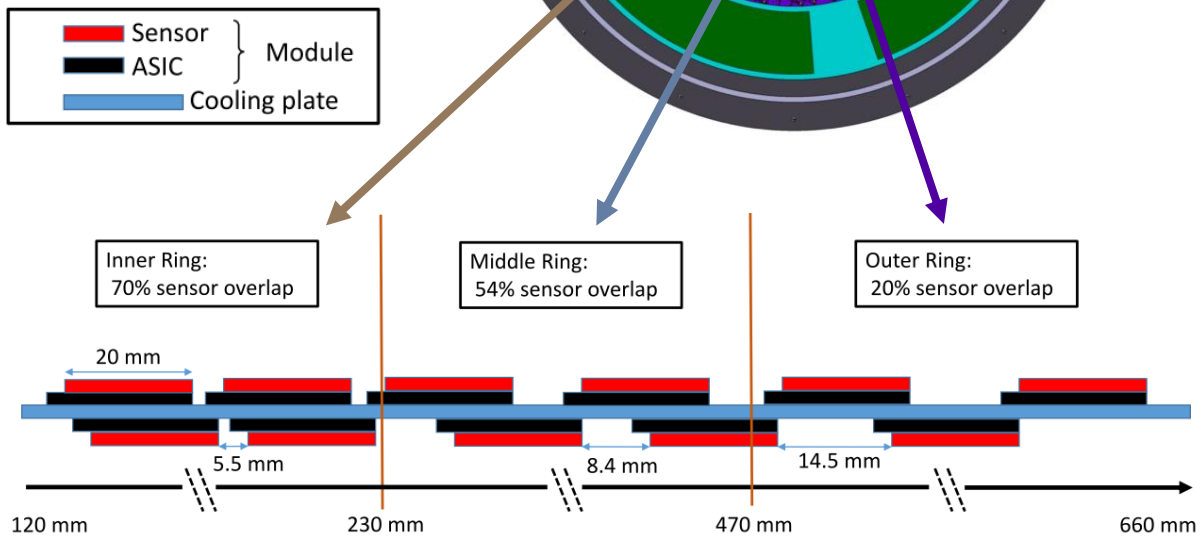
On each disk:
- Four quadrants
- Double-sided layers mounted on a cooling plate
- 3 ring layout for front-end modules



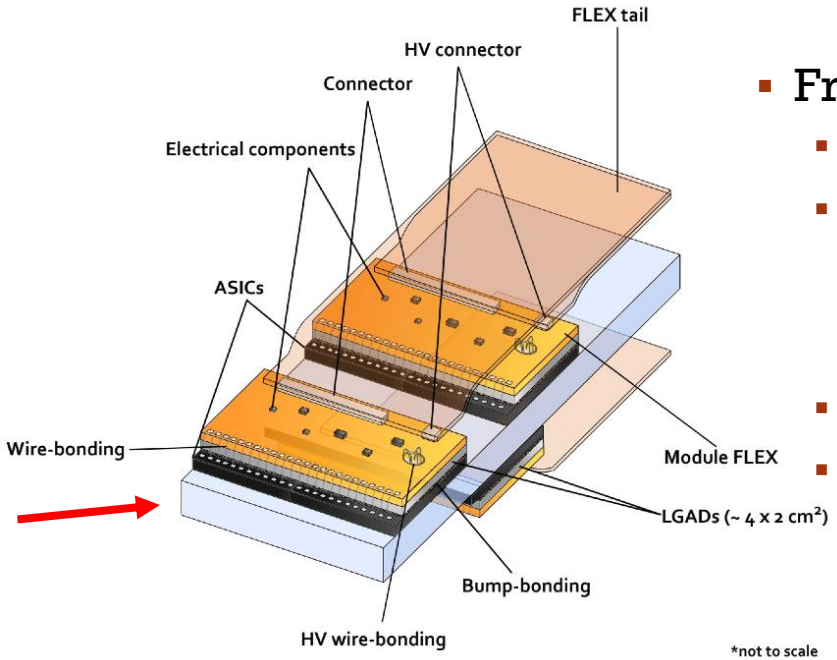


Peripheral Electronics Boards (PEB)

- Six types of PEB
  - Board 1F, 2F, 1B and 2B can be used both on front and back
    - According to the optimization of mirror structure for module layout
  - Each board covers three or more readout rows in order to have a similar number of modules
- The front-end modules are connected via flex tails



Overlap between the modules on the front and back of a cooling disk

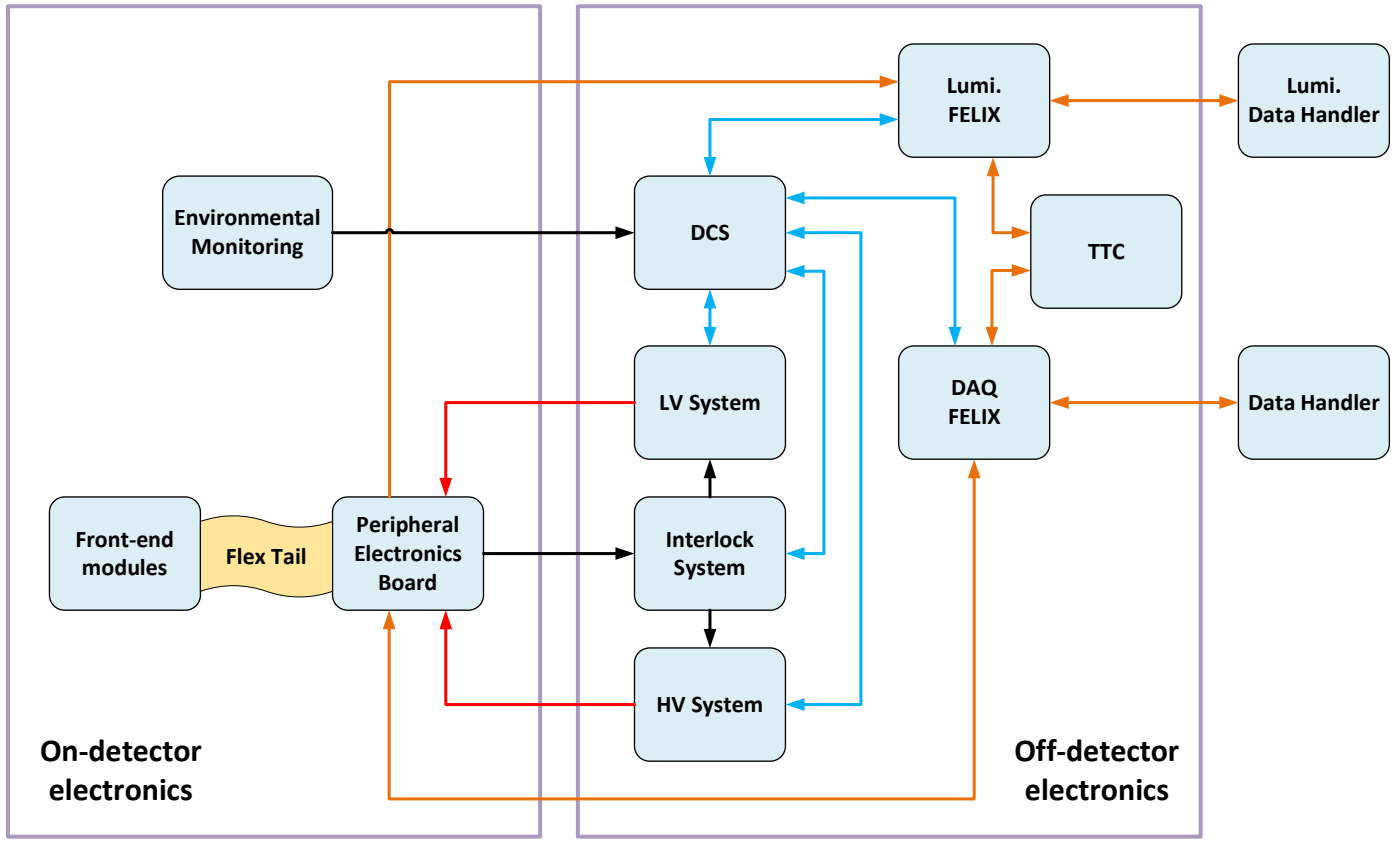


- Front-end module
  - Two LGAD sensors
  - Two ASICs
    - ATLAS LGAD Timing Integrated Read-Out Chips (ALTIROC)
  - Flex PCB
  - Radiation tolerance for modules
    - Up to 2 MGy, 2.5×10^{15} 1MeV neq/cm^2

(2 ASICs + 2 sensors)/module

OVERVIEW OF HGTD READOUT ELECTRONICS

- On-detector
  - Front-end modules
  - Flex tail cables
  - Peripheral Electronics Boards (PEB)
- Off-detector
  - Data Acquisition System (DAQ)
  - Luminosity System
  - Timing, Trigger and Control (TTC)
  - Detector Control System (DCS)
  - Low Voltage (LV)/High Voltage (HV) system
  - Interlock system



HGTD electronics architecture

Basic functions of PEB

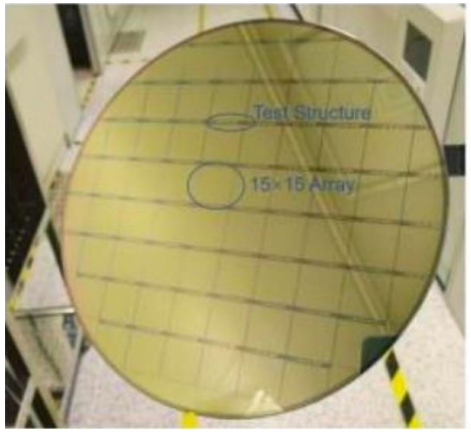
- Control, monitoring & data aggregation and transmission
  - lpGBT, VTRx+, MUX64
- Power-supply distribution: LV & HV
  - bPOL12V, HV filter
- Thermistor connection between the front-end modules and the interlock system

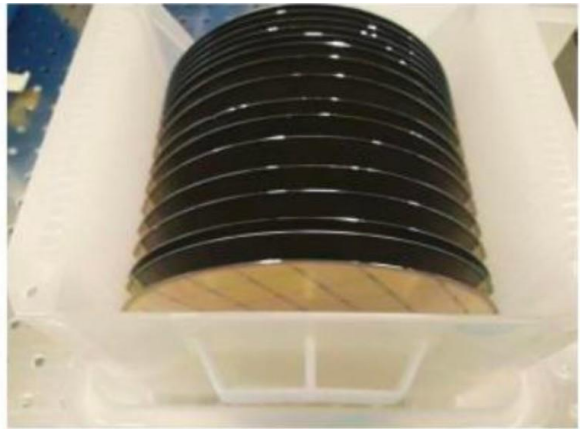
LGAD SENSOR

❑ Pre-production

IHEP-IME

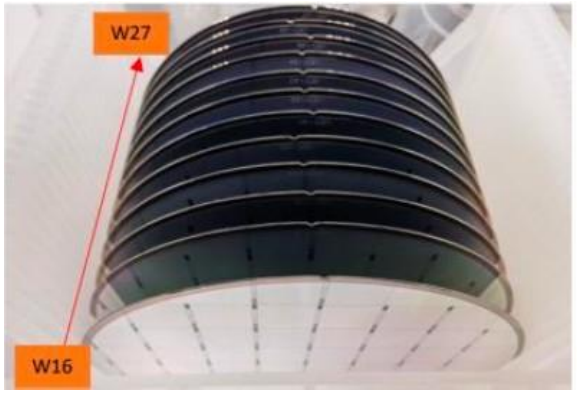
8” wafer

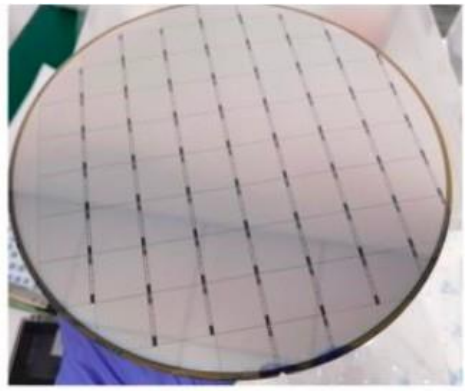




USTC-IME

8” wafer





52 sensors per wafer

➢ HGTD requirements

- 16064 good sensors installed on detector
- Production: 21700 good sensors (for module production yield of 74%)
- Pre-production: 5% of the total production → ~1100 sensors

117 wafers have been fabricated

	Wafers		Sensors		
	IHEP-IME	USTC-IME	IHEP-IME	USTC-IME	Total
Fabricated	90	27	4680	1404	6084
Passing pre-production requirements	52	9	1702	205	1907
Pre-production with UBM, so far	22	5	774	118	892

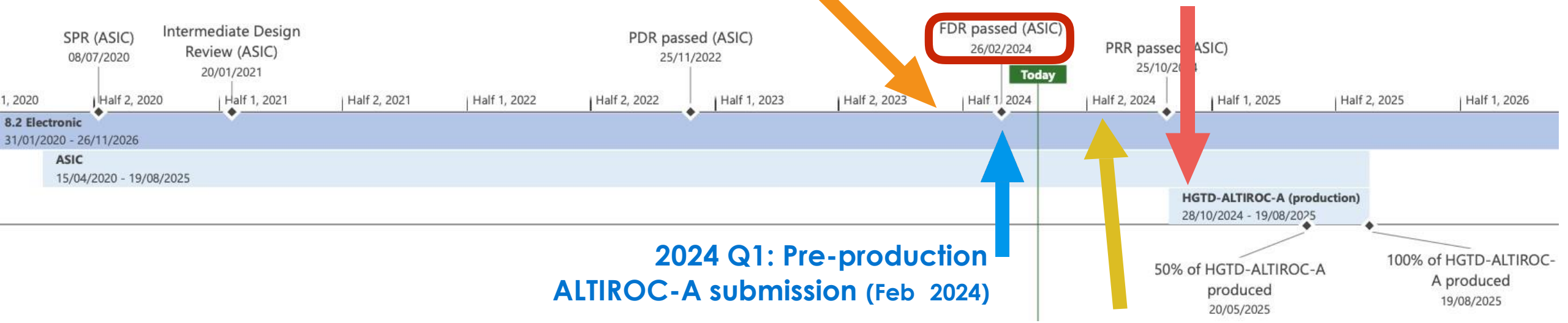
- Asked for PRR at the end of June, but the possible date is in the middle of July.

ASIC: ALTIROC

❑ Schedule

2023 Q4: Finished ALTIROC3 validation: beam test + irradiation, and designed pre-prod ASIC (HGTD-ALTIROC_A)

2024 Q4-2025 Q3: HGTD-ALTIROC-A production and QA/QC tests with probe station



2024 Q1: Pre-production ALTIROC-A submission (Feb 2024)

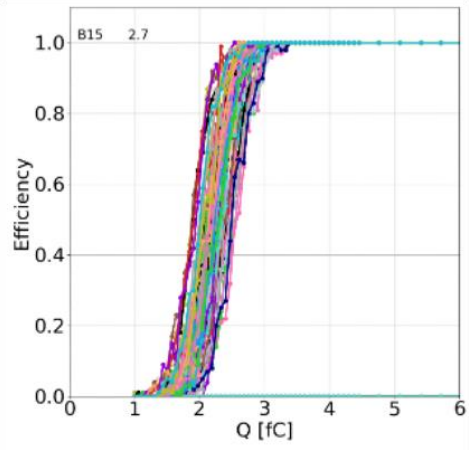
2024 Q3: HGTD-ALTIROC-A validation tests (including assembly and TID irradiation)

- ALTIROC3 is the last prototype before pre-production
- ALTIROC-A is now the production chip
  - First wafers released from TSMC, will ship to IMEC between 4th and 5th week of June

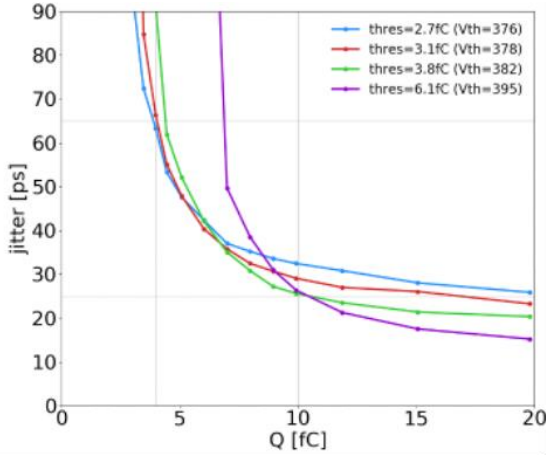
ASIC: ALTIROC

❑ ALTIROC3 validation (ASIC + sensor)

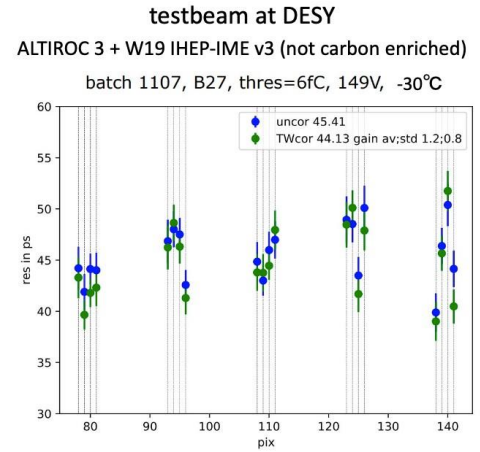
➢ Testing from ~April 2023 to February 2024, before FDR decision



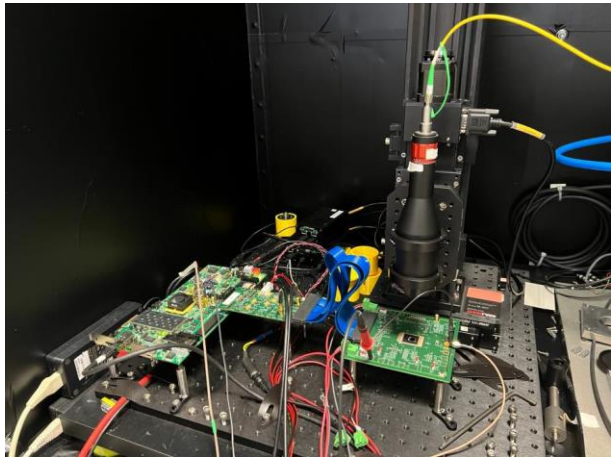
Lowest detectable charge~2.7fC



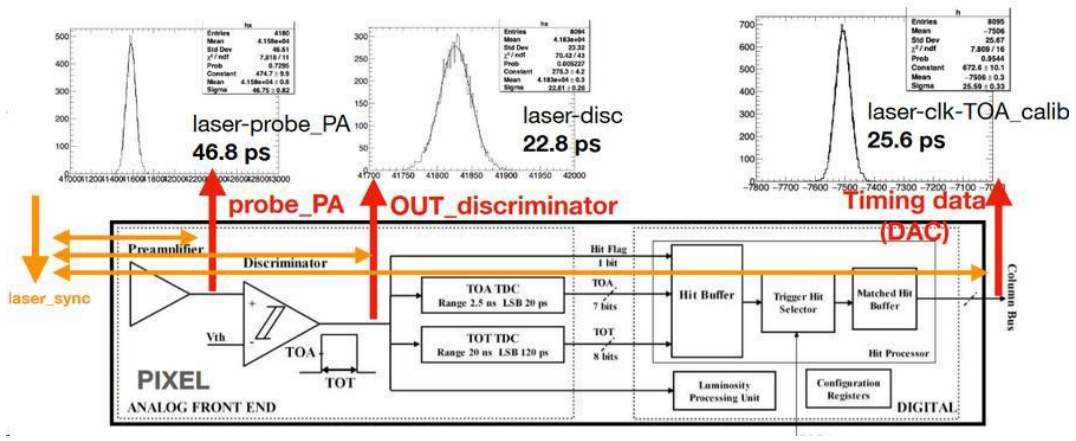
Jitter: 25 ps @ 10 fC, < 65 ps @ 4 fC



~45 ps after calibration and time walk correction



LASER tests



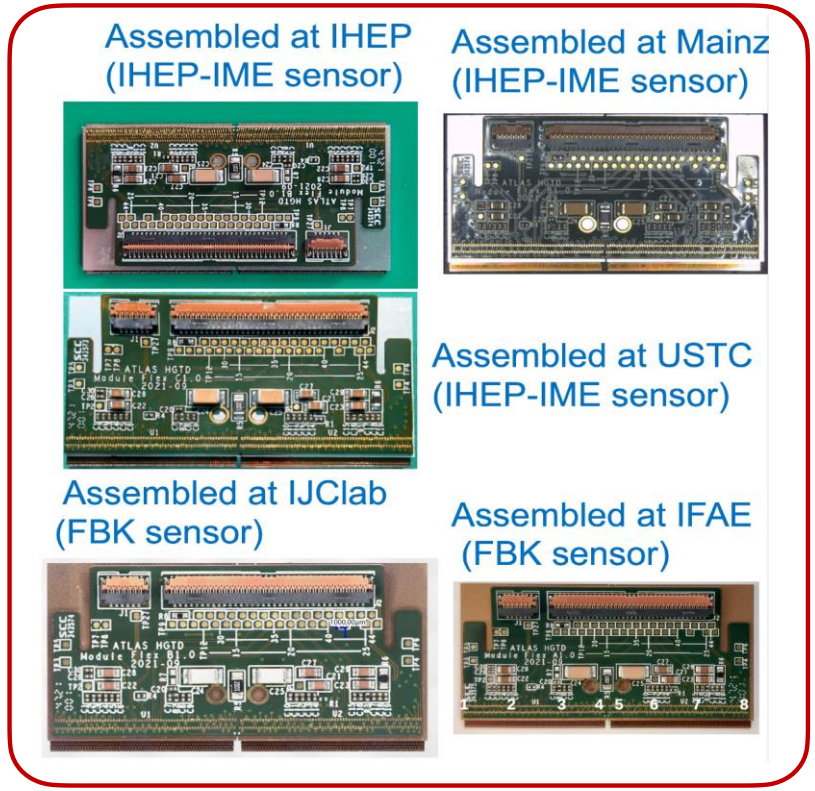
√(25.62 - 22.82) = 11.6 ps (tdc and ck jitter contributions)

➢ ALTIROC3 satisfies or is close to satisfy HGTD requirements

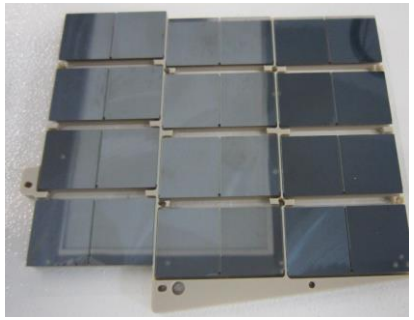
- A few minor digital and analog modifications were included in ALTIROC-A

MODULE AND DETECTOR UNIT ASSEMBLY

- **5 sites (out of 6) have assembled modules up to specs**
  - More than 60 modules assembled
- **2 sites (LPHNE, IHEP) has assembled detector units (ready)**
  - Three Detector Units (DU) already in the demonstrator



Front of FI01DU



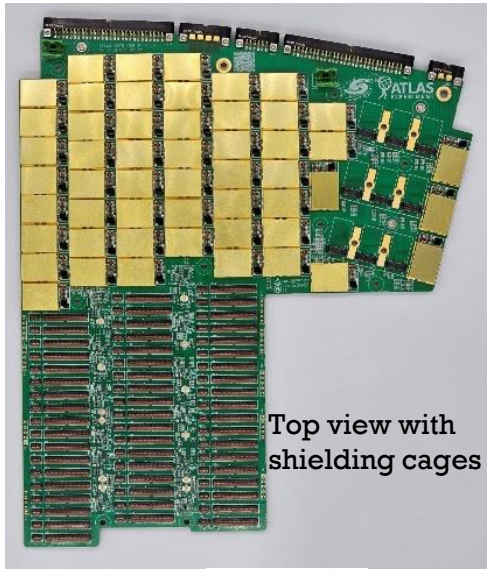
Back of FI01DU

PEB 1F

Peripheral board	Modules	lpGBT	bPOL12v	MUX	VTRx+
1F	55	9+3	52	9	9

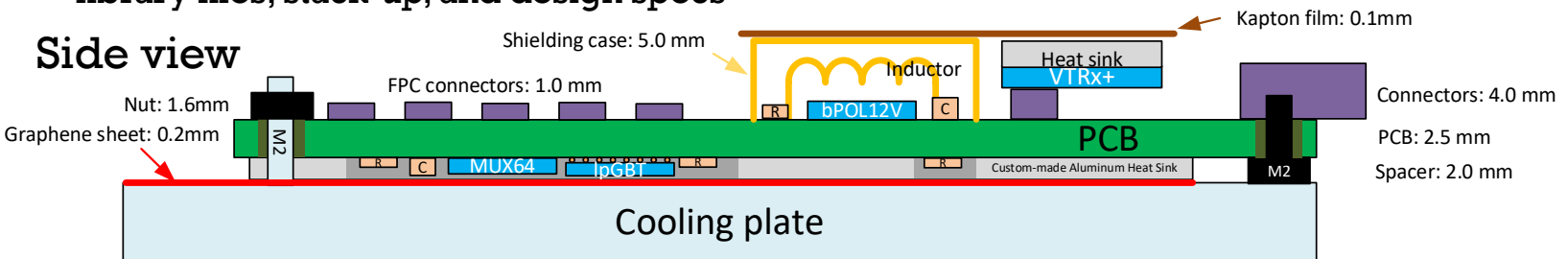
Key dimensions

- Total thickness: 9.7 mm
  - Shielding case: 5.0 mm
  - PCB: 2.5 mm
  - Spacer: 2.0 mm
  - Others: 0.1~0.2 mm
- 55 FPC connectors
  - Center to center distance: 6.5 mm
- 52 bPOL12v power blocks
  - Size: 24 mm x 14.5 mm
  - Height above PCB: 5 mm
  - Height under PCB: 2 mm


Top view with shielding cages

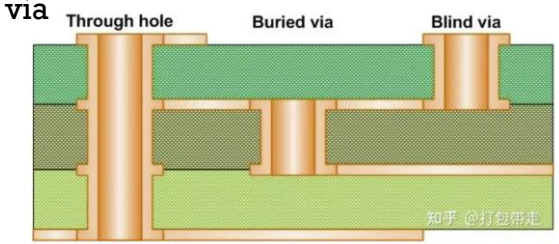
- PEB 1F prototype designed by IHEP, fabricated by Nanjing University
- Other shapes: derived from this board, sharing library files, stack-up, and design specs

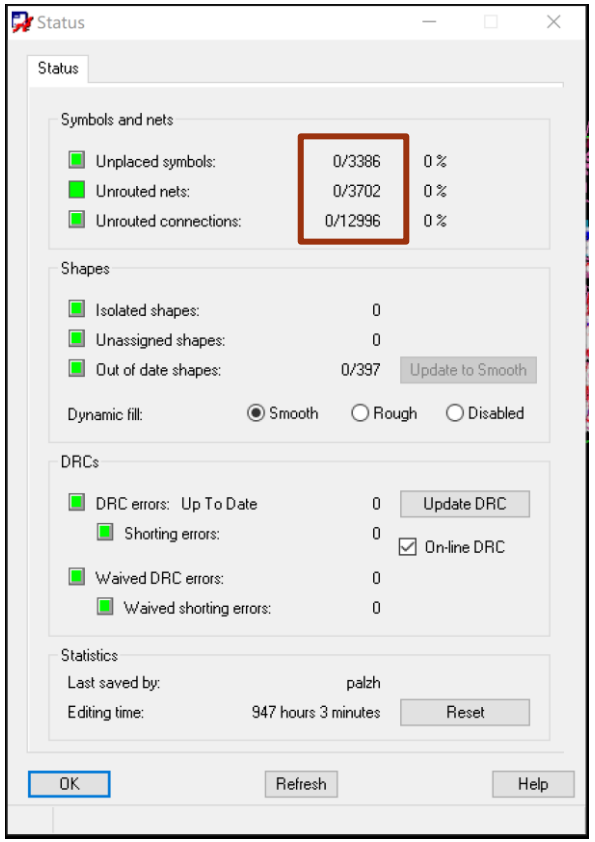
Side view



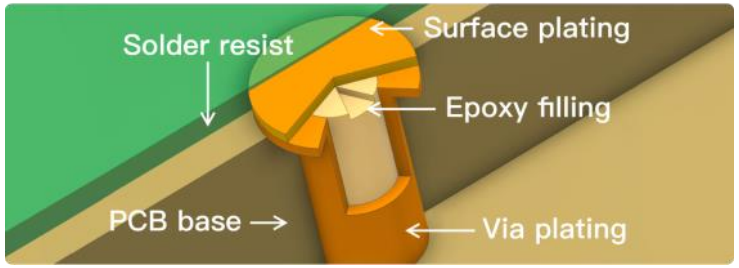
Complex PCB

- High speed, low loss multi-layer material
  - Impedance control
- Halogen free
  - EM-890 or IT-170/988 or R-5375(E)
- Symbols and nets
  - 3386 components, 12996 connections
- 22 layers PCB for PEB 1F, includes:
  - 8 layers for signals
  - 2 layer for HV and HV return ground
  - 4 layers for ground
  - 8 layers for power
- HDI (High Density Interconnector)
  - Micro via





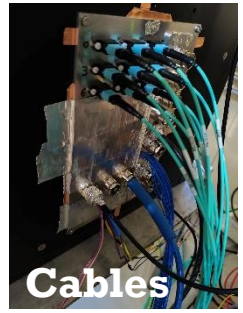
- VIPPO / POFV: Via-in-Pad Plated Over PCB

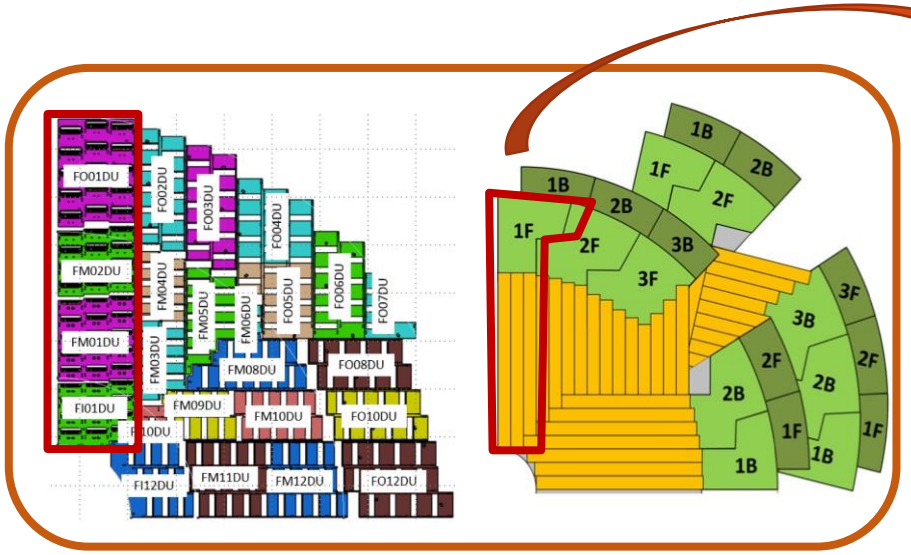


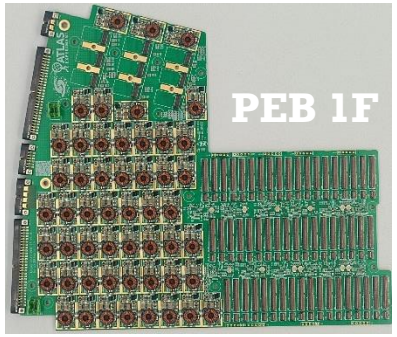
DEMONSTRATOR

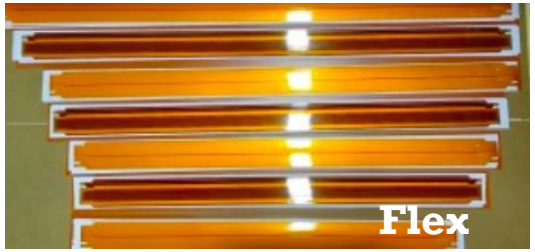
❑ Demonstrator at CERN

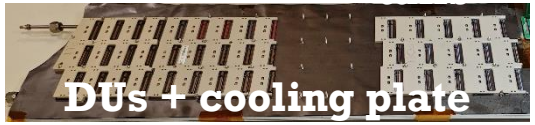
- ➢ With full chain from module to DAQ server
- ➢ PEB 1F + 42 modules in 3 columns + Flex tails + HV + cooling
  - PEB 1F: move forward to FDR
  - Flex tails: full set of flex tails fabricated
  - HV: FDR passed with recommendations in April, under bidding by IHEP











Demonstrator at CERN (Building 180)

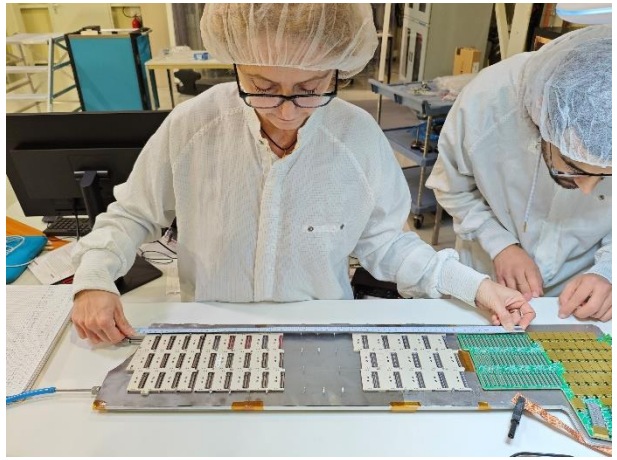
- **Cooling and vessel designed by IJCLab-Orsay**

DEMONSTRATOR

❑ Testing ongoing with demonstrator

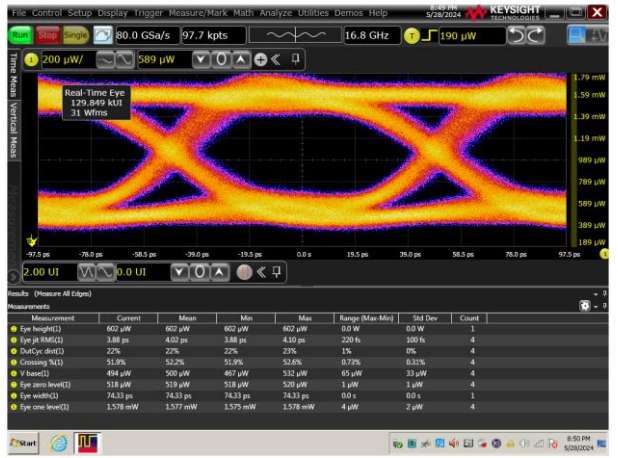
➢ The activities based on the demonstrator are crucial for validating the design, components installation, and connections.

DU installation



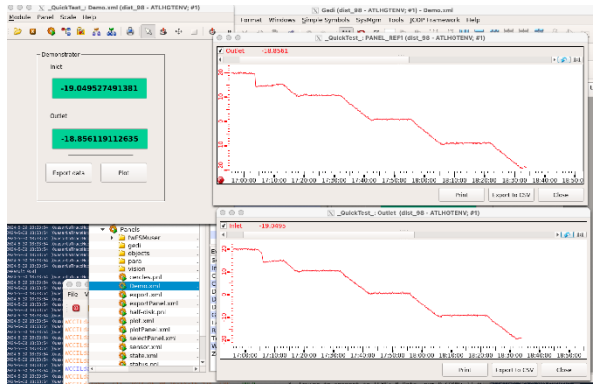
Flex tail length checking

Module-PEB connection

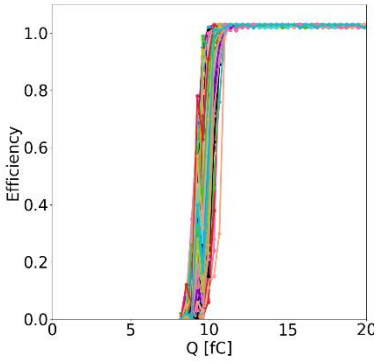


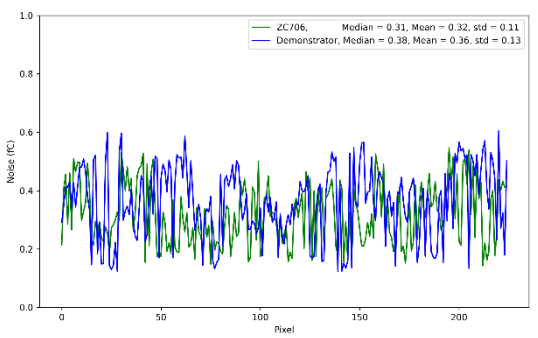
10.24Gbps communication

HV test



Cooling test





Charge scanning and noise analysis

SUMMARY

❑ Good progress in all the main areas of the project

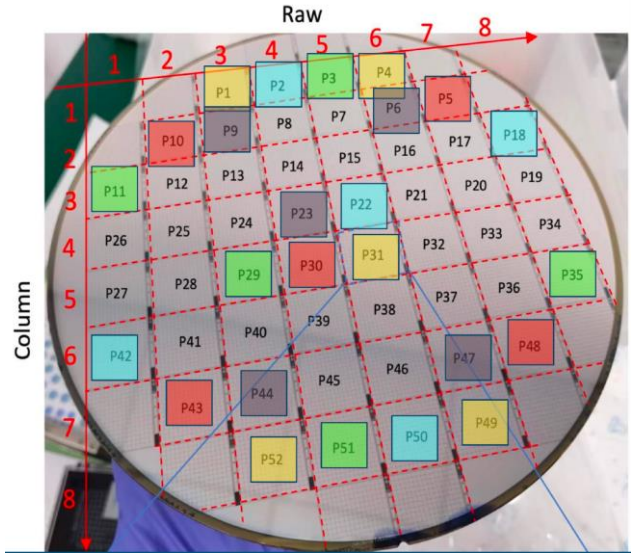
- ➢ Pre-production sensors so far in very good performance
  - PRR at the middle of July
- ➢ ALTIROC-A taped-out
  - A few minor digital and analog modifications included in ALTIROC-A
  - Finished FDR and ALTIROC-A submission in Feb., engineering run almost done, start to test soon
- ➢ Three detector units with 42 modules available and tested
  - The fourth detector unit under assembly
- ➢ PEB 1F prototype finished
  - Finished vendor qualification
- ➢ A lot of tests performed with demonstrator
  - under test at low temperature in CERN

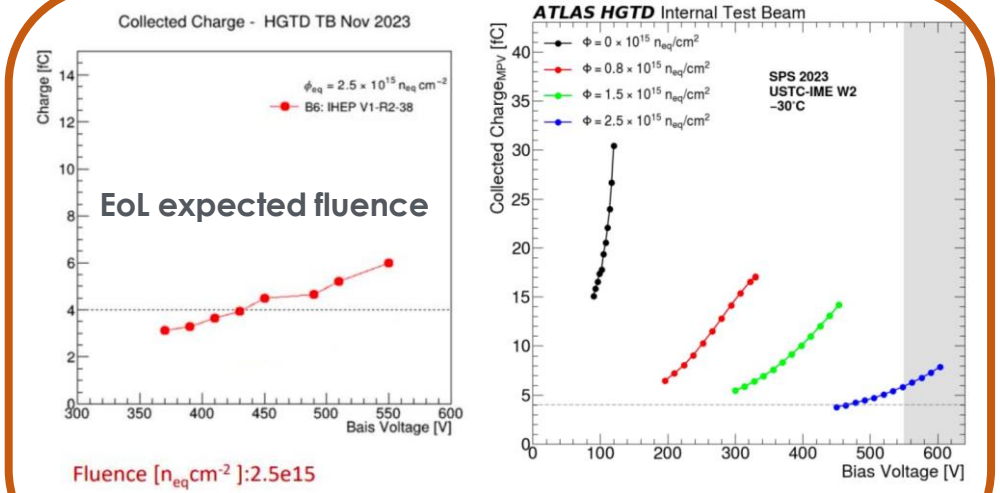
THANKS TO YOUR ATTENTION

LGAD SENSOR

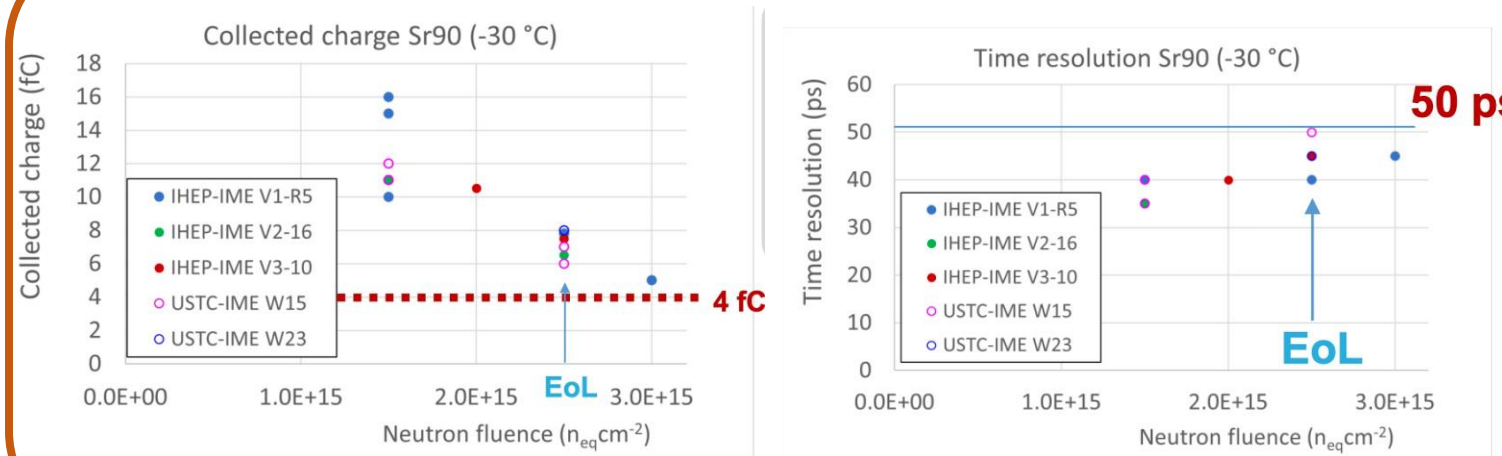
❑ Pre-production QA/QC

- ➢ Full QA/QC deployed for pre-production and final production
  - Full-size Sensor Quality Check by vendor, check by HGTD on a subsample
  - Irradiation Tests (IT) using Sr90 source and test beam
  - Process Quality Control using Test Structures (QC-TS)
- ➢ Few pre-production wafers were used for early tests ahead of UBM
- ➢ Pre-production sensors so far have very good performance
  - All UBM-ed wafers tested so far are within the 4 fC and 50 ps specification



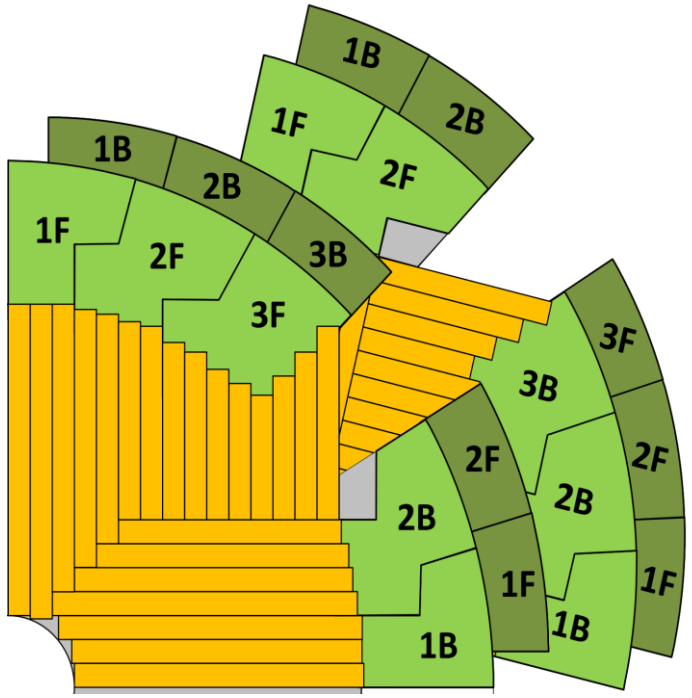


Test beam results



Sr90 source tests

PERIPHERAL ELECTRONICS BOARDS (PEB)



One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- Six types of PEB to be designed (front and back side)
  - Board 1F, 2F, 1B and 2B can be used both on front and back
    - According to the optimization of mirror structure for module layout
  - Each board covers three or more readout rows in order to have a similar number of modules
- The front-end modules are connected via flex tails, arranged in rows, to the PEB @ 660 < r < 920 mm

PEB	Front side	Back side
1F	54 modules	55 modules
2F	52 modules	56 modules
3F	39 modules	-
3B	-	39 modules
2B	52 modules	48 modules
1B	54 modules	53 modules

Number of modules attached to the different PEBs at the front and back sides

- 80 boards per HGTD vessel, thus 160 boards in total.

PEB	1F	2F	3F	3B	2B	1B
Total Qty.	32	32	16	16	32	32

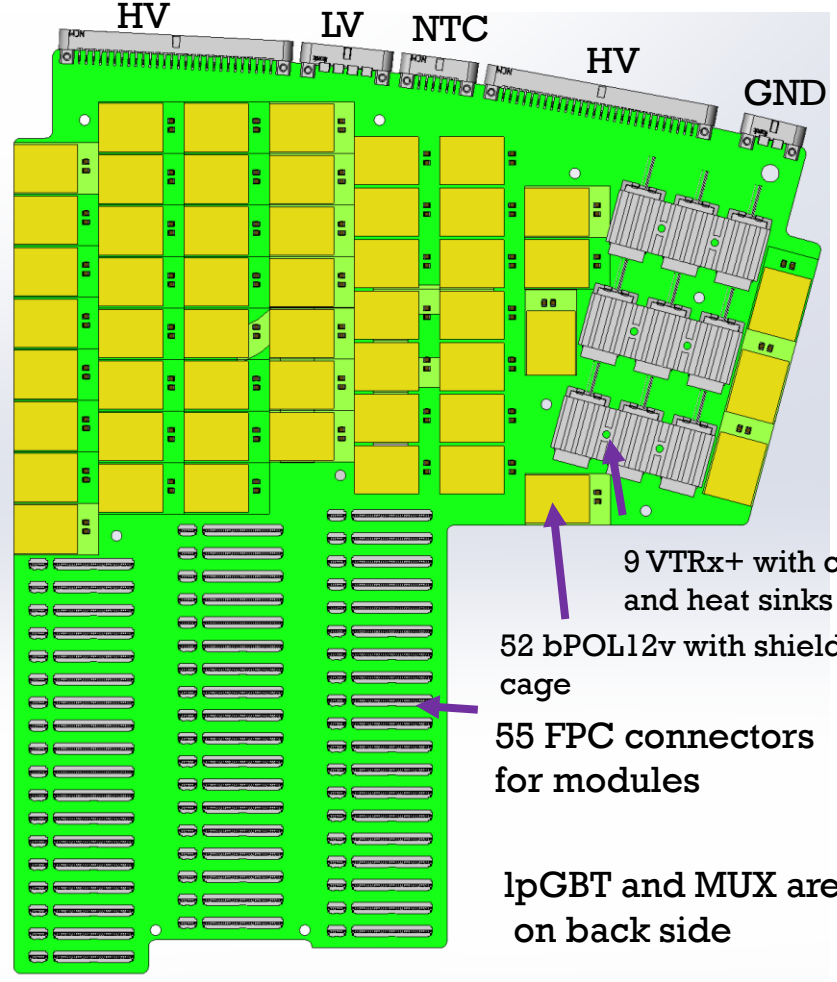
CHALLENGES TO ON-DETECTOR ELECTRONICS

Basic functions of PEB

- Control, monitoring & data aggregation and transmission
  - 8032 front-end modules
    - Clock and fast command distribution
    - Up to 50k analog monitoring
    - TOT/TOA data, up to 10 Tbps to TDAQ, on average, 63 Gbps per PEB
  - LV & HV power-supply distribution
    - Low noise, heat dissipation, system level shielding and grounding considerations
  - Thermistor connection between the front-end modules and the interlock system
    - 896 Negative Temperature Coefficient (NTC) sensors to monitor disk temperature
- Area and height restrictions
  - Limited surface area for connectors, chips and power blocks
  - Height < 10 mm, hard to find low-profile air-core inductors and connectors
- Radiation tolerance for PEB

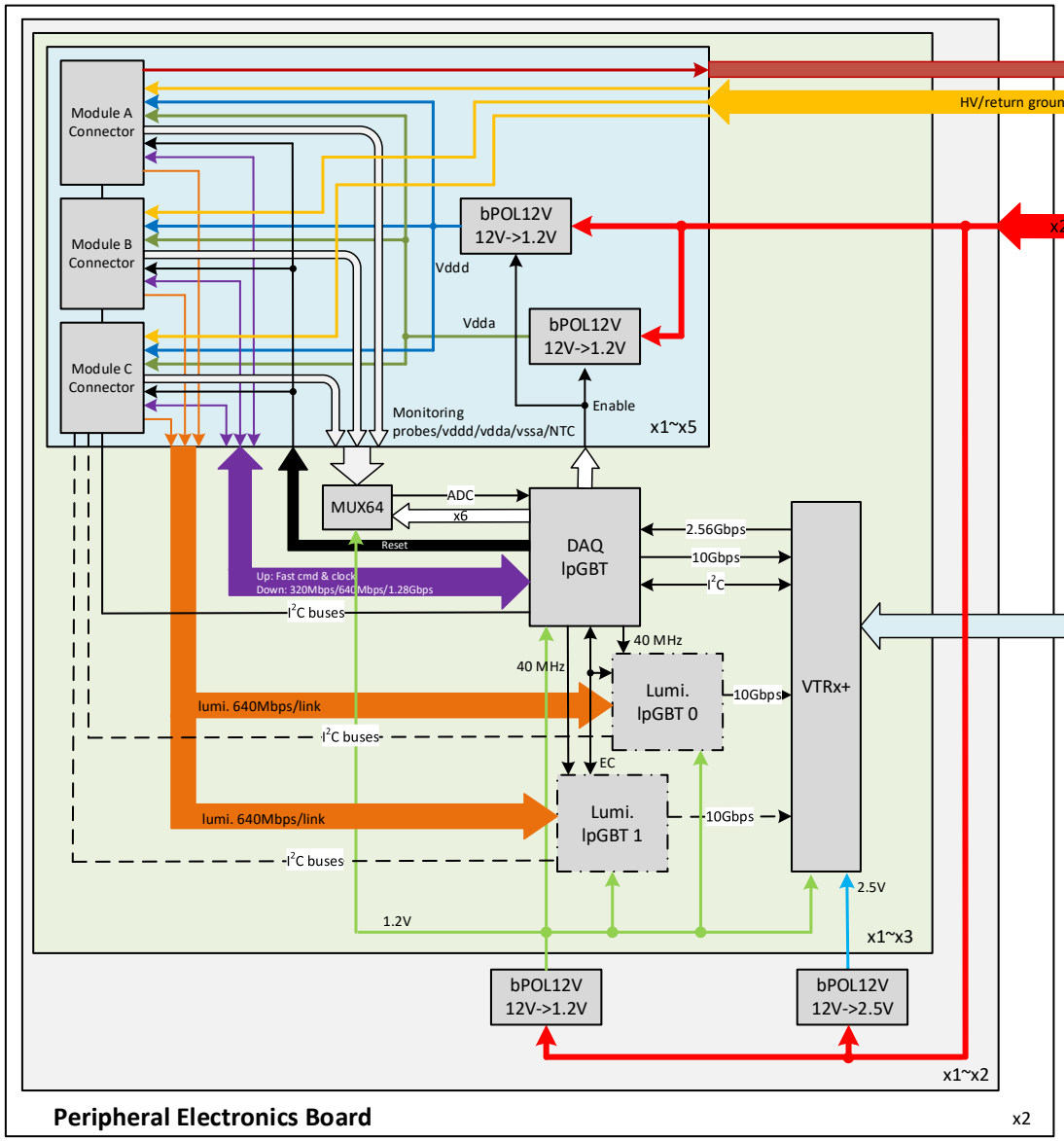
	From simulation	Safety factor	Design requirement
Si 1 MeV neutron equivalent	< 1.4 x 10^{15} neq /cm^2	1.5 x 1.3	2.73 x 10^{15} neq /cm^2
Fluence of hadrons > 20 MeV	< 0.32 x 10^{15} neq /cm^2	1.5 x 1.3 x 2	1.25 x 10^{15} neq /cm^2
TID	< 36 Mrad (0.36 MGy)	1.5	54 Mrad (0.54 MGy)

- Magnetic field
  - Amplitude: 0.382 T ~ 0.433 T
  - Angle 23.1˚ ~ 32.3˚
- Operating Temperature:
  - On disk (with front-end modules and CO2 cooling): -35 ℃ ± 5 ℃
  - Testing/debugging (with cooling): -40 ℃ to 55 ℃



Top view of PEB 1F

CONCEPTUAL DESIGN OF PEB



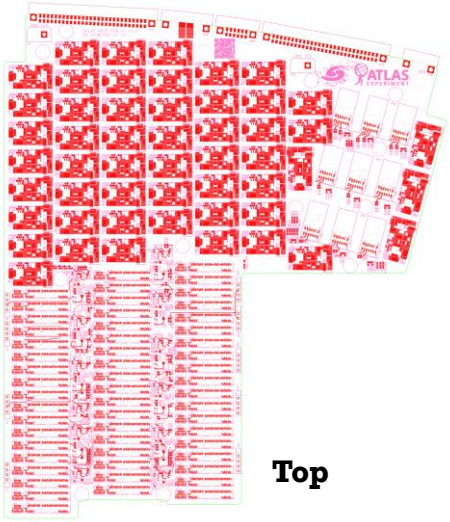
- Two LV channels
  - Each up to 12A @ 12V
- Up to 3 modules share two bPOL12v
  - One for analog power, the other for digital power
- One TDAQ lpGBT and 1~2 luminosity lpGBTs share one VTRx+
- Control
  - I2C of lpGBT
    - Module and VTRx+ configuration
    - I2C0 of TDAQ lpGBT is connected to the VTRx+ only
  - Output
    - Module reset
    - Module power on/off
    - MUX64 channel selection
- Monitoring
  - ADC of lpGBT
  - Module state monitoring
    - VDDA, VDDD, GNDA, PROBE0/1(internal state and temperature), NTC
  - PEB state monitoring
    - lpGBT voltage, temperature
    - VTRx+ RSSI(average optical power of the received light) and NTC
    - bPOL12v temperature
    - On board NTC
  - Input of lpGBT
    - bPOL12v power good signal

bPOL12V:
provide the 1.2V analog and digital voltages for the ALTIROCs

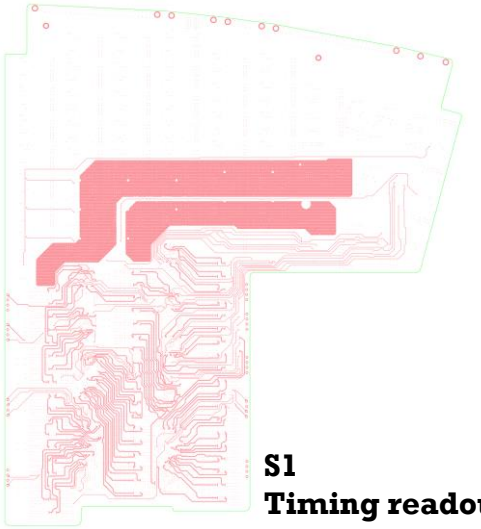
lpGBT:
Bi-directional slow control and monitoring communication between the FELIX and the lpGBT is done via the IC and EC channels.

Each lpGBT has a 8 channel multiplexed ADC.
With ~7 modules/lpGBT, an external 64-to-1 MUX is required: **MUX64**

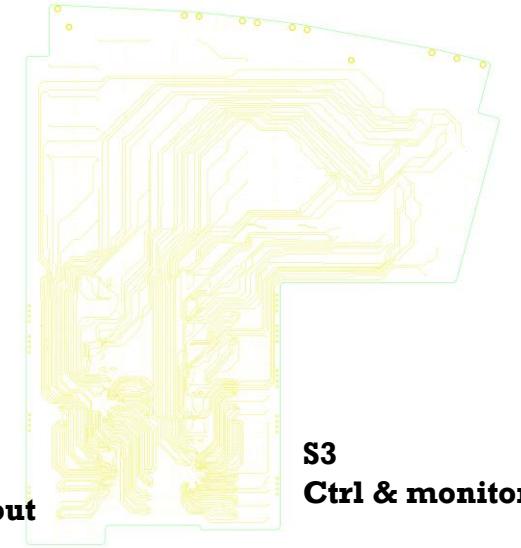
PEB 1F ROUTING



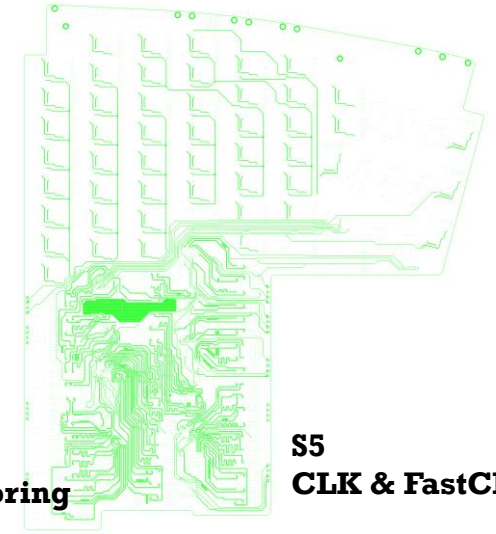
Top



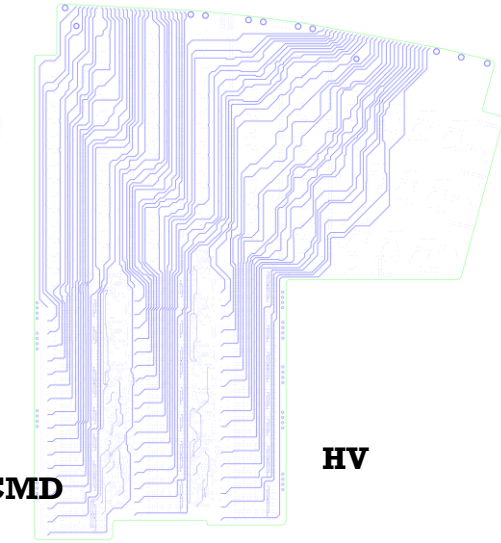
S1
Timing readout



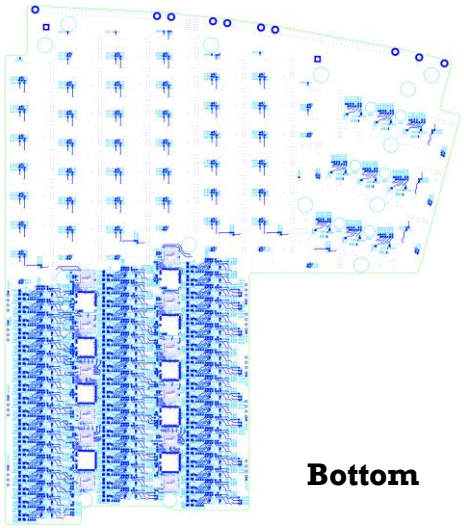
S3
Ctrl & monitoring



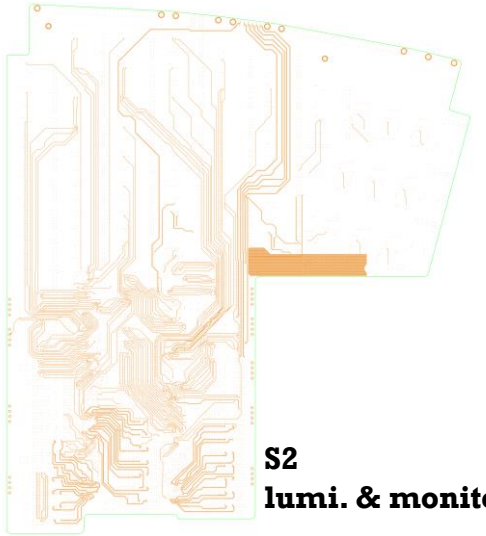
S5
CLK & FastCMD



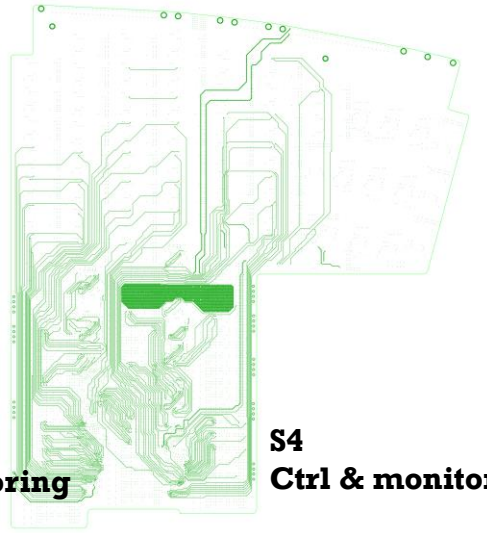
HV



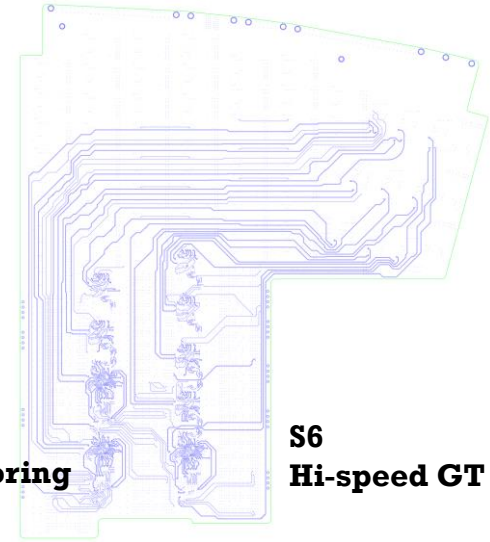
Bottom



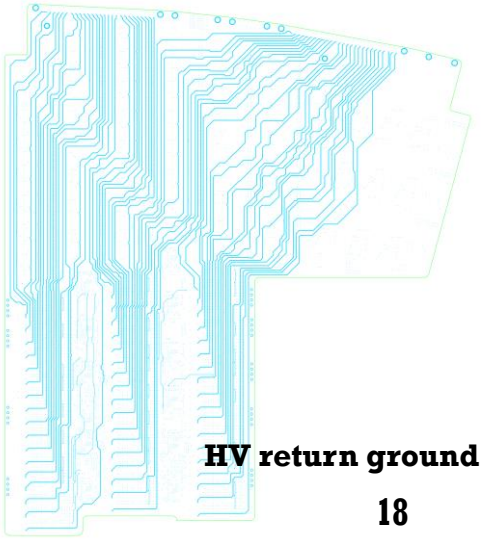
S2
lumi. & monitoring



S4
Ctrl & monitoring



S6
Hi-speed GT

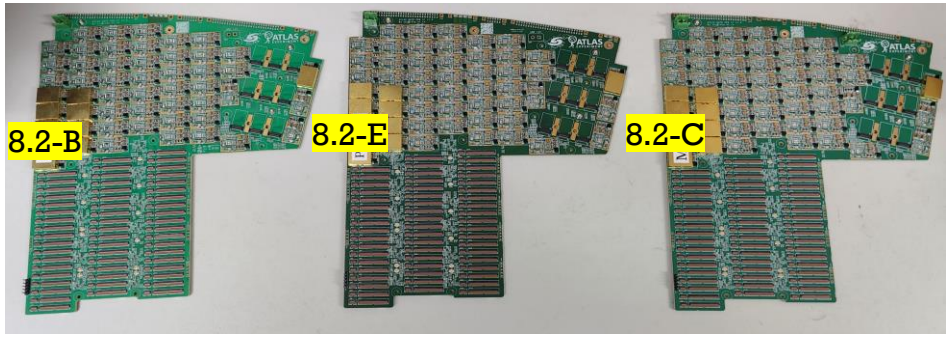


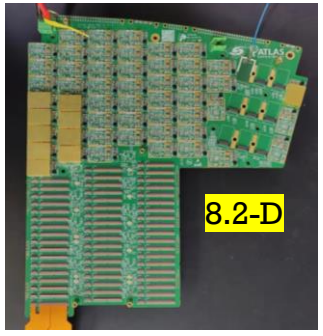
HV return ground

PEB 1F-PROTOTYPE FABRICATION AND PRE-QUALIFICATION

- Highly qualified vendor to be chosen for the PCB fabrication and assembly.
  - The qualification process includes participation of the candidate vendors in the PEB prototype, and evaluation of the quality of the delivered product
  - 4 companies joined PEB 1F prototype fabrication by Nanjing University

Vendor	2022 annual revenue in China (*)	PCB Material	Start date	Finish date	Fabrication time	Comment	Assembly: To verify the PCB and save the chips, only one group of each board is assembled	
8.2-D	In top20	IT-170	Sep. 27th	Nov. 20th	54 days	Failed to merge the sandwich in the first batch, alignment problem; The second batch is OK	1 group	Finished at Nov. 29th, 2023
							-	-
8.2-C	In top100	EM-890K	Sep. 15th	Dec. 13th	89 days	Failed in the first batch; The second batch is OK	1 group	Finished at Dec. 21st, 2023
							-	-
8.2-B	In top5	EM-890K	Nov. 10th	Dec. 19th	39 days	High quality, promised fabrication time	1 group	Finished at Jan. 2nd, 2024
							Full assembly	2 pcs finished at Jan. 15th, 2024 One kept in IHEP One sent to CERN at Jan. 22th, 2024 The third one under assemble for reliability testing
8.2-E	Taiwan	TU-883A	Nov. 28th	Dec. 18th	20 days	High quality, very fast, but need international transport	1 group	Finished at Dec. 27th, 2023
							-	-

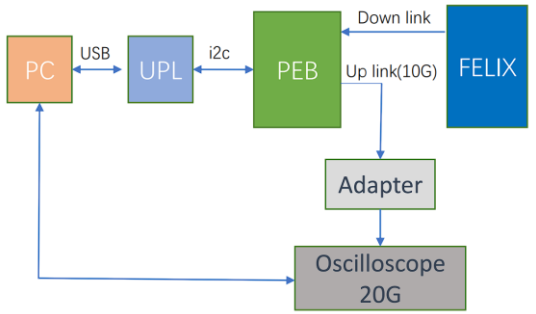




*Note: https://www.eet-china.com/mp/a133351.html

Photos of PEB 1F from four manufactures

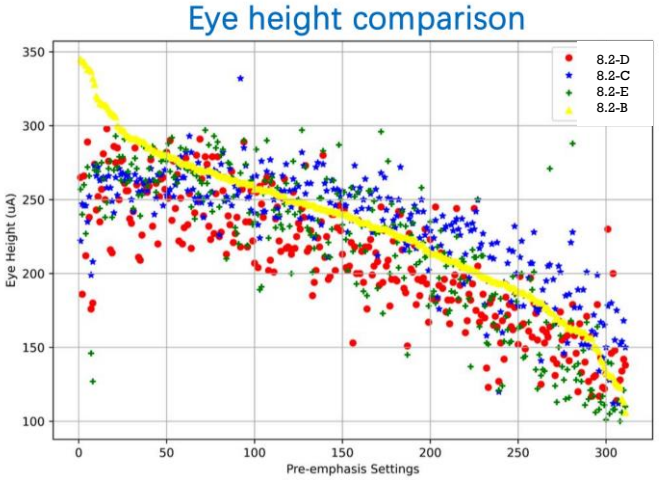
PEB 1F-PRE-QUALIFICATION

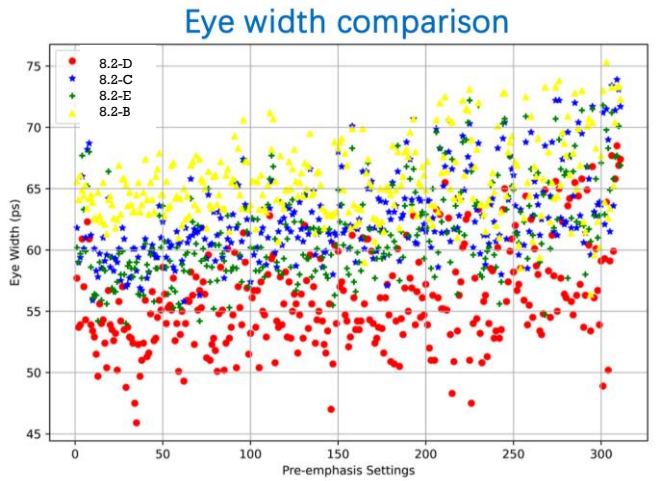


- Eye Diagram Test for 10Gbps
  - Setup
    - Use FELIX to provide down link data for lpGBT clock recovery
    - Use UPL to configure the pre-emphasis parameters of lpGBT
    - Use PC to configure Oscilloscope and record eye diagram parameters and waveforms.
    - Follow the steps below for scanning.

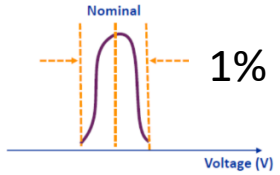
```
for T_modulation_current in range (47,128,3):
    for T_emphasis_enable in range (1,2):# always enable
        for T_emphasis_short in range (0,2):
            for T_emphasis_amp in range (20,101,3):

                try:
                    peb.timing.lpgbt.line_driver_setup(
                            modulation_current = T_modulation_current,
                            emphasis_enable = T_emphasis_enable,
                            emphasis_short = T_emphasis_short,
                            emphasis_amp = T_emphasis_amp
                        )
```

- Test result
  - Eye height: 8.2-B, 8.2-C are better than 8.2-D, 8.2-E
  - Eye width: 8.2-B > 8.2-C > 8.2-E > 8.2-D
  - The result is consistent with the materials used by each vendor
  - We plan to use 8.2-B as the qualified vendor
    - One of the "official" vendors from CERN,



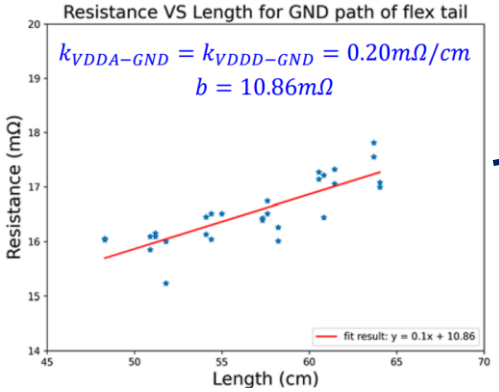


Challenges - PEB Power Settings

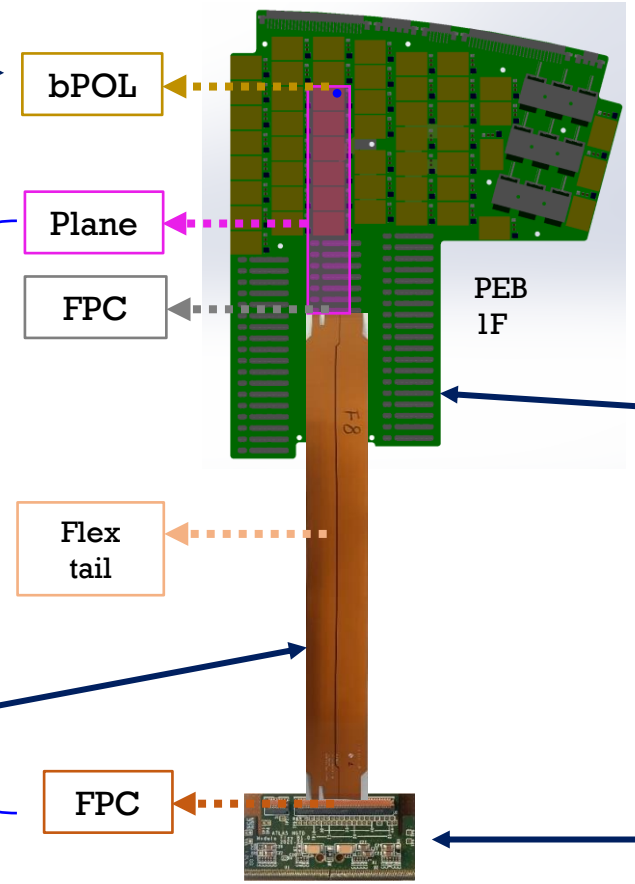


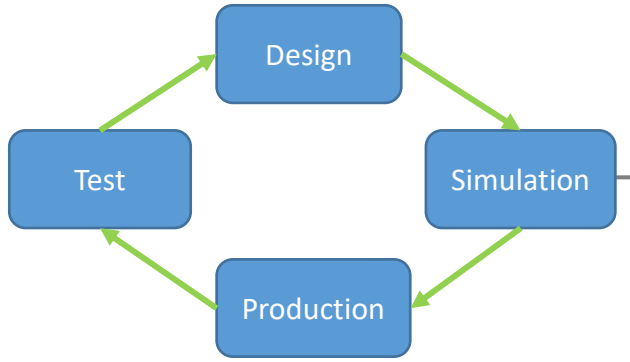
1%

bPOL output distribution from the modular PEB

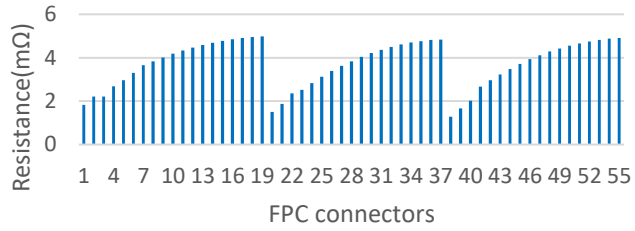


R

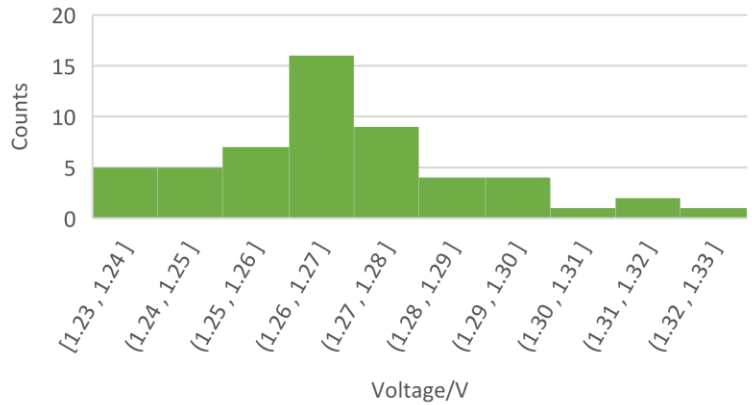




Resistance simulation of the GND power planes for 55 modules on PEB

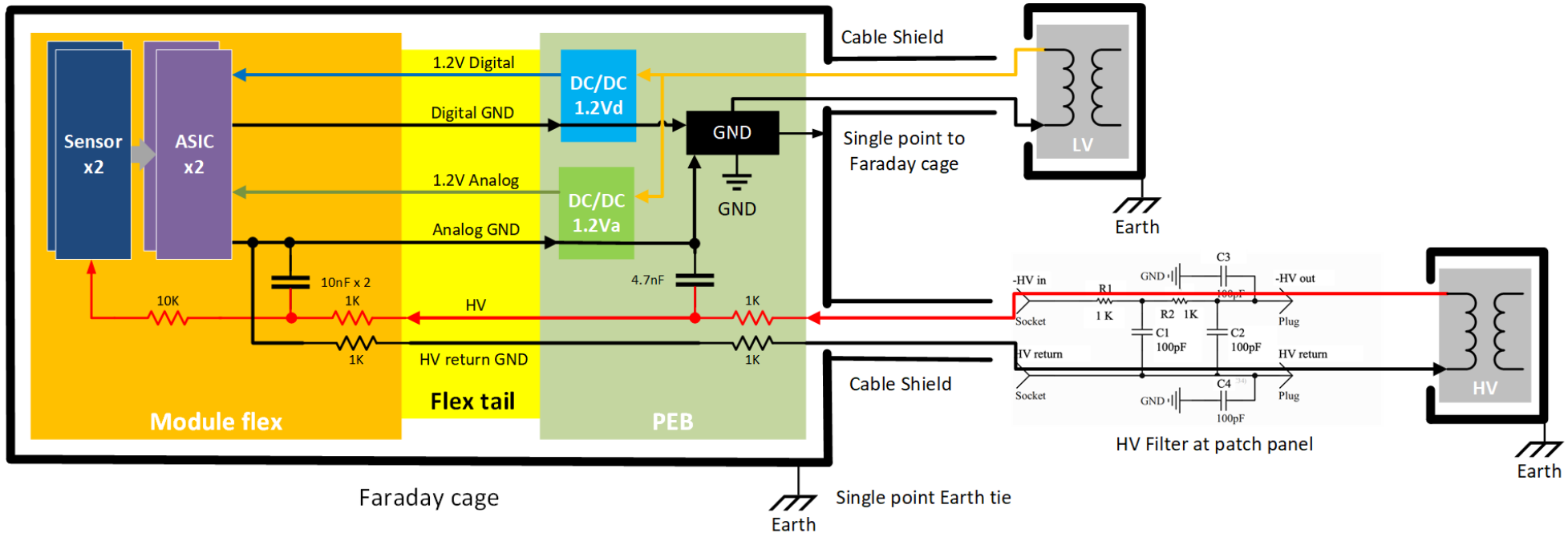


Tested analog power distribution for PEB 1F



21

GROUNDING & SHIELDING



- Single point connection
  - The hermetic vessel acts as the Faraday cage, which is referenced to the experiment ground by a single dedicated copper braid per end cap.
- Each PEB will have be referenced to the Faraday cage by one single low ohmic strap to the conductive layer of the outer ring.
  - The modules and the PEB shall have thermal conductive connection to the cooling plate but be electrically isolated from the cooling plate.
- The stage2 LV supplies are referenced to ground by their return lines being connected to the ground planes of the PEB which they supply.
- The HV at each module is then referenced to ground through the analog ground plane at the module end.