Progress of LHCb ECAL Upgrade II Studies

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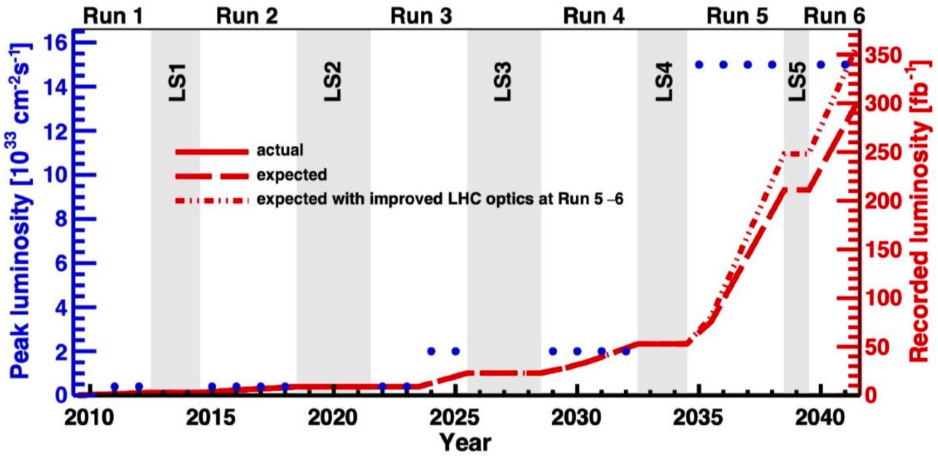
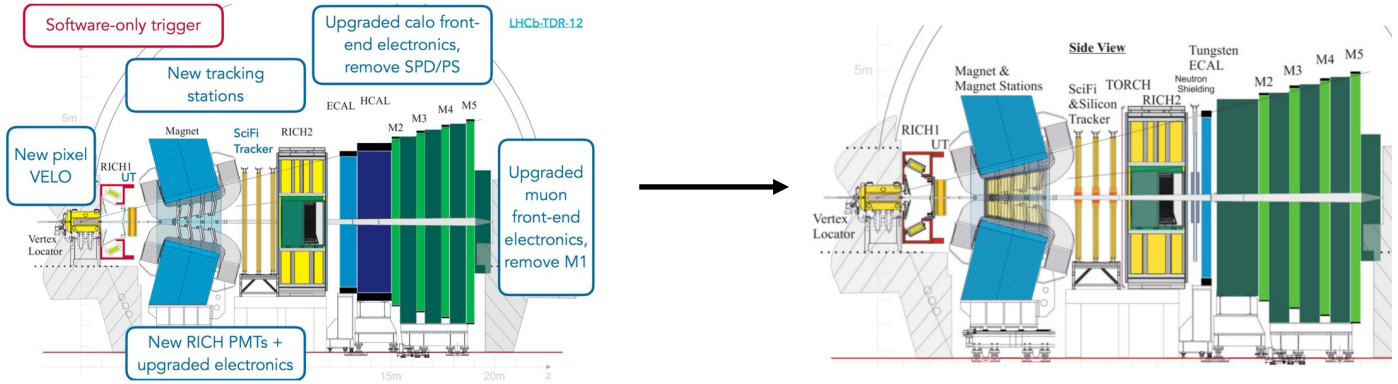
LHCb Upgrade II

- New detector proposed for LHCb during Runs 5 and 6 of the LHC to ingrate 300 fb^{-1} of data at the end of the LHC



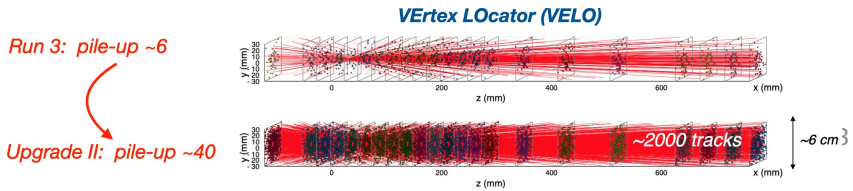
Detector for Upgrade II

- Same performances as Run 3, with a pile-up of 40 instead of 6



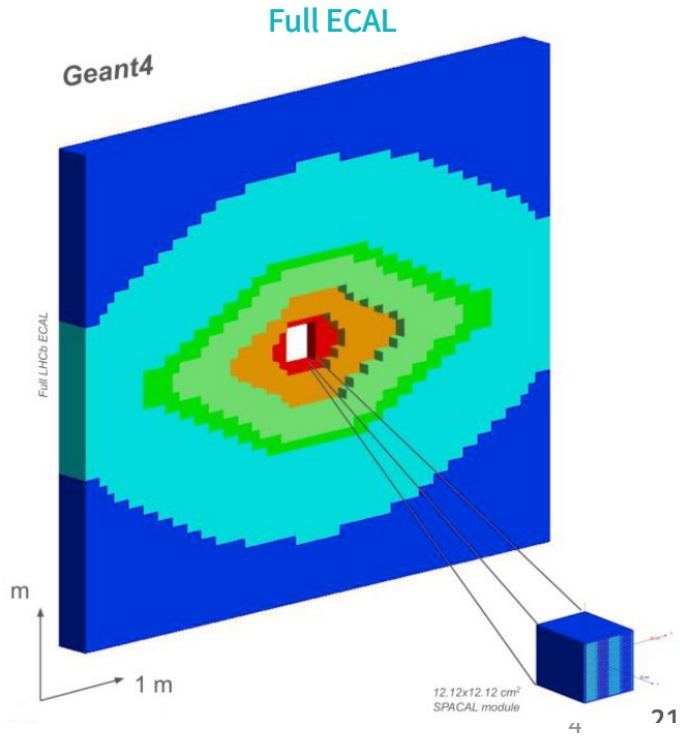
Run 3 Run 5

- Same geometry for the detector with innovative technologies for sub-detectors and data processing
- Main elements:
  - Increase granularity
  - Add timing measurement (resolutions up to 10-50 ps)
  - Radiation hardness (up to 10^{16} n_{eq}/cm^2)
  - Data rate: 200 Tb/s



ECAL Upgrade (PicoCal): Granularity

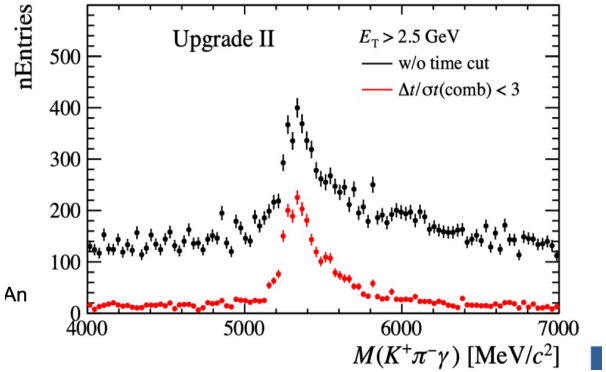
- Improve efficiently performaces at high luminosity
- Reorganize ECAL zones in rhomboic shapes to follow better the radiation and occupancy maps
- Five zones with cells of different sizes: (1 module = 1 bloc of 12x12 cm^2)
  - 1.5x1.5 cm^2: 32 modules (type SpaCal-W) – 2048 cells
  - 3x3 cm^2: 144 modules (type SpaCal-Pb) – 2304 cells
  - 4x4 cm^2: 448 modules (type Shashlik) – 4032 cells
  - 6x6 cm^2: 1344 modules (type Shashlik) – 5376 cells
  - 12x12 cm^2: 1344 modules (type Shashlik) – 1344 cells
- **Baseline option** = Add longitudinal segmentation at shower maximum (separation electron/hadron) in all cells
- One cell = 2 channels for readout (1 front and 1 back)
  - Total of **30208 voies**
- **Descoped option** = No longitudinal segmentation in outer modules (4x4 cm^2, 6x6 cm^2, 12x12 cm^2)



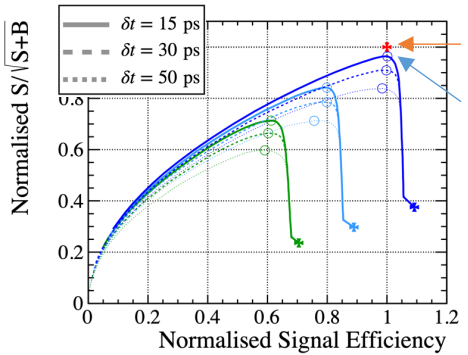
PicoCal: Precise time measurement

- To fight again the large background due to pile-up: add time measurement in ECAL with a precision of 15 ps = PicoCal
- Select cells where $|t_{ECAL}-t_{PV}|/\sigma(t)<3$
  - t_{PV} : collision time measured in other detectors (VELO for example)
  - t_{ECAL} : time measured in the ECAL, corrected from time of flight
  - $\sigma(t)$: ECAL time resolution
- <u>Participations of French and Chinese institutes</u>:
  - Performance studies with simulation in particular to compare baseline and descoped options
  - R&D and characterisation of new modules
  - R&D of new electronics

Effect of timing cut on invariant mass for B→ K*γ



Full simulation of signal $B^0 \to K^{*0}\,\gamma$ with pile-up



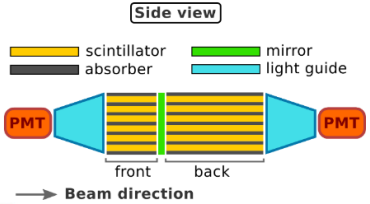
Run 2

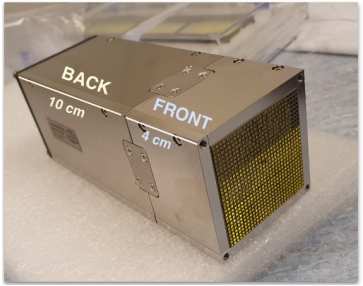
Run 5 (15 ps)

ECAL Modules

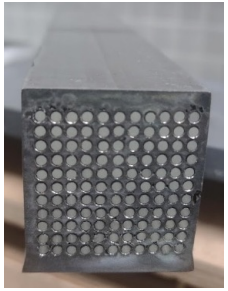
- Ongoing R&D to produce modules allowing a precise time measurement and a relative energy resolution of 10%/sqrt(E)

SPACAL:



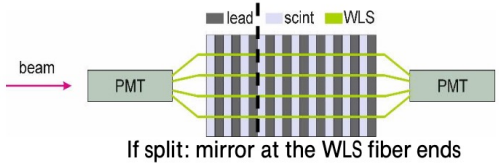


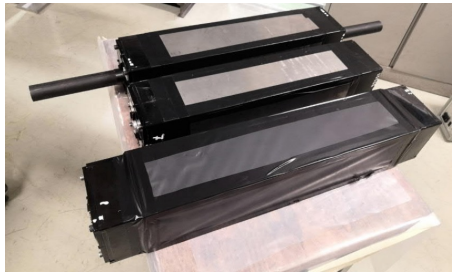
W absorber, cristal fibers (GAGG, gadolinium aluminium gallium garnet):
High radiation tolerance and small Molière radius



Pb absorber, polystyrene fibers

SHASHLIK:





Current modules: external regions

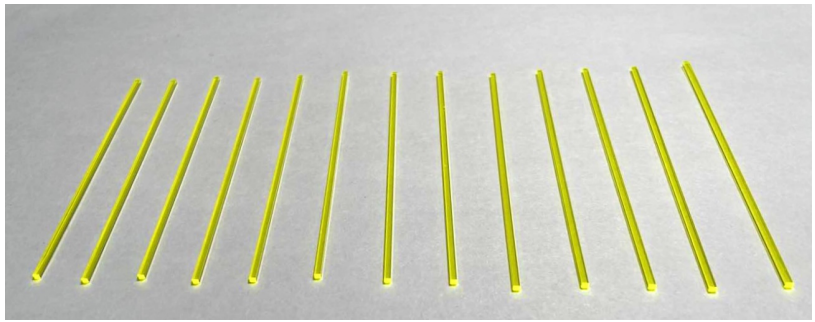
Optimisation of GAGG scintillators

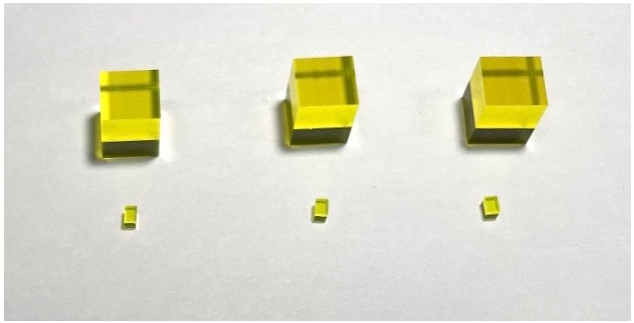
- Good scintillator for innermost part of PicoCal
  - ✓ Radiation-hard
  - ✓ High density
  - ✓ High light output and fast decay time

- Commercial GAGG decay time ~50 ns, desirable ~5 ns
  - ✓ Collaborate with SIPAT to reduce decay time by tuning composition and doping

Decay time ↘ at cost of light output ↘ ~5k/MeV acceptable

  - ✓ High-quality scintillator fibres and samples obtained

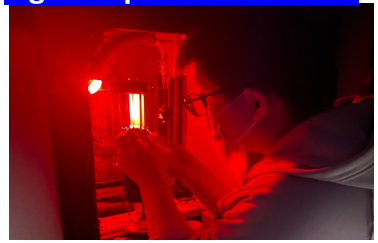




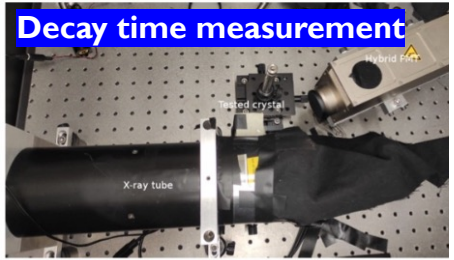
Optimisation of GAGG scintillators

- GAGG samples characterisation at CERN & PKU
  - ✓ Results feedback to SIPAT to iterate

Light output measurement



Decay time measurement



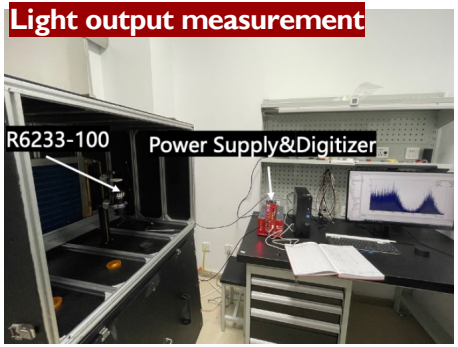
Absorbance

Perkin Elmer Lambda 650

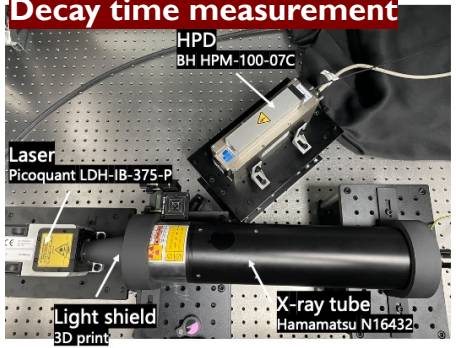
Photoluminescence

Perkin Elmer LS55

Light output measurement



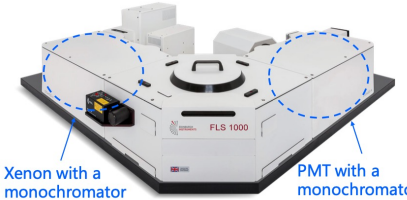
Decay time measurement



Absorbance

Edinburgh DS5

Photoluminescence



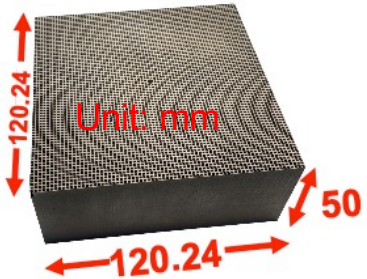
Edinburgh FLS1000

- Now decay time between $15-20$ ns; light output $\sim 10\text{k/MeV}$
- R&D still ongoing

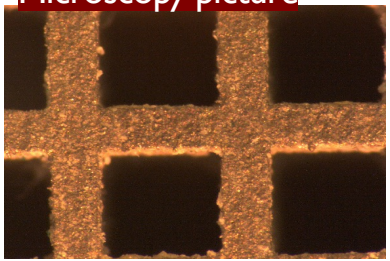
3D-printing tungsten (W) absorber

- W has small radiation length and small Moliere radius
- 3D-printing technology to ease W matrix production
- Collaboration with LaserAdd to produce W absorber
  - ✓ Good samples obtained
    - Good roughness needed not to scratch fibres
    - High density
  - ✓ Characterisation W samples, feedback results to LaserAdd to optimise

雷佳 LASERADD



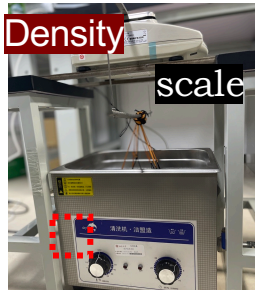
Microscopy picture



Surface roughness

Fiber insertion test

Density



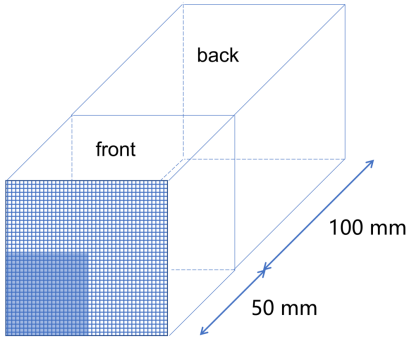
- Good roughness $R_a \approx 4\ \mu m$ achieved, can smoothly insert fibres
- Density (units: g/cm^3)

Pure W	LaserAdd
19.3	18.9

Prototype SPACAL-W+GAGG

➢ New prototype in construction

✓ 3 pieces of 3D-pinted tungsten absorber of $12\times12\times5\ \mathrm{cm}^3$ produced by LaserAdd in China



Prototype schematic

✓ 4x4 cells (1296 holes) equipped by GAGG fibers from SIPAT

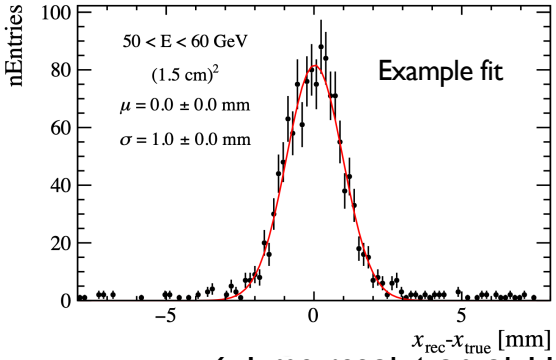
✓ Further cells will be equipped with fibers from other producers later for time resolution studies

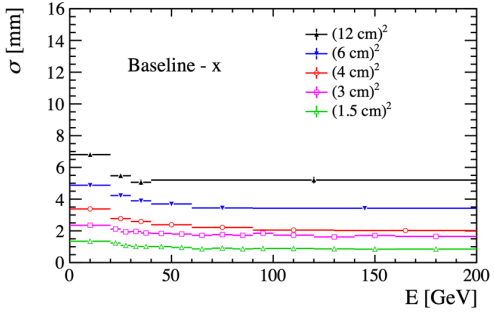
✓ Double-sided readout

➢ Testbeam at SPS this June

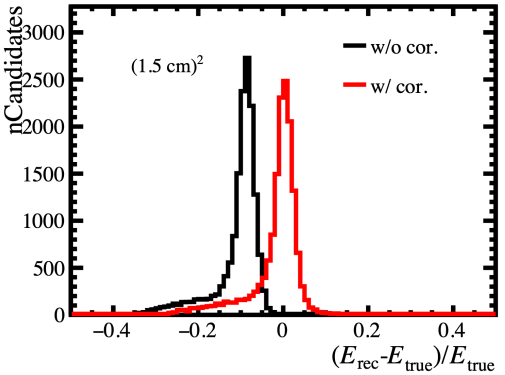
Resolution studies with full simulation

- Resolution studied with single-photon sample: good precision as expected
  - ✓ Position resolution of 1mm in the inner part:

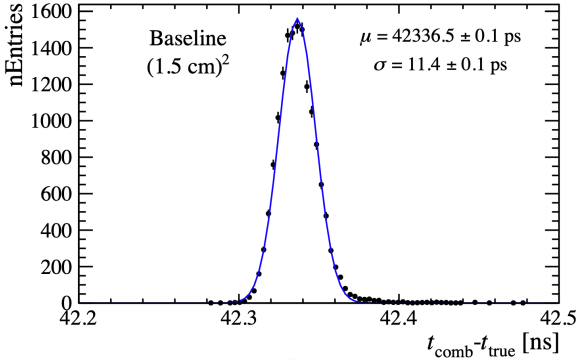




  - ✓ Energy resolution: relative 10%/sqrt(E)



  - ✓ Time resolution of 11ps in the central part:

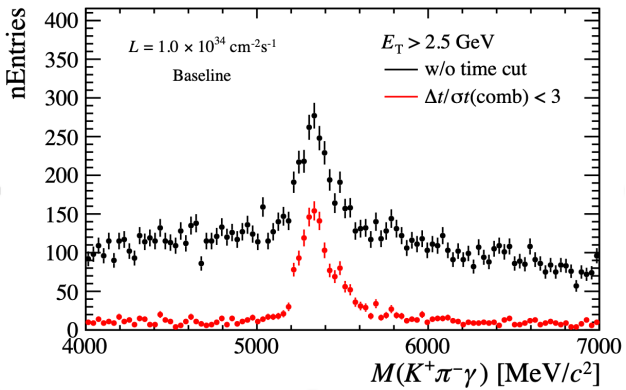


Cell size [cm²]	Time resolution [ps]	
	Baseline	Downscoped
1.5×1.5	11.4	11.4
3×3	13.8	13.8
4×4	20.2	43.4
6×6	22.4	42.2
12×12	24.3	44.0

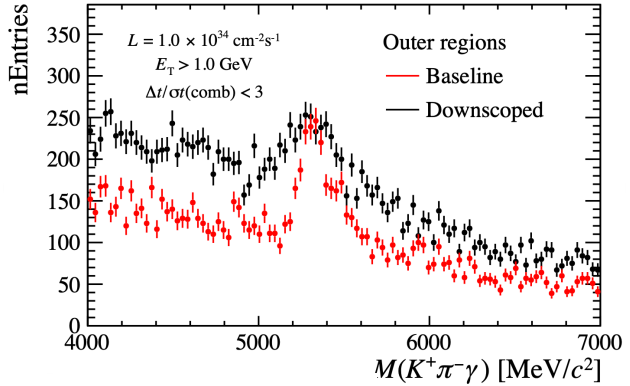
Performance studies with full simulation

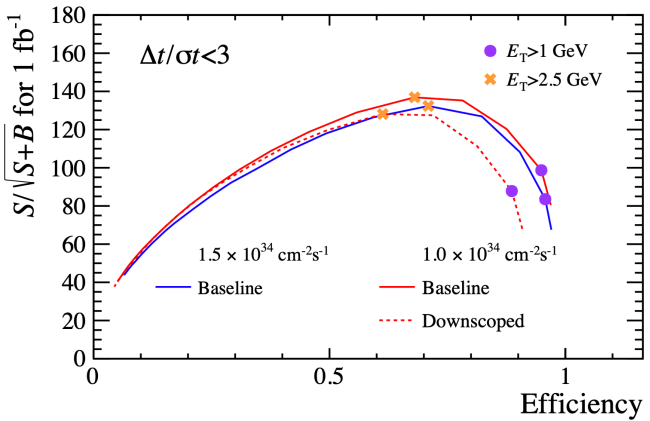
➢ Benchmark channel: $B^0 \to K^{*0}\gamma$

✓ Timing cut effective in reducing bkg.



✓ Larger background level with downscoped PicoCal setup (worse time resolution)

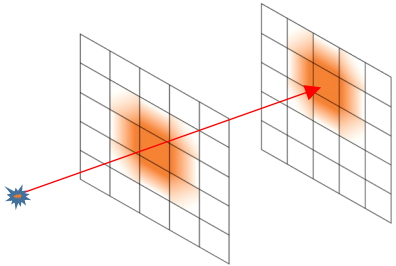




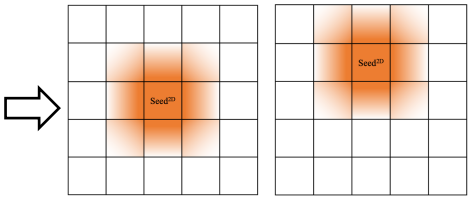
✓ Performance comparison taking $S/\sqrt{S+B}$ per fb^{-1} as Figure Of Merit : significantly worse performance with downscoped PicoCal setup

Reconstruction algorithm development

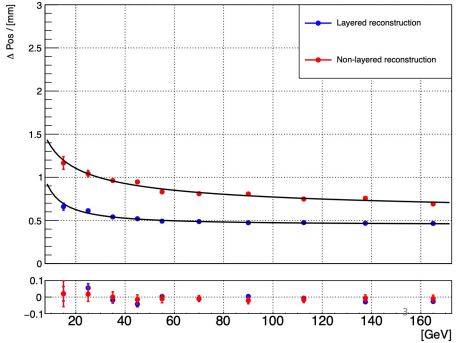
- A new reconstruction algorithm is being developed to take into account the longitudinal segmentation (i.e. Layered reconstruction)



Front section Back section



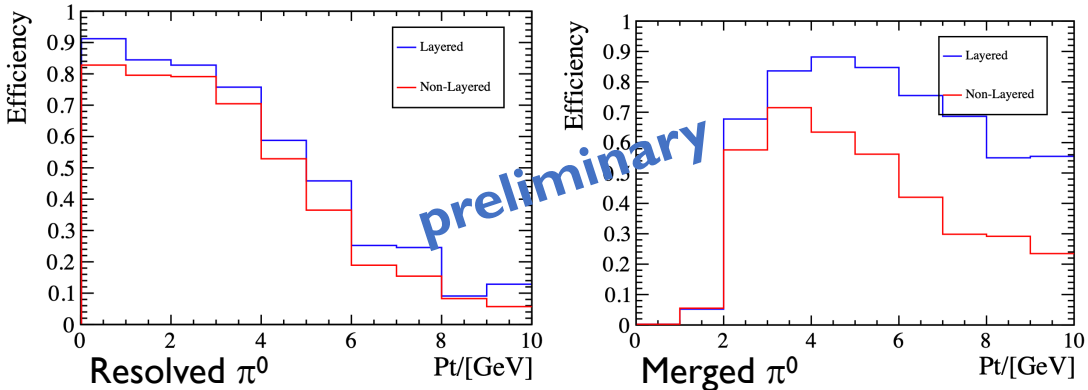
*Shift of seed cell from front to back section



*Position resolution with single-photon:large improvement with new algorithm

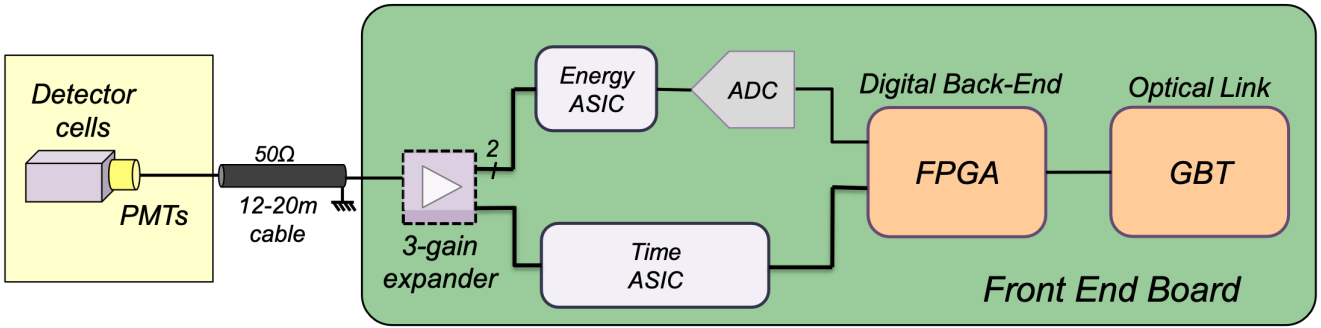
- The algorithm is promising to improve π^0 reconstruction efficiency

$*B^0 \rightarrow \pi^+\pi^-\pi^0$



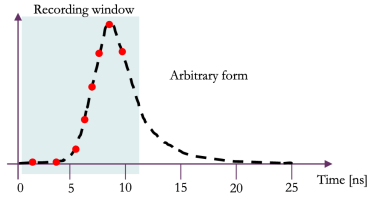
Electronics for PicoCal

- Architecture:

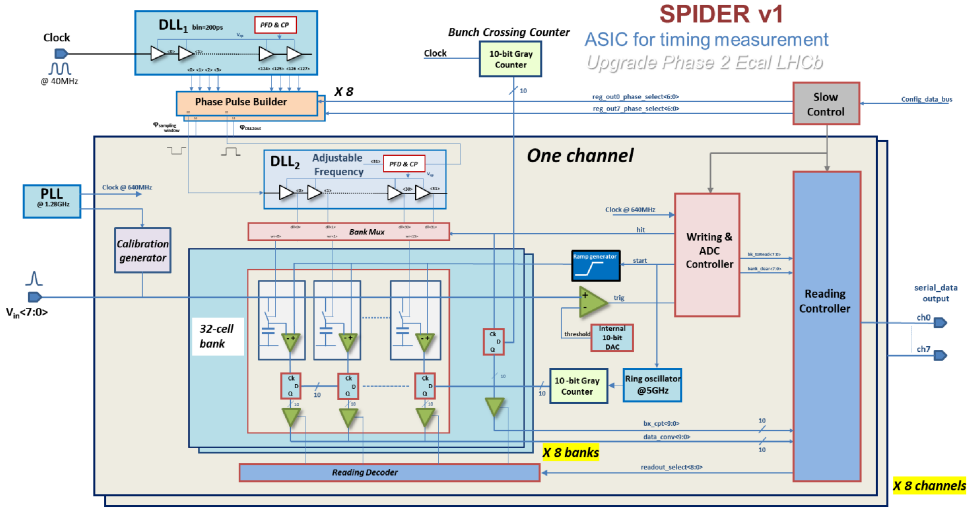


- Readout with PMTs
- Two separate paths with dedicated ASIC developed in parallel, with the same technologiy (TSMC 65 nm), running at 40 MHz:
  - **Time ASIC (SPIDER):** waveform TDC in analog memories (R&T IN2P3, Orsay/Clermont-Ferrand/Lyon/Caen/Nantes) (dynamic range of E_T = 50 MeV to 5 GeV, resolution 15ps RMS)
  - **Energy ASIC** (Barcelone, Valence), measurement of the integrated charge at 40 MHz over 12 bits with two gains (dynamic range between E_T = 0 and 40 GeV)

Mesure du temps: Waveform Digitizing



- Time measurement is done by sampling the signal shape using analog memories and a FPGA: development of a dedicated ASIC called SPIDER
- Time is computing using:
  - A counter (~1 ns step), **DLL2**
  - A DLL to define the region of interest (~100 ps step) **DLL1**
  - Samples on the signal shape: **Cell banks**
- The interpolation in a FPGA allows to measure the time with a precision of a few ps RMS with a precise calibration even with signals with small amplitudes.
- The main disadvantages that must be addressed in the new SPIDER chip:
  - Large deadtime (~ 100 µs) limiting usage at high rate (goal = 40 MHz) => ADC **massively parallel** to reach at least 50% occupancy
  - Need of a trigger: every channel is self triggered



Technologie: TSMC CMOS 65nm

- 10-bit Wilkinson ADC at 5 GHz
- Memory cells (switches/capacitors) with ~0.8V dynamic range and noise level ~0.5mV RMS
- DLL between 40 and 640 MHz

First prototype Automne 2024 (final version end 2029)

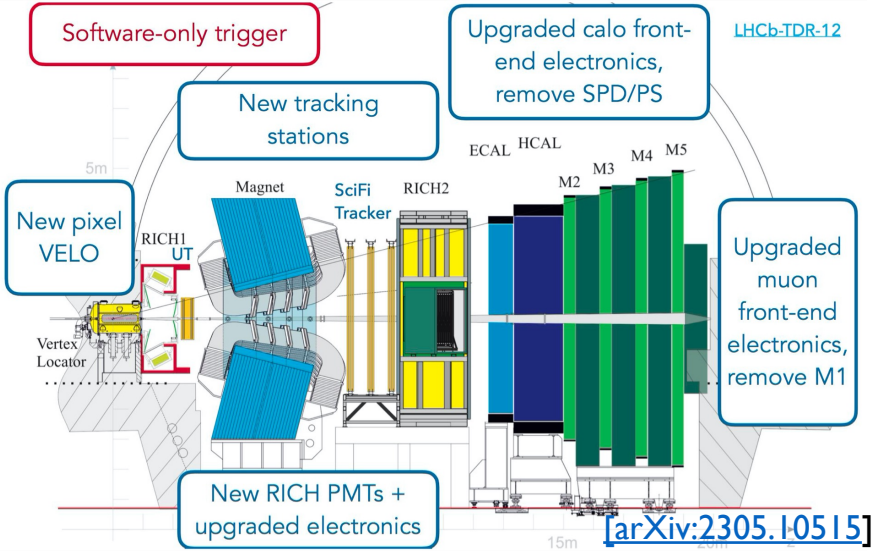
Conclusions

- Common activities in Chinese and French groups about LHCb ECAL Upgrade :
  - R&D for new modules with GAGG fibers
  - Performance studies with simulation
  - Design of ASIC to measure timing precisely
- In the near future:
  - Test beams at DESY and SPS to measure module characteristics
  - First prototype of electronics
- On the longer term:
  - Full production of innermost ECAL modules
  - Full production of Front-End electronics
  - Implementation of algorithms in FPGA to improve calorimeter reconstruction

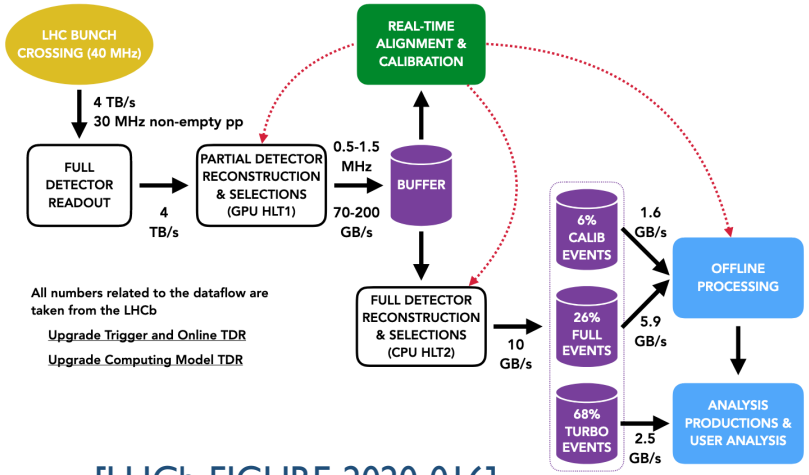
Backup

LHCb Upgrade I

- Un premier upgrade a été installé pendant LS2 (2018 – 2022) avec pour objectif principal de remplacer le trigger hardware par un système de lecture à 40 MHz (cartes PCIe40) et un trigger purement software.
- Remplacement des détecteurs de tracking également.



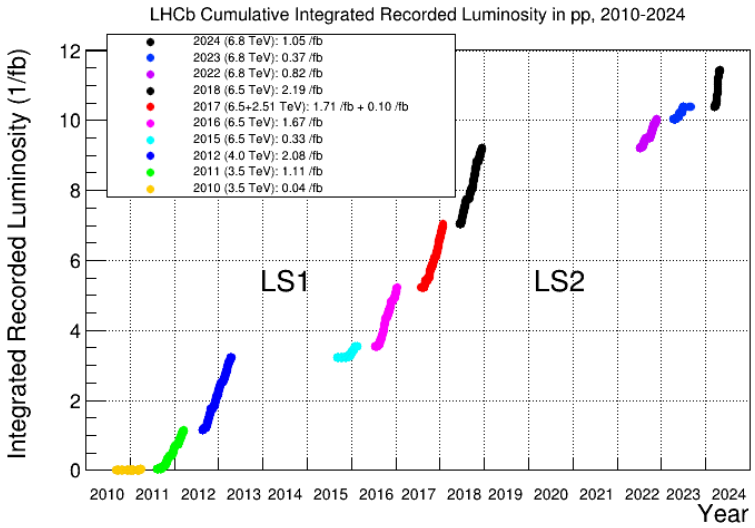
[arXiv:2305.10515]



[LHCb-FIGURE-2020-016]

LHCb Upgrade I: Status

- Installation et commissioning sans faisceau ont été perturbés par le COVID
- Début de la prise de données au début de 2022
- Un détecteur (UT) installé à la fin de 2022
- Incident du vide du LHC dans le VELO au début de 2023:
  - RF foil déformée: impossible de fermer complètement le VELO pendant 2023
  - Foil remplacée avec succès à la fin de 2023
- Instabilitées DAQ, liées à des problèmes dans le scrambling des données dans les GBT: mitigation en ajoutant des fake data bits
- 2024 est la première année aux conditions nominales: le but est d'atteindre la luminosité de design et opération avec le détecteur complet avant l'été: en bonne voie.

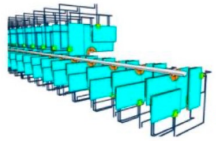


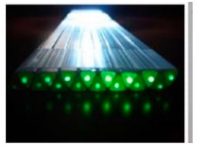
Détecteur pour Upgrade II

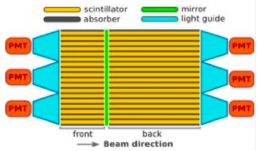
Vertex Locator (VELO):
Pixels 3D, 28nm
Timing 50ps
Nouvel RF-foil

Magnet Stations (MS):
Plaques de scintillateurs
Détection de traces à basse impulsion

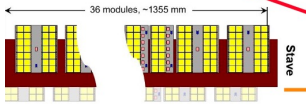
Picosecond ECAL (PicoCal):
Timing et segmentation
Intérieur: SpaCal
Extérieur: Shashlik

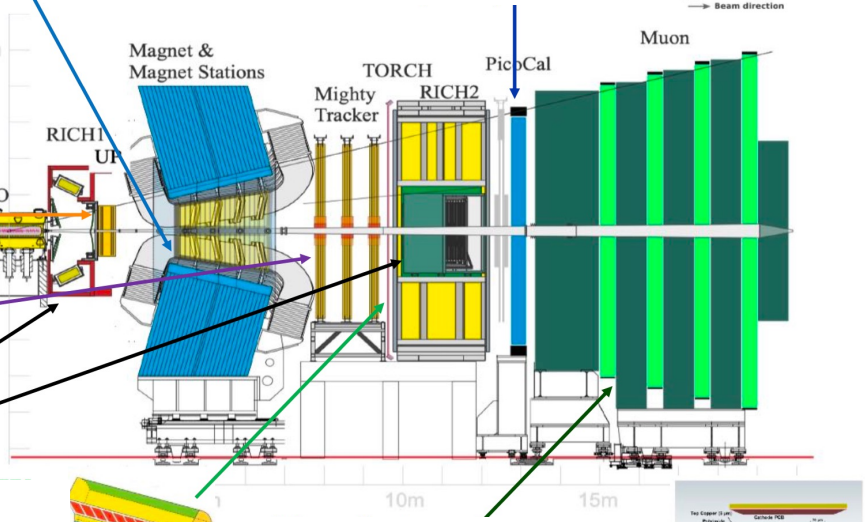




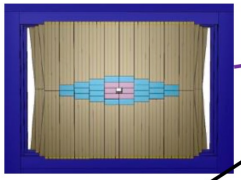


Upstream Tracker (UP):
Pixels CMOS MAPS
Résistant aux radiations

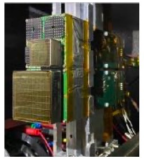




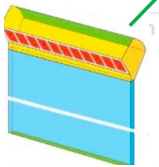
Mighty Tracker (MT):
Intérieur: pixels CMOS
Extérieur: Fibres Scintillantes (SciFi actuel)



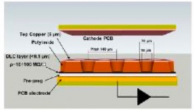
RICH1 & RICH2:
Petite taille de pixels
Mesure du temps
SiPM, MCPs



TORCH:
Time-of-flight
Plaques de quartz
SiPM, MCPs

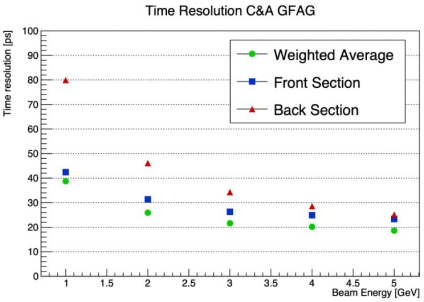


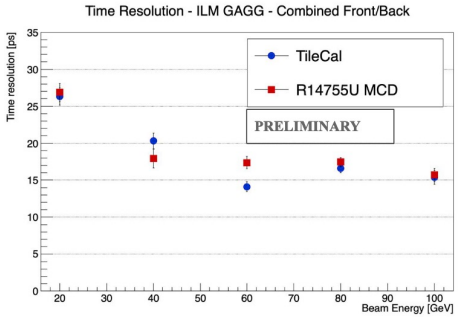
Muon System:
Intérieur: μ-Rwell
Extérieur: MWPC

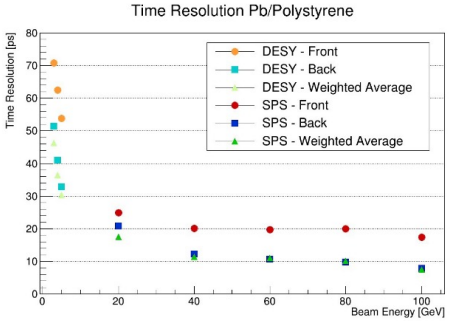


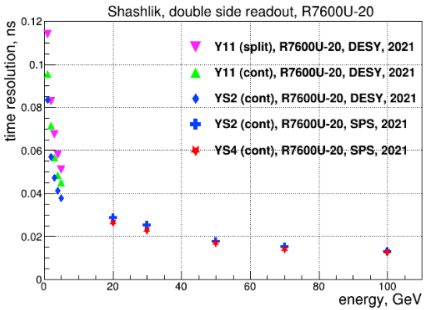
Test faisceau: résolution en temps

- Plusieurs campagnes, à **DESY** ($e^{\pm}$ 1 – 6 GeV) et au **CERN-SPS** (e^- 20 – 300 GeV)





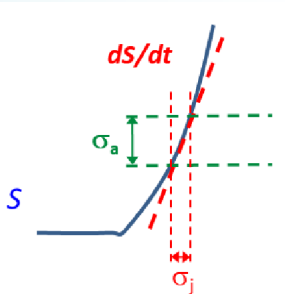




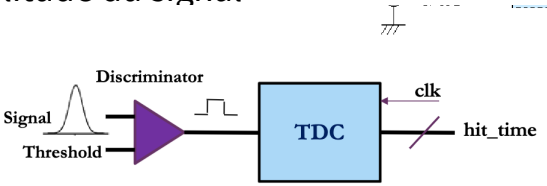
- Résolution en temps inférieure à 20 ps pour les grandes énergies
- DAQ avec 2 systèmes basés sur le “waveform sampling” dans des mémoires analogiques: **DRS4** et **WaveCatcher** (IJCLab – IRFU, Dominique Breton – Eric Delagnes)

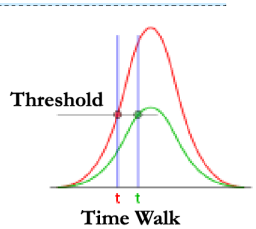
Mesure du temps

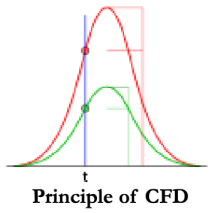
$$\delta_t = \frac{t_{rise\ time}}{SNR} = \frac{Noise}{Slope}$$

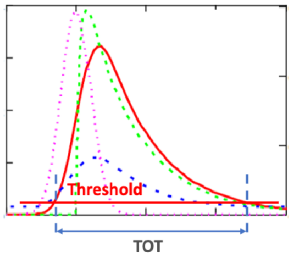


- Résolution théorique:
- Avec les candidats PMTs actuels, rise time de l'ordre de 1ns
- Système classique: TDC (Time to Digital Convertor)
  - doit être associé à un discriminateur, pour transformer le signal analogique en signal digital.
  - Cela introduit un jitter supplémentaire: "time walk", le moment de la conversion dépend de l'amplitude du signal





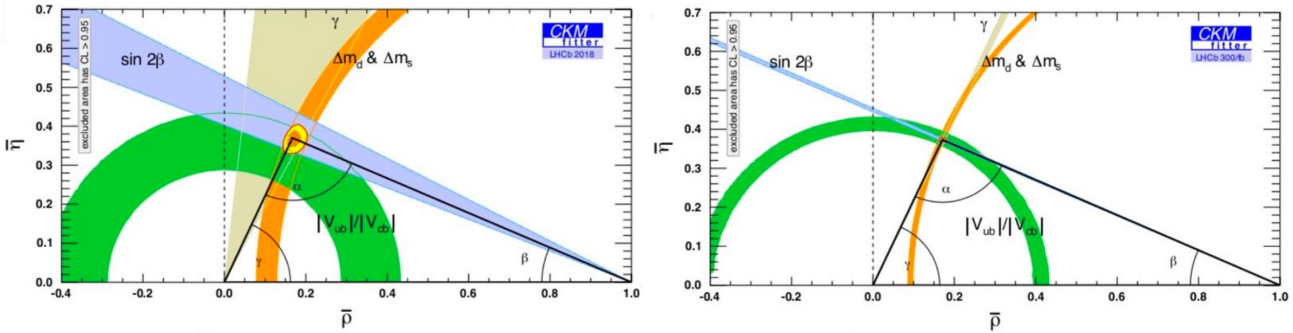




  - Cela peut-être compensé (en utilisant le TOT (Time over threshold)), mais avec une précision limitée, particulièrement avec des signaux asymétriques comme ceux des PMTs
- Le système TDC fonctionne bien avec de signaux bien au dessus du seuil dans une gamme dynamique restreinte, mais est peu adapté pour l'application dans PicoCal (grande gamme dynamique, mesure pour petits signaux près du seuil)

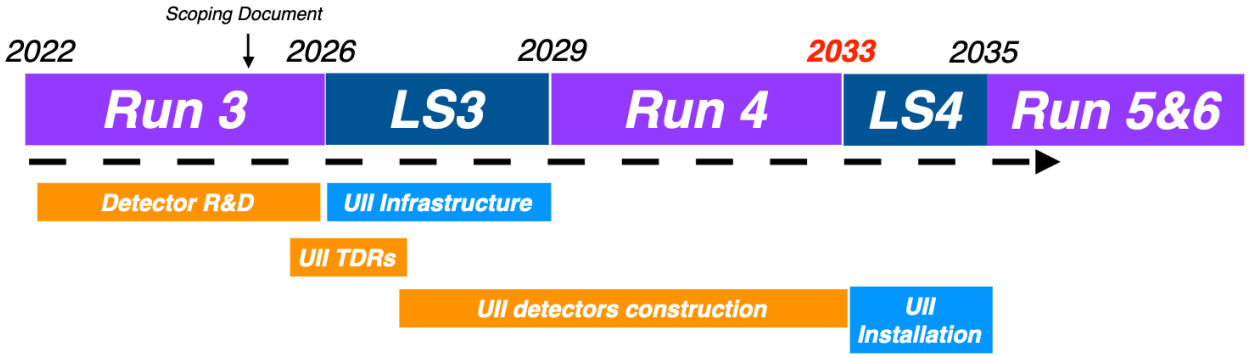
Programme de physique

- Physique des saveurs: recherche indirecte (sans produire directement les nouvelles particules) de nouvelle physique dans les désintégrations de *D* et *B*



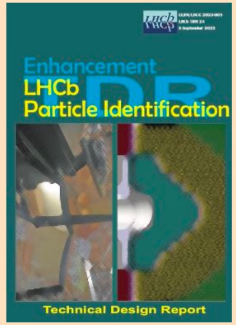
- LHCb a un programme de physique unique pour la découverte de la nouvelle physique:
  - Precision améliorée pour la physique du *B* et *D* (par exemple matrice CKM)
  - Avec aussi un programme de physique générique dans la region vers l'avant:
    - Spectroscopie, mesure de precisions physique electro-faible, physique du top et du boson de Higgs, matière noire, ions lourds, cible fixe
- Upgrade II = Exploitation maximale de la phase de haute luminosité du LHC: grande statistique, nouveaux détecteurs pour minimiser les erreurs systématiques et utiliser des techniques de reconstruction Nouvelles. Potentiellement la seule experience de physique des saveurs vers 2035

Planning



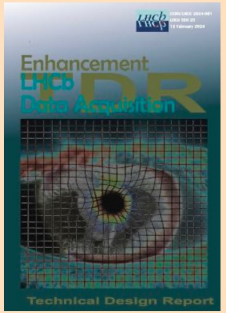
- Contraintes pour le planning de Upgrade II:
  - Tous les détecteurs doivent être prêts au début de LS4, en 2033
    - Démarrage de la construction pendant LS3
    - Première phase d'upgrade dès LS3: infrastructure, online, ECAL (amélioration granularité) et RICH (timing précis)
  - Durée de LS4 n'est que de 2 ans
  - Moins de 1 an de commissioning pour profiter au maximum des Runs 5 et 6:
    - Planification en avance de la phase de commissioning

PID Enhancement TDR



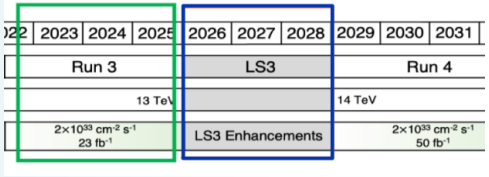
LHCC-2023-005
approved 03/2024

DAQ Enhancement TDR

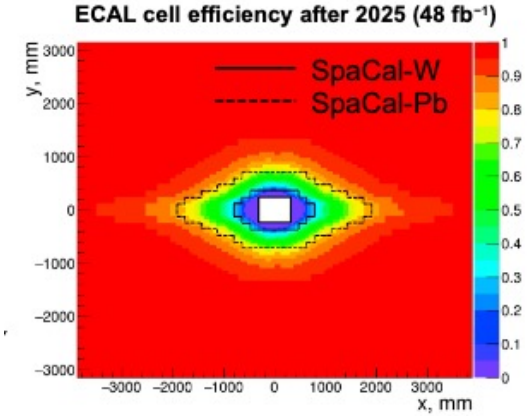


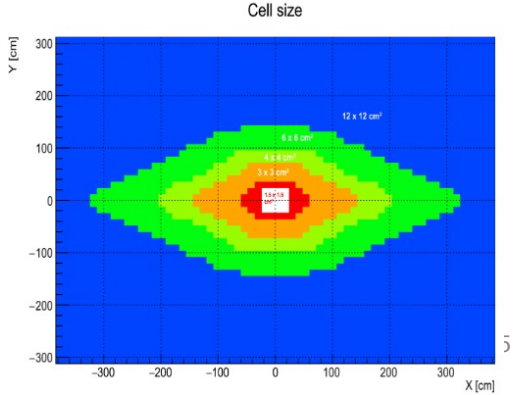
LHCC-2024-001
submitted 02/2024

LS3 Enhancements

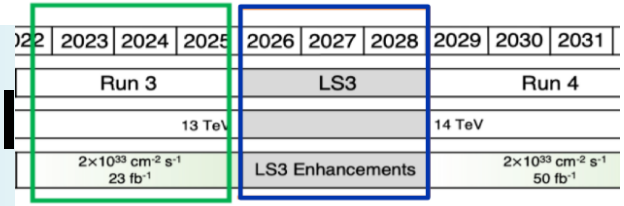


- At the end of Run 3, the inner-most modules of the ECAL will not function anymore due to radiation damages
- Since LS3 is long, replace these modules with new modules designed for Upgrade II and re-arrange the existing Sashlik modules in rhombic shape
- Configuration:
  - 2x2 cm^2: 32 modules (new SpaCal-W and polystyrene fibers) – 1152 cells
  - 3x3 cm^2: 144 modules (new SpaCal-Pb) – 2304 cells
  - 4x4 cm^2: 176 modules (existing Shashlik) – 1584 cells
  - 6x6 cm^2: 448 modules (existing Shashlik) – 1792 cells
  - 12x12 cm^2: 2512 modules (existing Shashlik) – 2512 cells
- No longitudinal segmentation: **9344** cells (vs. 6046 now)
- Since Run 4 conditions are the same as Run 3, no need of new electronics (no timing): reproduce the same electronics than the one developped for the Run 3 (Orsay, Barcelona)
- **September 2023**: TDR for LHCC submitted « LHCb Particle Identification Enhancement Technical Design Report », LHCC-2023-005
- RICH detectors have also plans to advance detector installation (Electronics with precise timing)

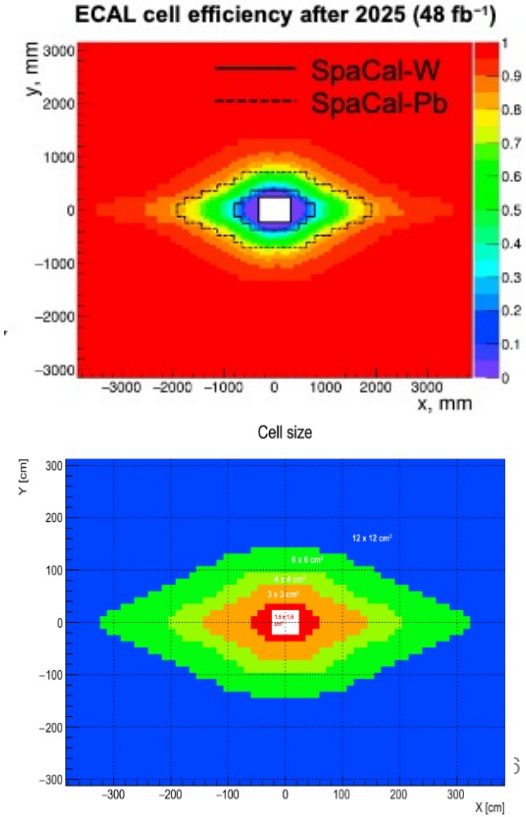




LS3 Consolidation: Upgrade I



- At the end of Run 3, the inner-most modules of the ECAL will not function anymore due to radiation damages
- Since LS3 is long, replace these modules with new modules designed for Upgrade II and re-arrange the existing Sashlik modules in rhombic shape
- Configuration:
  - 2x2 cm^2: 32 modules (new SpaCal-W and polystyrene fibers) – 1152 cells
  - 3x3 cm^2: 144 modules (new SpaCal-Pb) – 2304 cells
  - 4x4 cm^2: 176 modules (existing Shashlik) – 1584 cells
  - 6x6 cm^2: 448 modules (existing Shashlik) – 1792 cells
  - 12x12 cm^2: 2512 modules (existing Shashlik) – 2512 cells
- No longitudinal segmentation: **9344** cells (vs. 6046 now)
- Since Run 4 conditions are the same as Run 3, no need of timing, but this is the ideal test bench to install the Front-End electronics with timing capabilities foreseen for Upgrade II in the new modules and that we plan to design and build in Orsay
- **April/May 2023**: Internal review to approve this plan
- **September 2023**: Light-weight TDR for LHCC



Scheduling

Summary of proposed schedule:

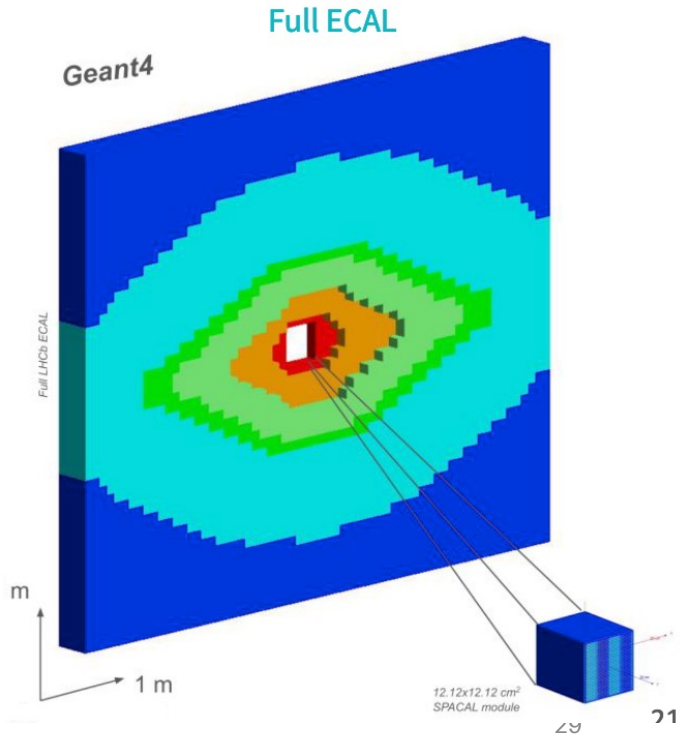
- ✓ April/May 2023: Light-weight internal U2PG review to approve ECAL LS3 consolidation (internal to LHCb Collaboration)
- ✓ September 2023: Light-weight PID TDR to LHCC for LS3 consolidation (ECAL & RICH)
- ✓ 2024: Scoping Document for LHCb Upgrade phase IIb (including ECAL)
- ✓ 2025-2027: production of 176 SPACAL modules, 3'500 new electronics channels and PCIe400
- ✓ 2026-2028: infrastructure modification (platform) and ECAL re-built (new modules, rhombic shape)
- ✓ 2026: TDR for ECAL Upgrade phase IIb in LS4
- ✓ 2028-2032: production/refurbishing shashlik modules, production of GAGG-SPACAL, introducing double sided R/O
- ✓ 2033-2034: ECAL re-built by adding new modules during LS4

ECAL upgrade 2: PicoCal

- Un des détecteurs d'intérêt pour les groupes français dans LHCb: Calorimètre électromagnétique (PicoCal):
  - Electronique: LPC Clermont-Ferrand, IJCLab Orsay, LAPP Annecy
  - Mécanique: LAPP Annecy
- Pour Upgrade 2:
  - Augmenter la granularité: nouvelle structure mécanique
  - Ajouter la mesure du temps dans les cellules: nouvelle électronique de Front-End et ASIC dédié (SPIDER: « **S**wift **PI**pelined **D**igitiz**ER** »

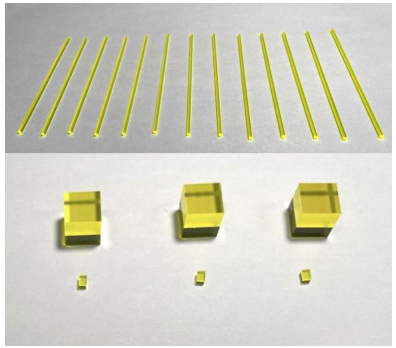
Upgrade II: ECAL Granularity

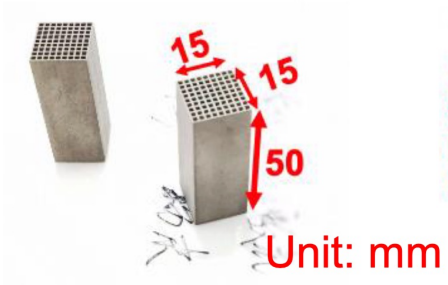
- Efficient way to increase performances at high luminosity
- Reorganize ECAL areas with a rhomboid shape to follow better the radation doses and then the cell occupancies.
- Five different areas of different sizes: (1 module = a 12x12 cm^2 bloc)
  - 1.5x1.5 cm^2: 32 modules (type SpaCal-W) – 2048 cellules
  - 3x3 cm^2: 144 modules (type SpaCal-Pb) – 2304 cellules
  - 4x4 cm^2: 448 modules (type Shashlik) – 4032 cellules
  - 6x6 cm^2: 1344 modules (type Shashlik) – 5376 cellules
  - 12x12 cm^2: 1344 modules (type Shashlik) – 1344 cellules
- Add also longitudinal position at shower maximum of the electromagnetic shower (improve time measurement and help for particle identification: electron/hadron separation)
- One cell = 2 readout channels (1 front and 1 back)
  - Total of **30208 channels**

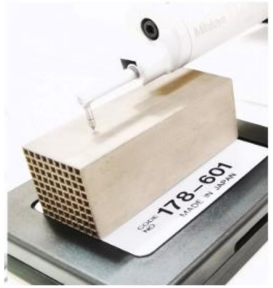


R&D activities in Beijing

- Fast and resistant scintillator for the inner W SPACAL modules: Cerium-doped multi-component Gadolinium Gallium Aluminium Garnet $Gd_3Al_2Ga_3O_{12}$ (GAGG:Ce), developed with SIPAT company
- Characterised in laboratory in Peking University
- W absorber for inner modules: obtained by 3-D printing by LaserAdd company in China or EOS company in Germany
- Characterised in laboratory in Peking University (roughness, …)
- Aim to produce a test module (W + GAGG fibers) for test beams in 2024
- And then full production



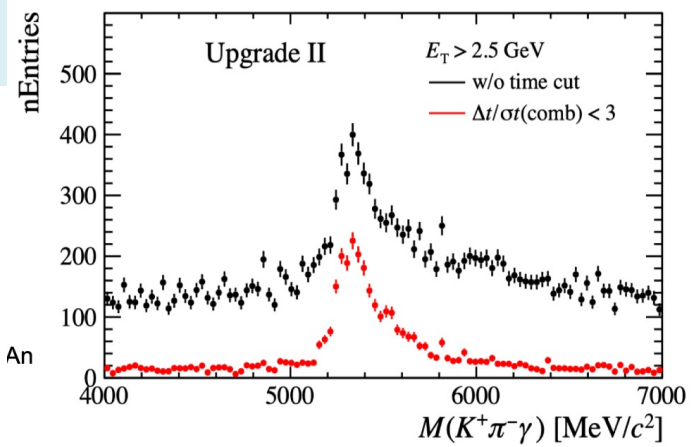




Precise time measurement

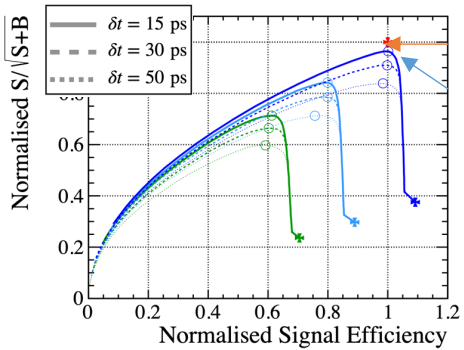
- To fight against the large background from pile-up interactions: add time mesurement in the ECAL with a precision of 15 ps = PicoCal
- Select cells where $|t_{ECAL}-t_{PV}|/\sigma(t)<3$
  - t_{PV} : time of the collision measured by other detectors (VELO for example)
  - t_{ECAL} : time measured in the ECAL, corrected from time of flight
  - $\sigma(t)$: ECAL time resolution

Effect of timing cut on invariant mass for B→ K*γ



An

Full simulation of signal $B^0 \to K^{*0}\,\gamma$ with pile-up

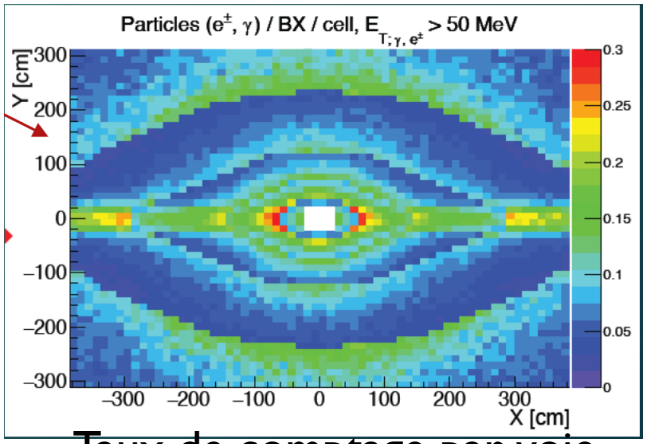


Run 2

Run 5 (15 ps)

Mesure du temps: contexte

- Resolution visée: 15 ps RMS
- Sur une gamme dynamique élevée: entre E_T = 50 MeV et 5 GeV (facteur 100)
- Avec un taux de comptage de 10% (à 40 MHz) initialement



Taux de comptage par voie

SPIDER: Status

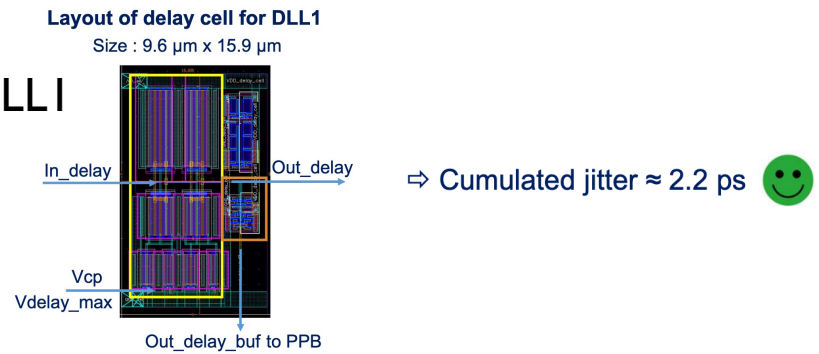
- Développement depuis 1 an en collaboration entre 4 labos in2p3 (Orsay, Clermont-Ferrand, Caen, Lyon) coordonné par Samuel Manen (LPC) et Philippe Vallerand (IJCLab)
- Travail réparti en packages:
  - 1 : Architecture
  - 2 : Delay Locked Loop (DLL1 & DLL2)
  - 3 : Partie analogique (cellule mémoire, comparateur pour le déclenchement, comparateur ADC, générateur de rampe) + Échantillonage et ADC (séquance de conversion, controller des banques)
  - 4 : Partie digitale pour ADC Wilkinson 10bit
  - 5 : Slow control et readout
  - 6 : Phase Locked Loop (non critique pour le premier prototype)

WP2: DLLs

- Design de 2 DLLs pour SPIDER: avec contraintes sur consommation et jitter
  - Si $jitter_{DLL}$ < 2.5 ps sur chaque DLL, la degradation du jitter total est de ~1ps

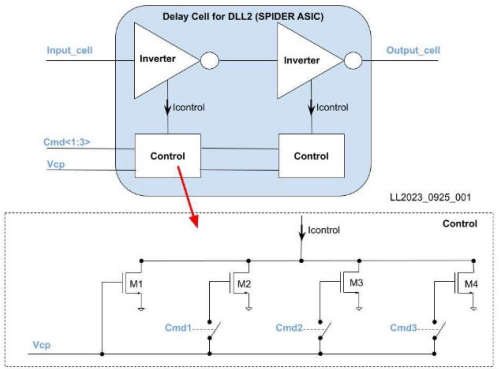
	DLL1	DLL2
Locking frequency	40 MHz Equal to the input frequency	Variable : 80 MHz to 640 MHz Multiple of the 40 MHz
Number of outputs	128	32
Bin ΔTdelay	~ 200 ps (195.3ps)	~ 50 ps (48.8 ps) to 400 ps (390.6 ps)
Power consumption	As low as possible	
Jitter	< 2.5 ps	

DLL1



⇨ Cumulated jitter ≈ 2.2 ps

DLL2

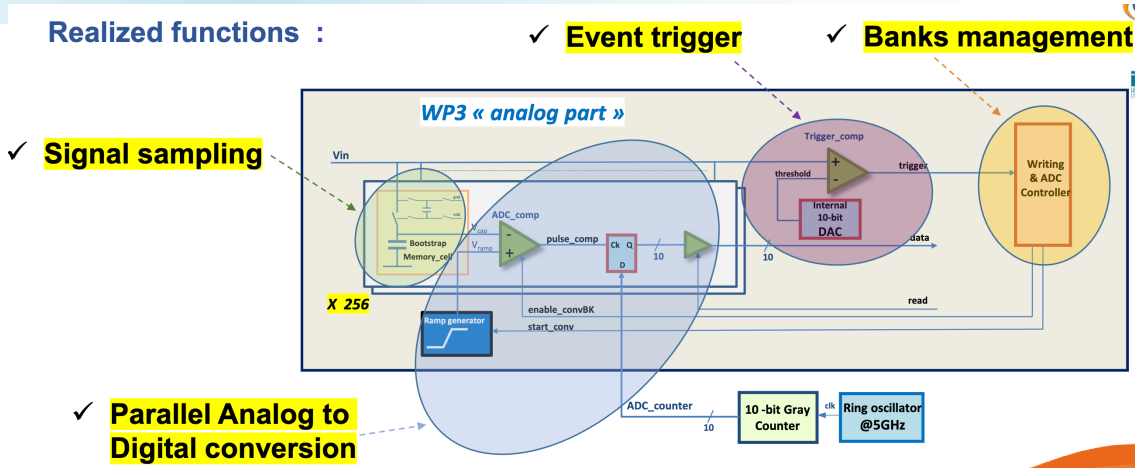


En cours de finalisation

Ludovic Alvado, Laurent Leterrier (LPC Caen)

WP3: Partie Analogique

- Fonctions réalisées
- Simulation de la chaine complete en cours



	designers							status					main specifications			
	Nicolas Arveuf	Dominique Breton	Baptiste Joly	Samuel Manen	Christophe Sylvia	Philippe Vallerand	Richard Vandaele	1st schematic (or HDL)	schema optimisation	1st layout	layout optimisation	system simulation	dynamic range	INL max	power	other
memory cell			■	■			■	■	■	■	■	■	0-1V	<1%	<25µW	bandwidth, noise
ramp generator					■	■	■	■	■				0-0.9V	<1%		slope fine tuning, noise, time to reset
ADC comparator				■		■	■	■	■				0-0.8V	<1%*	<25µW	noise, fast enable/disable, *resp time uniformity
trigger comparator		■						■	■	■			0-0.85V			sensitivity, speed
writing & ADC controller	■					■	■	■	■							robust handling of all cases, synchronous logic
DAC				■		■	■	■	■				0-0.8V	few 0.1%		10 bit resolution, noise

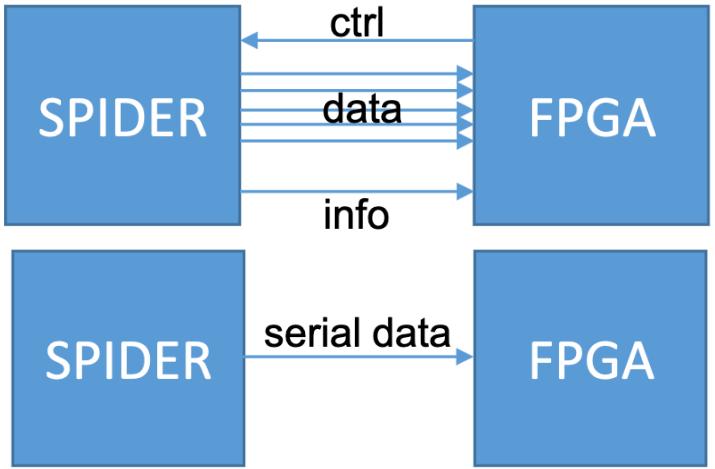
Baptiste Joly (LPC Clermont), Philippe Vallerand (IJCLab Orsay)

WP4: Partie digitale

- 3 modules: Time Stamp Gray counter, Fast gray counter (ADC Wilkinson), Ring oscillator
- Status:
  - 10b Time Stamp Gray counter : Simulated & PnR done using digital flow
  - Ring Oscillator 5GHz : Almost Simulated & PnR done using analog flow
  - 10b Fast Gray counter Simulated & PnR done using analog flow
  - RO + Fast Gray counter simulated together and working
- TODO : Use a gray buffer tree with low skew to feed all FF in memory cell (256 cells) analog vs digital flow in discussion …

WP5: Slow control et lecture

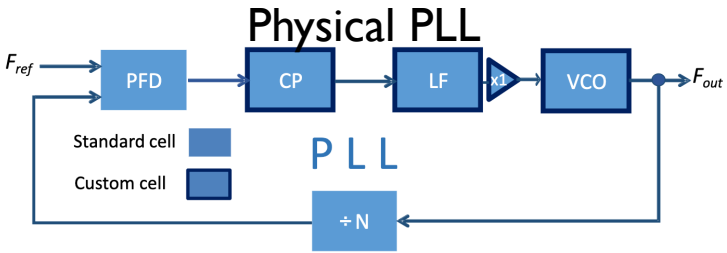
- 3 modules: Controlleur de lecteur central, controleur de lecteur par voie et slow control (i2c)
- Pour le prototype: implementation simple avec bus paralleles
- Pour la version finale: implementation plus complexe avec serialisation



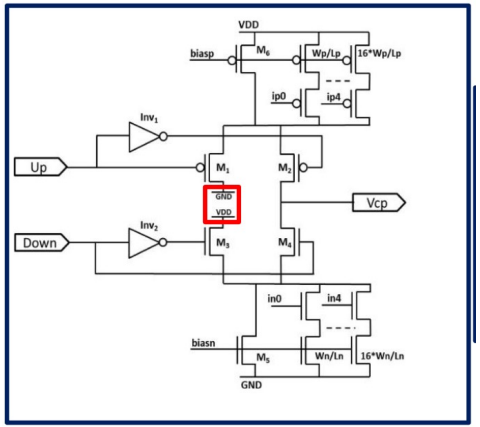
Done	TODO
Channel read controller Simulated & PnR with digital flow	
Central read controller Simulated & PnR with digital flow	
	Finalize requirements for Slow control
	Get complete register list
	Finalize Reset strategy
	Do synthesis & PnR
SC main scripts flow	
Some working simulation for SC	

WP6: PLL

- Design base sur 2 R&T precedentes : Lojic130 et FASTIME
- Résultats pour le projet SPIDER:
  - migration de technologie 130nm à 65nm
  - Fréquence d'entrée: 40 MHz, fréquence de sortie: 2.56 GHz, jitter absolu amélioré à 0.5ps RMS, locking time < 2µs
  - Horloge utilisée pour la calibration et les machines d'états
- Prochaines étapes:
  - Layout, et post-layout simulation
  - SLVS transmitter/receiver (transition ongoing from 130 nm process)



CP

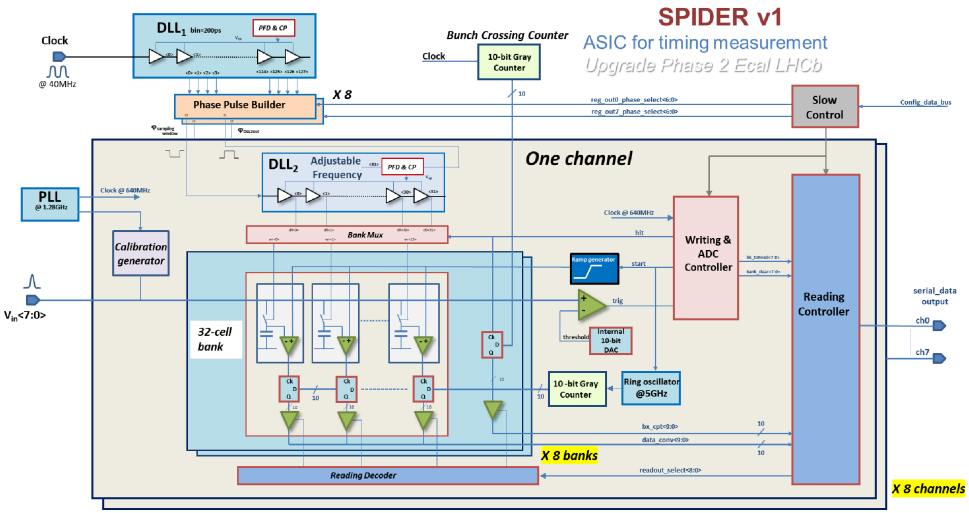


SPIDER: Calendrier

- Objectif: LS4 (2033), 30000 channels
  - 2023: Design SPIDER V0 (2 voies + validation de la technologie)
  - 2024: Characterisation de SPIDER V0 et design SPIDER V1 (2 voies)
  - 2025: Characterisation de SPIDER V1 et design SPIDER V2 (multi-voies + tolérence aux radiations)
  - 2026: Characterisation de SPIDER V2 et design SPIDER V3 (multi-voies + tolérance aux radiations + optimisation)
  - 2027: Characterisation de SPIDER V3 et design SPIDER V4 (multi-voies + tolérance aux radiations + optimisation + yield)
  - 2028: Characterisation de SPIDER V4 et design pre-production
  - 2029: Characterization of SPIDER pre-production
  - 2030: Production de SPIDER

SPIDER: Architecture

- Chaque voie est “self-triggering”, avec des discriminateurs individuels
- 8 banques par voie, qui peuvent être déclanchées sur des Bunch Crossings consécutifs: derandomizer analogique
  - La fenêtre d’échantillonage est calée sur le temps de vol des particules par rapport au point d’interaction
- La conversion Analogue-Digitale est massivement parallèle, pour pouvoir convertir toutes les banques qui ont déjà “triggé”
  - Cela permet d’augmenter le taux d’occupation acceptable (jusqu’à 50% au niveau ADC)
  - Le point de blocage devient la lecture et la capacite en sortie d’envoi des données (jusqu’à 2Gbit/s/voie)

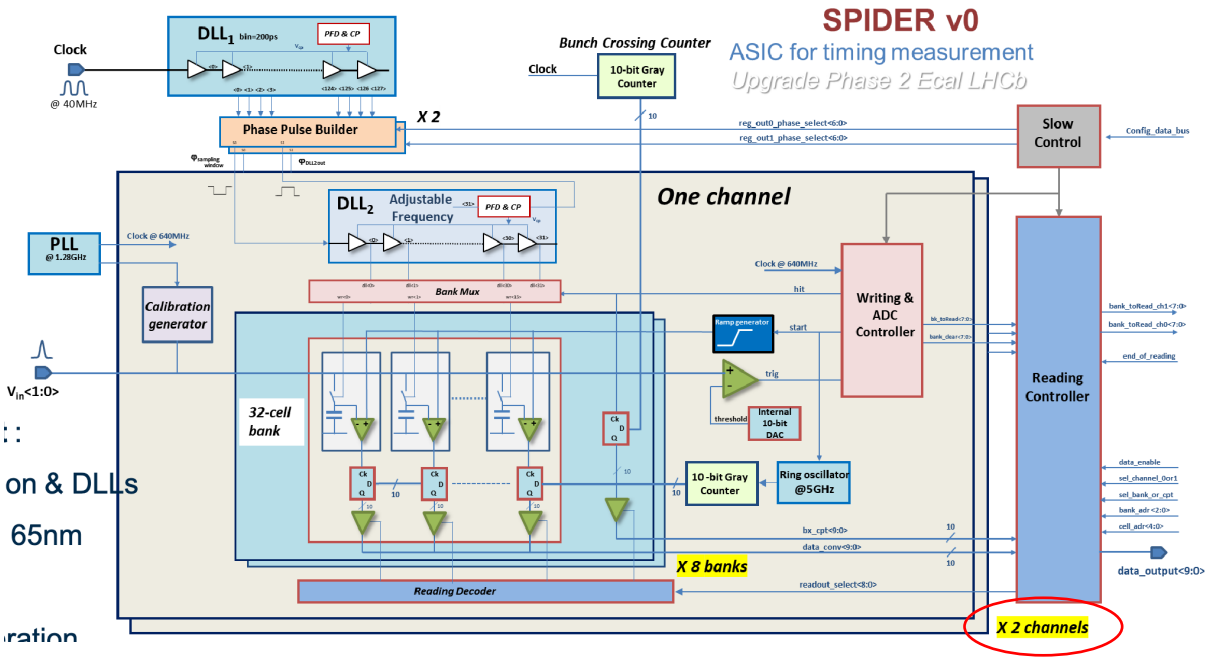


SPIDER: Characteristiques

- Technologie: TSMC CMOS 65nm (diponible pour au mons 10 ans), mais seulement 1.2 V pour l'alimentation
  - Difficile pour la partie analogique (utilisation de transistors à 2.5 V envisagée mais pas pour la baseline)
- Signal d'entrée: rise time 1 – 1.5ns, gamme dynamique: 8mV – 0.8 V dans LHCb
  - Mais bande passante de quelques GHz pour utilisation avec des détecteurs plus rapides.
- Pour des resolutions mieux que 15 ps RMS sur la grande dynamique:
  - Une cellule de mémoire (switches/capacitors) avec ~0.8V de gamme dynamique et un niveau de bruit ~0.5mV RMS
  - Une resolution de 10 bits pour la conversion: 10-bit Wilkinson ADC à 5 GHz pour réduire le temps de conversion
  - Une DLL1 (128 cellules) @40 MHz, pour fournir un bin de 200ps pour définir le début de la zone d'échantillonage
  - Une DLL2 (32 cellules) @80 – 640 MHz, bin de 50ps à 400ps pour définir la fréquence d'échantillonage entre 2.5 GS/s et 20 GS/s

SPIDER: Premier prototype

- Contient tous les blocs critiques:
  - Distribution d'horloge et DLL
  - Cellules de mémoires en 65nm
  - "Self-triggering"
  - Utilisation de plusieures banques
  - 10-bit ADC Wilkinson @5GHz
  - PLLs
- Production au début 2024 et tests dans la foulée



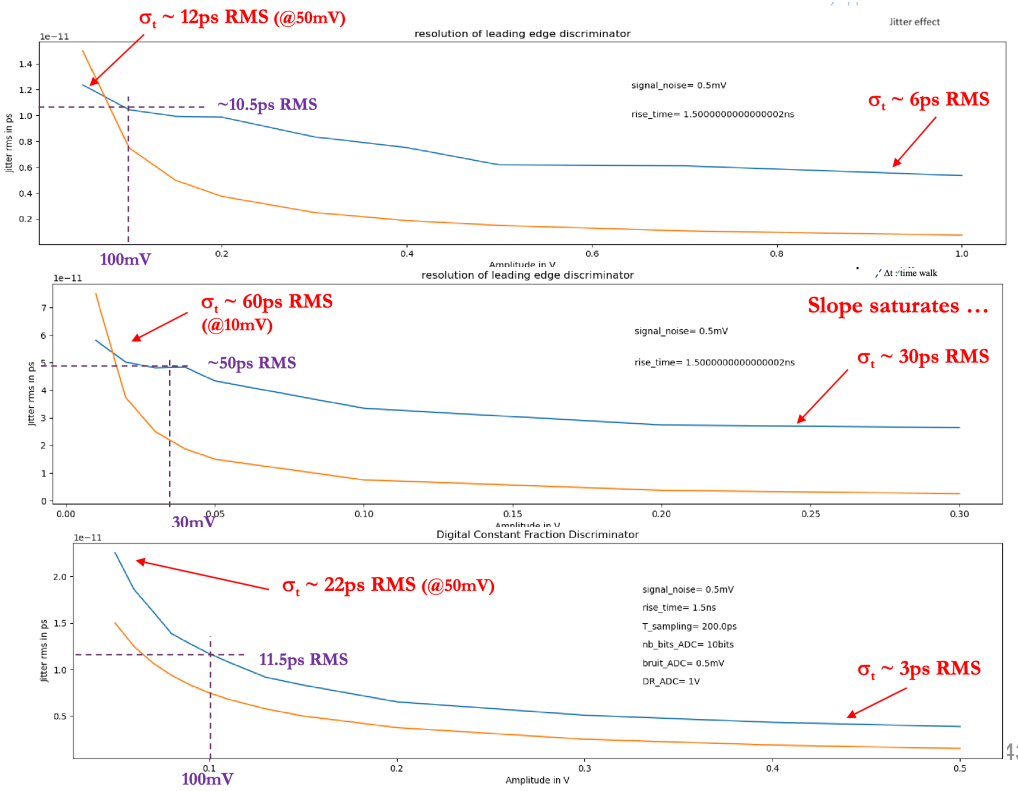
Simulations

- Simulation du jitter sur le timing en function de l'amplitude du signal en utilisant un signal typique d'un module du ECAL lu par un PMT: rise time = 1.5ns, σ_{noise} = 0.5mV RMS (Philippe Vallerand, IJCLab Orsay)

Discriminateur avec gamme dynamique de 1:20 (Vin de 50mV a 1V, seuil à 25mV)

Discriminateur avec gamme dynamique de 1:100 (Vin de 10mV a 1V, seuil à 5mV)

Digital CFD basé sur la forme du signal avec gamme dynamique de 1:100 (Vin de 10mV a 1V)



SPIDER

- L'utilisation discriminateur + TDC est bien adaptée pour des gammes dynamiques pas trop élevées mais pas pour le cas du ECAL de LHCb
- Developpement d'un ASIC implémentant digitisation de la forme du signal dans des mémoires analogiques: SPIDER:
  - Jitter visible dans la region des basses énergies (où aussi les modules ont des performances dégradées), mais contribution négligeable à haute énergie
  - Calibration simple, générée de façon interne
  - L'algorithme d'extraction du temps peut etre modifié pour suivre la degradation du signal avec les radiations
  - Challenging mais solution robuste adaptée
- Idée principale: enregistrer le signal dans une fenetre en temps qui est une fraction de la periode de l'horloge et selectionner 8 echantillons qui sera utilise pour la mesure de temps via CFD
  - Cela limite le temps de lecture des memoires analogiques (40ns/evt @ 200 MHz/echantillon)
  - Extraction du temps dans un FPGA