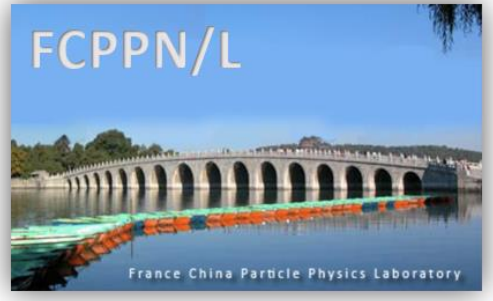
环形正负电子对撞机
Circular Electron Positron Collider



CEPC electronics and TDAQ

Wei Wei

On behalf of the CEPC electronics-TDAQ group

IHEP, CAS

2024-06-10

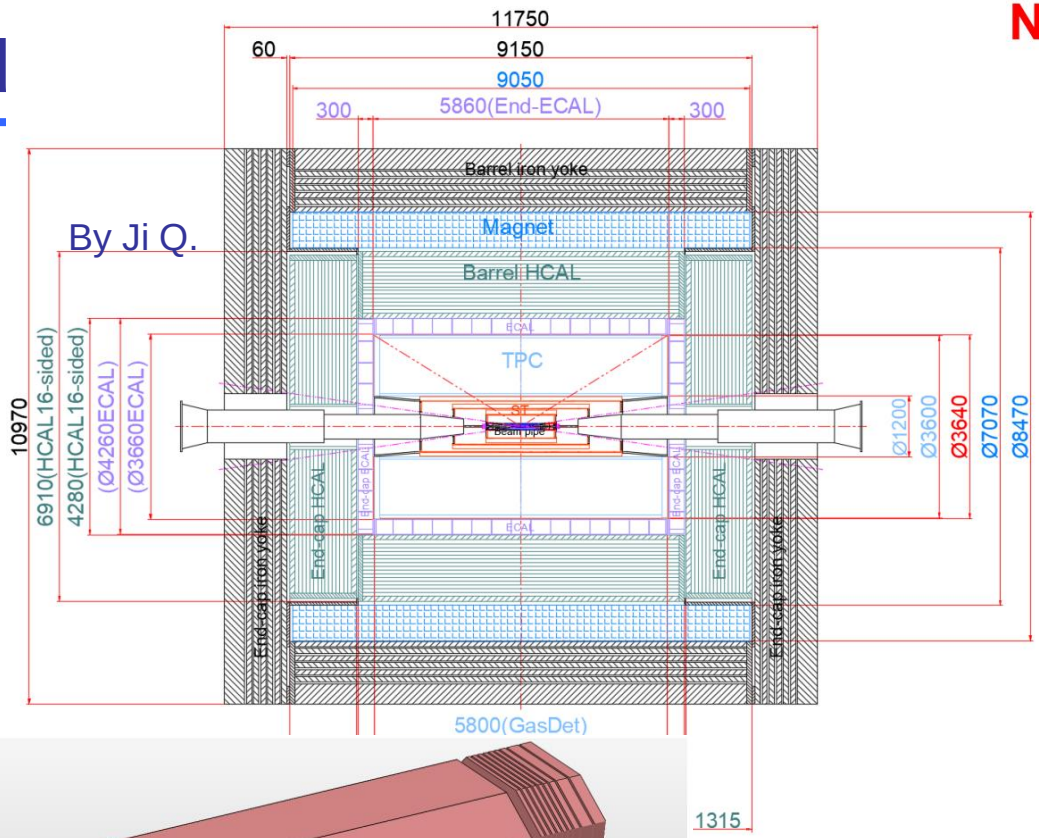
15th FCPPN/L Workshop, Bordeaux, France

Outline

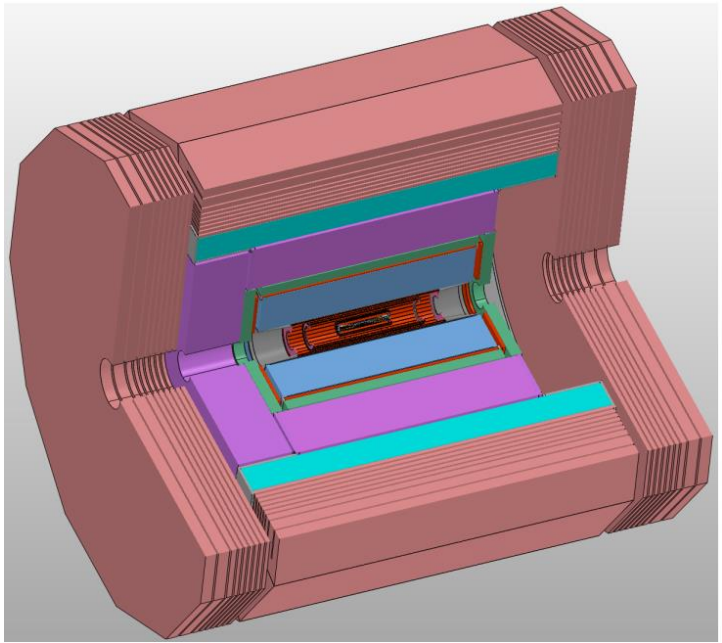
- **Detector background**
- **Requirements from the CEPC detectors**
- **The current CEPC electronics-TDAQ designs**
  - The detector frontend electronics (FEE)
  - The common projects
  - The Backend Electronics (BEE) and the interface to TDAQ -- to be coming
- **Summary and the to-do list**

Detector Background

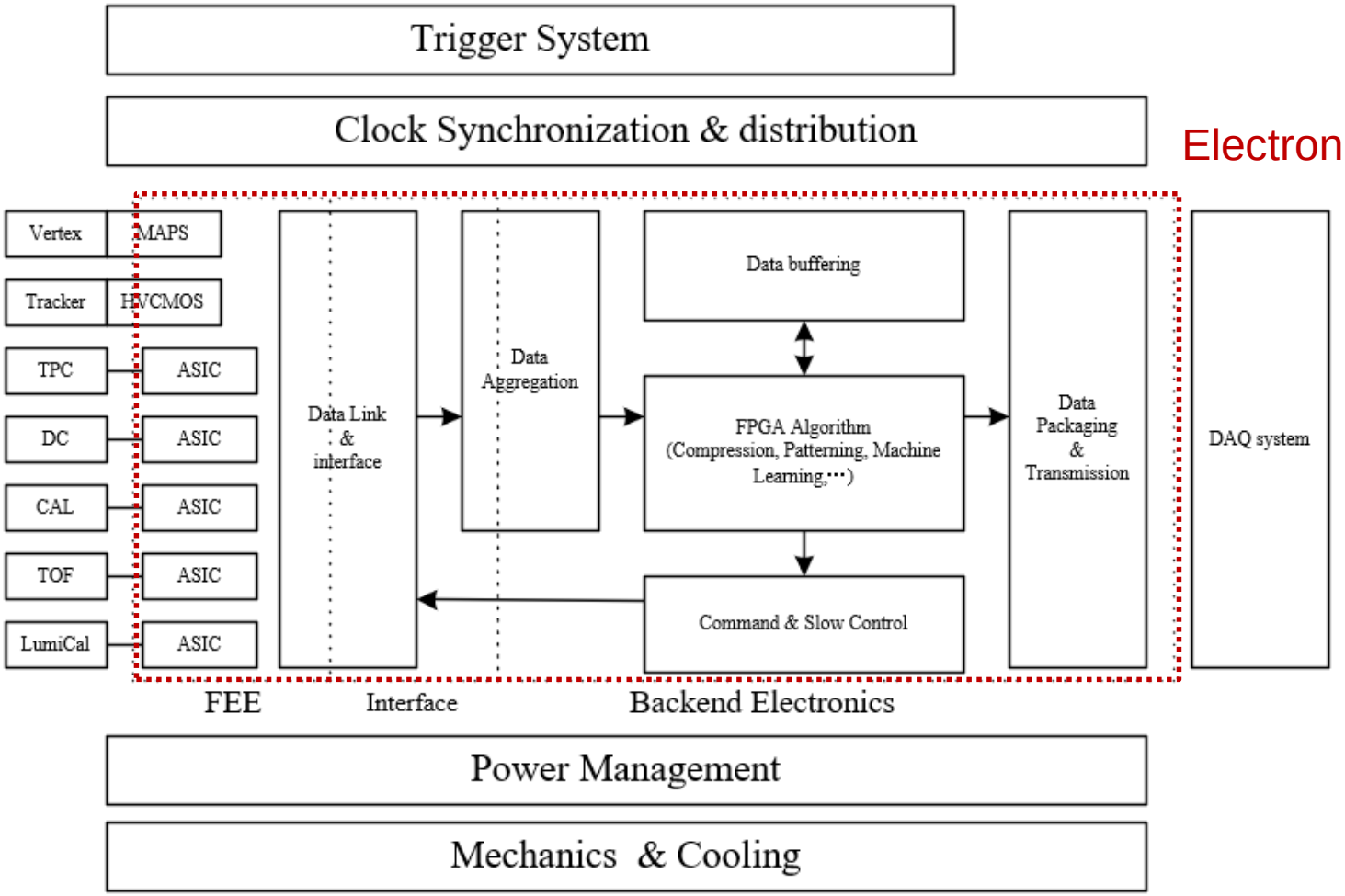
- **Tracker**
  - Vertex (CMOS Sensor)
  - Inner Tracker (ITk): Si Pixel Tracker (HVCMOS)
  - Middle Tracker (MTk) : TPC / Drift Chamber
  - Outer Tracker(OTk): Si Strip / LGAD-TOF / Pixel (HVCMOS)
- **ECAL & HCAL**
  - Crystal bar / Stereo crystal / Plastic scintillator / SiW / Glass / RPC …
- **Muon**
  - Plastic scintillator / RPC
- **Electronics**
  - Detector front-end electronic: FEE
  - Off detector: BEE
  - Trigger and DAQ: TDAQ



By Ji Q.



Electronics-TDAQ overall framework



- **Two main recent targets:**
  1. **To collect the detailed requirements from all sub-dets**
  2. **To define the preliminary readout frame & strategy of Elec-TDAQ**

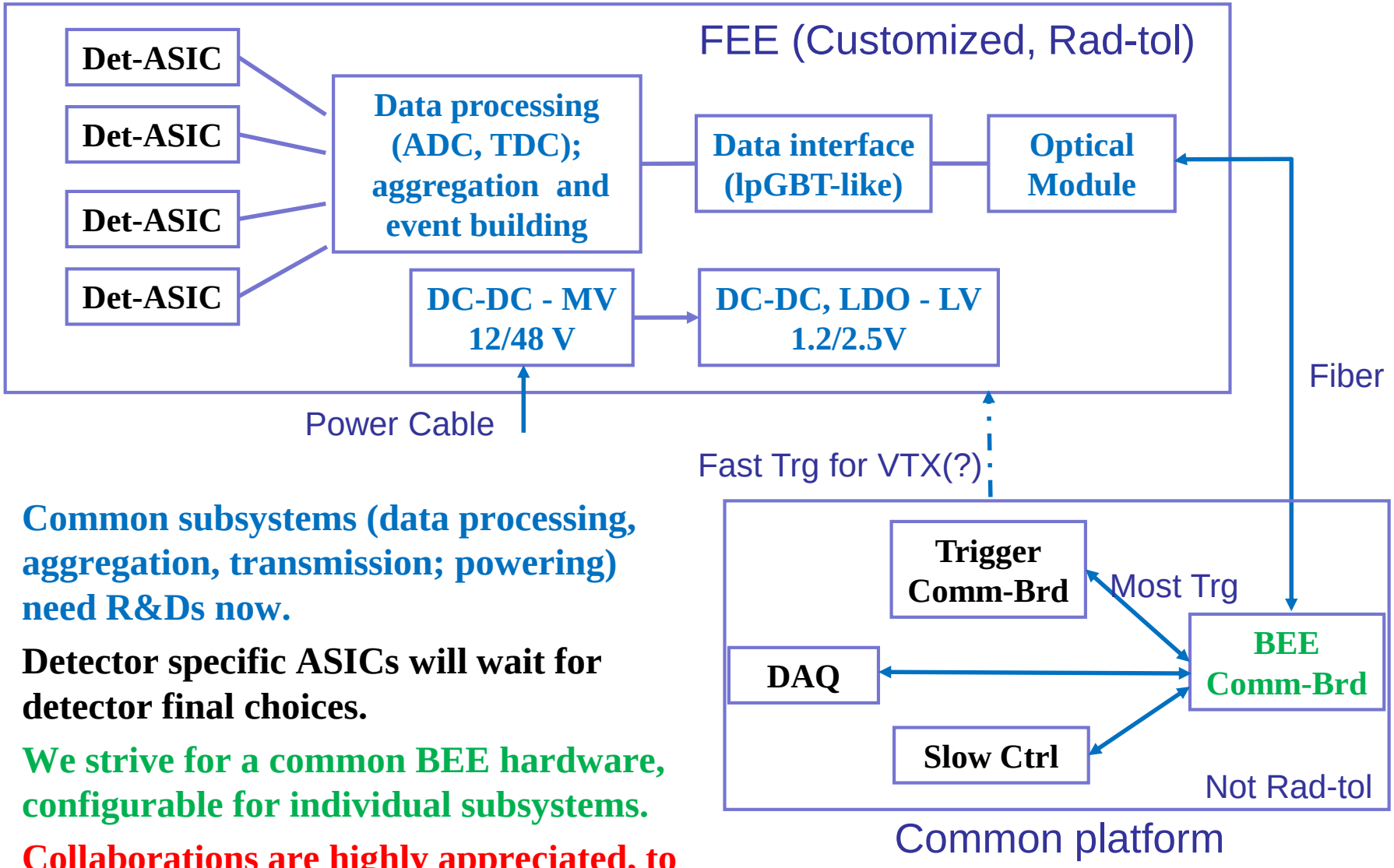
Requirements from detector subsystems

	Vertex	Pix Tracker	TOF	Si Strip	TPC	DC	CAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT
Channels per chip	500k Pixelized	50k Pixelized	128	128	128	-	16
Ref. Signal processing	XY addr + BX ID	XY addr + timing	ADC + TDC / TOT+TOA	Discri.	ADC + BX ID	Ultra fast PA + ADC	TOT + TOA/ ADC + TDC
Main challenge for FEE	• Small pixel size • Fast readout • Low power	• Large area • Cost effective • Low power	• ~50ps timing		• Low power • High density integration	• Ultra fast PA • Ultra fast ADC	• ~10^5 dynamic range • ~400ps timing • Huge channel Low power
Data rate for FEE	160Mbps/chip @Trigger Innermost	~30Mbps/chip Innermost	<kHz/chip	<kHz/chip	~70Mbps/module Innermost	~500Mbps/module /a sector	<100MHz/module

- **We are still working on the data rate between the FEE and the BEE, especially for the endcaps.**
- **We aim for a data-stream mode (FEE triggerless) for all subsystems.**
- **We are preparing a review by experts in our field about the electronics and TDAQ.**

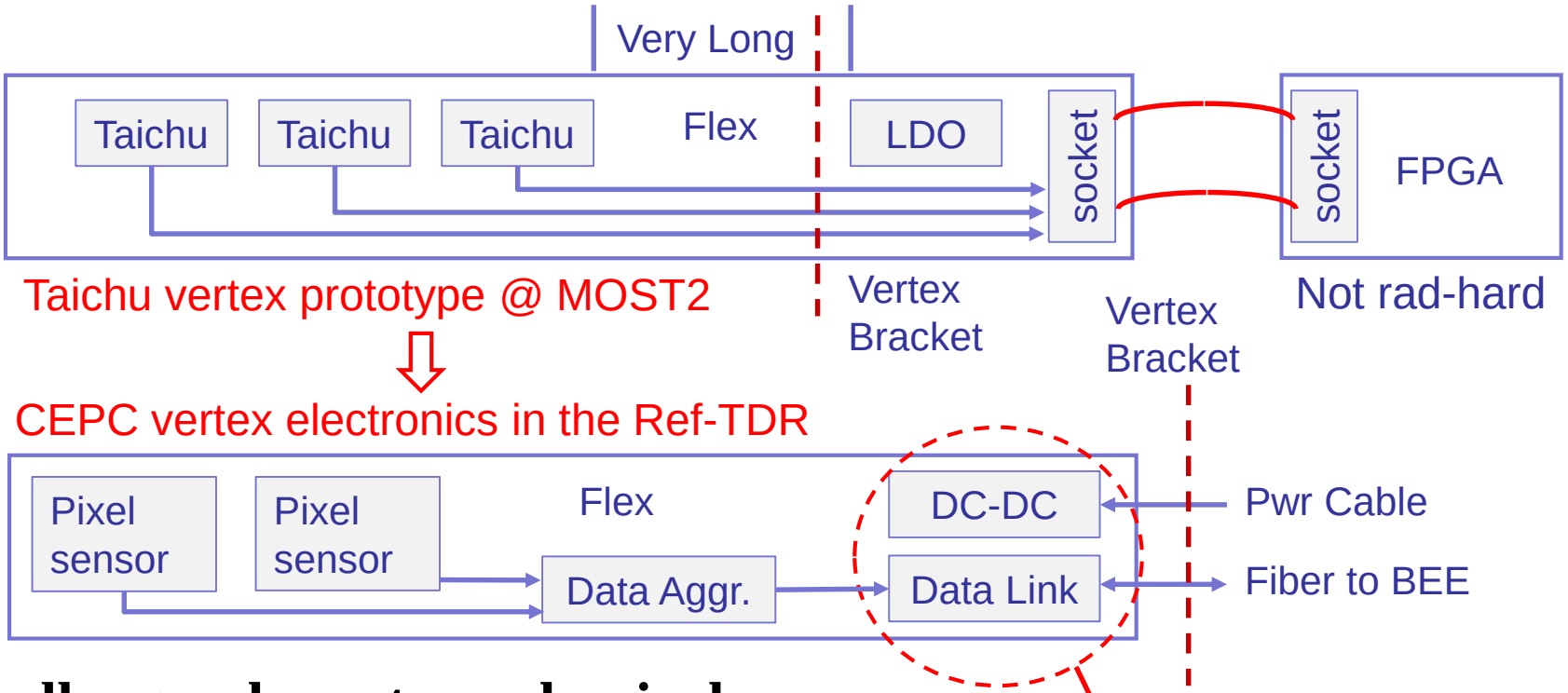
Thanks for the inputs from colleagues working on the detector

The current electronics and TDAQ block-diagram

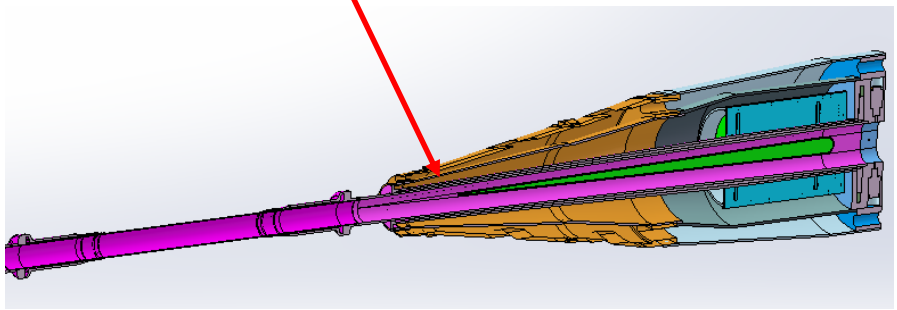


- **Common subsystems (data processing, aggregation, transmission; powering) need R&Ds now.**
- **Detector specific ASICs will wait for detector final choices.**
- **We strive for a common BEE hardware, configurable for individual subsystems.**
- **Collaborations are highly appreciated, to survive and succeed.**

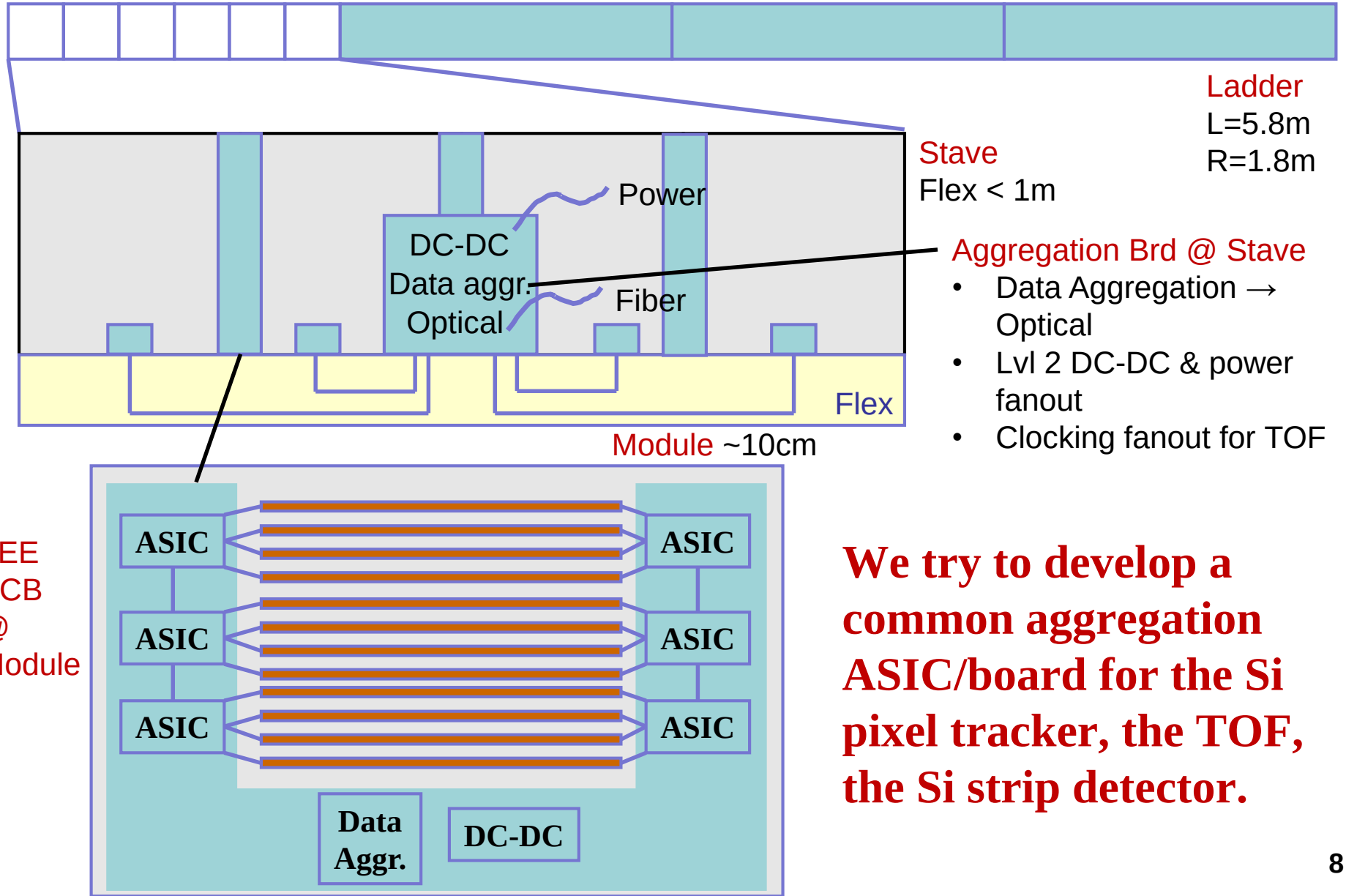
Electronics scheme for the vertex detector



- **Challenges: layout, mechanical and power constraints, data transmission, etc.**
- **Possibly the only sub-det that needs fast trigger due to beam background – under study.**



Electronics scheme for the silicon tracker

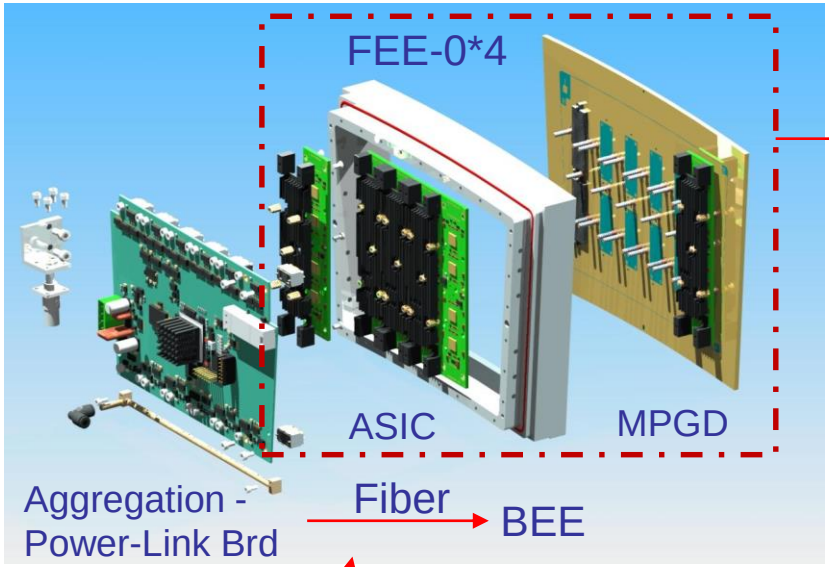


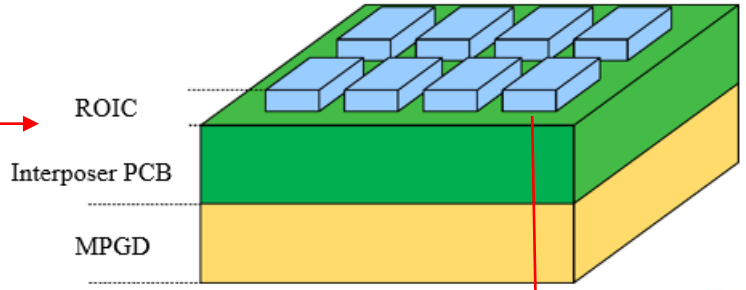
Aggregation Brd @ Stave

- Data Aggregation → Optical
- Lvl 2 DC-DC & power fanout
- Clocking fanout for TOF

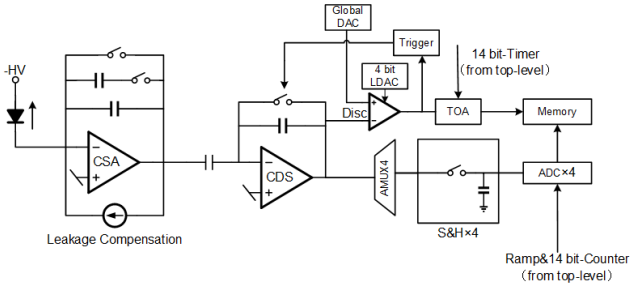
We try to develop a common aggregation ASIC/board for the Si pixel tracker, the TOF, the Si strip detector.

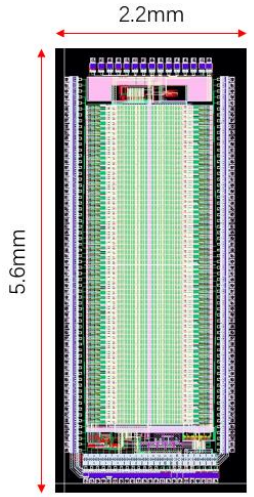
Electronics scheme for the pixel TPC



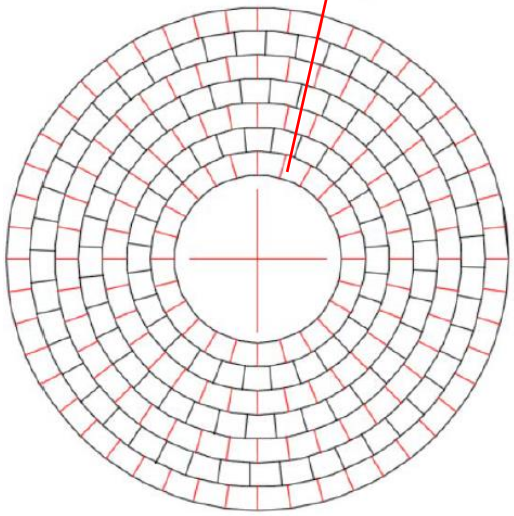


An integrated board with ASIC & MPGD, N(now 4) for a module
0.5mm*0.5mm / pixel





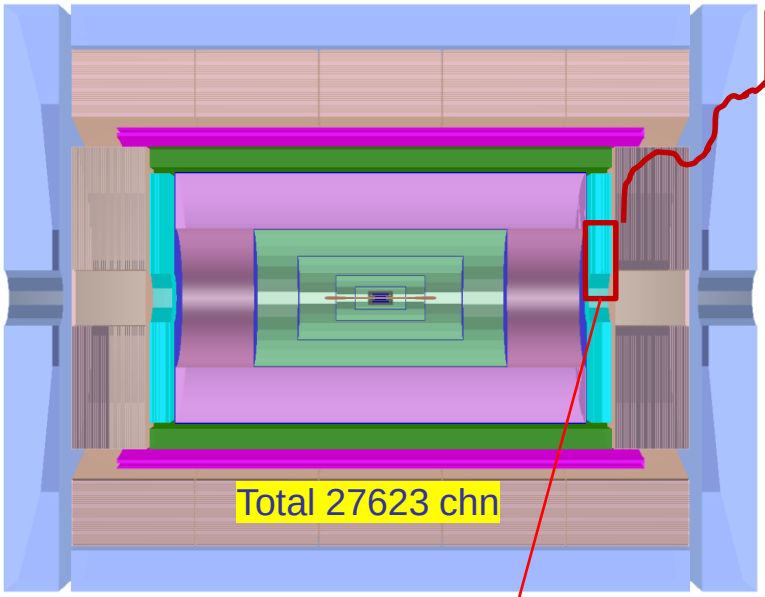
128 chn ASIC, Q+T measurement
142.8k pixel/module → 1115 chip/module→ 279 chip/FEE-0

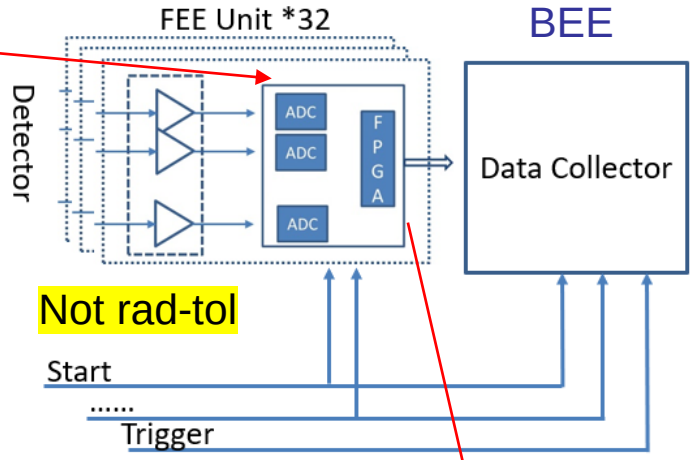


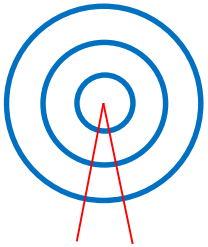
~258 Module/Endplate

Power:
Limit: <10 kW/endplate ~ 39.7 W/module ~10 W/FEE-0
35mW/ASIC ~ 280μW/chn
Data rate:
80 particles/BX, 12,000 hit/particle, 32(48)b/hit, @ 40M BX Z pole
1 Module: ~100 Mbps(@ innermost)

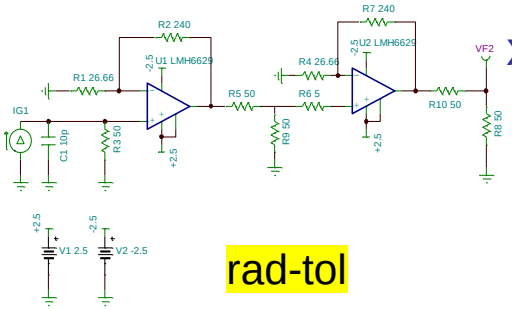
Electronics scheme for the Drift Chamber



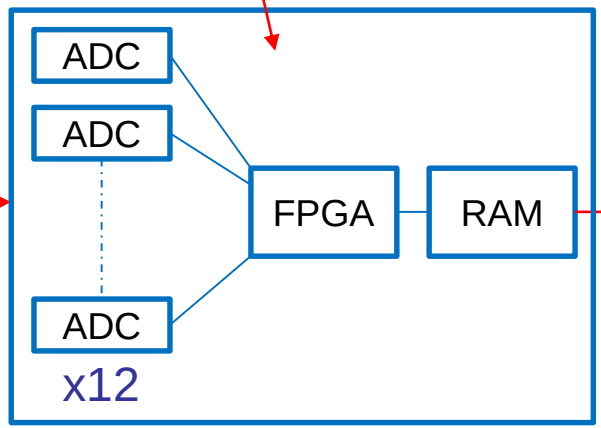




12 chn
Grp by sector



x12

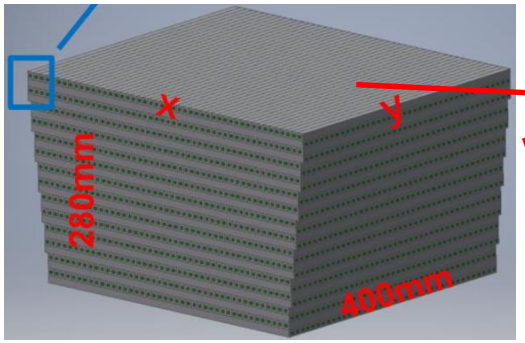


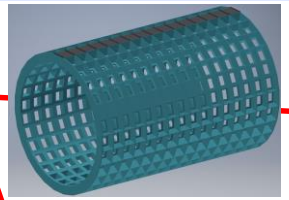
High Bandwidth Preamp
100mW/ch -> 2.7kW

Analog signal on Cable
2.8mm per co-ax
12 signals + 1 Power
3dB attenuation @ 280MHz

ADC @1.3Gsps 12bit
RAM to average 12 chn in a sector
Read by wave envelope of 1.5 us with waveform-- compatible with calibration requirement (0.5Gbps/ 12chn)

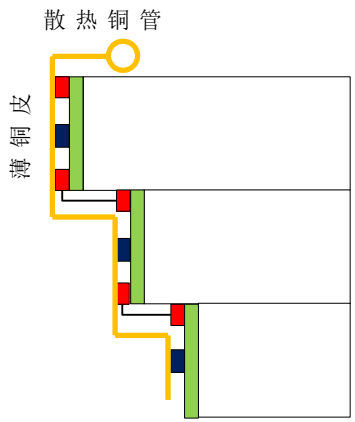
Electronics scheme for the ECAL



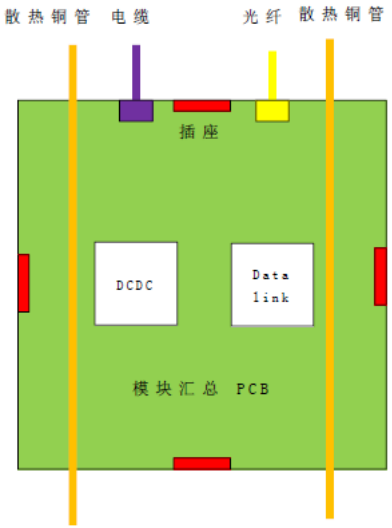


SiPM ROC + PCB end data aggregation

Challenges: very limited space (5 mm height) for the readout & DC-DC module; difficult for heat dissipation.

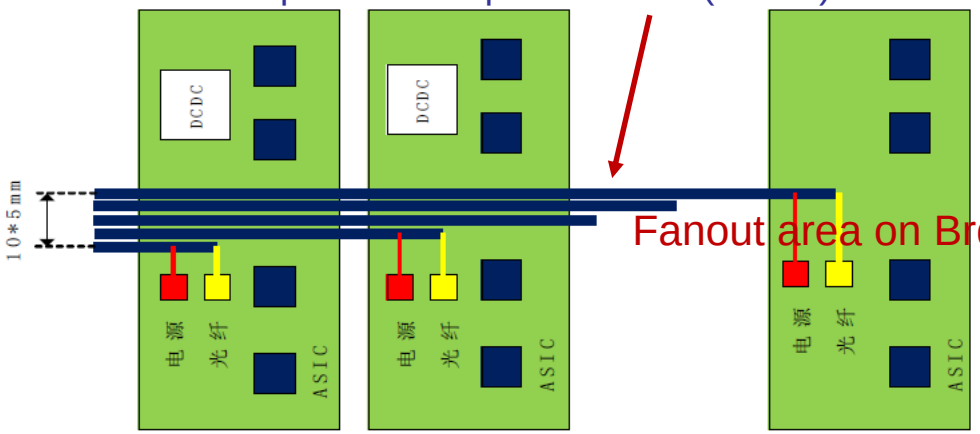


SiPM ROC @ cryst. ends



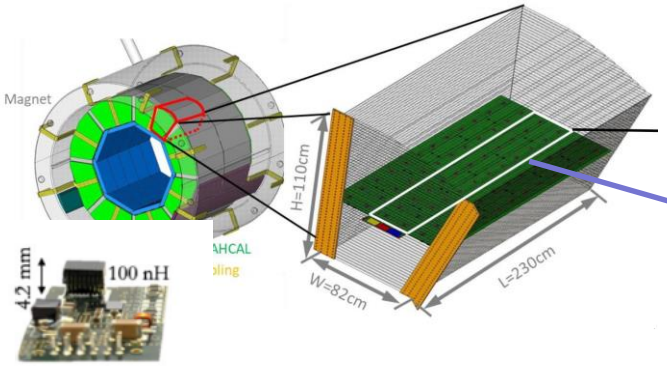
Data aggr. @ module end

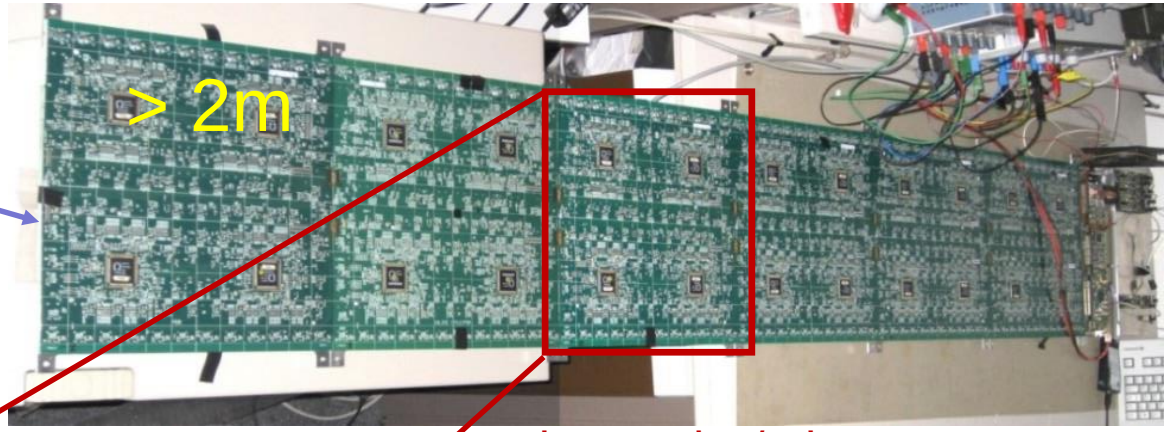
Opt-Elec Composite Cable (~5mm)



Module end goes to barrel fanout @ half barrel

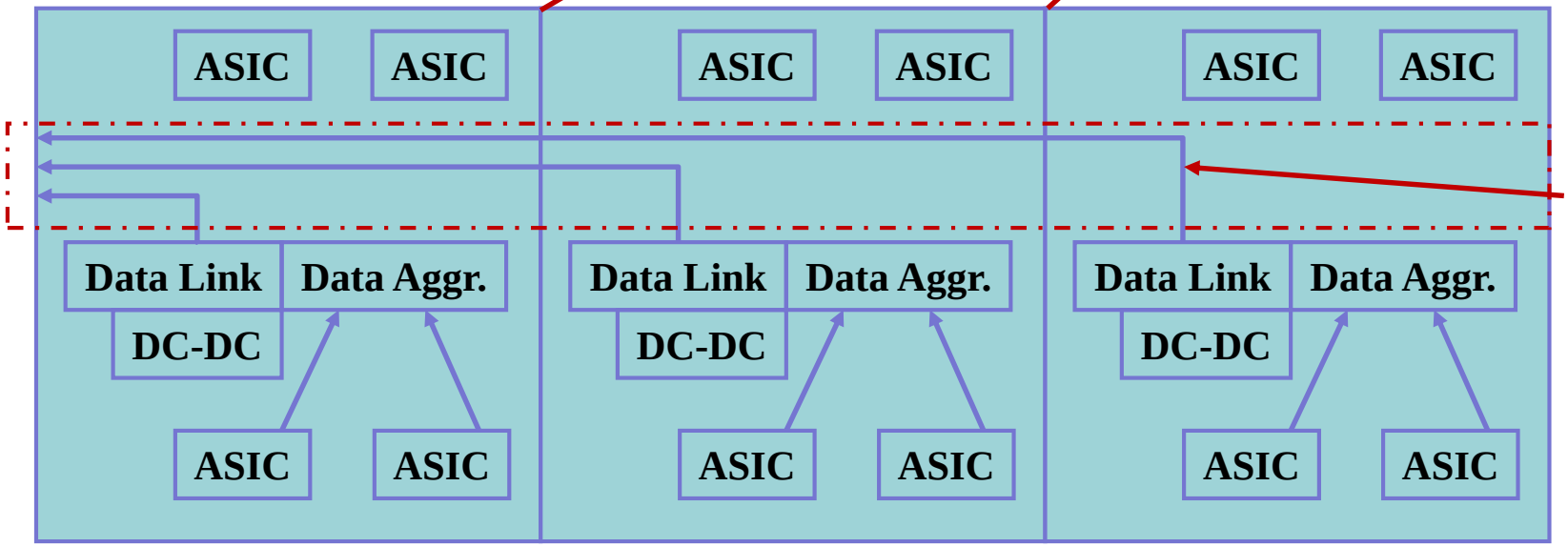
Electronics scheme for the HCAL





Glass+**SiPM** evenly distr. on the top side

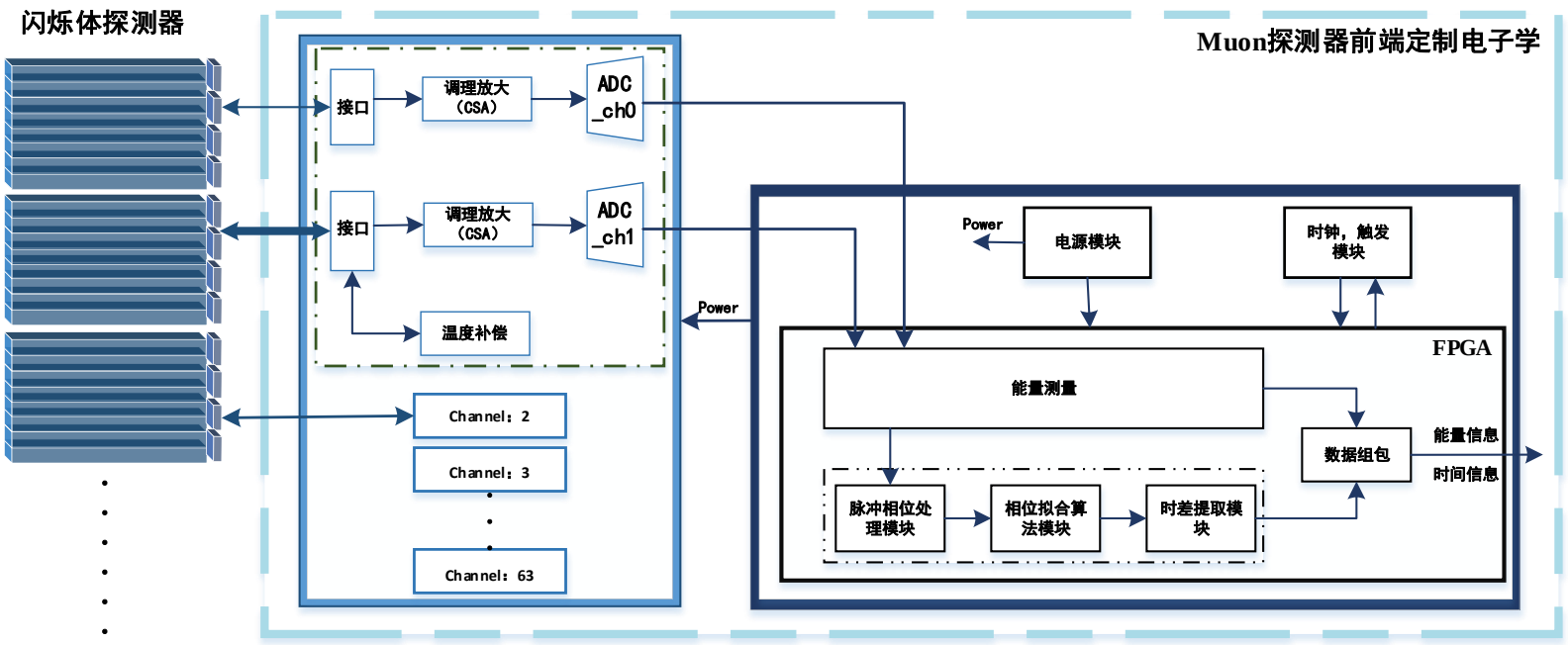
Indep. Brd w/o inter-conn.



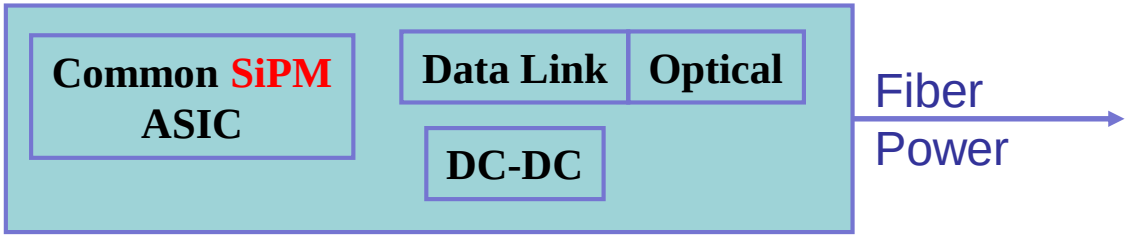
Fanout area by opt-elec composite cable

The same challenges: little space for electronics boards, electric cable plus optical at the end of the detector, difficult in heat dissipation.

Electronics scheme for muon system

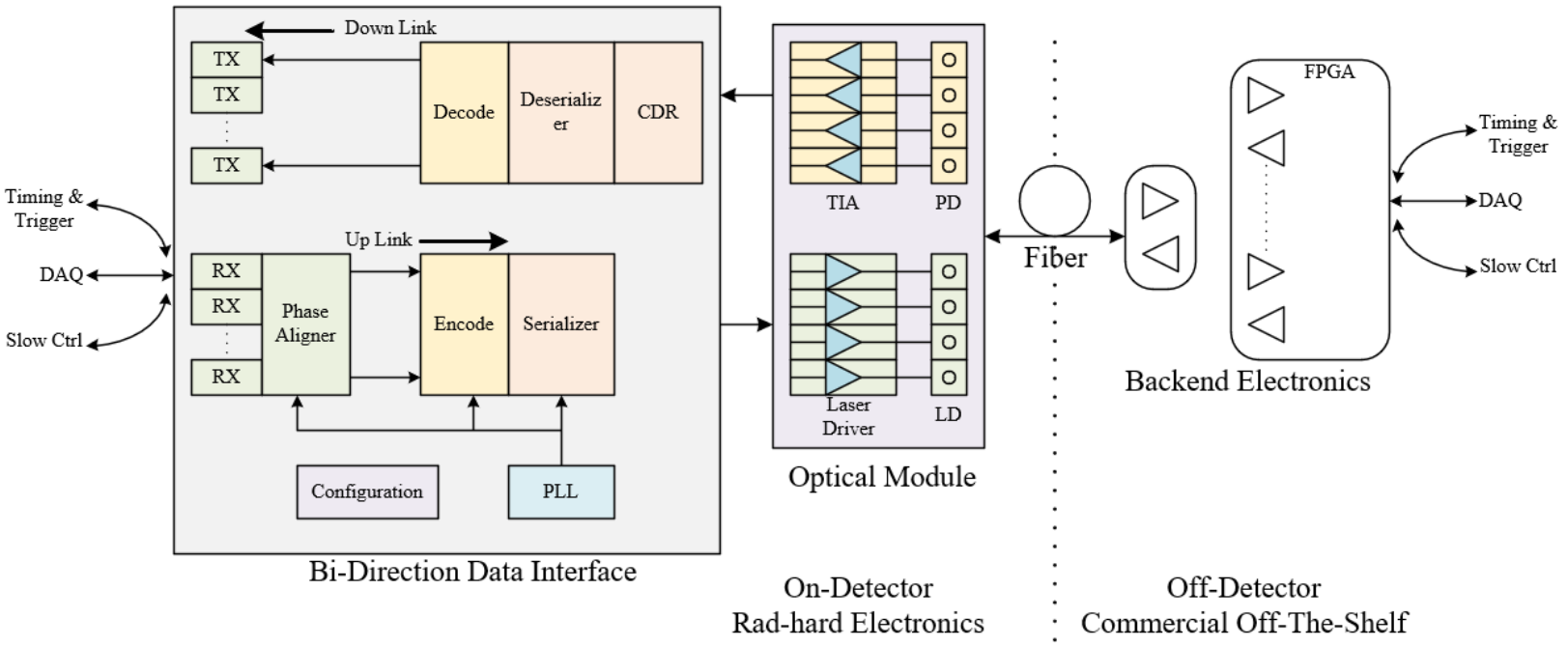


Muon Elec R&D

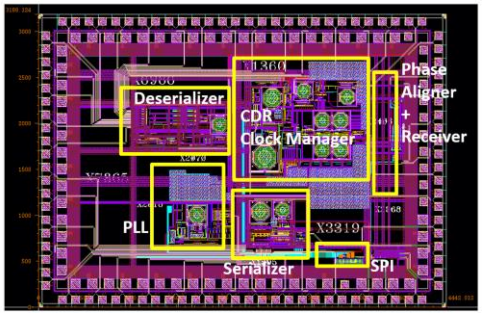


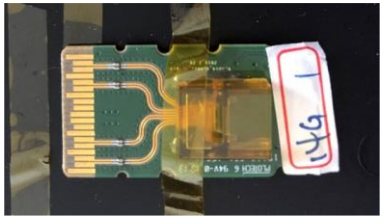
CEPC Muon FEE

A common project for the data link

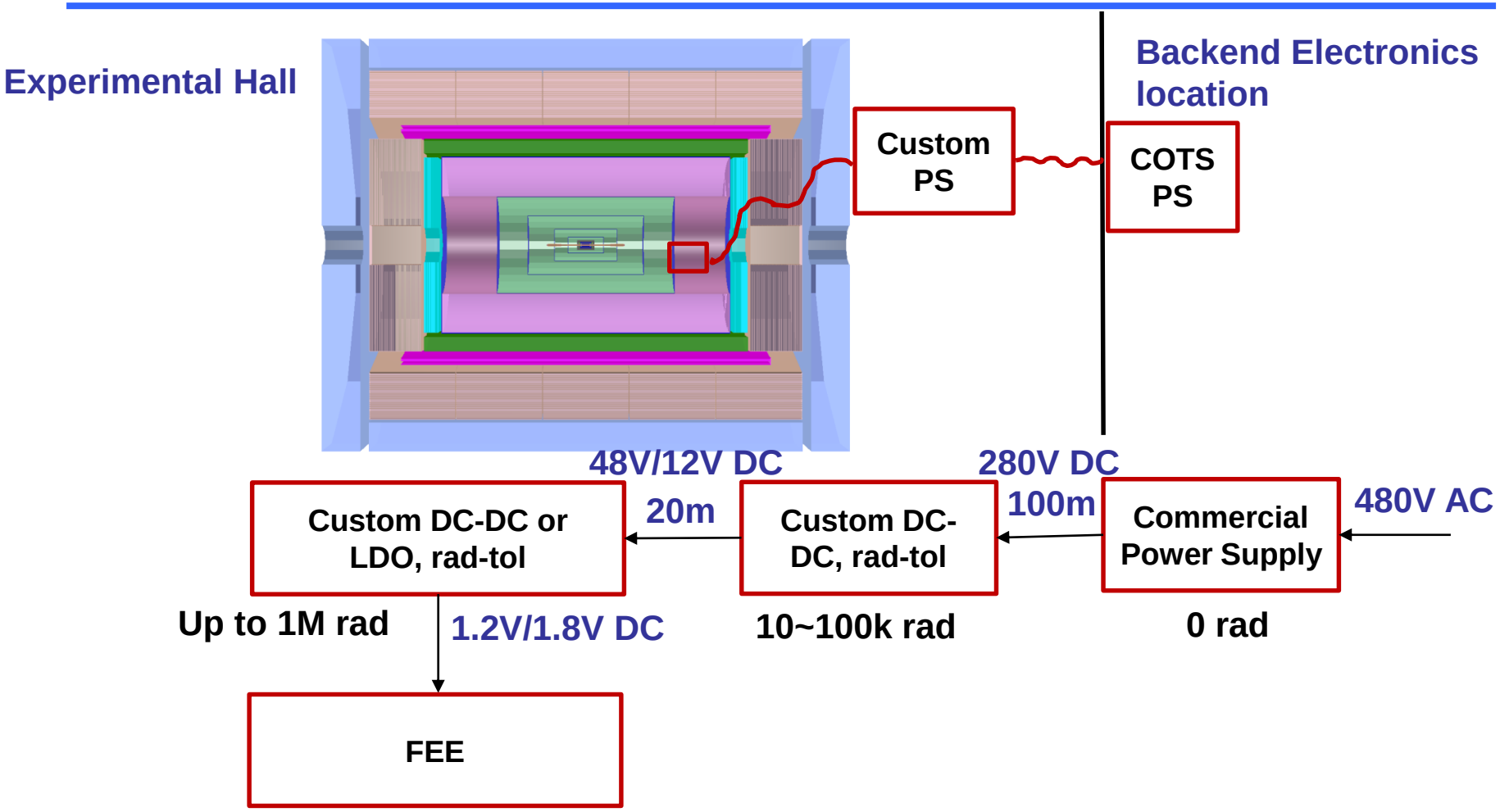


- **Based on prior R&Ds, we plan to develop a lpGBT and Versatile-Link-like common data transmission hardware (ASICs and modules) for all sub-detectors.**
- **Stringent size limitations from the Vertex detector and the calorimeters (ECAL and HCAL).**
- **Requirement on radiation tolerance comes from the Vertex to be O (Mrad/yr)**





A common project for powering the FEE



- **The custom DC-DC will be GaN based. Other than the requirements of tolerance to the radiation and strong magnetic field, the DC-DC modules must meet the stringent mechanical constraints in the detector, especially the Vertex detector.**
- **Because of this, we still keep serial powering on the table.**

Summary

- **Detector requirements and the FEE**
  - **We are working on the moving target: detector requirements/constraints to the FEE**
  - **We strive for a triggerless FEE, even for the innermost Vertex detector**
  - **Detector signals will be digitized in the FEE, enabling a common data link between the FEE and the BEE**
  - **We focus on the R&Ds for common projects: the data link and the powering**
- **Although not discussed, we aim for a common BEE hardware, configurable for individual subdetectors, and interfaces to TDAQ.**

To-do towards the Ref-TDR

- **We must converge according to the plan for the Ref-TDR**
  - **We are working with detector colleagues on the input to FEE, signal characteristics, data rate, power budget and mechanical constraints.**
  - **We are identifying key R&Ds in the two common projects, to show proof-of-principles or discover major road-blocks.**
    - **The data link will be based on lpGBT-like ASICs and optical modules.**
    - **The custom DC-DC for the FEE will be based on GaN. Serial powering will be looked at because of the extreme space constraints in the Vertex detector.**
- **R&Ds on detector specific readout ASICs will follow the detector choice. When possible, we will try to develop ASICs that cover multiple needs in CEPC.**
- **The BEE should not be forgotten. Many FEE developments will need to go with the BEE designs.**

Thank you!

Backup

Preliminary consideration on common BEE

	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory(Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- **A common station for fibers from FEE**
- **Providing data buffers till trigger comes**
- **Possible calculation resource needed for trigger algorithm**
- **Number of IOs, port rate & the cost are the major concerns**

Specification calculation- from hit density

		Hit density (Hits/cm^2/BX)	Bunch spacing (ns)	Hit rate (M Hits/cm^2)	Hit Pix rate (M Px/cm^2)	Hit rate/chip (MHz)	Data rate@triggerless (Gbps)	Pixel/bunch	FIFO Depth @3us rg latency	Data rate@trigger (Mbps)
CDR	Higgs	2.4	680	3.53	10.59	34.62	1.1	23.5	103.9	105.28
	W	2.3	210	10.95	32.86	107.44	3.4	22.6	322.3	101.248
	Z	0.25	25	10	30	98.1	3.1	2.4	294.3	53.76
TDR	Higgs	0.81	591	1.37	4.11	13.44	0.43	7.96	40.4	0.017
	W	0.81	257	3.16	9.45	30.90	0.98	7.96	92.8	3.6
	Z	0.45	23	19.6	58.7	191.9	5.9	4.4	575	118

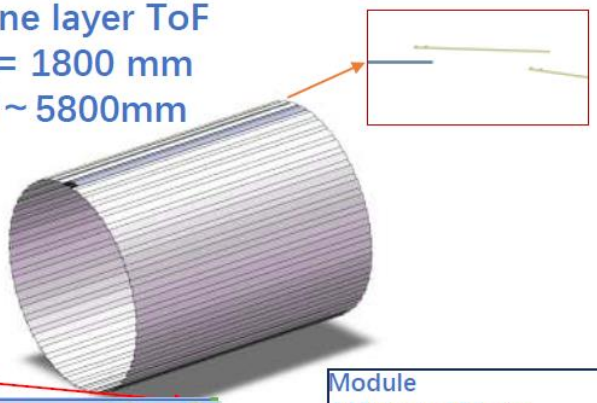
- **TDR raw hit density: Higgs 0.54，Z 0.3；Safety factor: TDR 1.5, CDR 10;**
- **Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)**
- **Area: 1.28cm*2.56cm=3.27cm^2 (@pixel size 25um*25um)**
- **Word length: 32bit/event (@Taichu's scale, 512*1024 array)**
- **Trigger rate：20kHz@CDR，120kHz@Z, 10Hz@Higgs, 2kHz@W TDR**
  - **Trigger latency: 3us(very likely not enough), Error window: 7 bins**
  - **FIFO depth: @3us * hit rate/chip**
  - **Data rate=pixel/bunch*trigger rate*32bit*error window**

LGAD as a TOF @ Outer Tracker

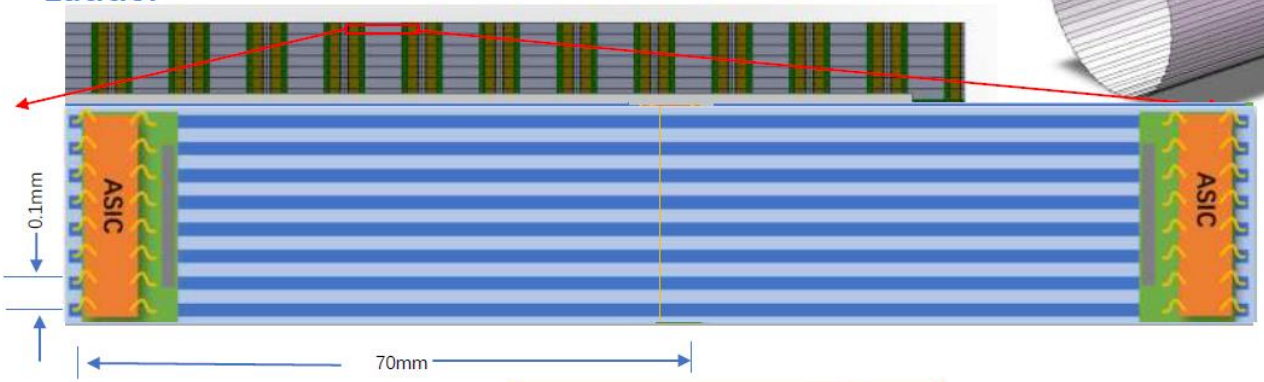
- One layer:
  - 90 ladders, 45 ladders each side,
    - 42 modules/ladder
      - 22 ASIC/module
        - 128 channels/ASIC
- Total modules needed:

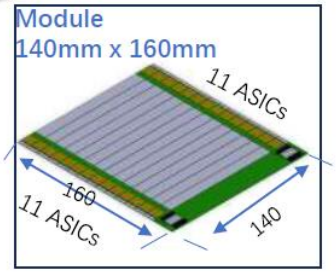
  45 *2*42 = 3780 modules

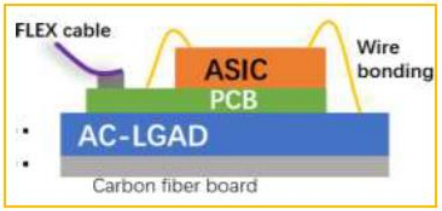
One layer ToF
R= 1800 mm
H ~ 5800mm



Ladder

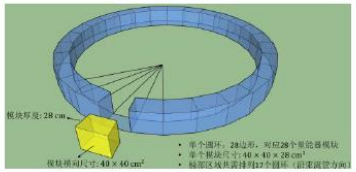




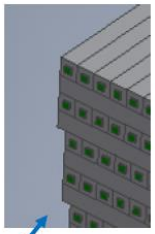


ECAL

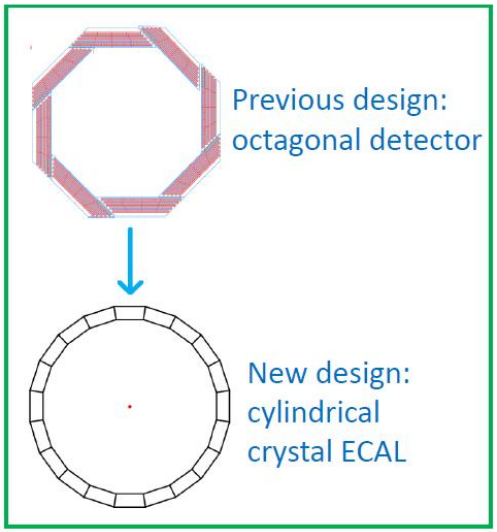
- CEPC crystal ECAL barrel geometry design
  - Finer segmentation of towers for better homogeneity
  - Decrease outer radius for lower cost of the outer detectors
  - 28 towers per ring, 17 rings along beam direction
  - ~25 radiation length: 28 layers

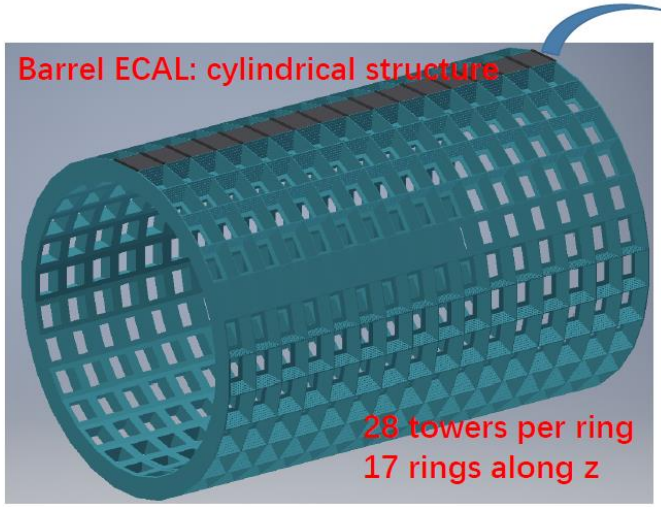


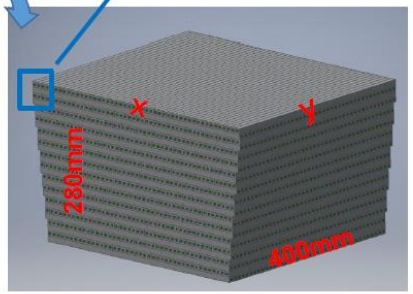
Quan Ji, Chang Shu (IHEP)



4 layers per "step" with the same transverse size







Key questions
- Space for electronics and cooling
- Assembly