Common R&D efforts on CMOS pixel sensors for the experiment of electron-positron colliders

15th FCPPN/L Workshop,10 – 14 Jun 2024, Bordeaux

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on behalf of the FCPPN/L collaboration teams

PROJECT TITLE: Belle II vertex detector upgrade (BUV)

French Group: IPHC/IN2P3, *Jérôme BAUDOT, Christine Hu-Guo, ...*

Chinese Group: IHEP/CAS, *Qun OUYANG, Yunpeng Lu, …*

Outline

- Introduction
  - Short review of collaboration history
  - BELLE II VTX upgrade proposal
  - R&D for CEPC vertex detector
- Common interests in MAPS* development
  - Large area sensor design OBELIX and JadePix-5
  - Digital on Top design methodology
  - Sharing mask area in TJ 180 nm CIS process
- Summary

*Monolithic Active Pixel Sensor, or CMOS Pixel Sensor are used interchangeably in this talk without distinction

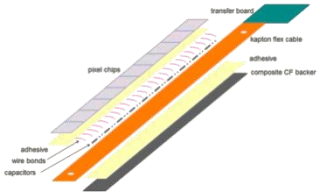
Short review of the collaboration history

- **Starting from 2010, common R&D efforts of MAPS for the e^+e^- collider experiments:** *BES III upgrade, ILC/CEPC, BELLE II upgrade*
- **Regular visits on both institutions and on-line meetings**

1、The prototype of CMOS pixel sensor for the upgrade of BESIII-inner tracker

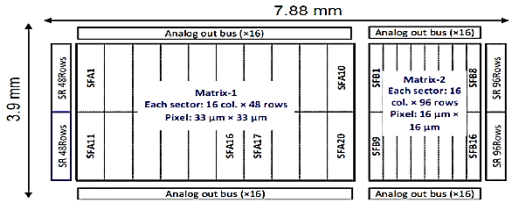
✓ Development of pixel detector ladder based on the MIMOSA28 sensors from IPHC

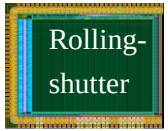
✓ common participation of beam test at DESY, to validate the ladder performance, space resolution, material budget, …

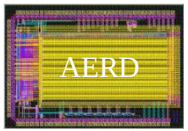


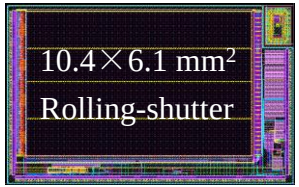
Ref.: *NIMA924(2019)287-292, NIMA986(2021)164810*

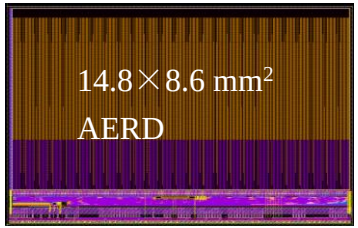
2、CMOS Pixel Sensors R&D for future e^+ e^- colliders: *pixel sensor and double-sided ladder development*
Since 2015, four engineering runs have been shared with TJ 180 nm CIS process











2015: JadePix-1 → 2017: JadePix-2/MIC4 → 2020: JadePix-3 → 2022: JadePix-4/MIC5

Physics program @ SuperKEKB with Belle II

- Thorough test of Std Model
- DIrect/indirect search for New Physics
- Hadronic Physics

} with billions of $B\bar{B}, c\bar{c}, \tau\bar{\tau}$ pairs In "clean" environment of B-factory

⇒ The Belle II physics book PTEP 12 (2019) 123C01

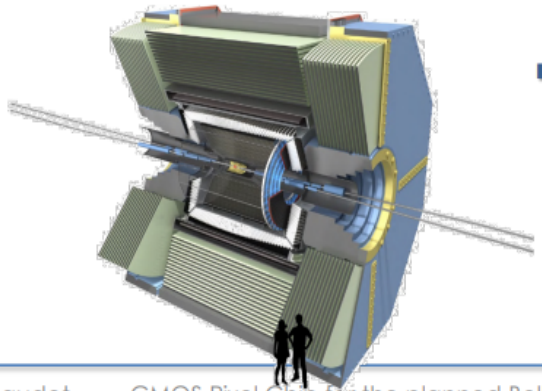
- Based on accumulation of 50 ab^{-1} of e^+e^- at $\sqrt{s} = M_{\Upsilon(4S)}$
  - requires instantaneous luminosity close to 6×10^{35} $cm^{-2}.s^{-1}$

→ SuperKEKB collider implementing the nano-beam scheme @ high currents

→ High collision rate High beam-induced bkg

The Belle II experiment

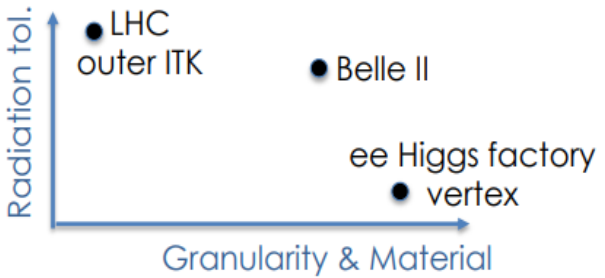
- "classical" B-factory detector + enhanced features



The vertex detector (VXD)

- Better vertexing ← lower boost
  Smarter tracking ← higher hit rate

+ Harsher radiation environment
+ Belle II trigger rate ~ 30 KHz

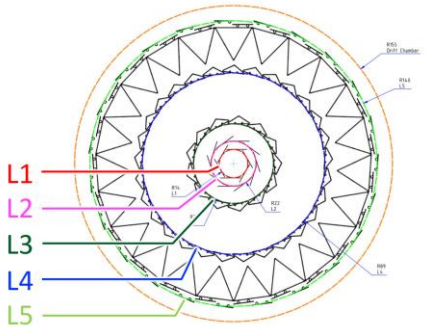


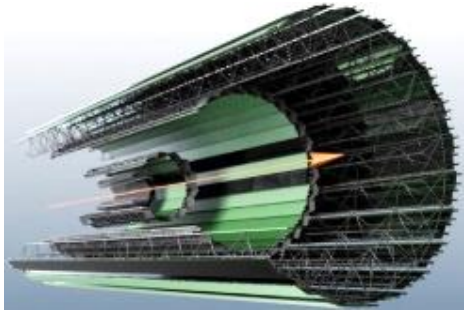
➔ Proposal for replacement of VXD = PXD (DEPFET sensors) + SVD(Double Sided Strip Detector) by VTX detector.

VTX proposal

Proposed BELLE II VXT upgrade scheme

- 5 straight layers with **D**epleted **M**onolithic **A**ctive **P**ixel **S**ensors
- Identical chips on all layers: Optimized BELle II pIXel (OBELIX) sensor
- ~1m² silicon surface

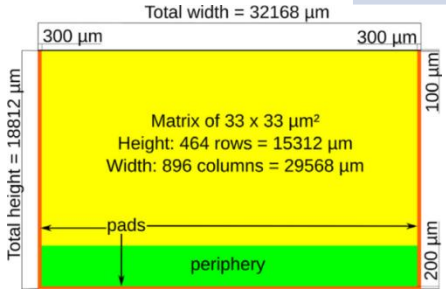




From simulations	Belle II VTX
Spatial res.	<10-15µm
Total material budget Inner-outer layers	0.1 – 0.8 %Xo
Max hit rate	120MHz/cm²
Time precision	<100ns
Trigger (freq.) (delay)	30 kHz 5-10µs
Rad. hard. (TID) (fluence)	<100 kGy/year <$50\times10^{12} n_{eq} cm^{-2}$/year
Power	<200mW/cm²

OBELIX

– Tower 180 nm process
– Extension of TJ-Monopix2
→ OBELIX sensor
– <40 µm pitch, 100 ns integration



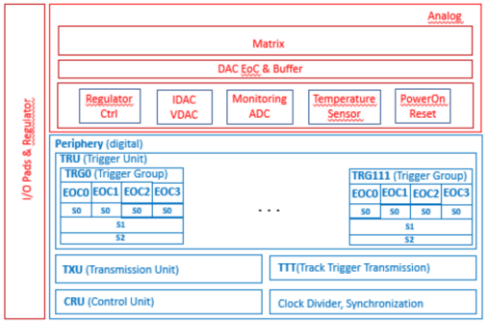
Key sensor specifications:

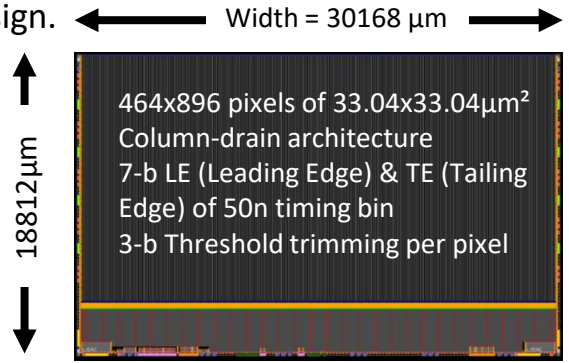
- Pixel pitch: *30-40 µm*
- Integration time: *≲100 ns*
- Power dissipation: *≲200 mW/cm²*

OBELIX (Optimized for BELle II pIXell)

- Developed from **TJ-Monopix2 sensor** (*Developed for ATLAS-ITK: doi: 10.1016/j.nima.2020.164460*)
- Increase **active area** from 17x17 mm² to 15x29,6 mm²
- LDO implementation on lateral sides for **power drop compensation** on ladder
- Re-design digital periphery for handling **VTX trigger requirements** with additional features: TTT (Track Trigger Transmission) & PTD (Peripheral Time to Digital)
- Additional analog functionalities for improved **monitoring and safety** : Monitoring ADC, Temperature sensor, Power On Reset

- **Design collaboration:** IPHC, CPPM, HEPHY, KEK, INFN, University of Bergamo, University of Pavia, University of Pisa, University of Applied Sciences and Arts Dormund, University of Bonn, University of Valencia
  - ✓ With their expertise in MAPS, Chinese laboratories are **candidate** for Belle II VTX contributing in different development aspects, such as chip characterization or detector design.





Physics requirements on the CEPC vertex detector

- Br (H -> cc) is extremely sensitive to the vertex design
- Br (H -> bb) is not really sensitive to the vertex design

Ref: *ZG Wu, Optimization on silicon detectors at CEPC, CEPC workshop 2019*

	Scenario A (Aggressive)	Scenario B (Baseline)	Scenario C (Conservative)
Material per layer/X_0	0.075	0.15	0.3
Spatial resolution/μm	1.4 - 3	2.8 - 6	5 - 10.7
R_{in}/mm	8	16	23

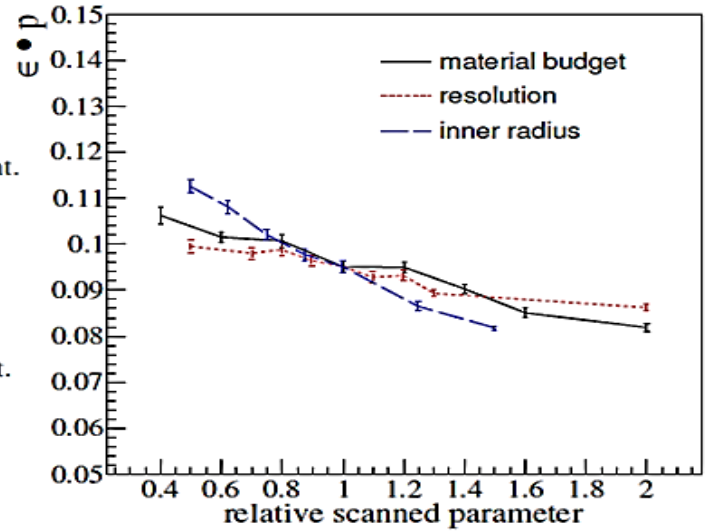
Table 3. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \rightarrow c\bar{c})$ measurement.

σ_{SP}< 3 μm very difficult

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.133 ± 0.002	0.095 ± 0.001	0.078 ± 0.001
		41%	-22%

Table 4. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \rightarrow b\bar{b})$ measurement.

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.925 ± 0.001	0.914 ± 0.001	0.900 ± 0.001
		1%	-1.5%

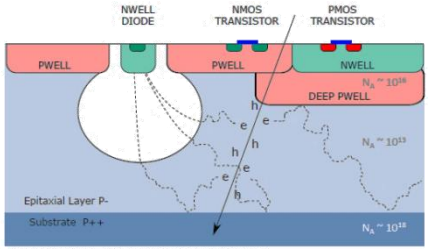


H-> ττ has similar analysis and results

$$\epsilon \cdot p = 0.095(1 - 0.14\frac{\Delta x_{material}}{x_{material}})(1 - 0.09\frac{\Delta x_{resolution}}{x_{resolution}})(1 - 0.23\frac{\Delta x_{radius}}{x_{radius}})$$

Ref.: *ZG Wu et al., Study of vertex optimization at the CEPC, 2018 JINST 13 T09002*

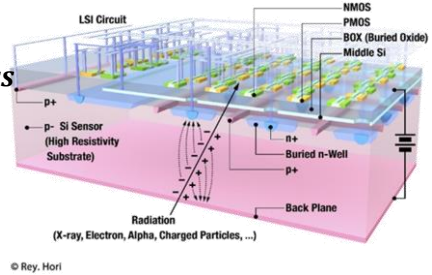
R&D for CEPC Vertex detector



pixel capacitance ≈5 fF (@ V_{bb} = -3 V)

HR-CMOS pixel sensor

- ***TowerJazz CIS 180 nm process***
- *Quadruple well process*
- *Thick (~20 μm) epitaxial layer with high resistivity (≥1 kΩ•cm)*
- *Thinning to 50 μm proved*



SOI-CMOS pixel sensor

- ***LAPIS 200 nm process***
- *High resistive substrate (≥1 kΩ•cm)*
- *Double-SOI / PDD-SOI layers available*
- *Thinning and backside process*
- *3D connection technology available*

Towards Baseline Requirements: CMOS and SOI R&D in Synergy

Fine pitch Low power frontend + Fast readout architecture

Spatial resolution thinning Analog power

Readout speed Digital power

Before 2020 ---- CPV1/2/3 (SOI) JadePix1/2/3 (CMOS) MIC4 (CMOS) TaichuPix1/2 (CMOS)

2020-2022 ---------- JadePix4/MIC5, TaichuPix3 CPV4-3D

	Pixel size	Readout Scheme
JadePix-3	16 X 23.1 μm^2	Rolling shutter
CPV-4	17 X 21 μm^2	AERD
JadePix-4	20 X 29 μm^2	AERD
TaichuPix-3	25 X 25 μm^2	Column drain

R&D for CEPC Vertex detector

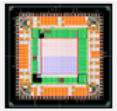
2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022

SOI pixel

Compact Pixel for Vertex

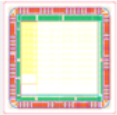
Double-SOI process

CPV1



3×3 mm²

CVP2



SOI-PDD process

6×6 mm²

CVP3

CVP4-3D

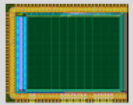
HR-CMOS pixel

Tower-Jazz CiS process

Sensing node study

JadePix1

3×3.3 mm²



JadePix2

Small pixel size, in pixel digitization and low power design

3.2×3.7 mm²

MIC4

10.4×6.1 mm²

JadePix3

JadePix4/MIC5

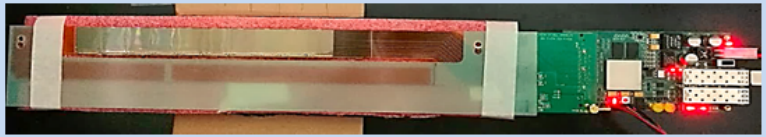
Fast readout, +time stamp (25ns)

TaichuPix1/2

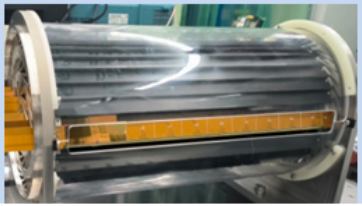
TaichuPix3

Ladder and prototype

Single-sided ladder with MIMOSA28 sensors, 0.39%X_0/layer



Double-sided prototype



FCPPL project: BELLE II vertex upgrade

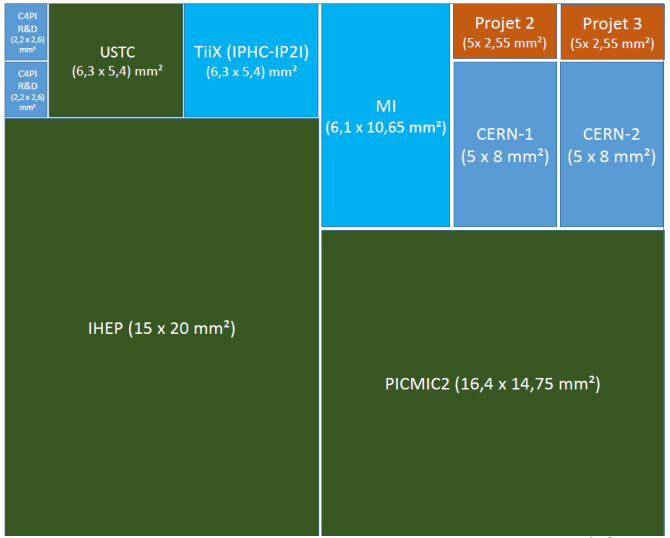
- FCPPL collaboration proposal in 2023/2024 (approved)
- Common interests in **OBELIX design**:
  - Analog design →

  Critical issues in large area chip: Powering and Signal driving
  - Digital design → Data buffering and data transmission of low power
  - Digital on Top integration flow → Verification of complex design before tape-out

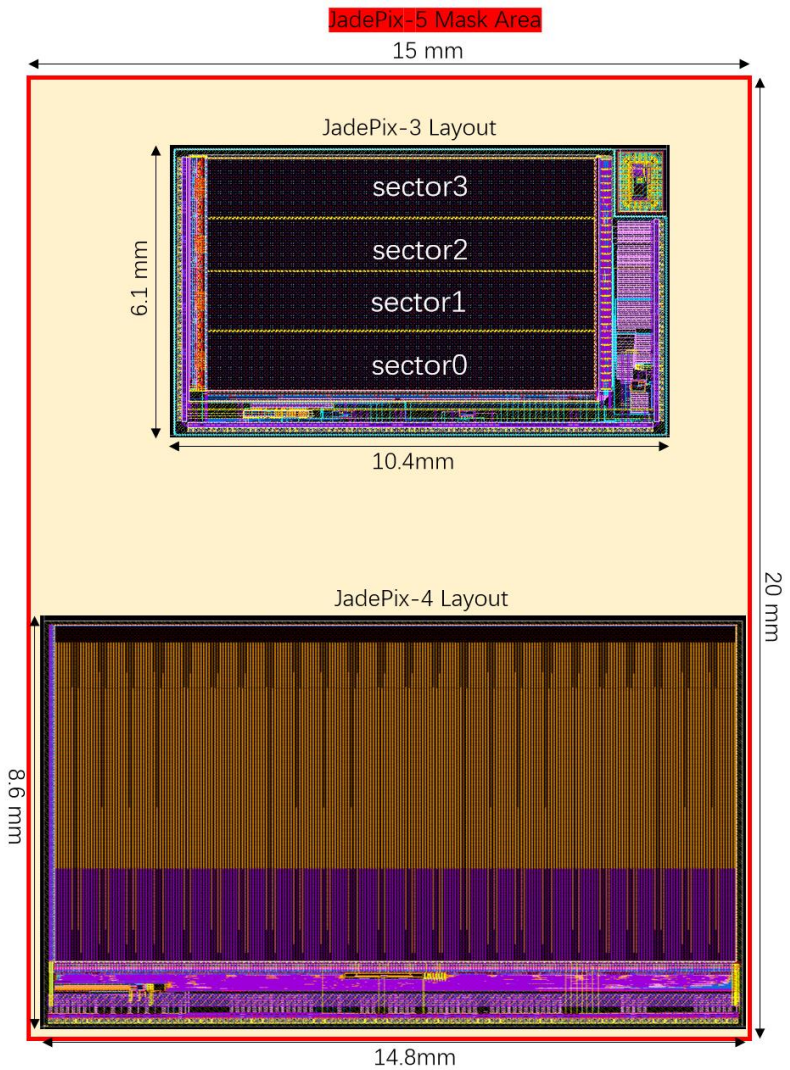
- Shared submission to Tower 180 nm process (Engineering Run)
  - 3/8 mask area for IHEP team (2 cm x 1.5 cm)
  - **JadePix-5 design** for CEPC R&D
  - Planed in Sep. 2024

- Discussion sessions have been launched on demand and

Visit in person is foreseen during
  - Pixel 2024 workshop, Strasbourg, from 18 to 22 Nov. 2024



JadePix-5



- The largest design of JadePix series
  - Pixel array 896 rows × 480 col.
  - Sensitive area 17.9 mm × 14.4 mm (86%)

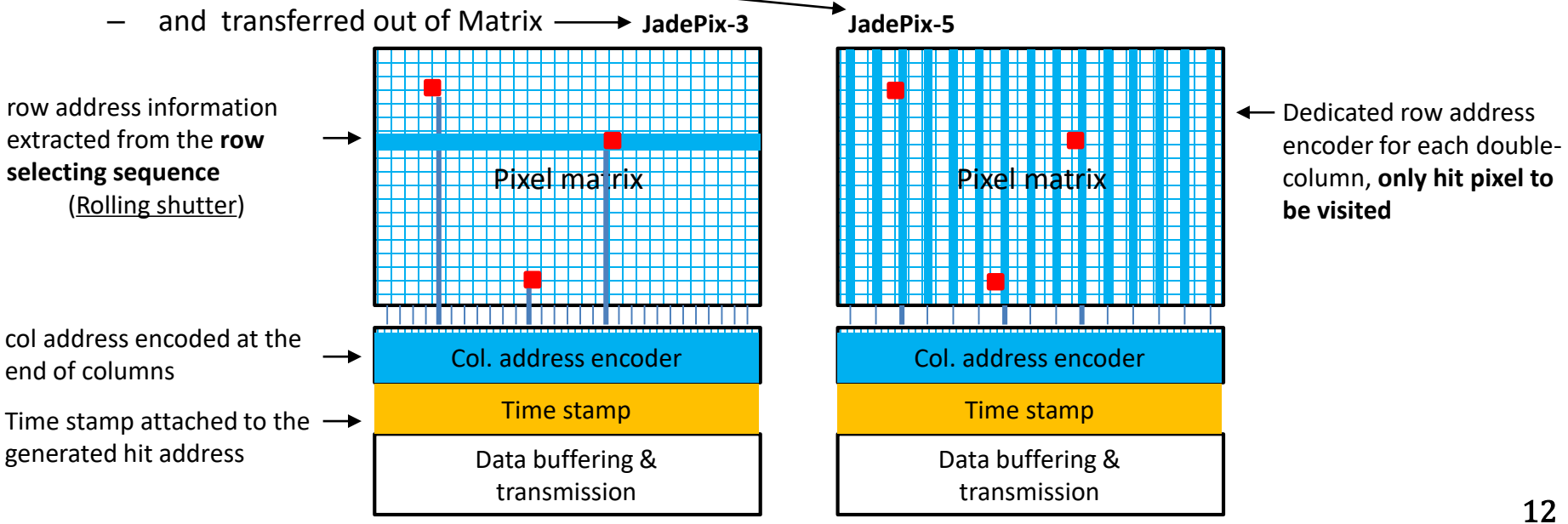
- Functional blocks verified in JadePix-3/4
  - Sensing diode
  - Analog frontend
  - Pixel logic
  - AERD and DAC

- Optimizations on power distribution and signal driving
  - Voltage drop across the matrix
  - Signal transition on long metal lines

- Optimizations on peripheral readout
  - SRAM size and clock frequency

Readout Architecture

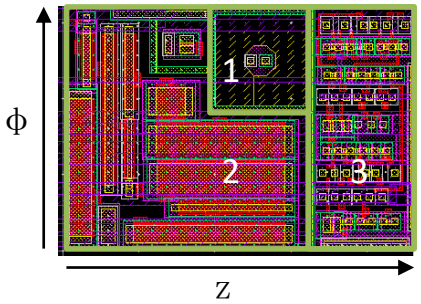
- A major improvement: Rolling shutter (JadePix-3) → Hit-driven readout logic(JadePix-5)
  - **Faster by 3 orders of magnitude and remain the same low power**
  - Larger pixel size: 20 μm × 30 μm
- Time stamp depends on how fast the hit information can be
  - registered in the pixel
  - and transferred out of Matrix



Comparison of JadePix-3 and JadePix-5

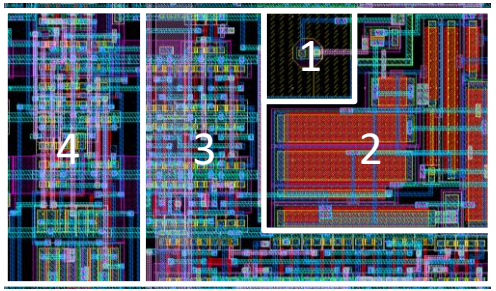
- JadePix-3 targeting on smallest pitch of 16 μm× 23.1 μm for **spatial resolution ~ 3 μm**
- JadePix-5 targeting on **fast time stamp ~ 1 us**, improved by a factor of 100
  - Trade off between shaping time and amplifier current in the analog frontend
  - Hit-driven readout logic, occupied ~ 1/4 pixel area

JadePix-3



Pixel footprint:
1: Sensing diode
2: Analog frontend
3: Digital frontend
4: Hit-driven RO logic

JadePix-5



	JadePix-3	JadePix-5
Pixel size	**16 μm × 23.1 μm**	20 μm × 30 μm
Time stamp precision	98.3 μs	**~ 1 μs**
Average power	< 100 mW/cm^2	< 100 mW/cm^2
Pixel array	512 row × 192 col.	896 row × 480 col.
Mask area	10.4 mm × 6.1 mm	20 mm × 1. mm

Supply voltage distribution

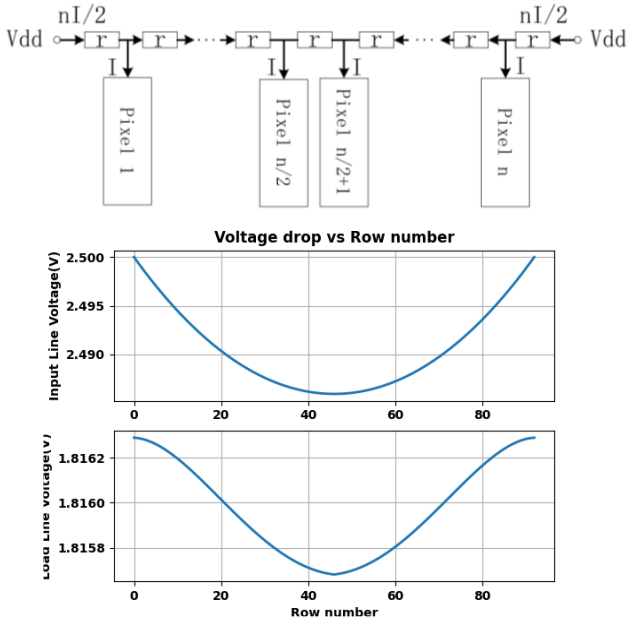
- A major concern as JadePix-5 has a dimension of half full size (2 cm × 1.5 cm)
  - Voltage drop and ground bounce across the pixel matrix
  - Due to r_{metal_line} = 40 mOhm/square
- Estimated by a simple model based on the actual pixel layout
  - Line width of TOP_M = 5 μm
  - Pixel pitch = 30 μm
  - Load current in each pixel ~ 20 nA
  - 480 pixels in a row
  - Voltage drop on the center pixel 0.14 mV

$$\Delta V = \frac{n}{4}\left(\frac{n}{2}+1\right) \mathrm{Ir} \times \frac{\mathrm{pitch\_x}}{\mathrm{d}} = 0.14\ mV$$

Smaller n in row-wise

Very low current/pixel

- Detailed results will be given after power analysis



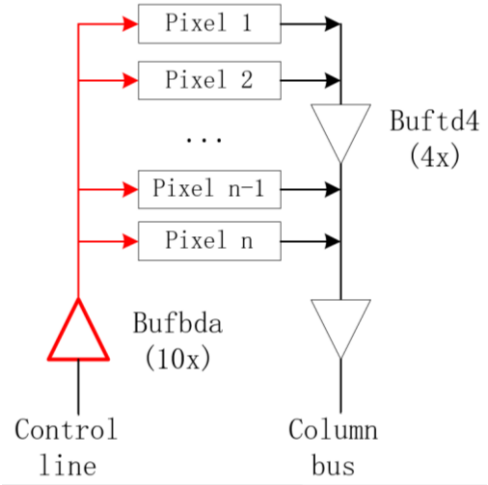
Compensation of IR drop adopted in OBELIX design

Ref: 2024 JINST 19 C04020

Transition delay on long signal lines

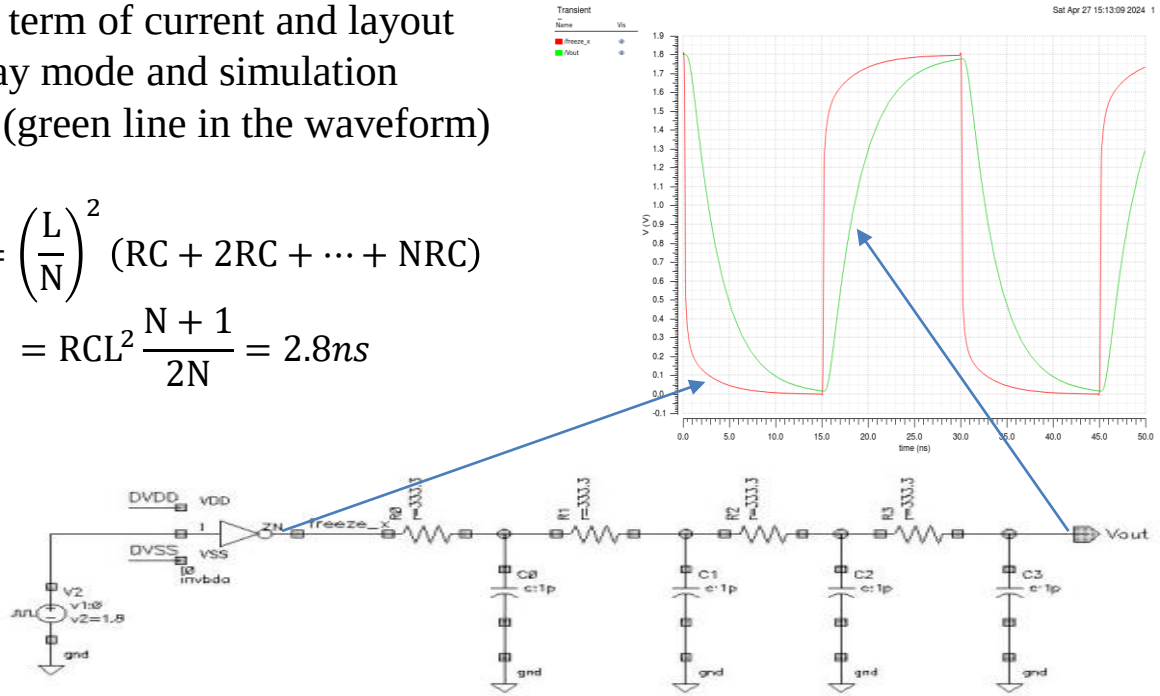
- Control lines
  - Driven from outside of pixel matrix
  - Buffering with large cells in term of current and layout
  - Verified with ELMORE delay mode and simulation
  - **Fast transition time ~ 3 ns** (green line in the waveform)

2 cm long metal line, C = 4 pF/cm
80 mOhm/square, line width = 0.28 um



$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (RC + 2RC + \cdots + NRC)$$

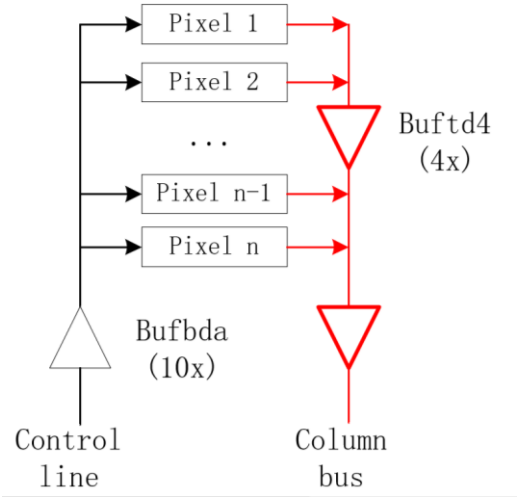
$$= RCL^2 \frac{N+1}{2N} = 2.8ns$$



circuit simulation of control lines

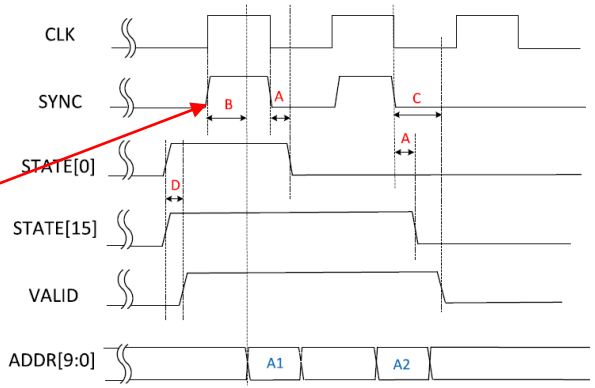
Transition delay on long signal lines

- Column bus lines
  - Driven out of pixel matrix
  - Buffering cells limited by layout area
  - Insertion of Buftd4 **improved transition time** from 58 ns to 38 ns
  - Verified by circuit simulation
- Pixel hits sent to end of column at this speed



JadePix-5 simulation results on ADDR[0]

Delay name	Delay time
D	9.8 ns
B	58→38 ns
C	8.3 ns
A	18.8 ns



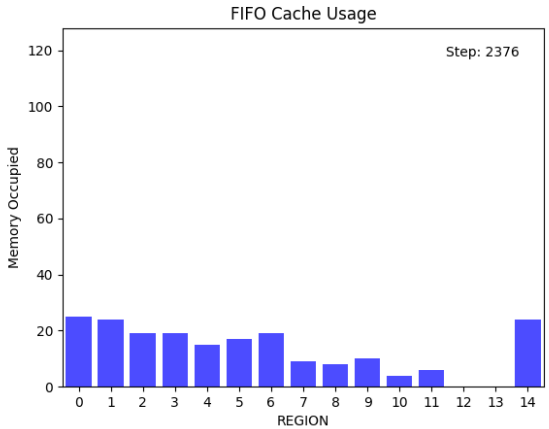
Readout timing diagram of the AERD
Ref: NIMA 785 (2015) 61-79

SRAM block size

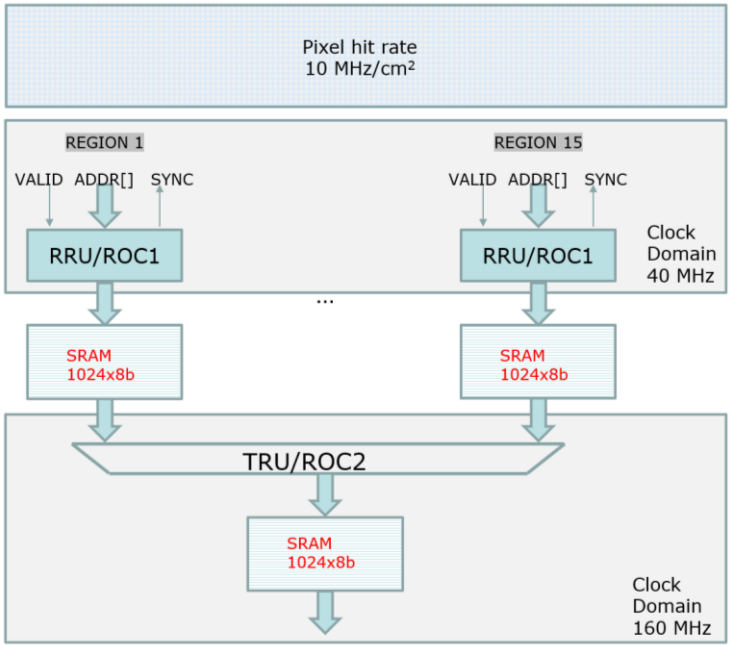
- 15 SRAM blocks, as data buffer, receive **hit information** from pixel matrix
  - Poison distribution in time, 10 MHz hit/cm^2 on average
  - Evenly distributed in position
  - Each 1024×8b SRAM handle one matrix region

  (16 double-columns each region)
  - Numerical simulation results:

  Maximum usage < 30, Average usage 6



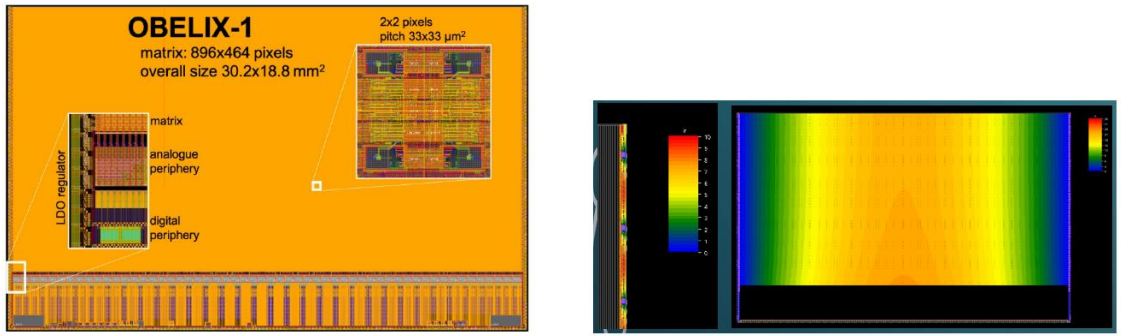
Typical SRAM usage at 10 MHz/cm^2 hit rate



Peripheral readout circuit (block diagram)

Digital on Top integration flow

- There is a gap in terms of design methodology
  - IPHC team: **more advanced** Digital on Top flow is in regular use
  - IHEP team: **traditional** Analog on Top flow with digital implemented blocks
- Common interests for IHEP team to participate the **simulation and verification** of OBELIX design
  - Static Timing Analysis, supply voltage distribution, Power Analysis …
  - Work together will help fill the gap both in terms of methodology and expertise



OBELIX floorplan and IR drop simulation of the matrix without regulator
Ref: 2024 JINST 19 C04020

Summary

- Common R&D efforts of monolithic CMOS Pixel Sensor for the e^+e^- collider experiments since 2010
  - BES III upgrade, ILC/CEPC, BELLE II upgrade
- The IPHC team is a main participant of the VTX project for BELLE II upgrade, currently designing the OBELIX
  - The IHEP team is not yet a member of the VTX collaboration, but willing to work with the OBELIX design team for the preparation of next submission
- JadePix-5 will be submitted this year in a shared engineering run with IPHC team
- Common interests in addressing design challenges in terms of large area CMOS pixel sensors
  - Supply voltage distribution
  - Signal transition on long lines
  - SRAM and low power design
  - Verification with digital flow tools
- Plan to visit Strasbourg in Nov. this year

Thank you for your time!