MAPS-based Upstream Tracker for LHCb upgrade phase II

France China Particle Physics Laboratory

Manuel Guittière
Subatech, Nantes

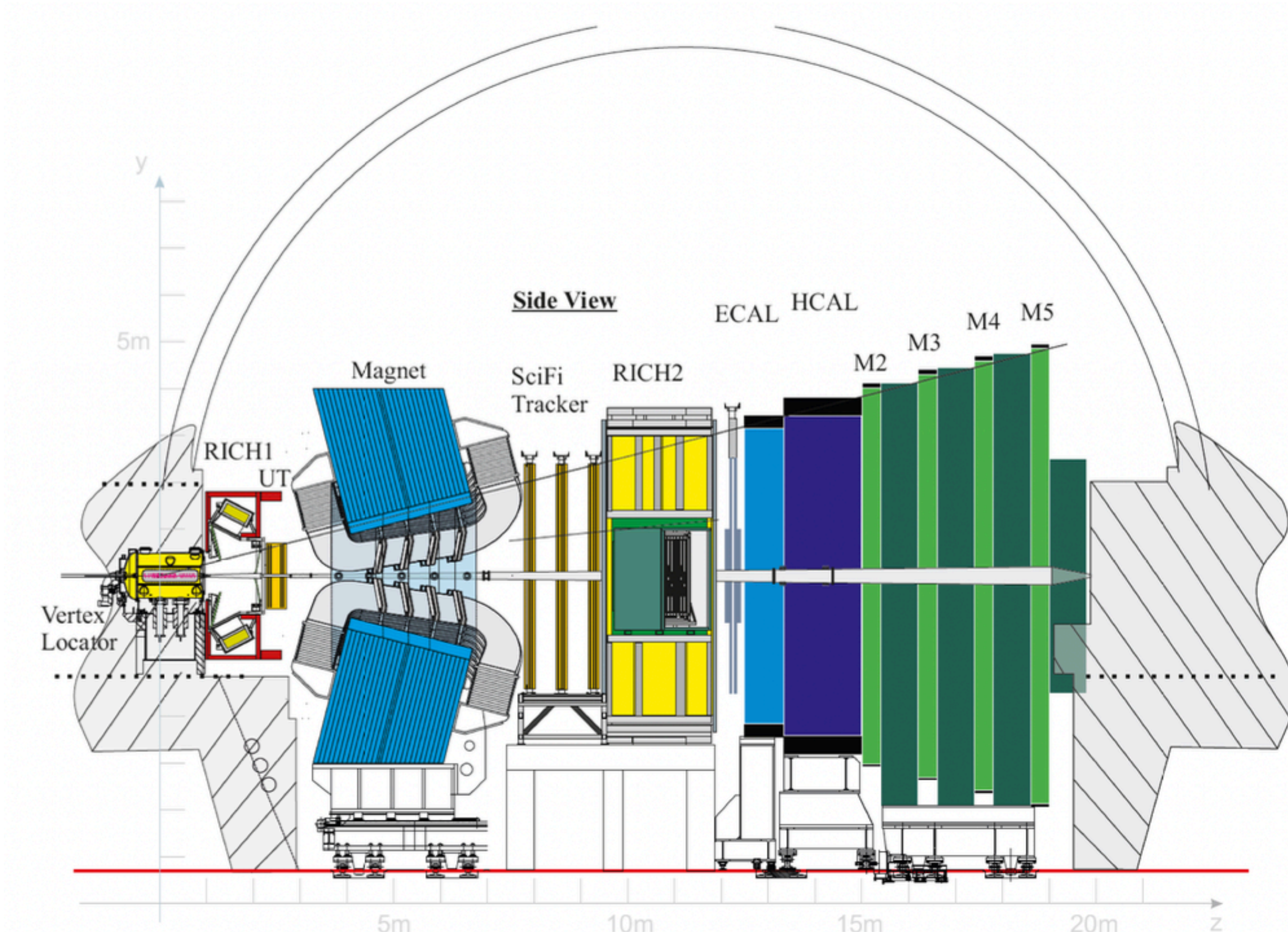
Contact: manuel.guittiere@subatech.in2p3.fr, manuel.guittiere@cern.ch

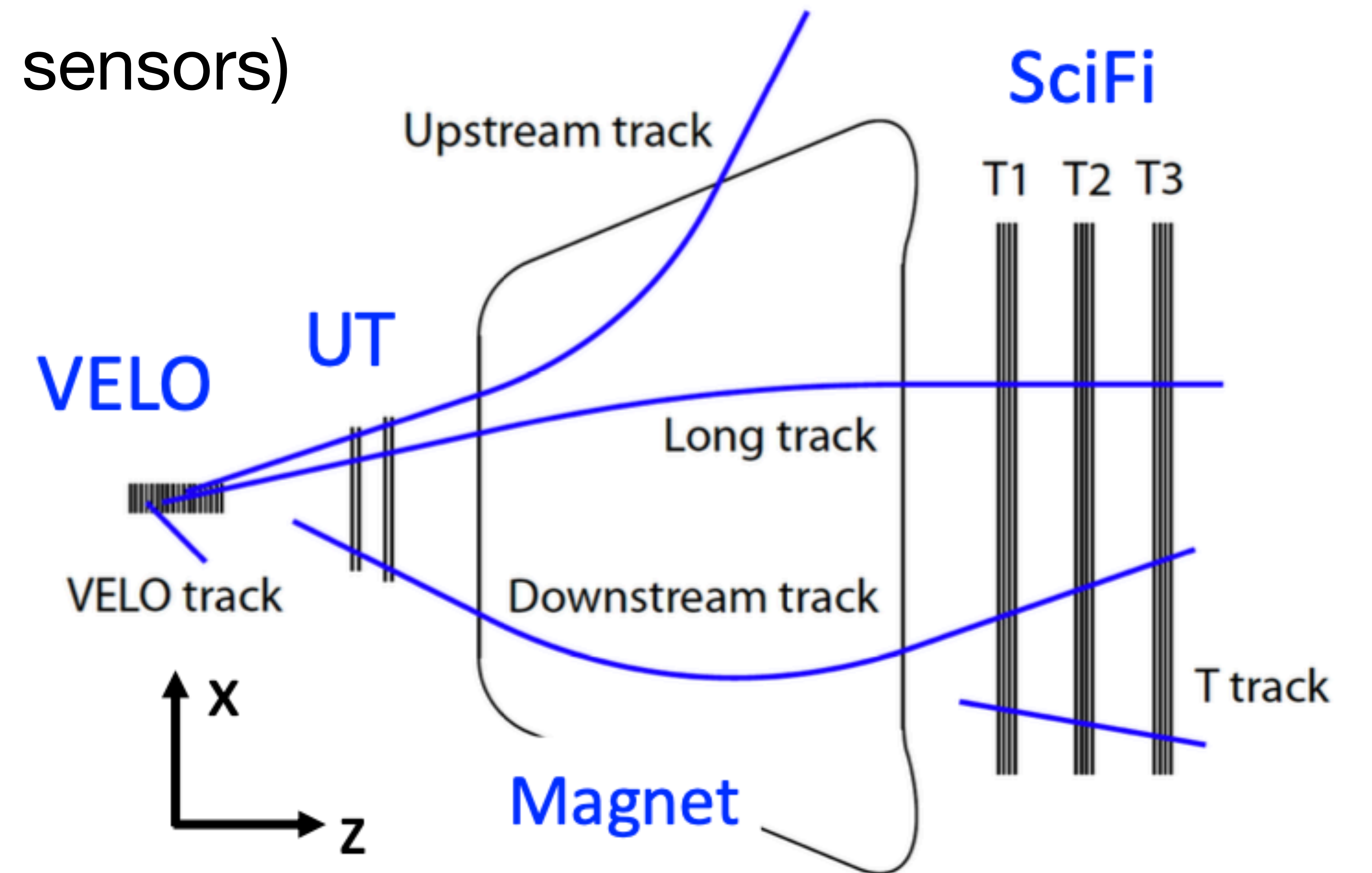
15th FCPPN/L workshop, Bordeaux - 11/06/2024

LHCb tracking at Run 3-4 (Upgrade I)

LHCb: Single-arm spectrometer dedicated to heavy flavor studies at LHC

- Upgrade phase I completed in March 2023: $2x10^{33}$ $cm^{-2}.s^{-1}$ (x5 w.r.t Run 2)
- Tracking with LHCb UI: VELO (CMOS pixel ASICs) + UT (silicon-strip sensors) + SciFi (Scintillating Fibers)

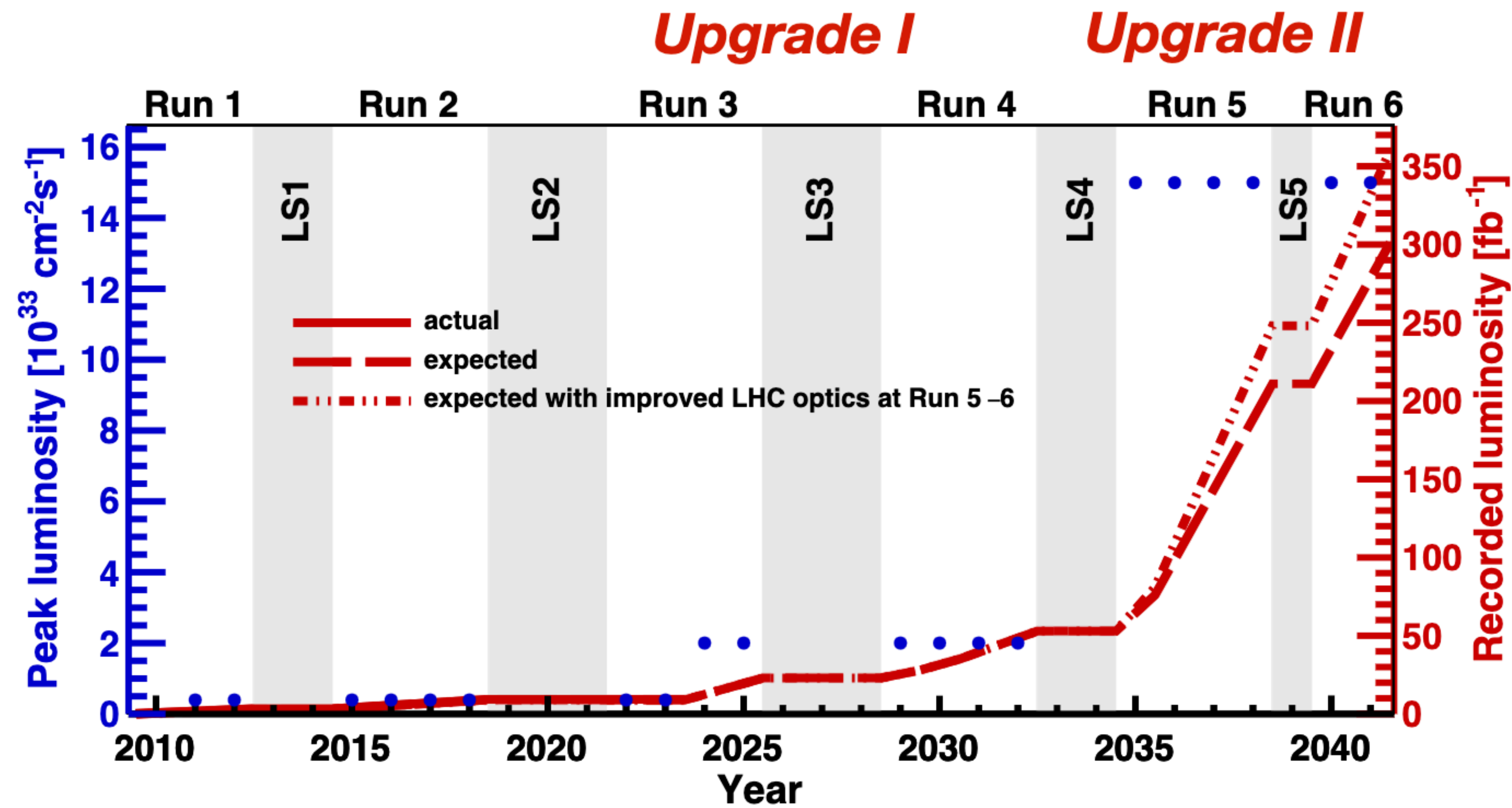


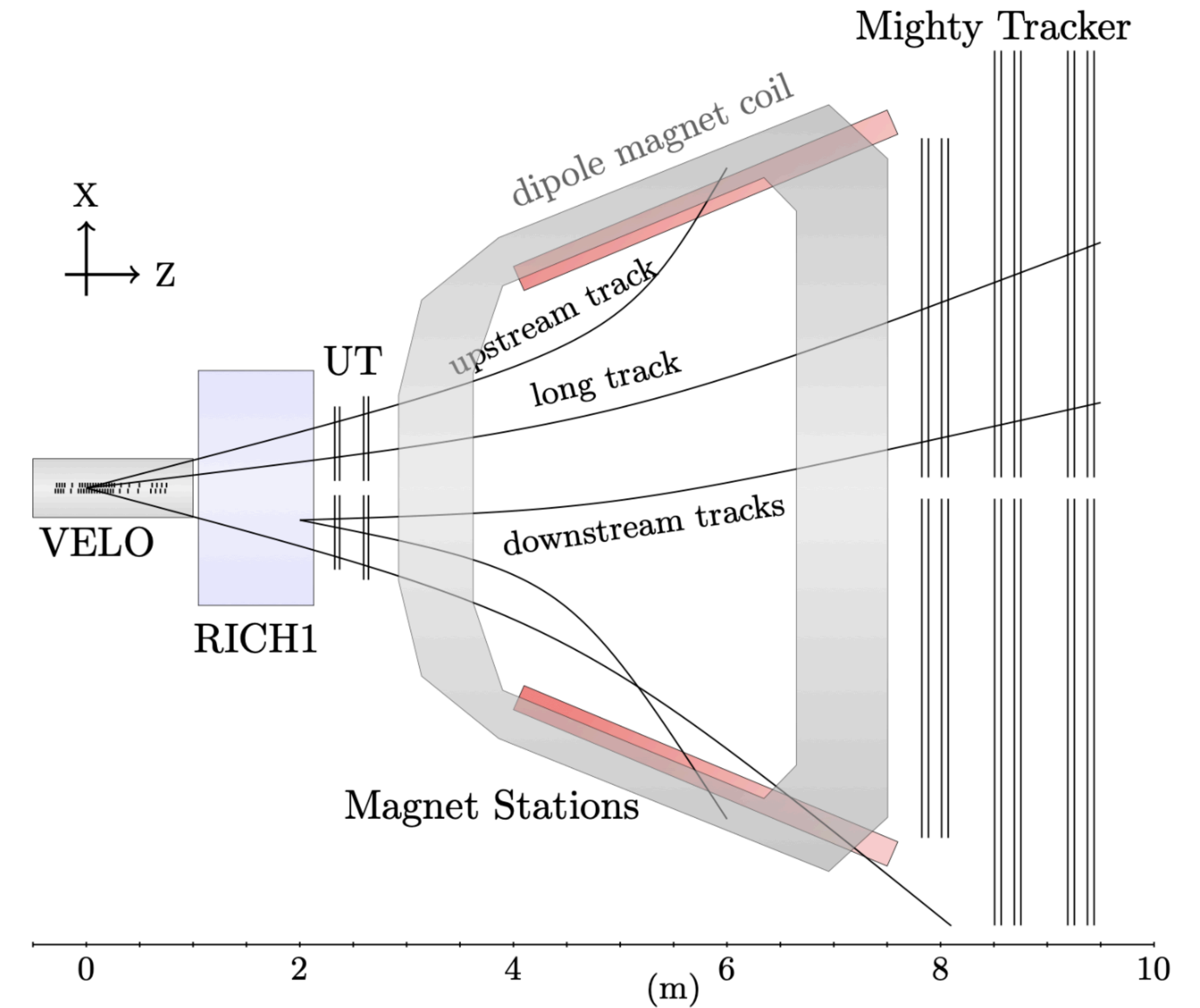


Upstream Tracker (new detector) is essential to:

- Speed-up and strengthen VELO-SciFi matching
- Reduce the ghost rate
- Reconstruct long-lived particles

LHCb tracking at Run 5 (Upgrade II)





HL-LHC era:

- Aim at inst. luminosity of **1.5 x 10^{34} cm^{-2}s^{-1} (x8 w.r.t Run 3-4)**
- Expected accumulated luminosity **~300 fb-1** (end of LHC operations)
  - ↗ **pile-up**: 1 → 5 (UI) → **40** (UII)
  - ↗ **multiplicity** (high occupancy)
  - ↗ **radiation damage**

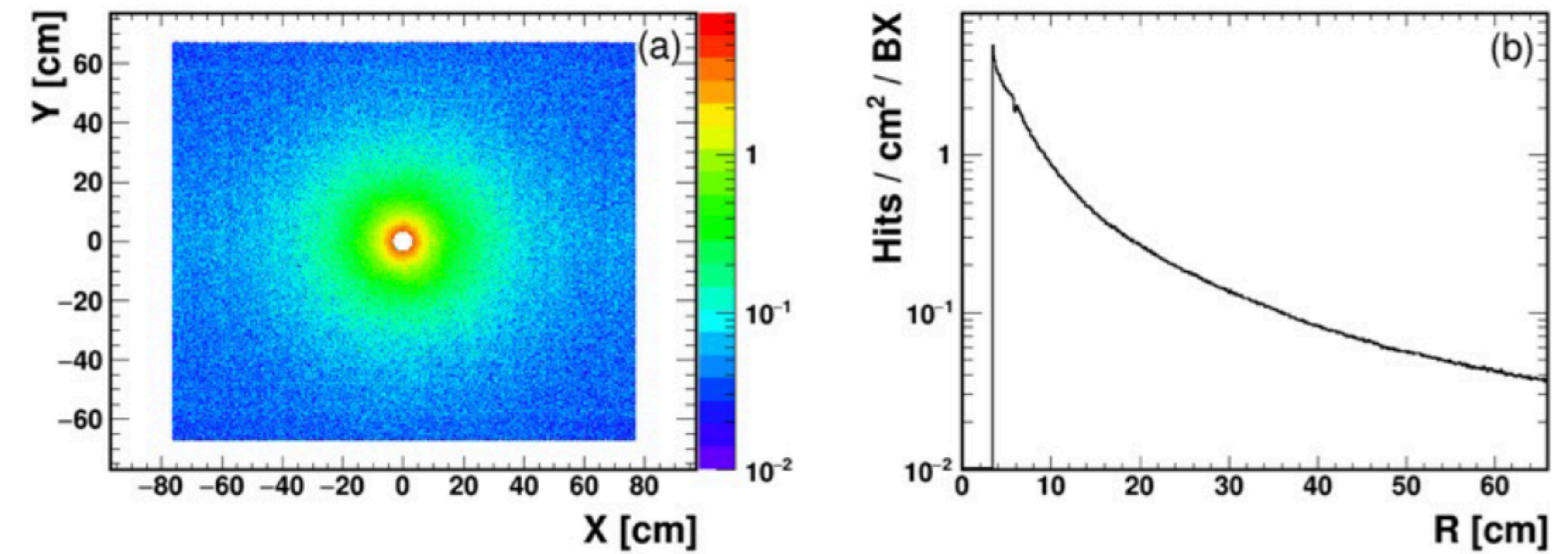
Current detectors cannot operate safely in HL-LHC conditions

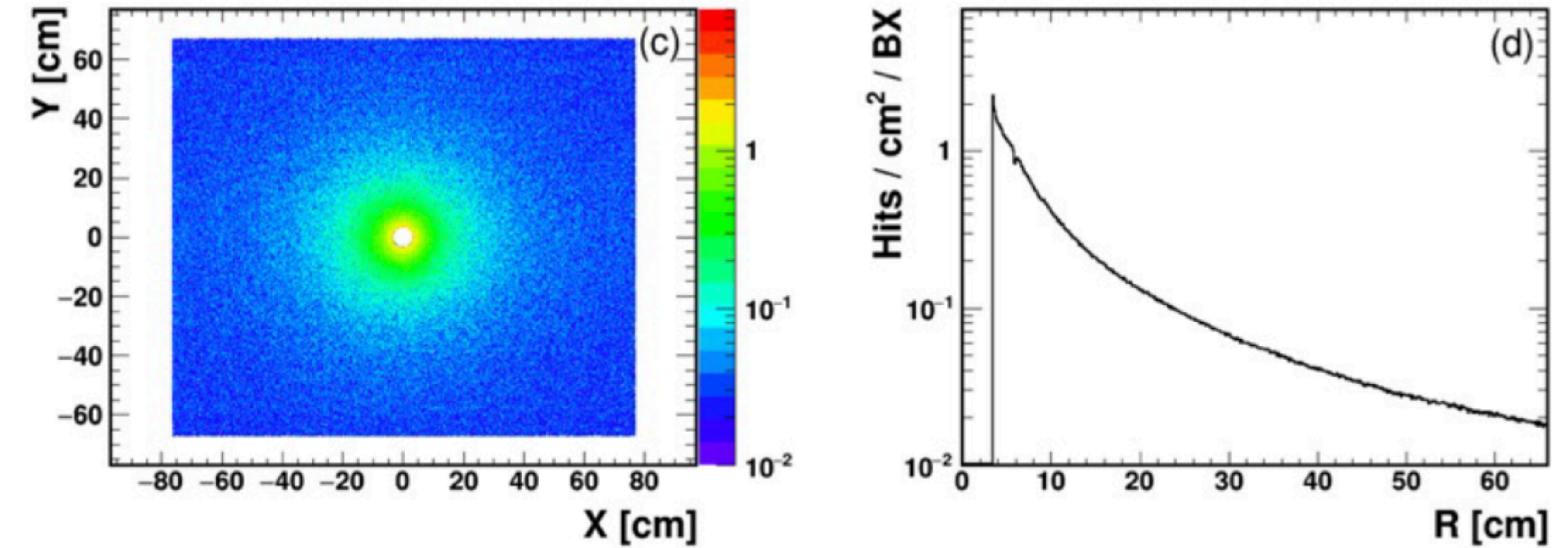
➡ **New design/technologies required**

LHCb tracking at Run 5: Upstream Tracker

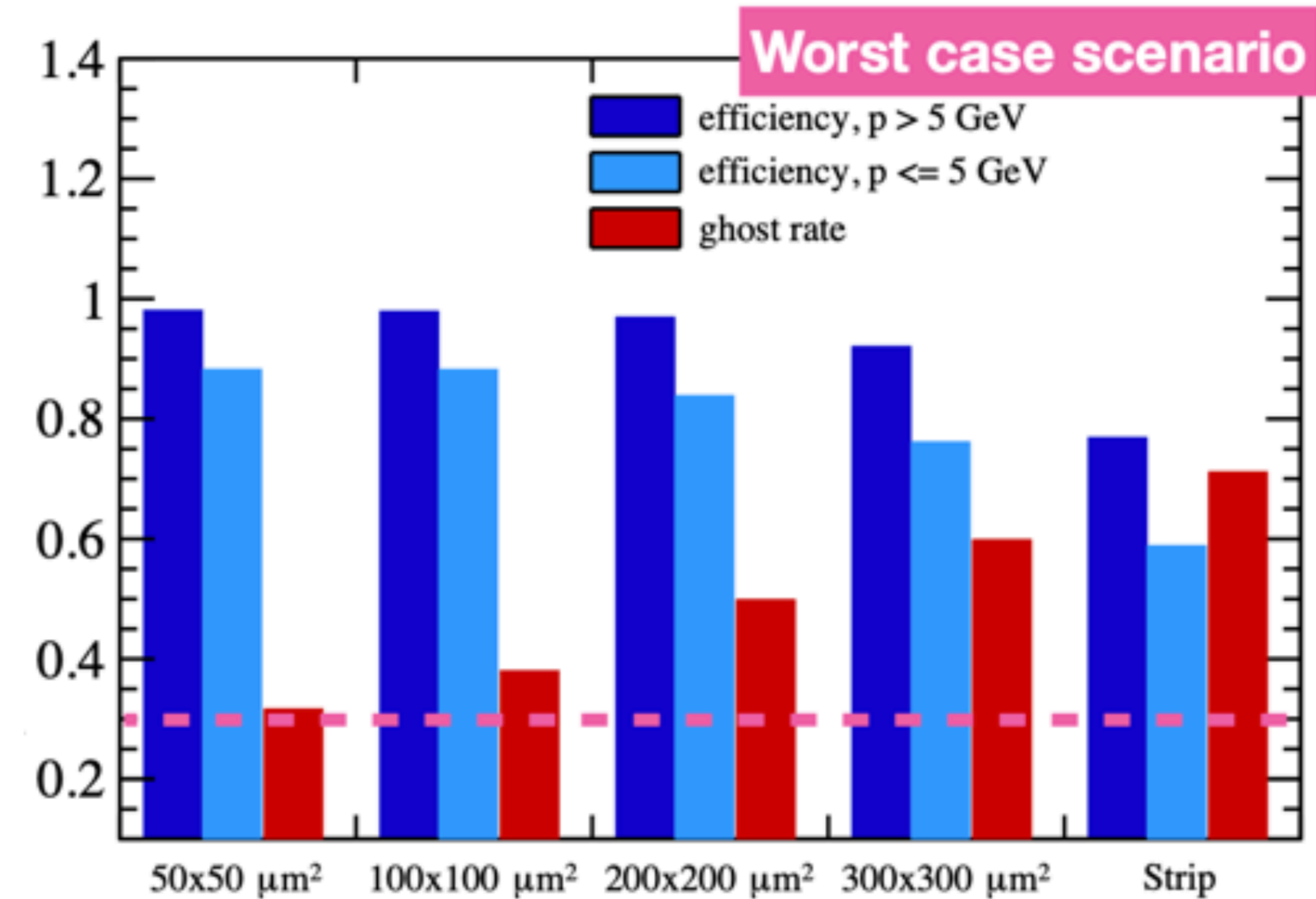
Characteristics	Specification
Hit rate in hot event and region	160 MHz / cm^2 pp (~52.5 hits / cm^2 / BX for Pb/Pb)
Time resolution	O(1 ns) for BX tagging
Pixel size	O(30×30 μm^2) or (100×300 μm^2)
Power consumption	O(100-300 mW/cm^2)
Radiation dose for 350 fb^{-1}	3×10^{15} 1-MeV n_{eq}/cm^2, 240 Mrad

Hit rate



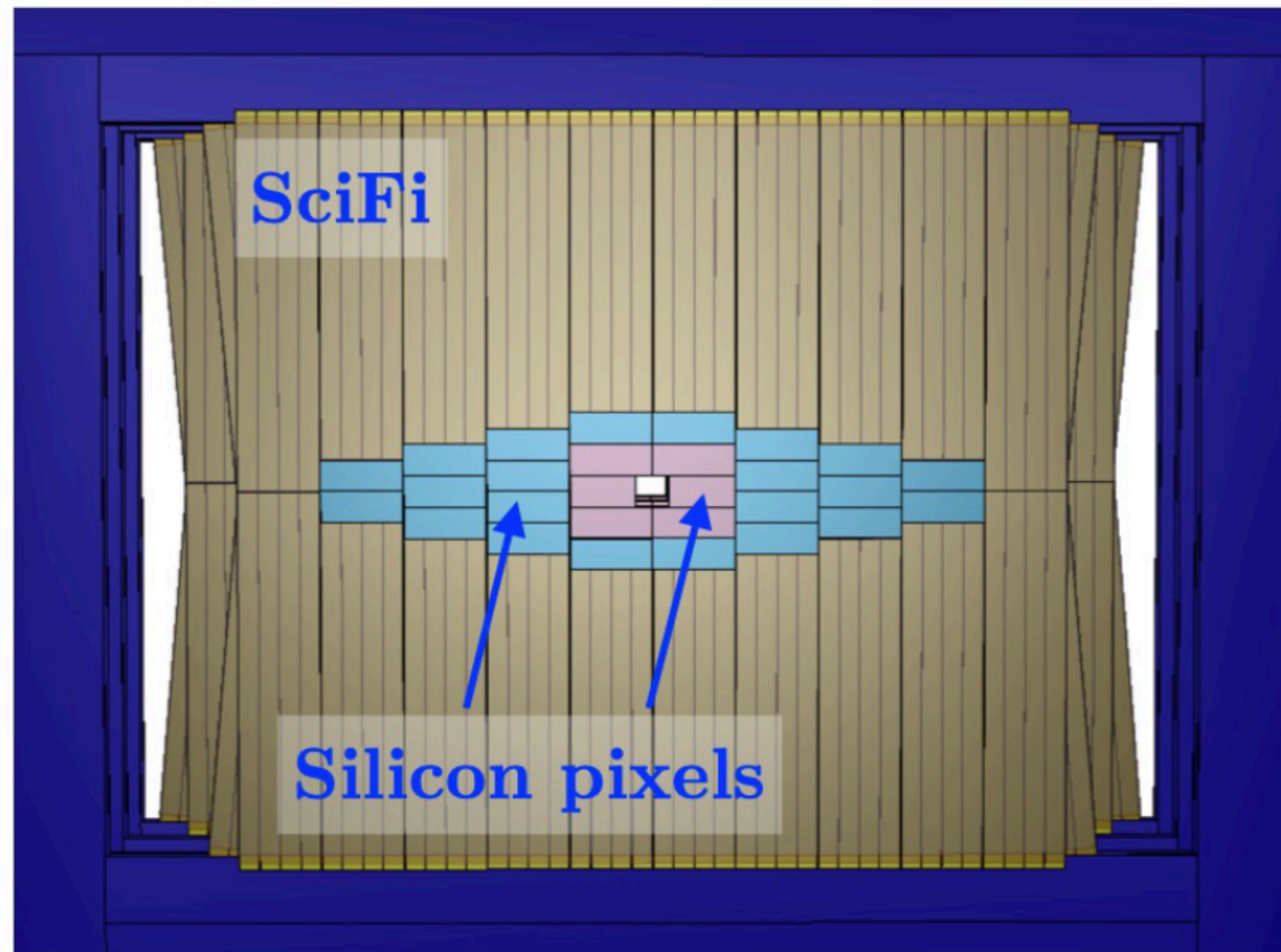


Ghost rate

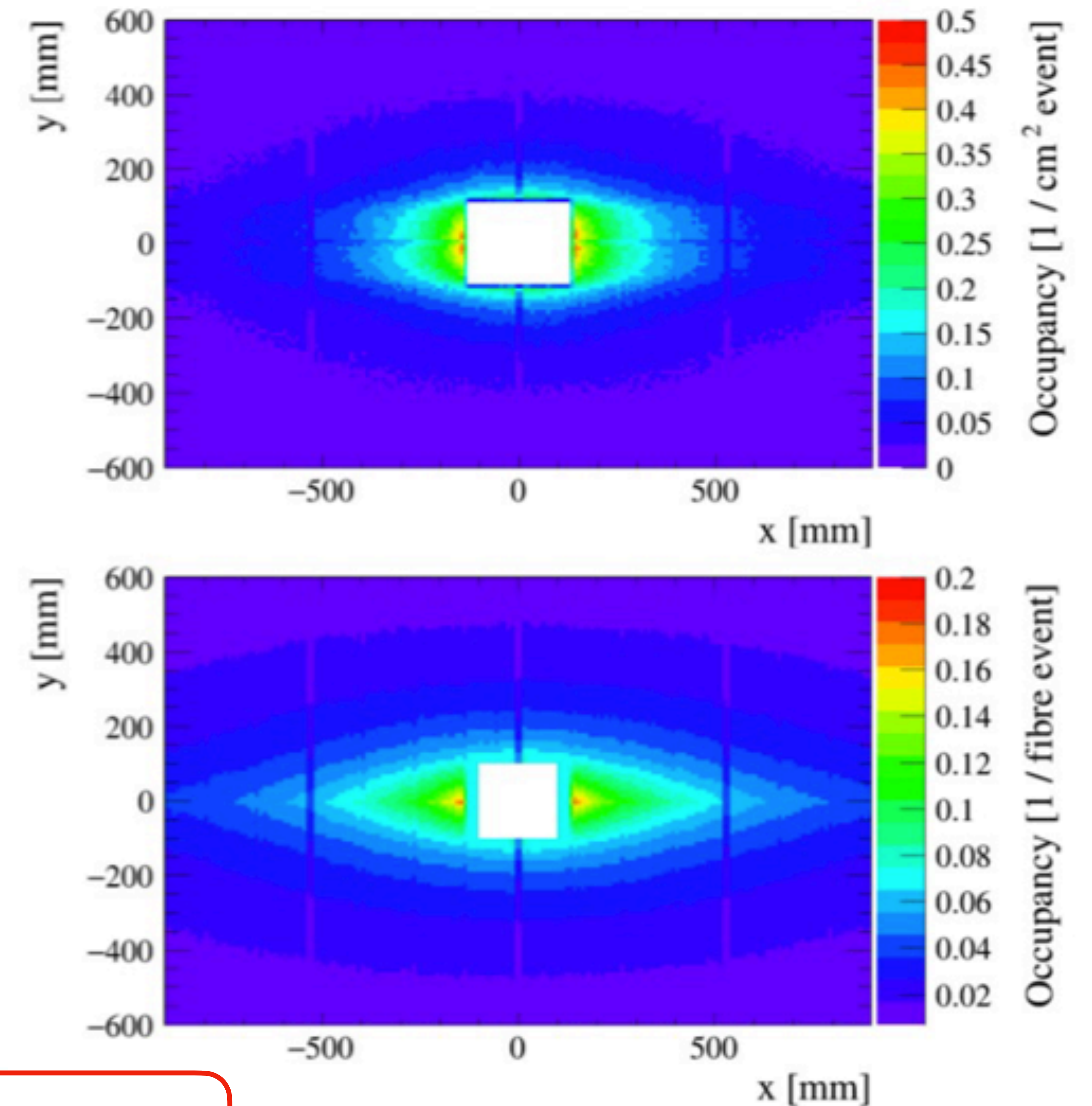


LHCb tracking at Run 5: Mighty Tracker

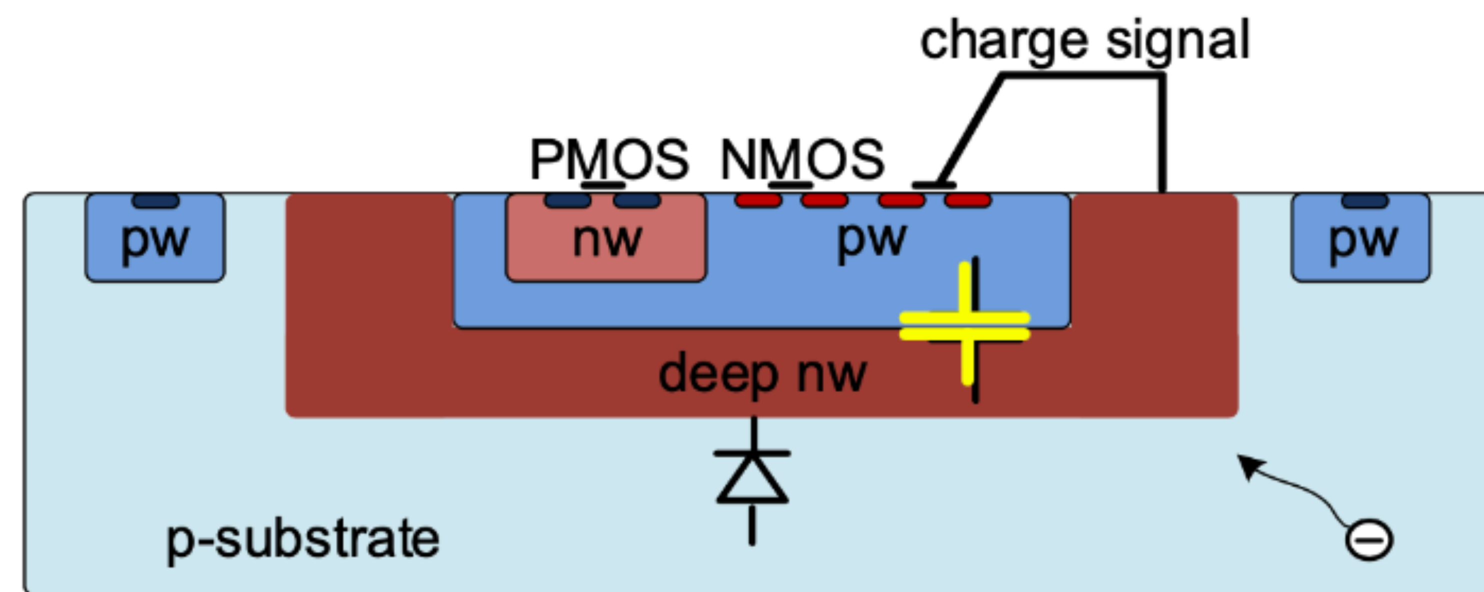
- $\int \mathscr{L} = 300\text{fb}^{-1}$ ⇒ significant fibre radiation damage in inner region
- $\mathscr{L}_{\text{inst}} = 1.5{\times}10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}$
  ⇒ very high occupancy (up to 20%/fibre/event)
  ⇒ SciFi must be replaced near beam pipe to maintain the same (or better) tracking performance
- Solution: instrument the inner region with a pixel detector, while keeping scintillating fibres in the outer region



Inner + Middle + SciFi Tracker
=
Mighty Tracker

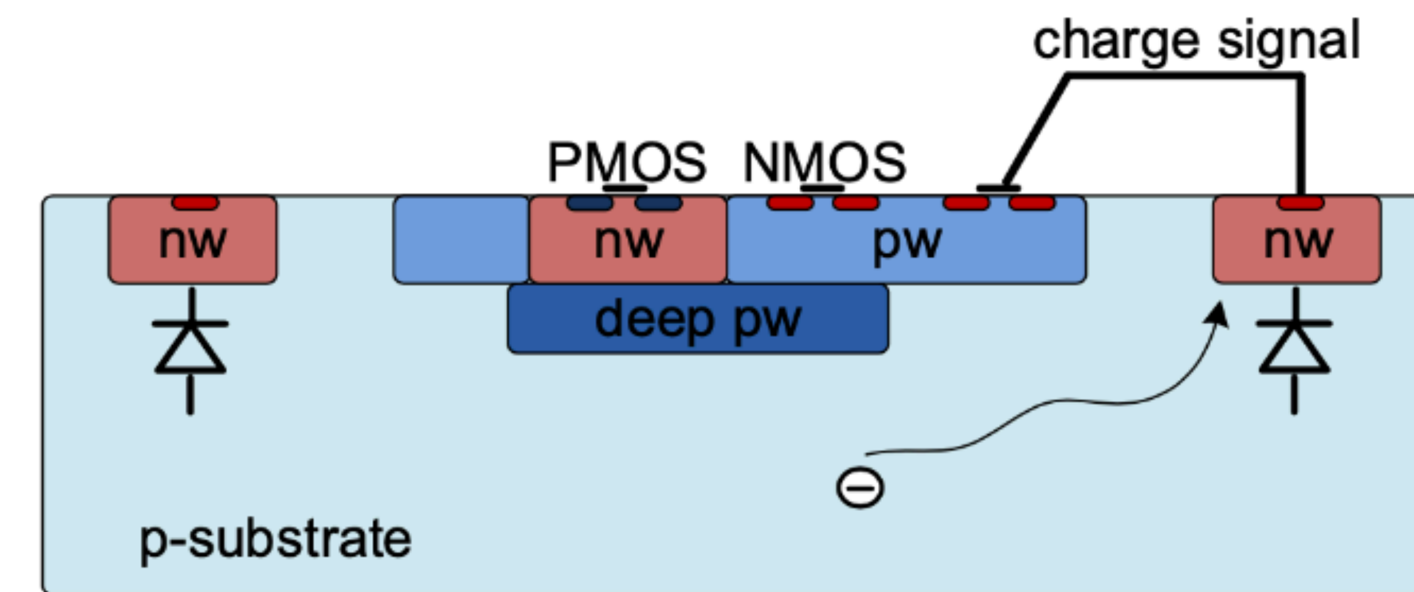


MAPS sensors R&D: 2 CMOS families



Large collection electrode

- Typical pixel size: 50 x 150 μm^2
- Circuitry inside the collection well (requires high field: “HV-CMOS”)
- High radiation hardness
- Higher noise (high capacitance)
- Higher power consumption
- Possible cross-talk (digital to sensor)



Small collection electrode

- Typical pixel size: 30 x 30 μm^2
- Circuitry outside the collection well (requires low/moderate field: “LV-CMOS”)
- High radiation hardness thanks to process modification (increase of depletion zone)
- Lower noise (low capacitance)
- Lower power consumption
- Less sensitive to cross-talk

Several parallel R&D on CMOS sensors

	UT	MT
Pixel size	$< 50 \times 50\ \mu m^2$	$< 100 \times 300\ \mu m^2$
Space resolution	$5\ \mu m$	$< 10\ \mu m$
In-time efficiency	$> 99\%$ within 25 ns	$> 99\%$ within 25 ns
Time resolution	O(1 ns) for BX tagging	few ns for BX tagging
Radiation dose	3.10^{15} 1 MeV n_{eq}/cm^2, 240 Mrad	6.10^{14} 1 MeV n_{eq}/cm^2
Maximum data rate	4.5 Gb/s (without ToT in data) 160 MHz/cm^2 (6 hits/BX/cm^2 in pp)	2 Gb/s (with ToT in data)
Power consumption	100-300 mW/cm^2	< 150 mW/cm^2

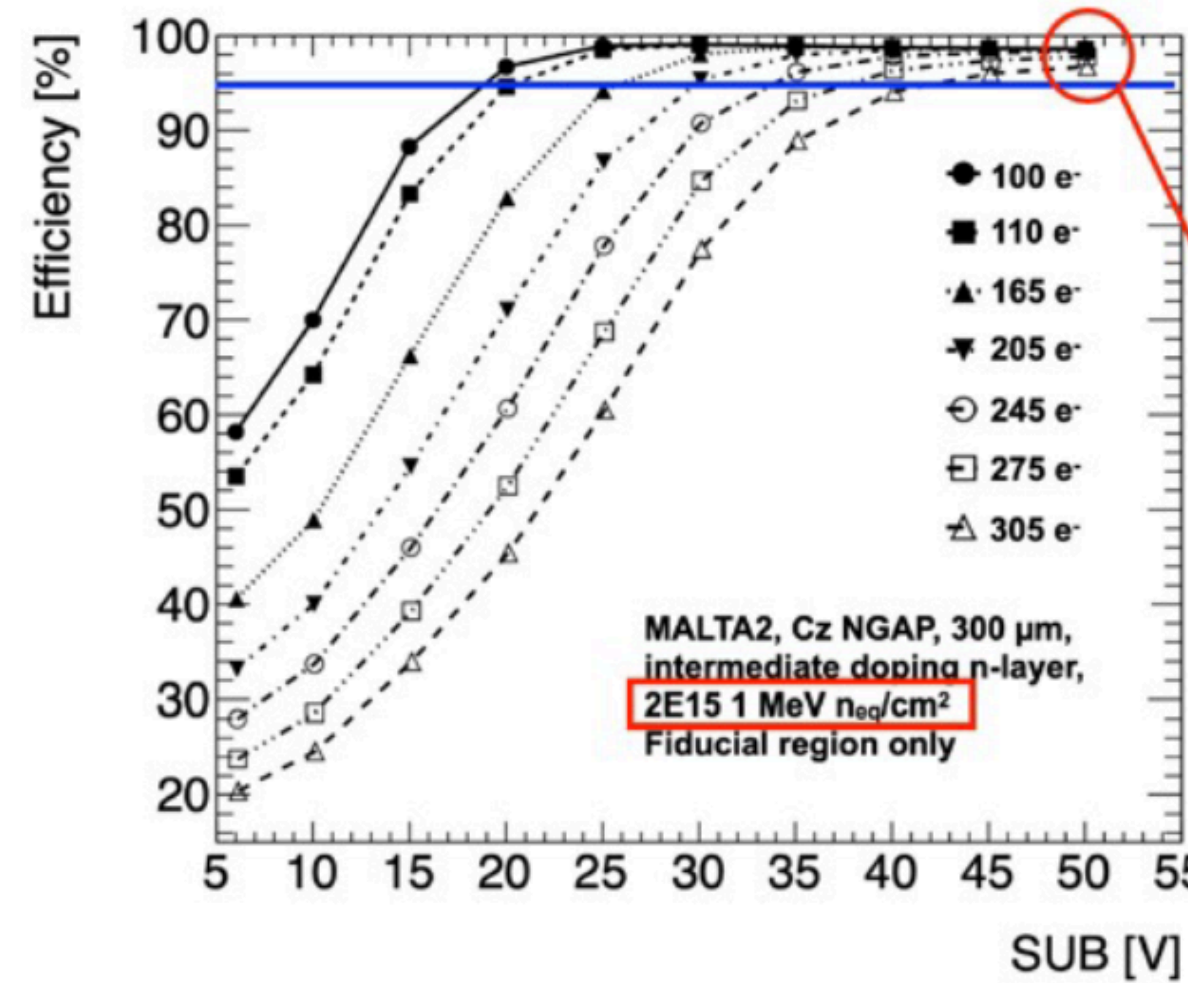
Technology	Small pixel (LV-CMOS)	Large pixel (HV-CMOS)	Sensor
TowerJazz 180 nm	X		MALTA
AMS/TSI 180 nm		X	MightyPix
TPSCo 65 nm	X		SPARC
SMIC 55 nm		X	COFFEE

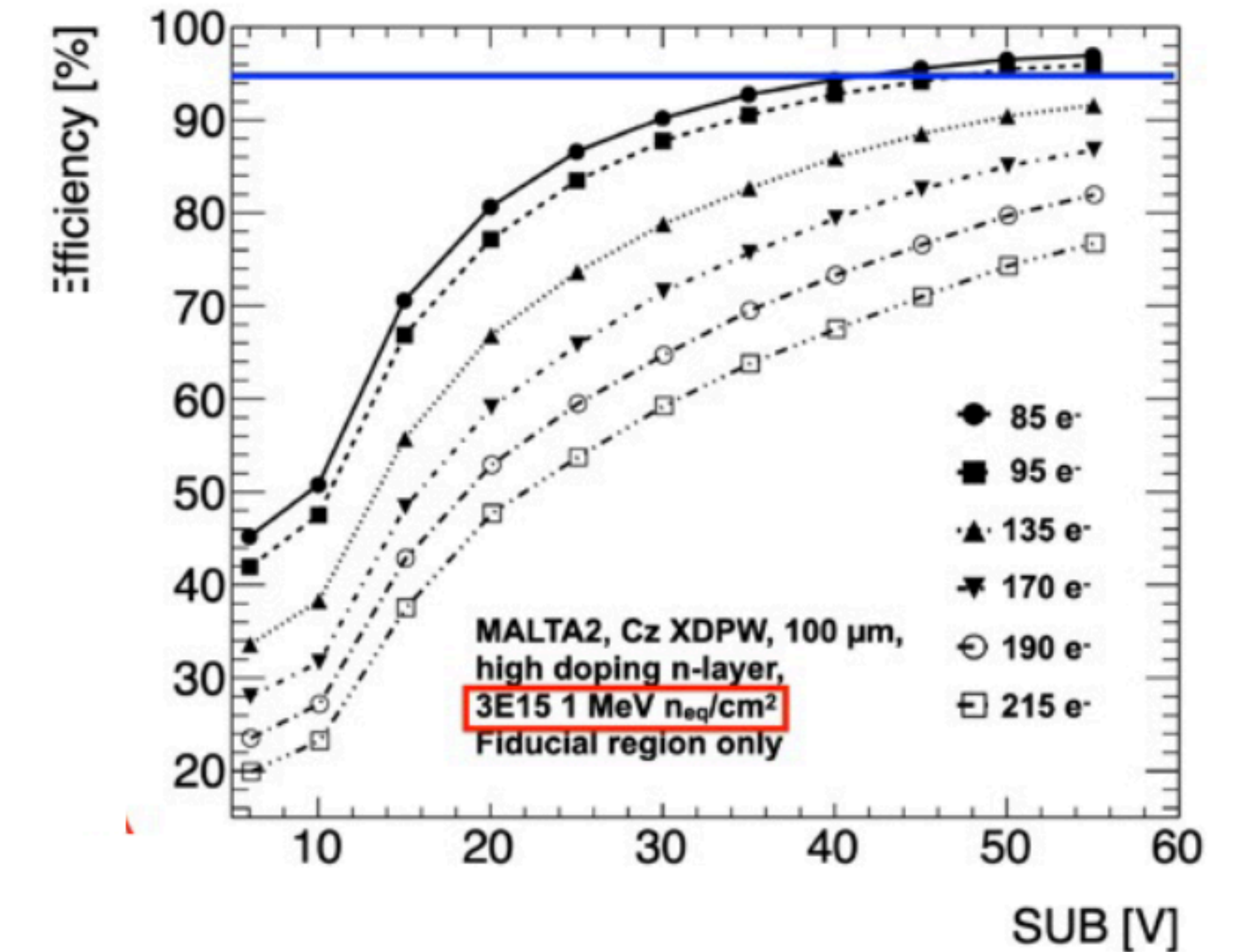
- **More stringent requirements for UT sensors**
  - ➡ Candidate matching UT specs will fulfill MT ones
- **Wish to use same sensors for both UT and MT** (cost and complexity optimisation)
  - ➡ UT-MT synergy in MAPS-based R&D

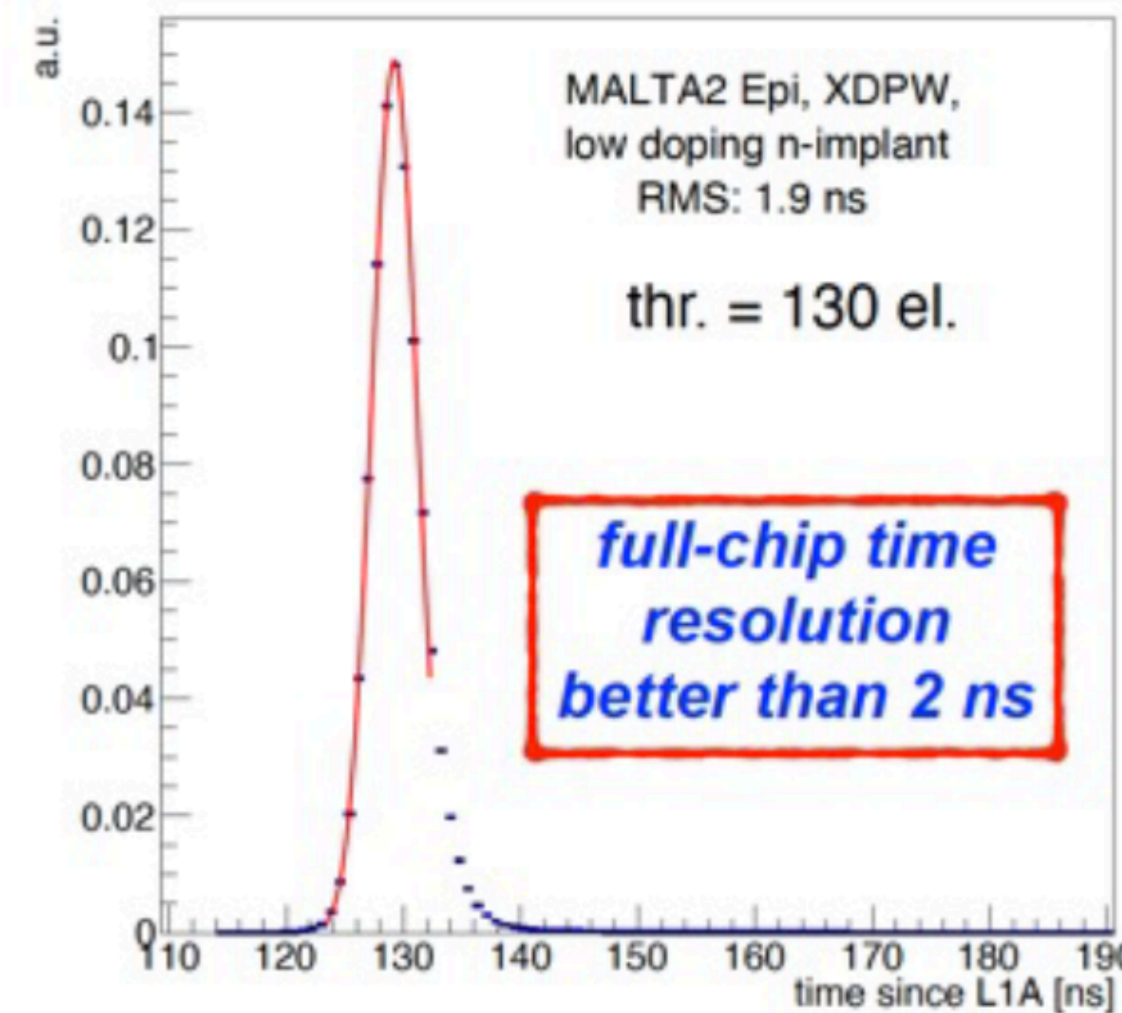
MALTA - TJ180

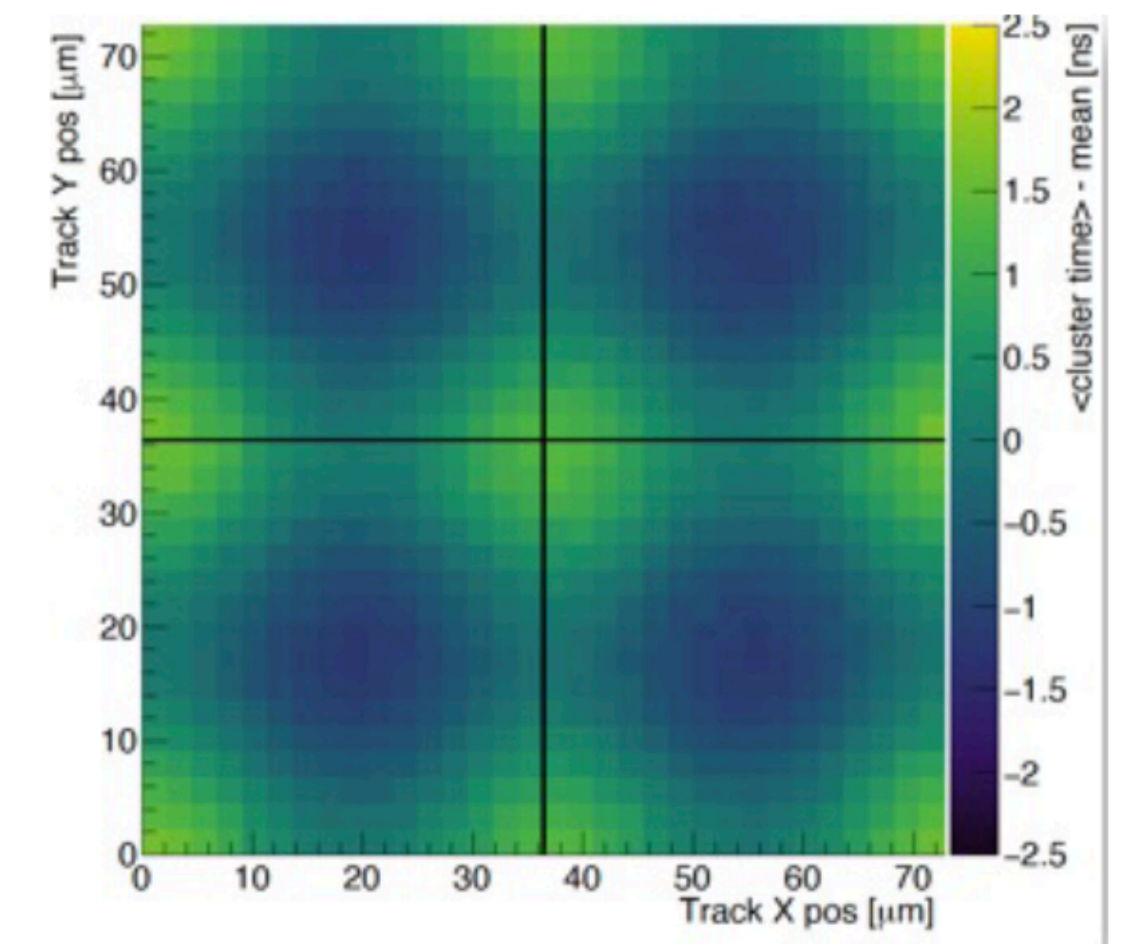
S. Panebianco

- Existing chip in well proved technology and extensively qualified
- Present version is MALTA3
  - Ongoing chip testing and qualification (in lab and on test beams for irradiated and not irradiated chips)
- Present performances:
  - Position resolution: ~ 5 μm
  - Time tagging (without ToT): fully efficient in 25 ns
  - Power consumption: ~ 90 mW/cm^2
  - High efficiency (>95%) for a dose rate of 3x10^{15} 1 MeV n_{eq}/cm^2 (but cooled down to -20 °C)
- Development of LHCb-oriented readout periphery blocs to cope with the high data rate
  - Virtual pixel: cluster or group of pixels
  - Creation of the building blocks of a generic data compressor







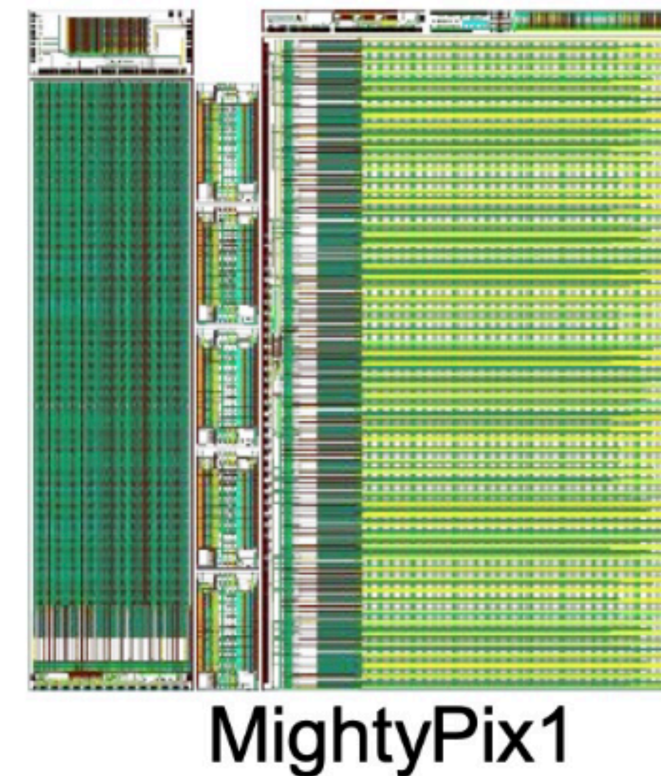


MightyPix - AMS180

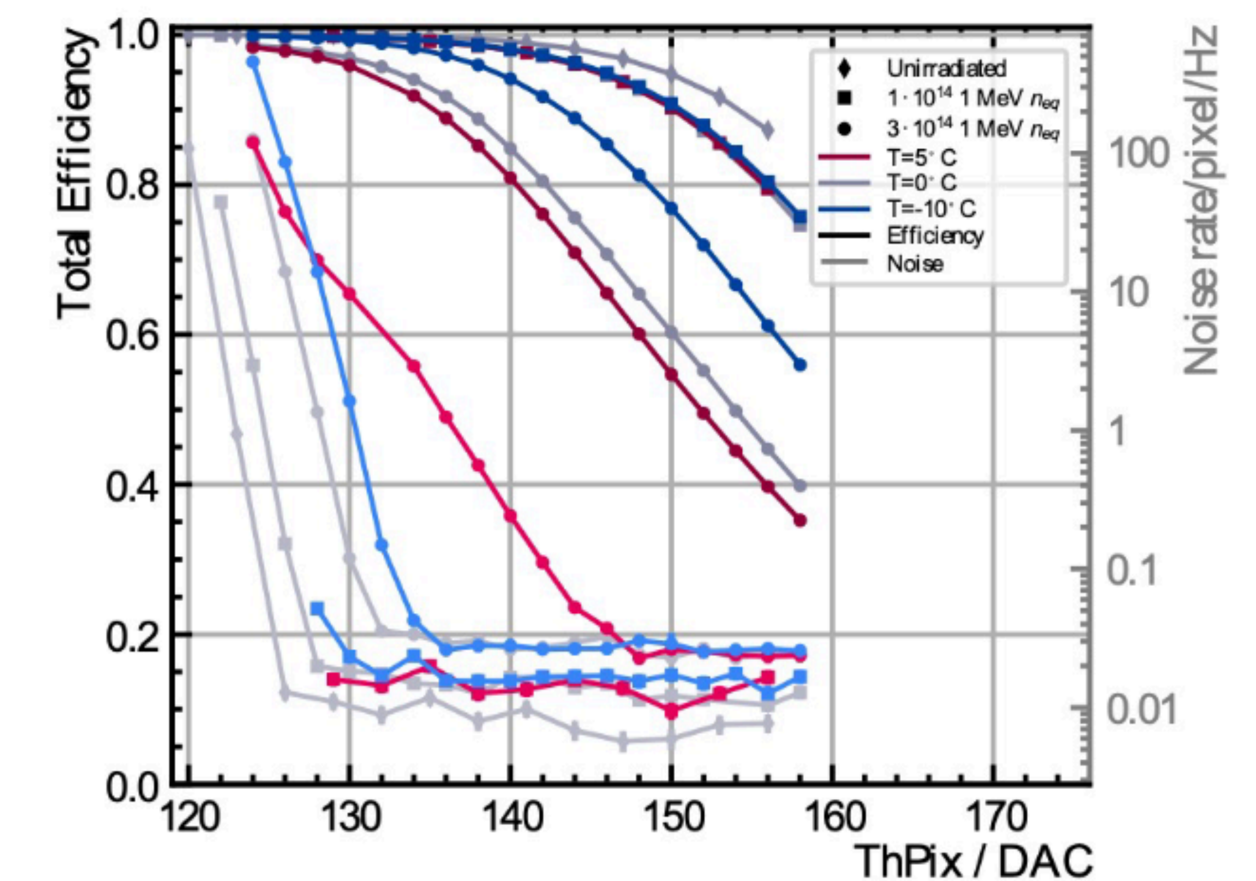
S. Panebianco

LHCb

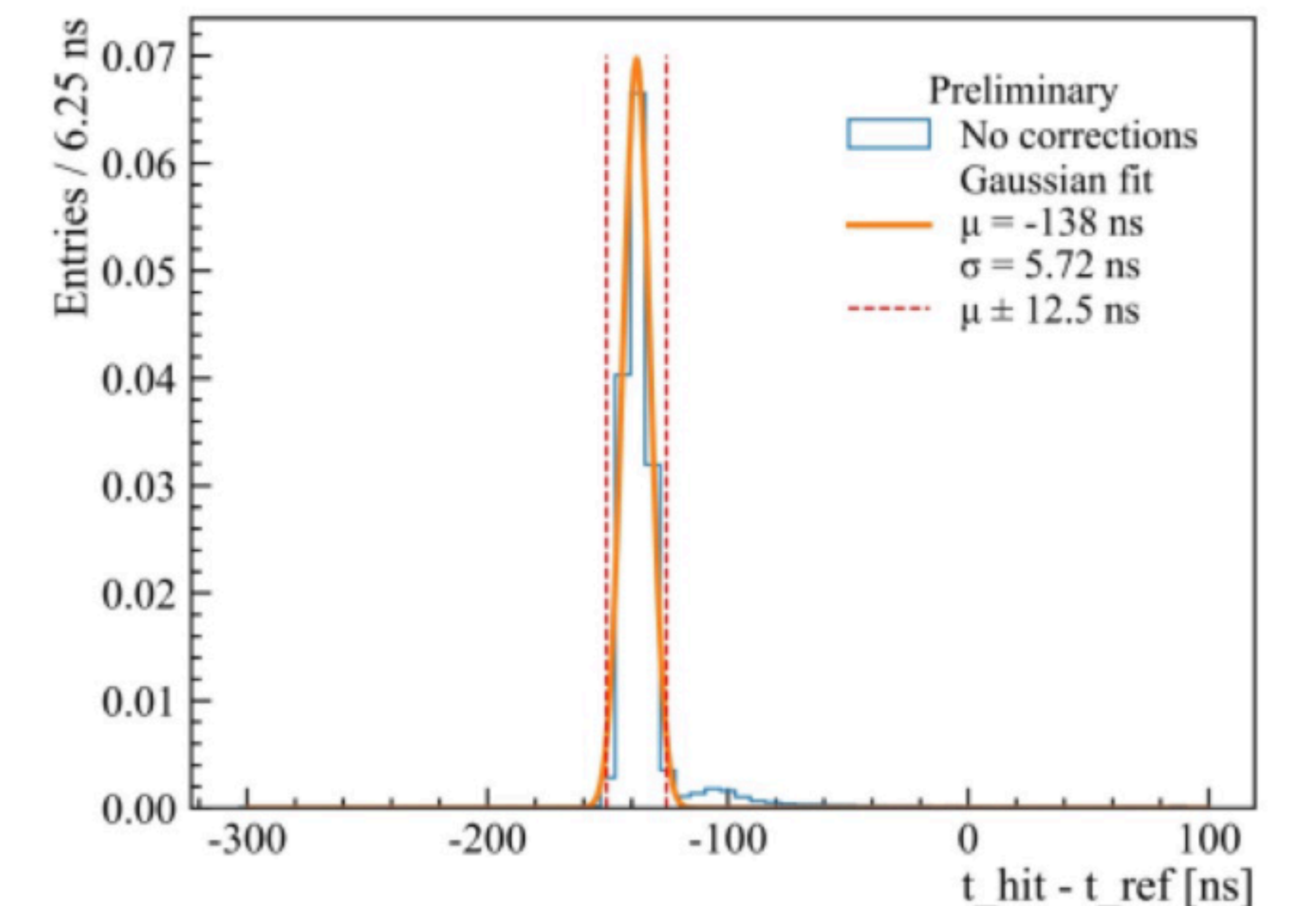
- Existing chip in well proved technology and extensively qualified
- Present qualified version is MightyPix1
  - Production in TSI180 is stopped
  - Redesign in AMS180
  - Possible design in LF150
- Very encouraging results from MightyPix1
  - Position and time resolution
  - Power consumption: 56 mW/cm^2
- The present design does not meet the UT specs in terms of data rate and radiation dose



MightyPix1



Radiation hardness tests

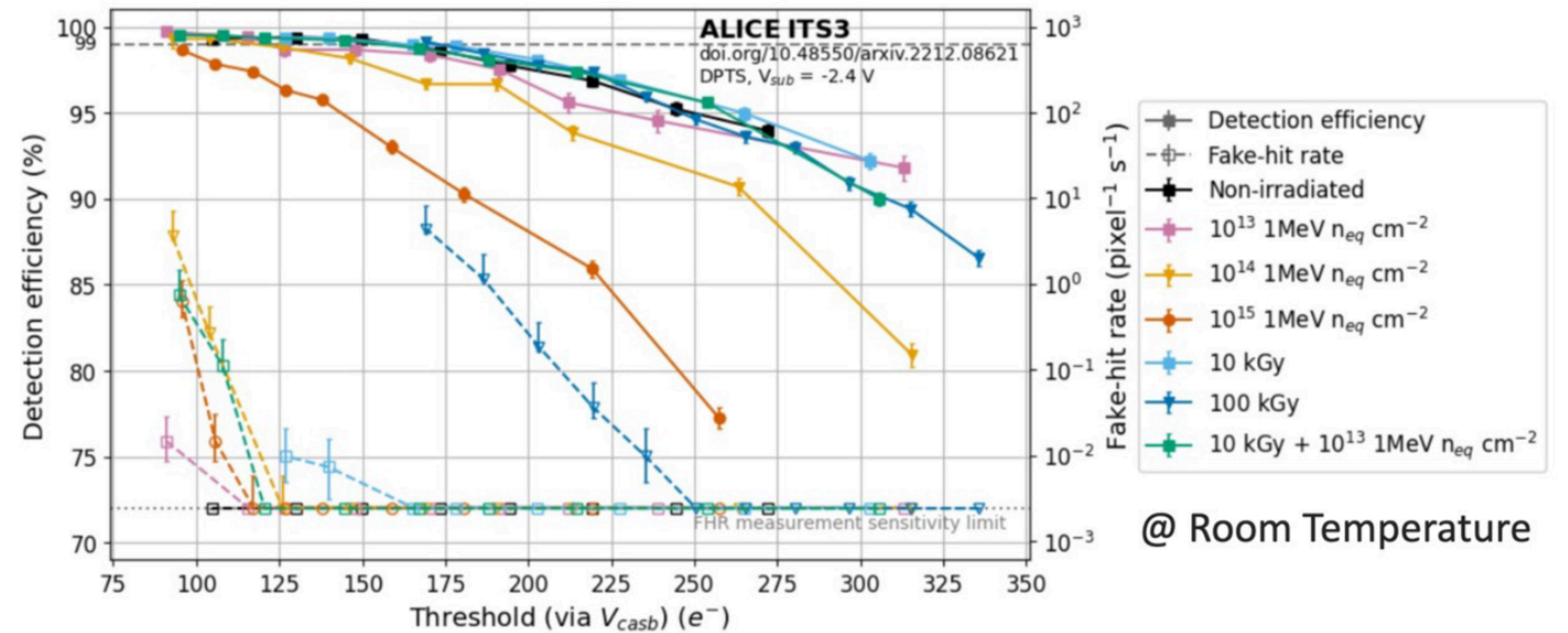


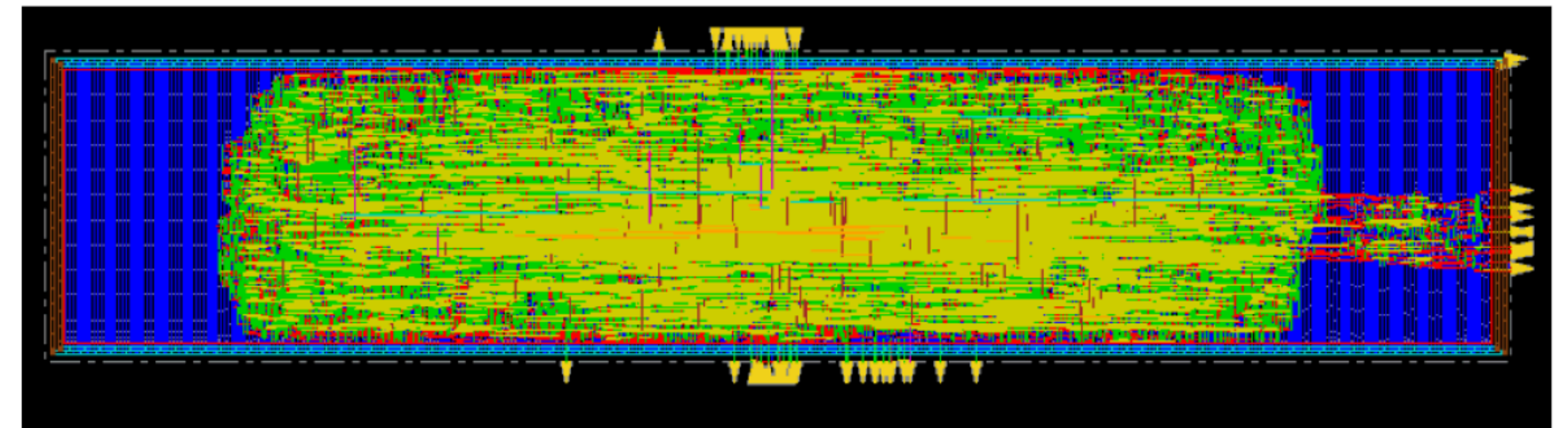
Time resolution of MightyPix1 (preliminary)

SPARC - TPSCo65

S. Panebianco

- New and challenging technology for MAPS
- Very encouraging results within ALICE-ITS3 project
  - High efficiency (>95%) for a dose rate of several 10^{15} 1 MeV n_{eq}/cm^2 (at room temperature!)
- Ongoing collaboration between IPHC (Strasbourg) and Irfu (Saclay) on the development of digital blocks of readout periphery (as for MALTA)
- Development of a TV for ER2 (2024) to assess TPSCo 65nm radiation hardness + in-chip time tagging investigation
- MLR2 for a second prototype in 2025.





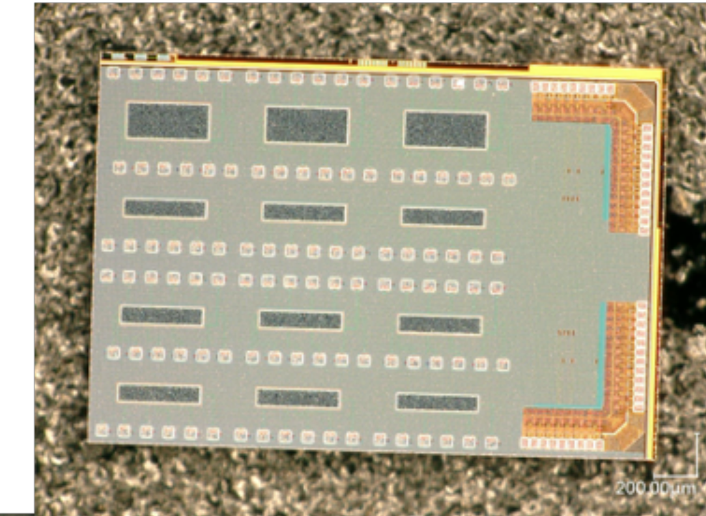
FIFO memory in 65 nm designed at Irfu for SPARC

COFFEE - SMIC55

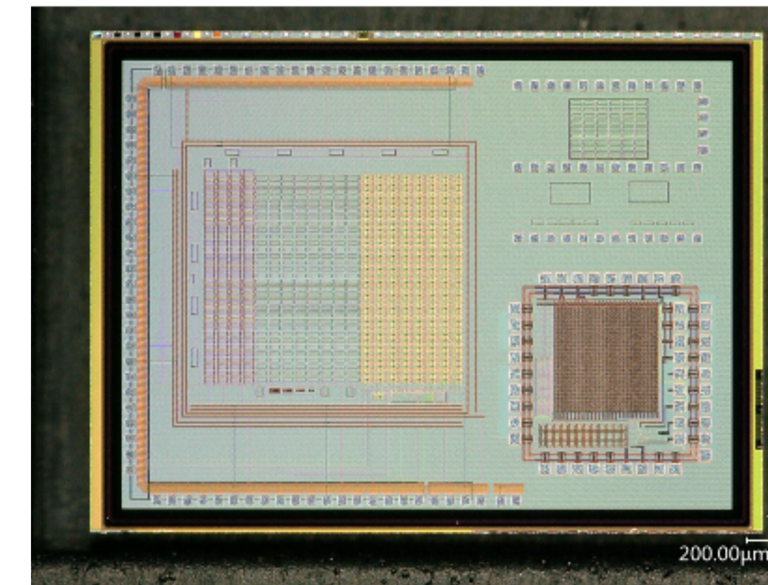
Y. Li

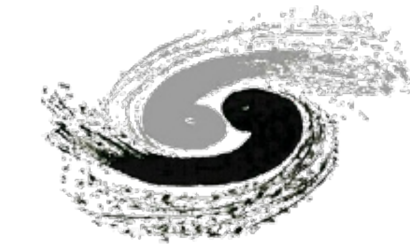
- SMIC 55nm Low-Leakage process
  - Not HV, yet with a similar deep n-well structure
  - MPW submitted in Oct 2022 in normal wafer
  - COFFEE1 received in Apr 2023
- SMIC 55nm HVCMOS process
  - HVCMOS process, with 1kΩ ·cm wafer
  - MPW submitted in Aug 2023
  - COFFEE2 received in Dec 2024
- Ongoing tests and first results
  - Breakdown voltage up to -70V
  - Capacitance scalps with sensor area
  - Diodes irradiated to ~10^{14} n_{eq} .cm^{-2} (ongoing analysis)
  - Ongoing developments

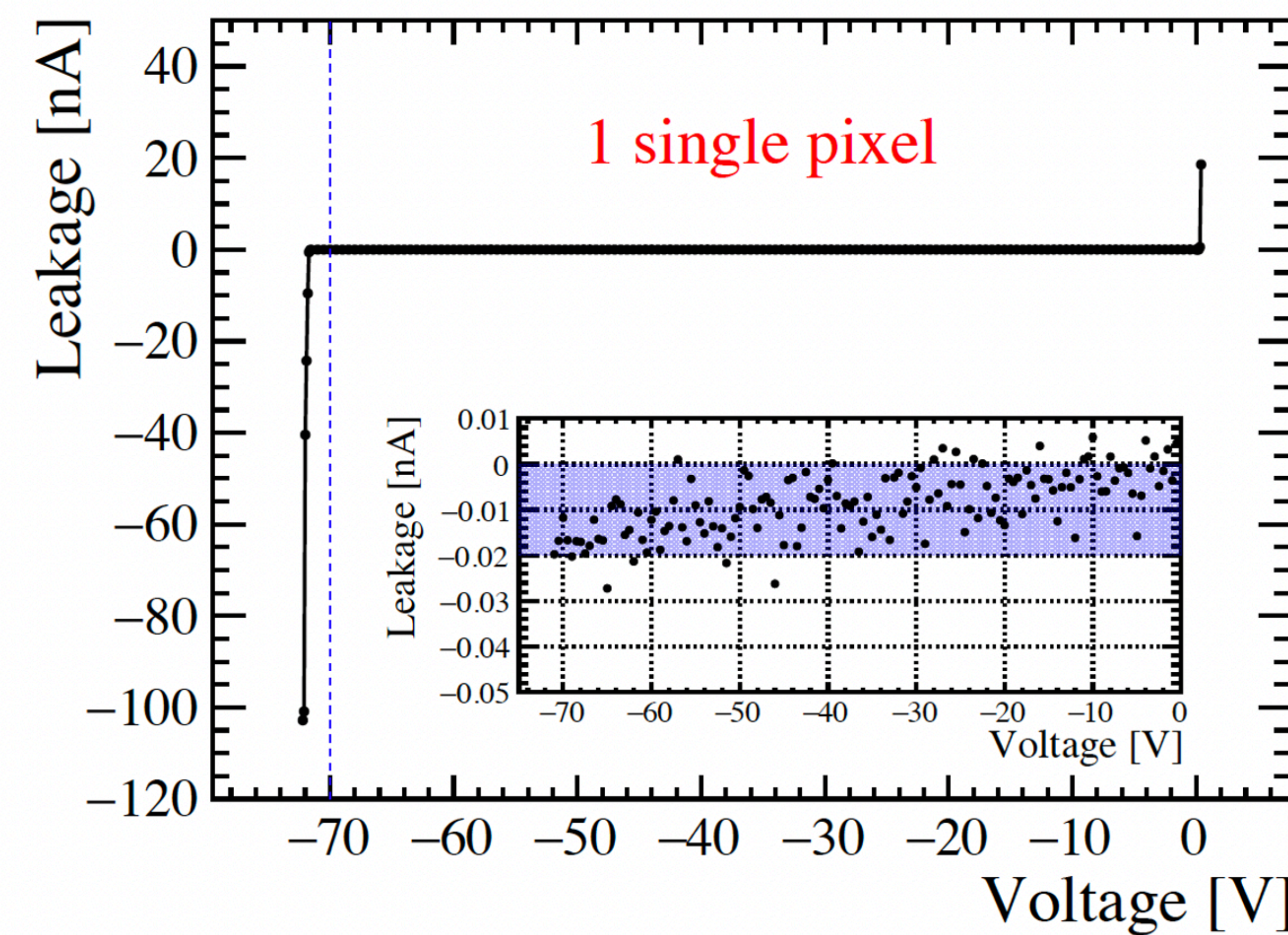
COFFEE1

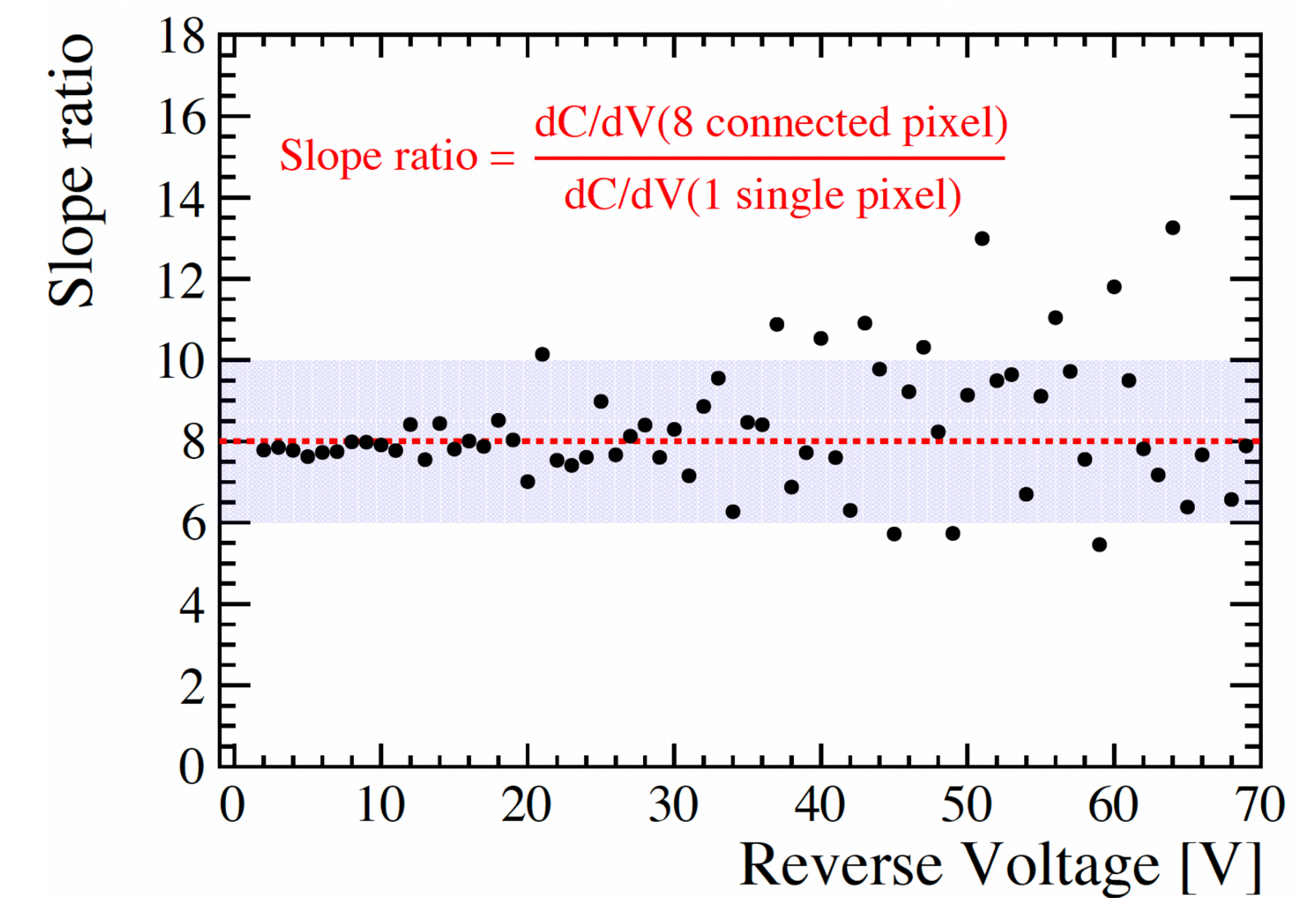


COFFEE2

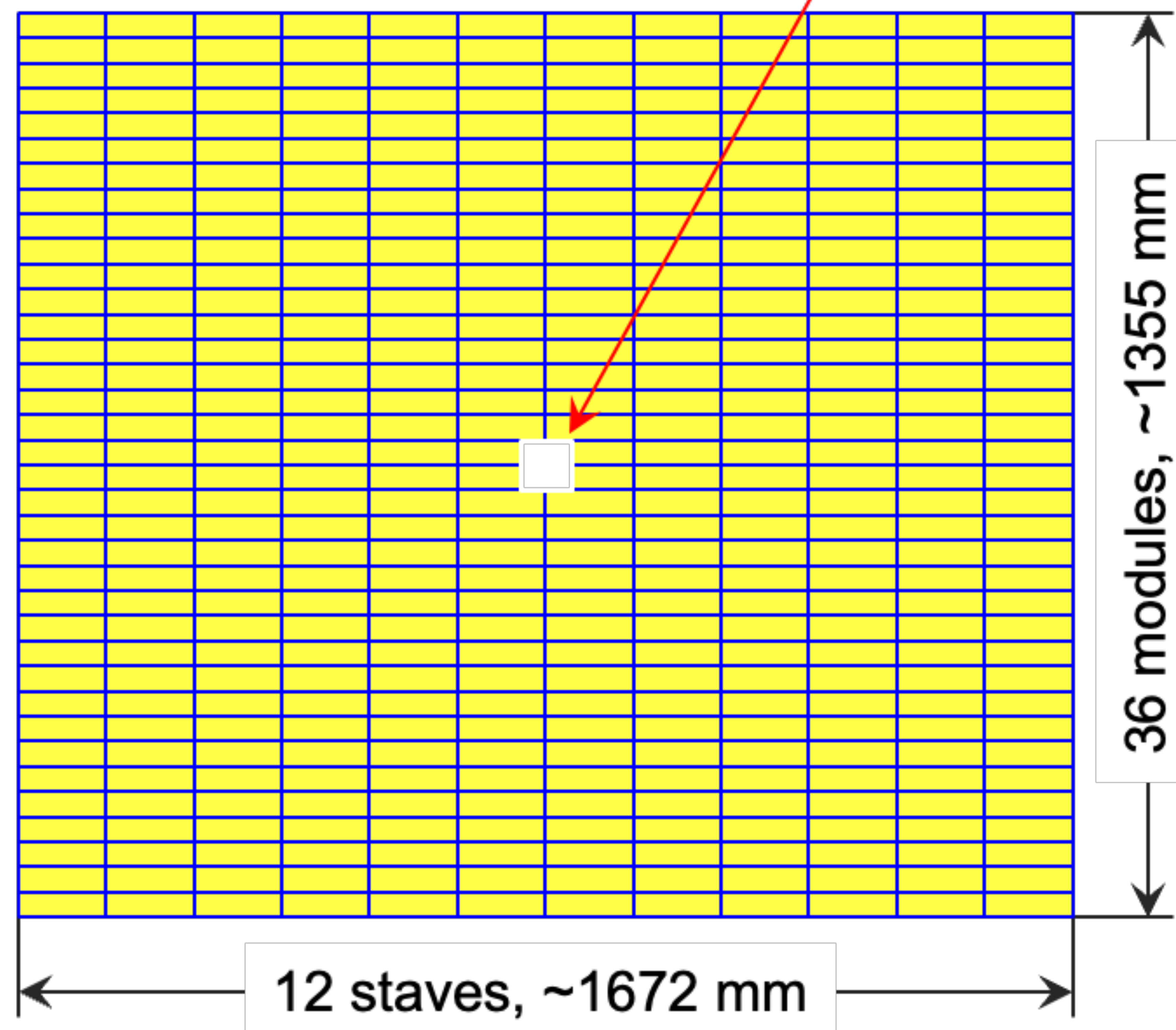








UT baseline geometry

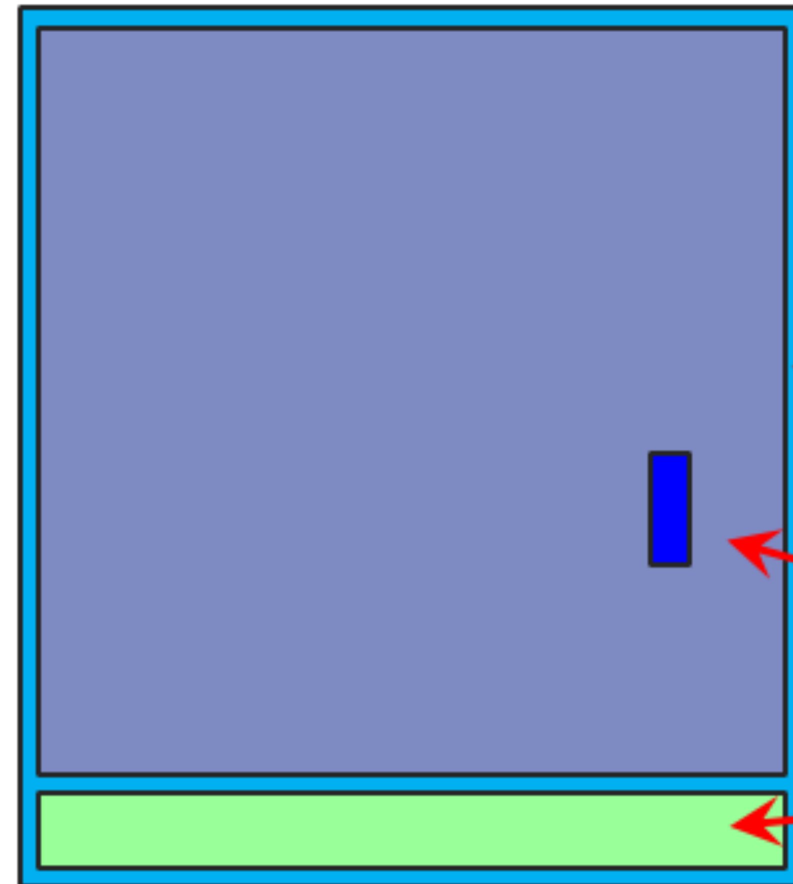


4 planes, 48 staves, 1728 modules, 24128 sensor chips

- **Preliminary design**:
  - 4 detector planes, at Z positions similar to the current UT
  - **Plane**: 12 staves, covering ~1672 mm in X, with 2 mm overlap
  - **Stave**: 36 modules, covering ~1355 mm in Y
  - **Module**: 2x7 sensors of ~ 2´2 cm2
    - In the outer regions of each plane, dual modules are used
  - Central hole (beam pipe) of (±39mm)x(±37mm)

UT preliminary design

Chip (HV-CMOS)



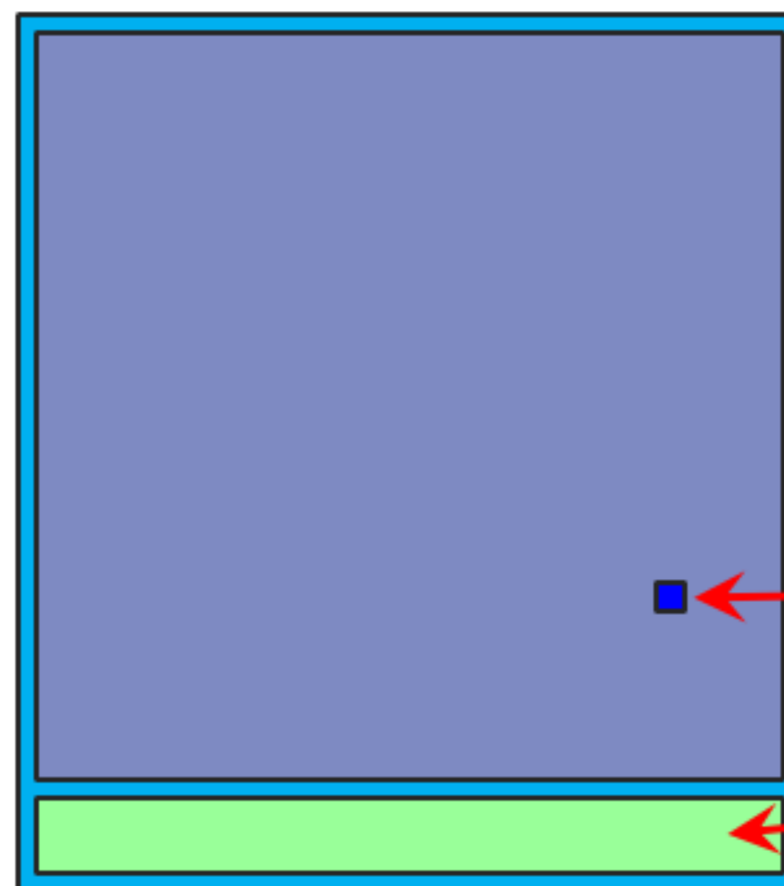
Reticle size
~ 20.2×21.4 mm²

Guard ring = 80 µm
Tolerances ~20-40 µm

Pixel = 50×150 µm
Matrix = 400×128

Periphery ~ 2 mm

Chip (LV-CMOS)



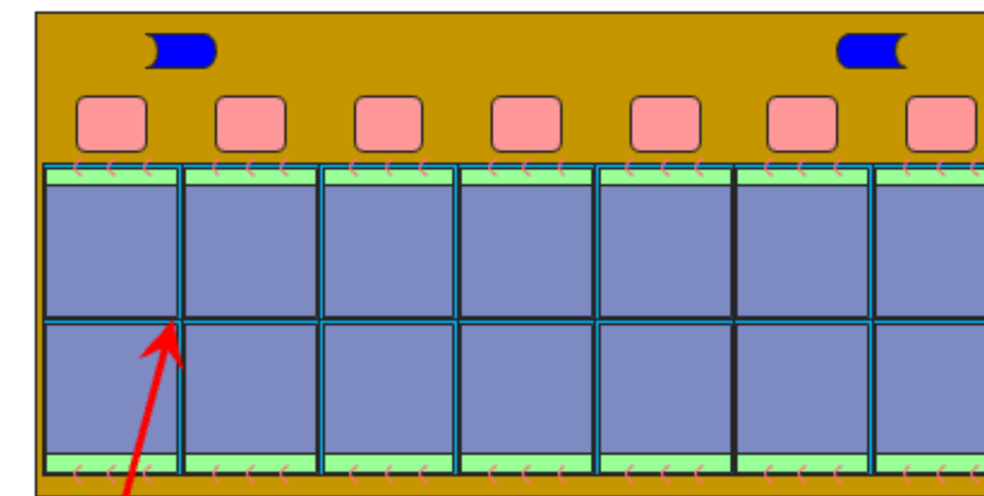
Reticle size
~ 18.6×19.8 mm²

Guard ring = 80 µm
Tolerances ~20-40 µm

Pixel = 36.4×36.4 µm
Matrix = 512×544

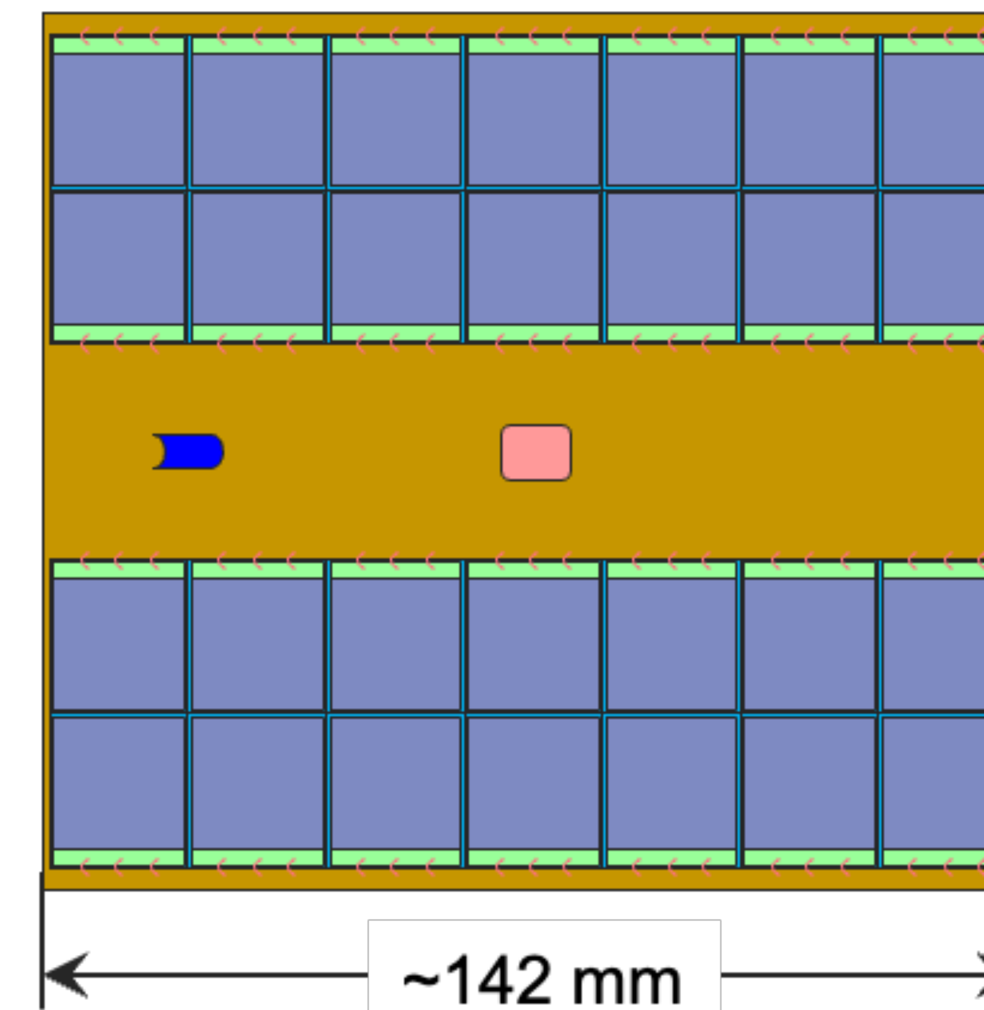
Periphery ~ 2 mm

Module

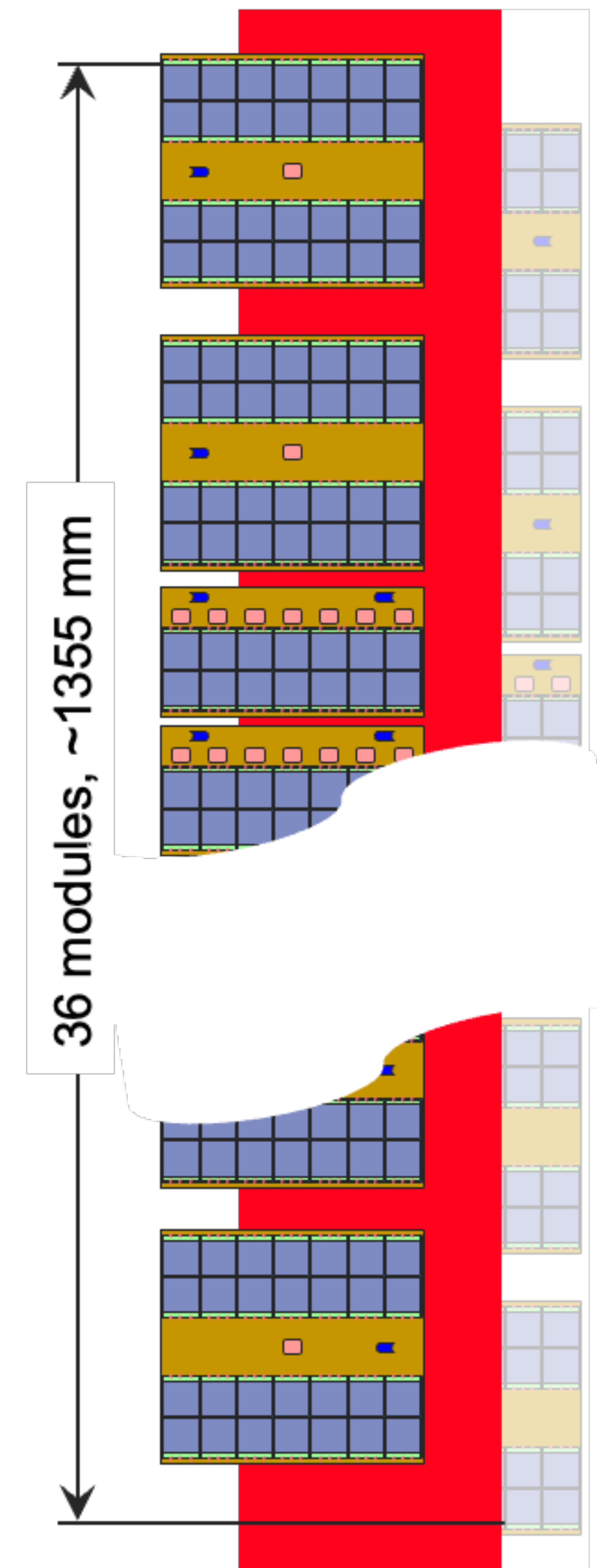


Dead space ~ 200 µm

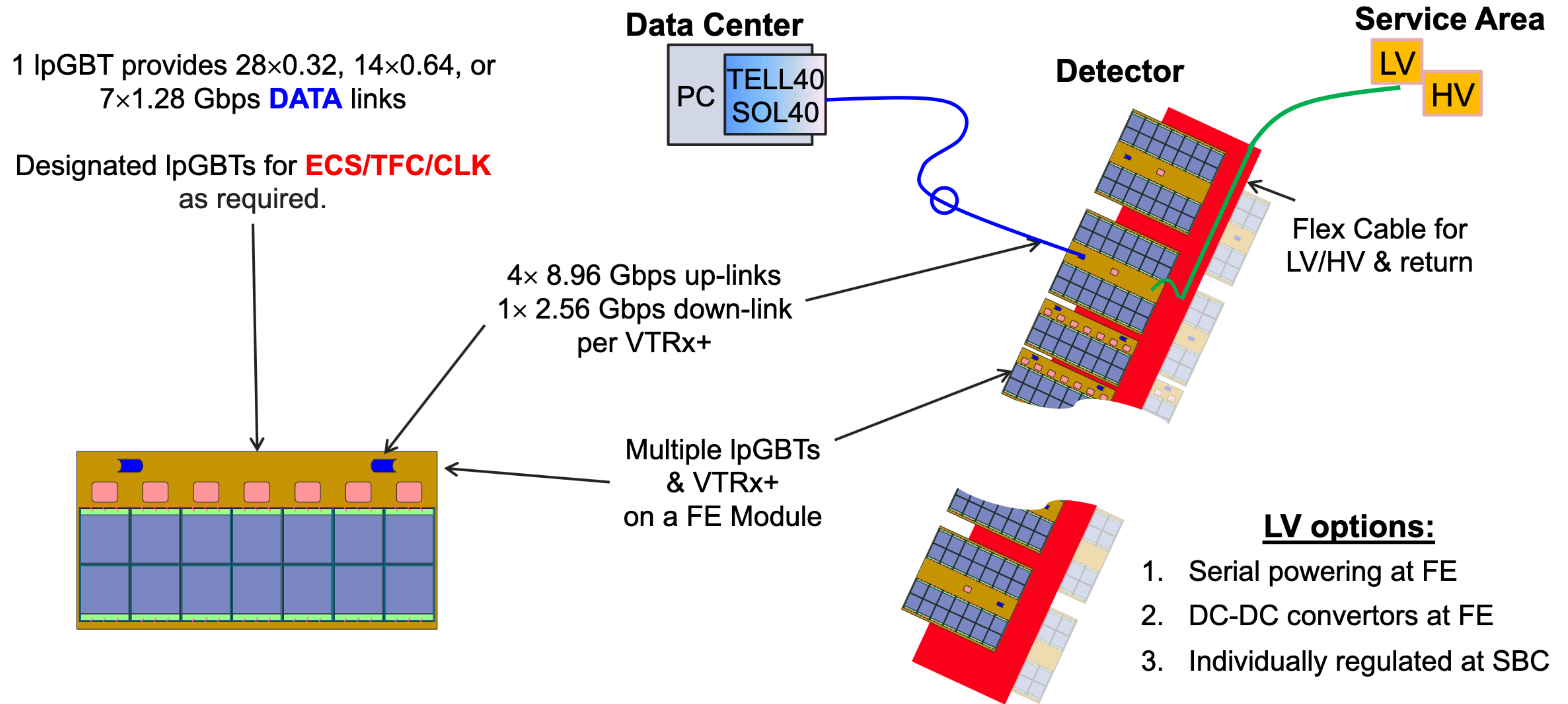
Dual-Module



Stave



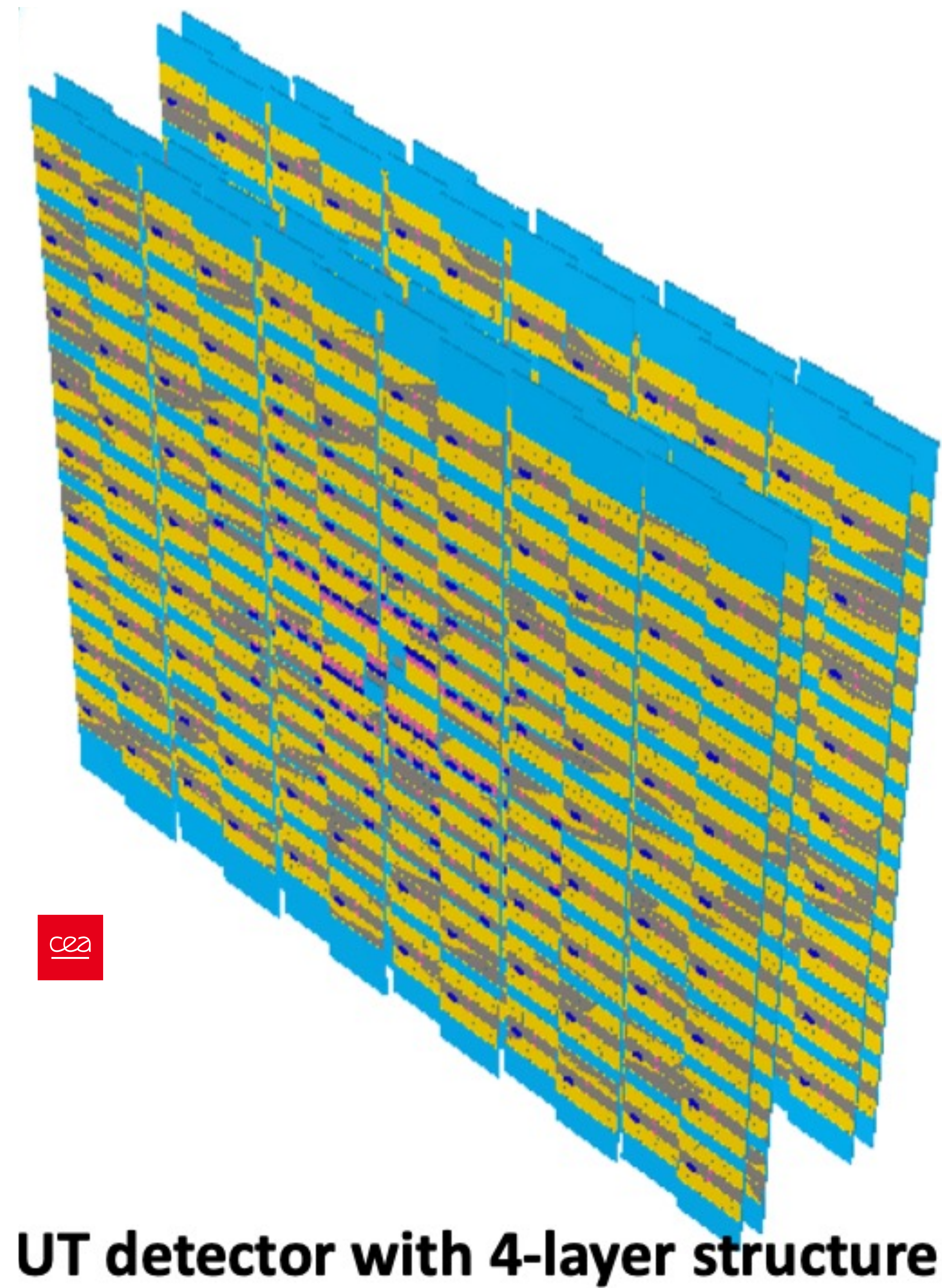
UT readout scheme design



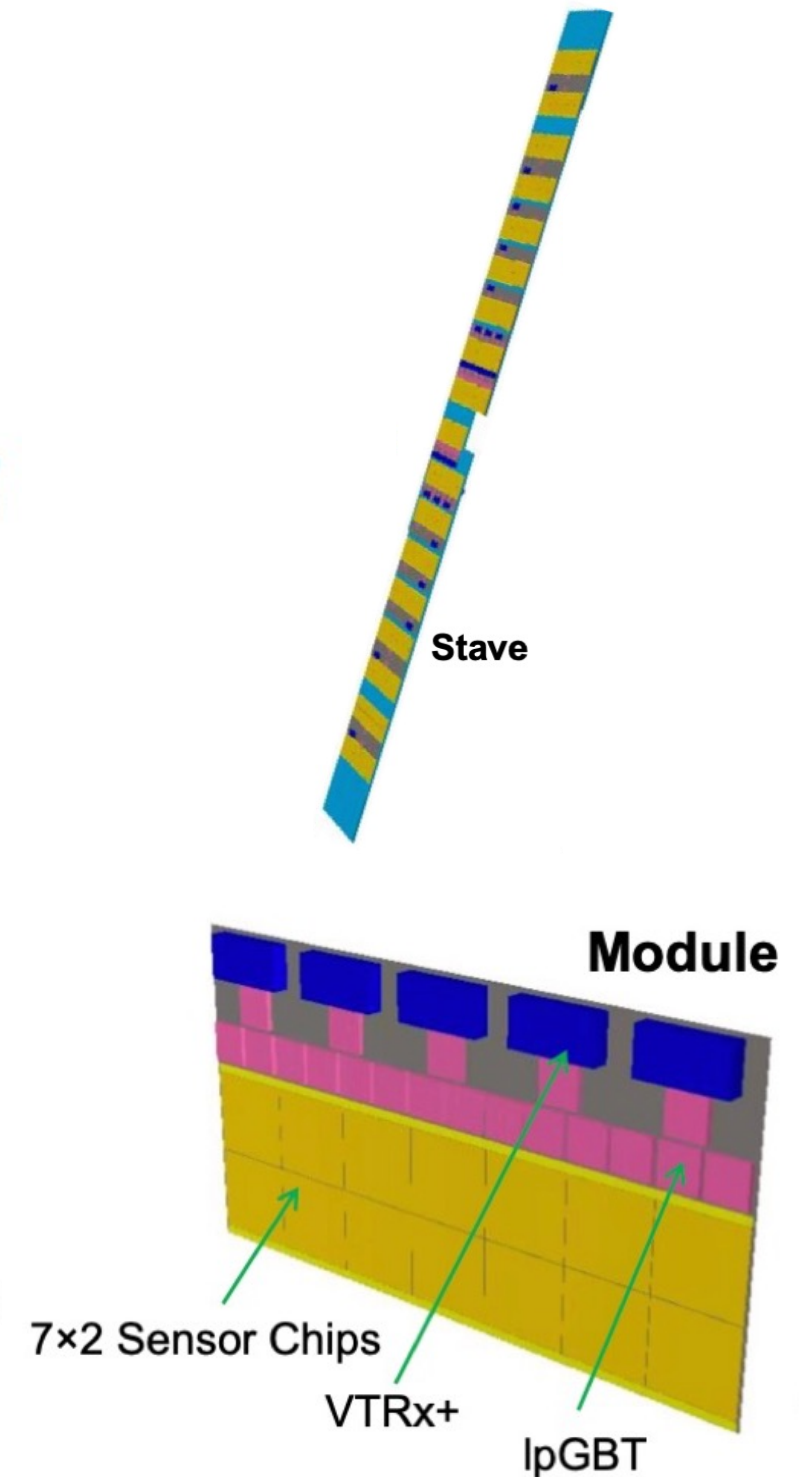
Simulations

UT baseline geometry description implemented in LHCb Run 5 simulation framework:

- 4 planes, 12 staves
- Design with only 3 planes and/or 10 staves implemented as well (descoping scenarios)
- HV-CMOS-based geometry
- LV-CMOS is work in progress

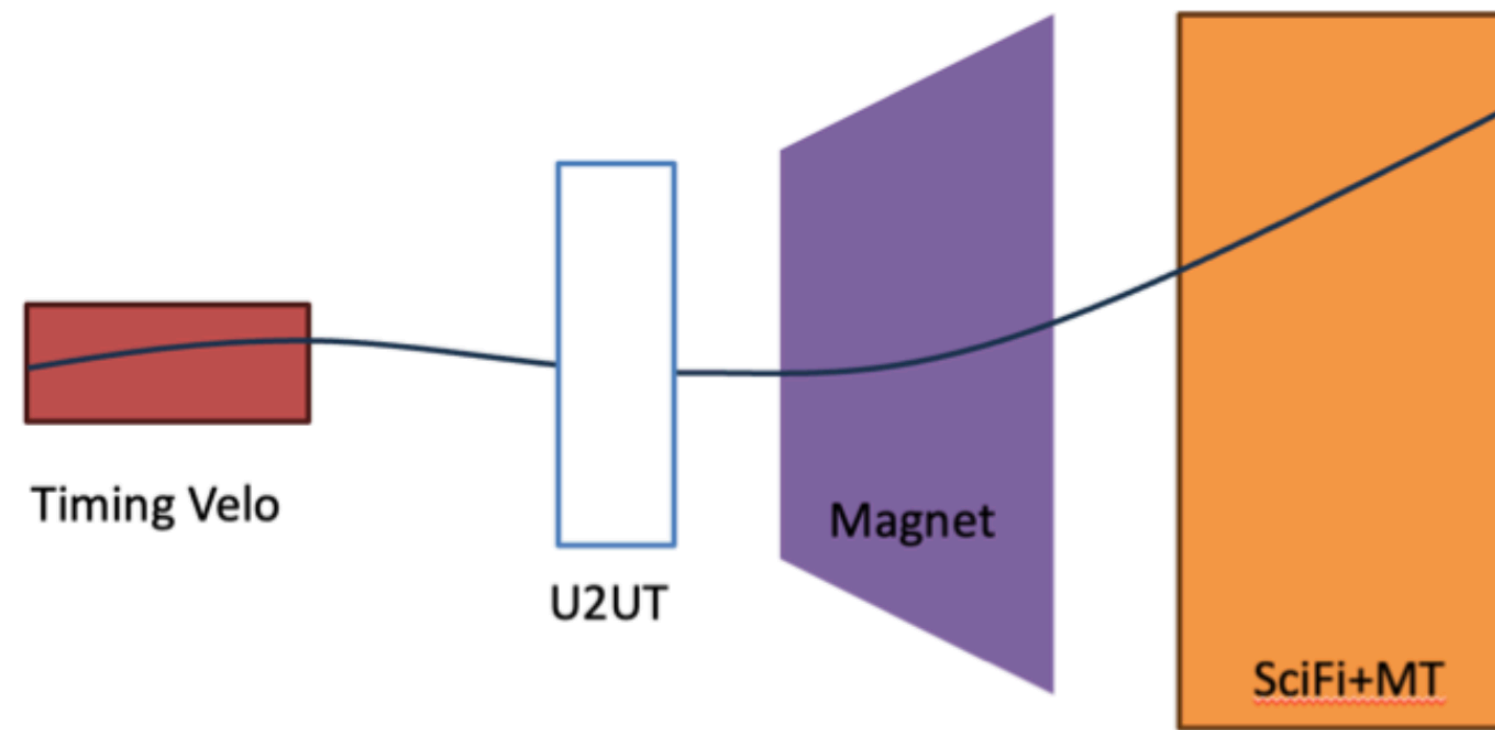


UT detector with 4-layer structure

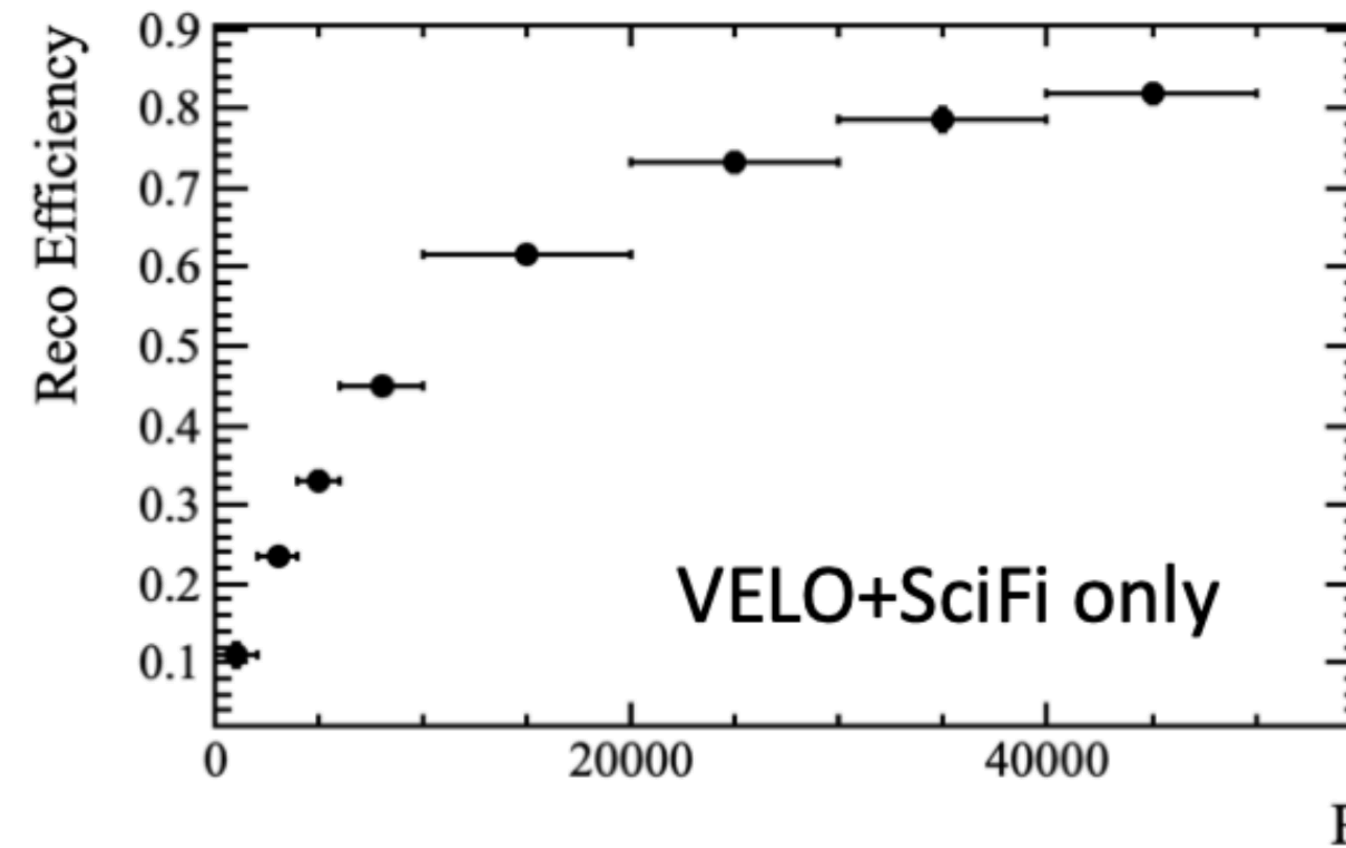


Preliminary tracking studies

Test with only kaon tracks and Run 3 conditions

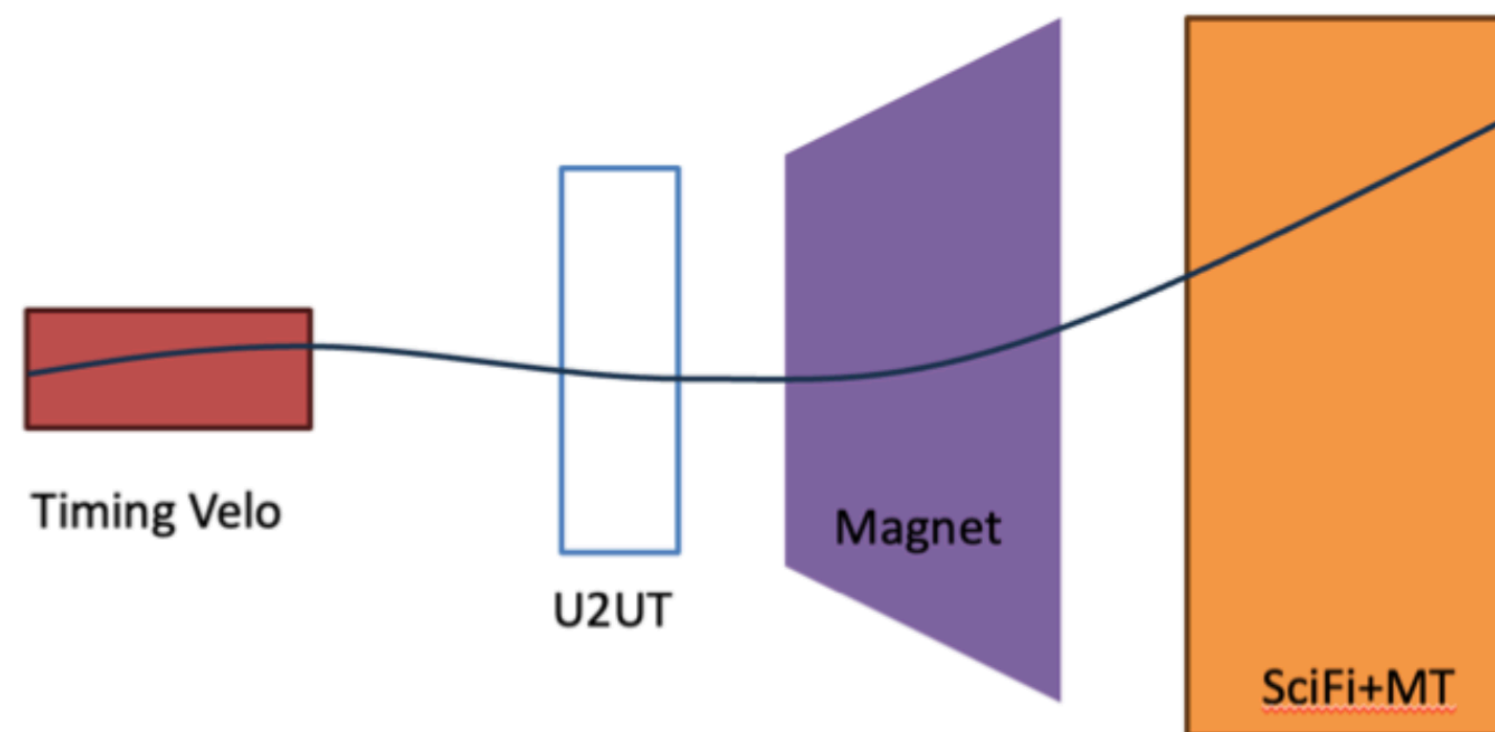


VELO-SciFi tracks w/o UT

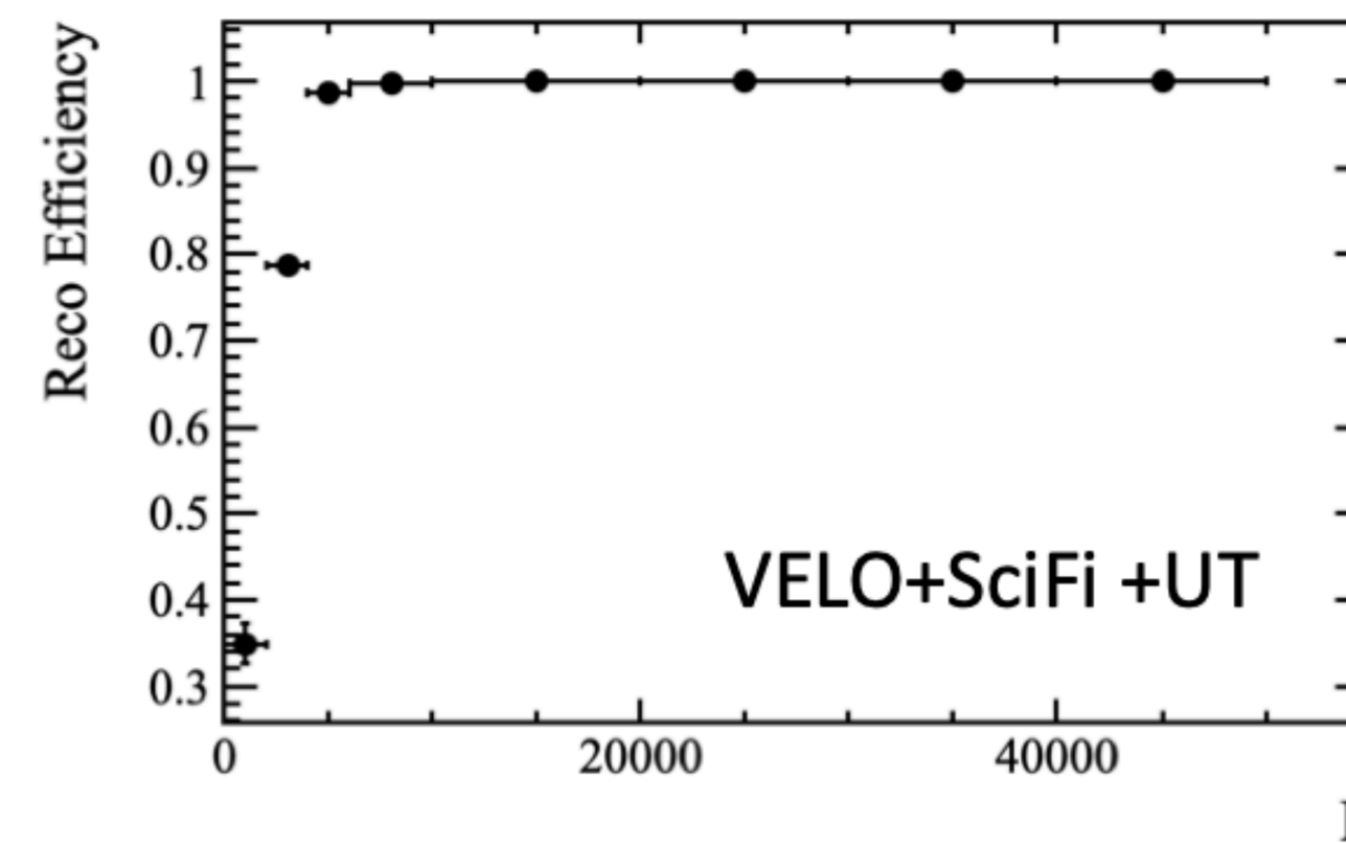


Velo+MT only:

- Total efficiency = 50.2±0.4%
- Ghost rate = 34.24±0.1%



VELO-SciFi tracks w/ UT tracks

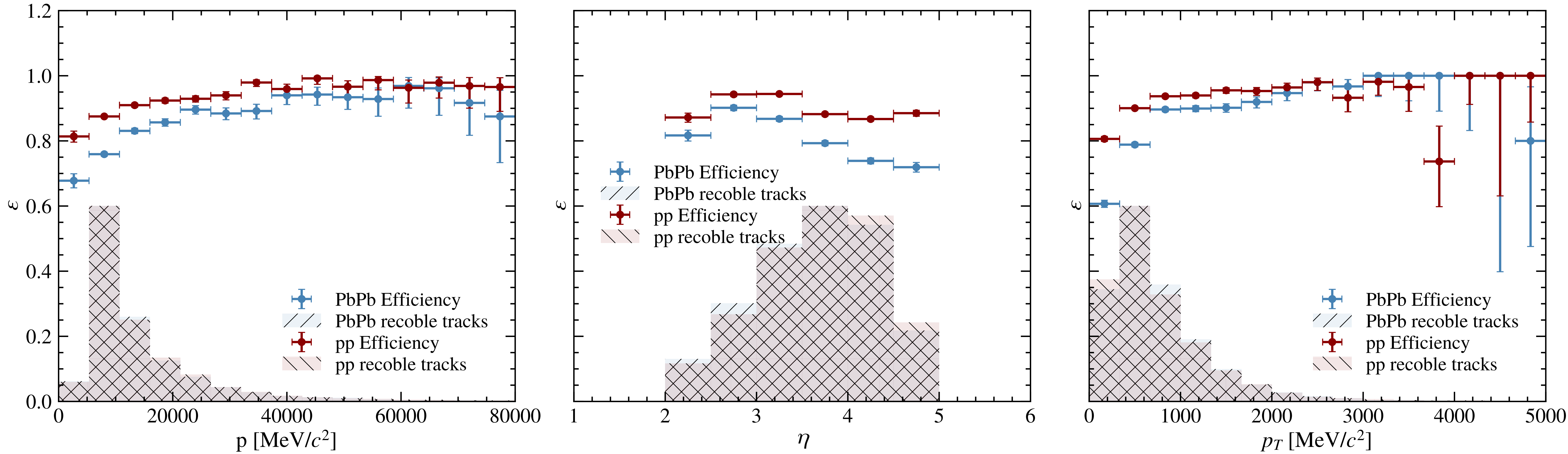


Velo+UT+MT:

- Total efficiency = 94.4±0.2%
- Ghost rate = 4.5±0.01%

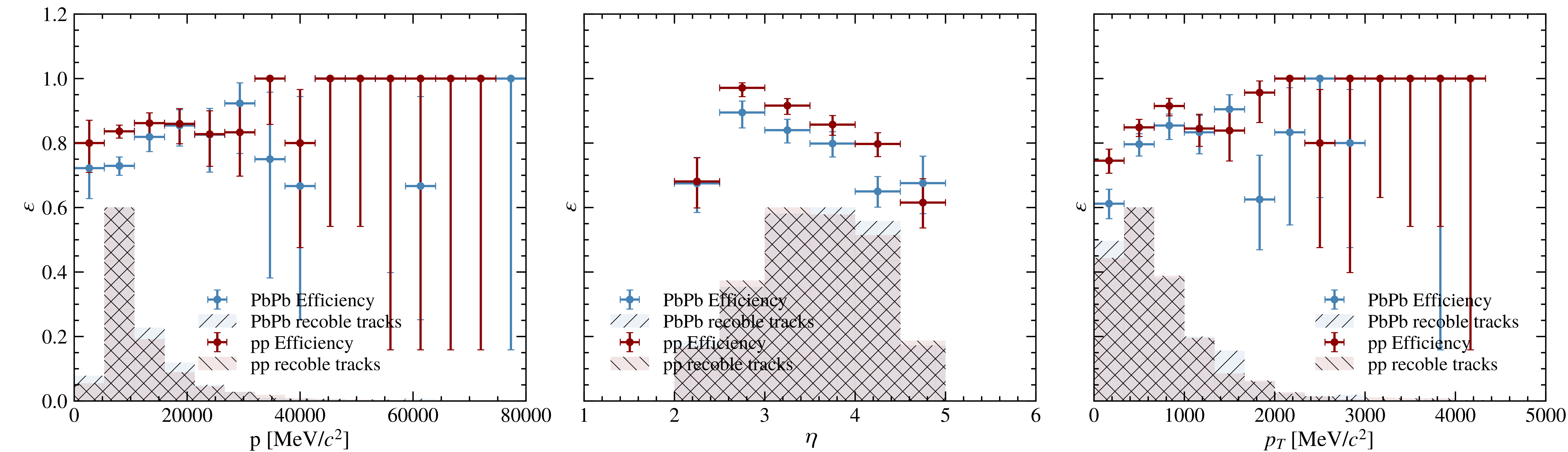
The UT is essential

Preliminary tracking studies



Long tracks (V+UT+MT)

	Efficiency	Ghost rate
pp	90 %	24 %
PbPb (Central)	80 %	39 %



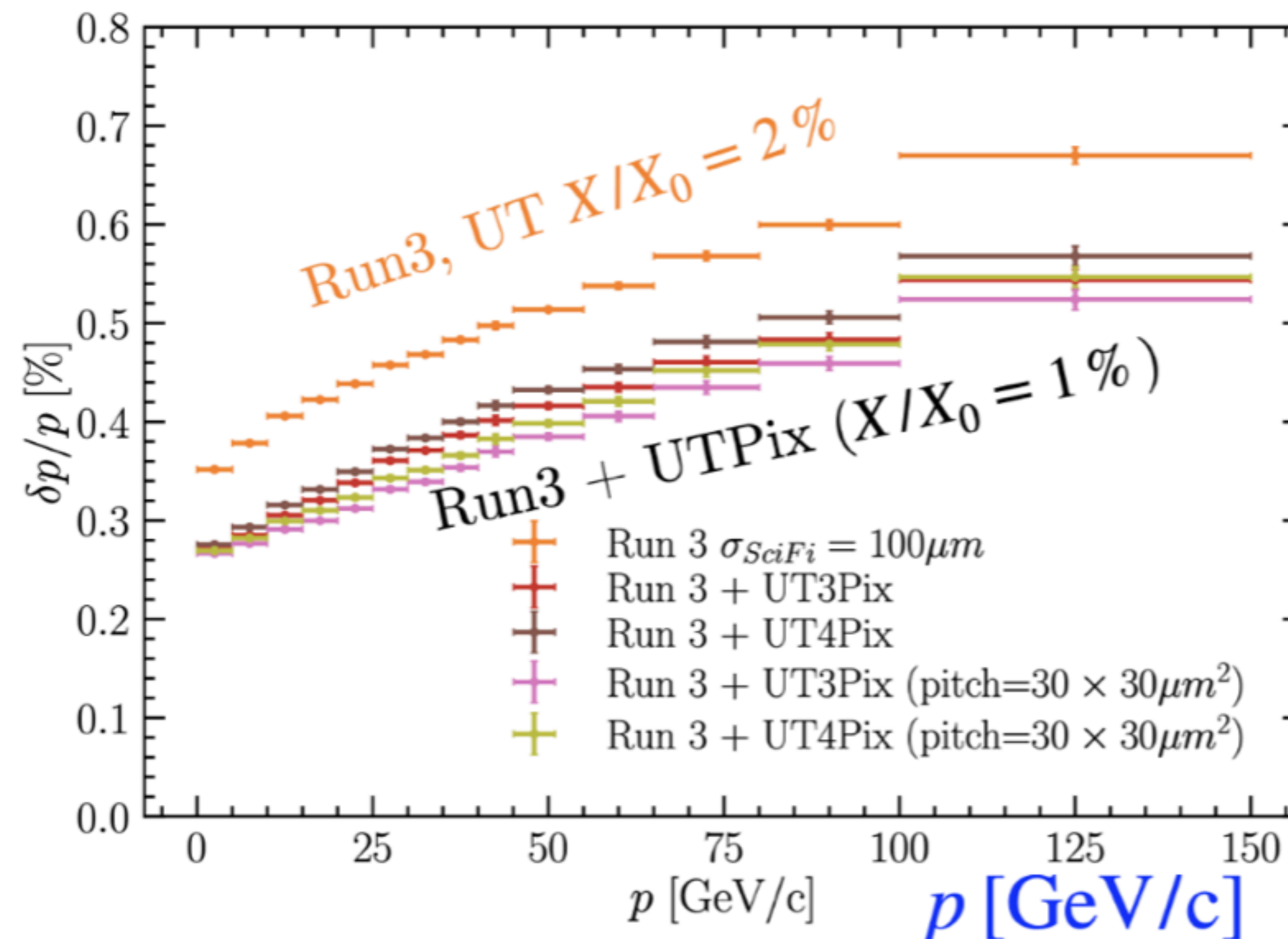
Downstream tracks (UT+MT)

	Efficiency	Ghost rate
pp	85 %	27 %
PbPb (Central)	78 %	38 %

Material budget studies

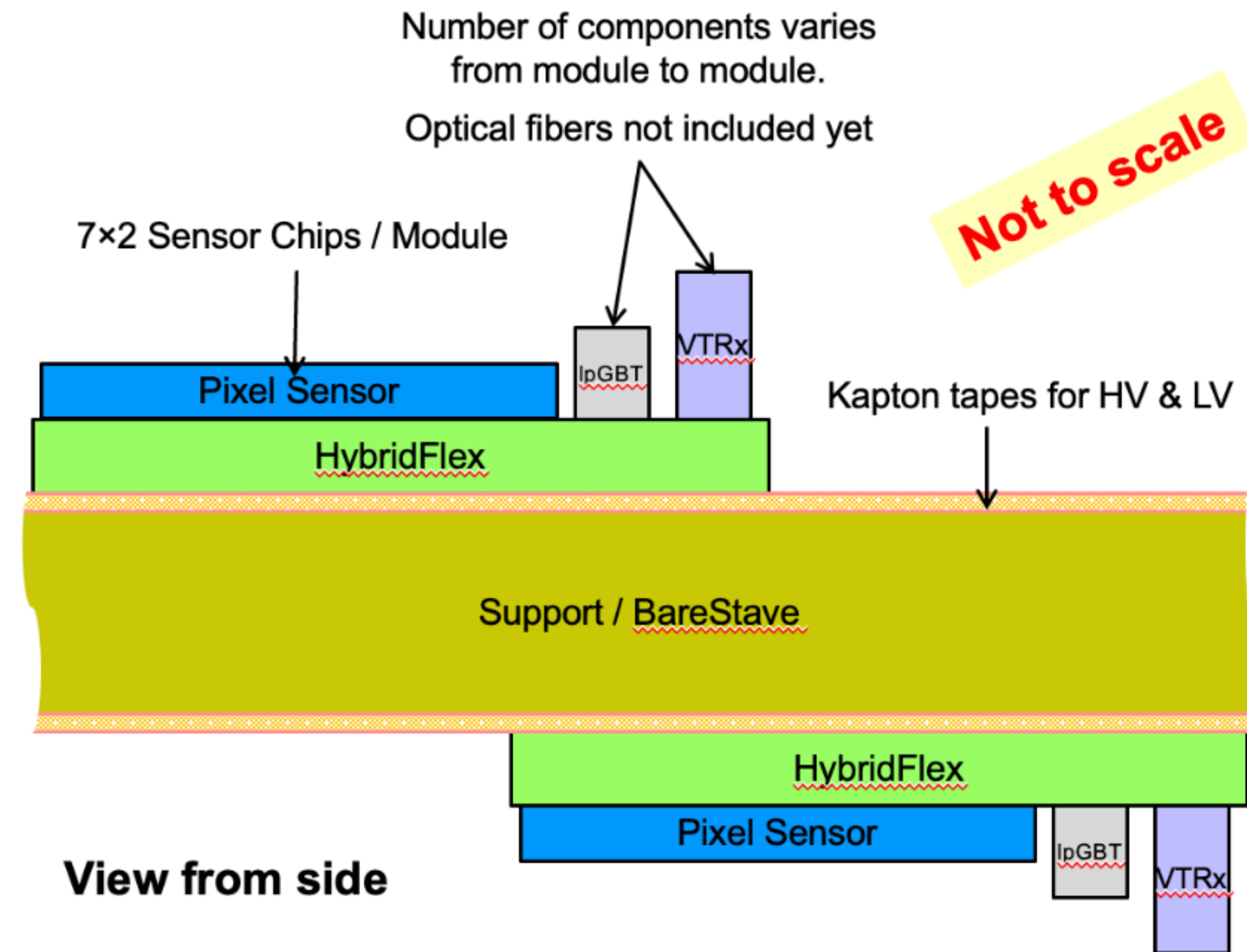
The amount of material creates a strong interplay between tracking detectors, affecting (not limited to):

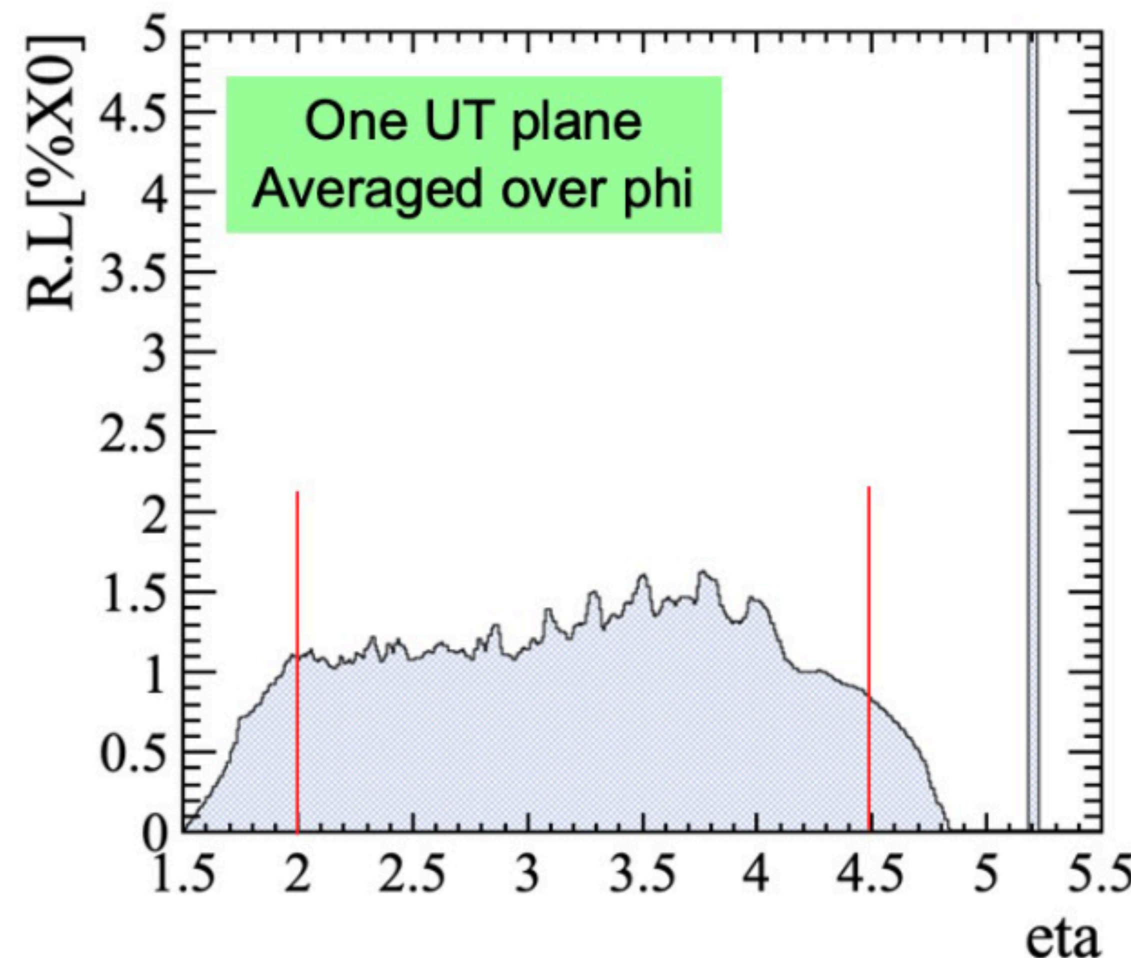
- Benchmark performance metrics such as parameter resolution
- Track slopes and invariant mass resolution
- Momentum resolution
- Amount of secondaries (driving up cost), ghost track performance, data processing cost…



Material budget studies

(Unit: mm)	Thickness	W×L
Pixel Sensor	0.200	20.2 × 21.4
lpGBT	1.250	9 × 9
VTRx+	4.000	20 × 10
HybridFlex	0.200	142.16 × 59.18
Kapton Tape	0.100	142.16 × 1357.72
BareStave	4.000	142.16 × 1600.28





	Thickness [mm]	RL ($2<\eta<4.5$) [% X_0]
Pixel Sensor	0.200	0.24
lpGBT	1.250	0.07
VTRx+	4.000	0.13
HybridFlex	0.200	0.28
Kapton Tape	0.100	0.27
BareStave	4.000	0.21
One plane	**-**	**1.20**

Too high!

It must be close to 1% X_0 per plane and not everything is including:

- Optical fibers
- DCDCs
- Cooling and mechanics
- …

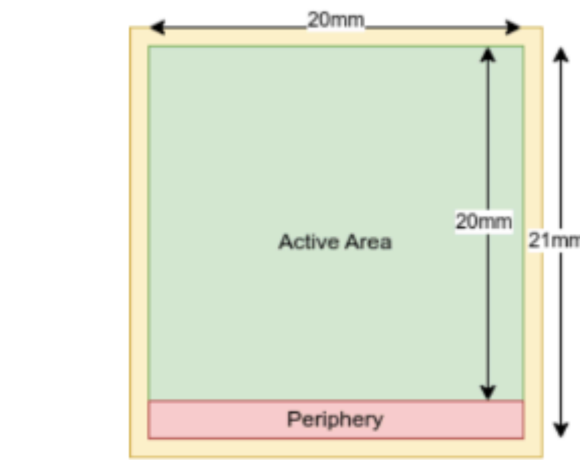
➡ Ongoing studies to estimate the MB more precisely and to explore possible solutions.

Summary and outlooks

- **Upgrade of LHCb UT and MT based on MAPS**
- **Several parallel R&D**
    - Small electrode/pixel: MALTA-TJ180, SPARC-TPSCo65
    - Large electrode/pixel: MightyPix-AMS180, COFFEE-SMIC55
    - Choice will be driven by radiation hardness and data rate capabilities
    - Power distribution/consumption and cooling solution will be challenging
    - Module, stave, readout chain design in progress (with still several sensor options)
    - Material budget reduction (essential to keep good momentum resolution)
- **Simulations**
    - UT (MT) geometry implemented in LHCb Run 5 simulation
    - First tracking studies show encouraging results
    - Many ongoing studies dedicated to descoping scenarios
- **Important French-Chinese combined efforts on hardware and software R&D studies for UT UII**

Additional slides

Mighty Tracker preliminary design

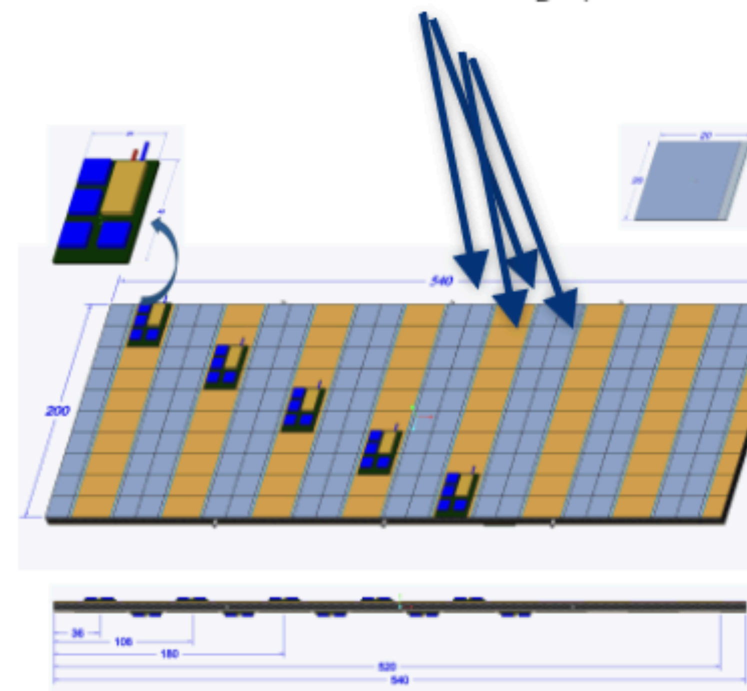


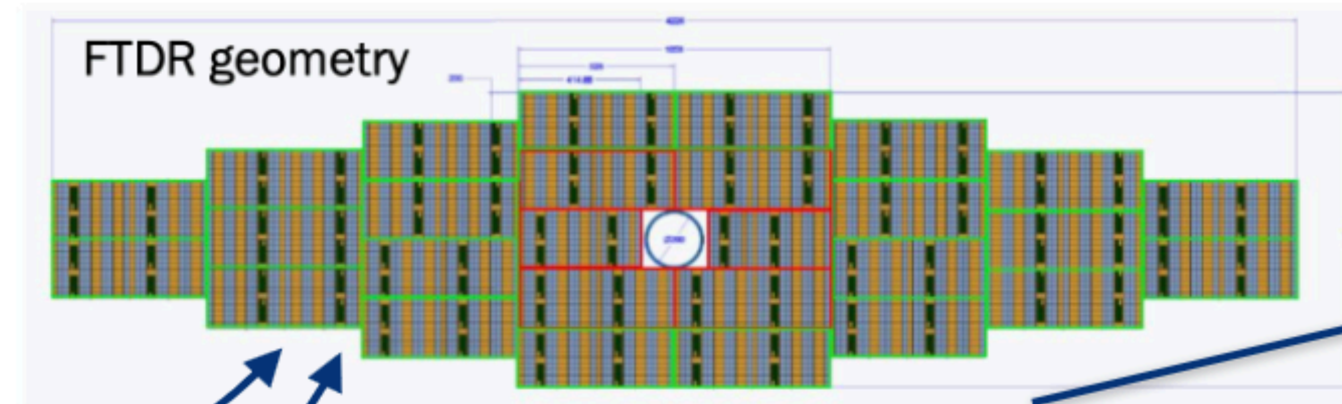
MAPs ASIC

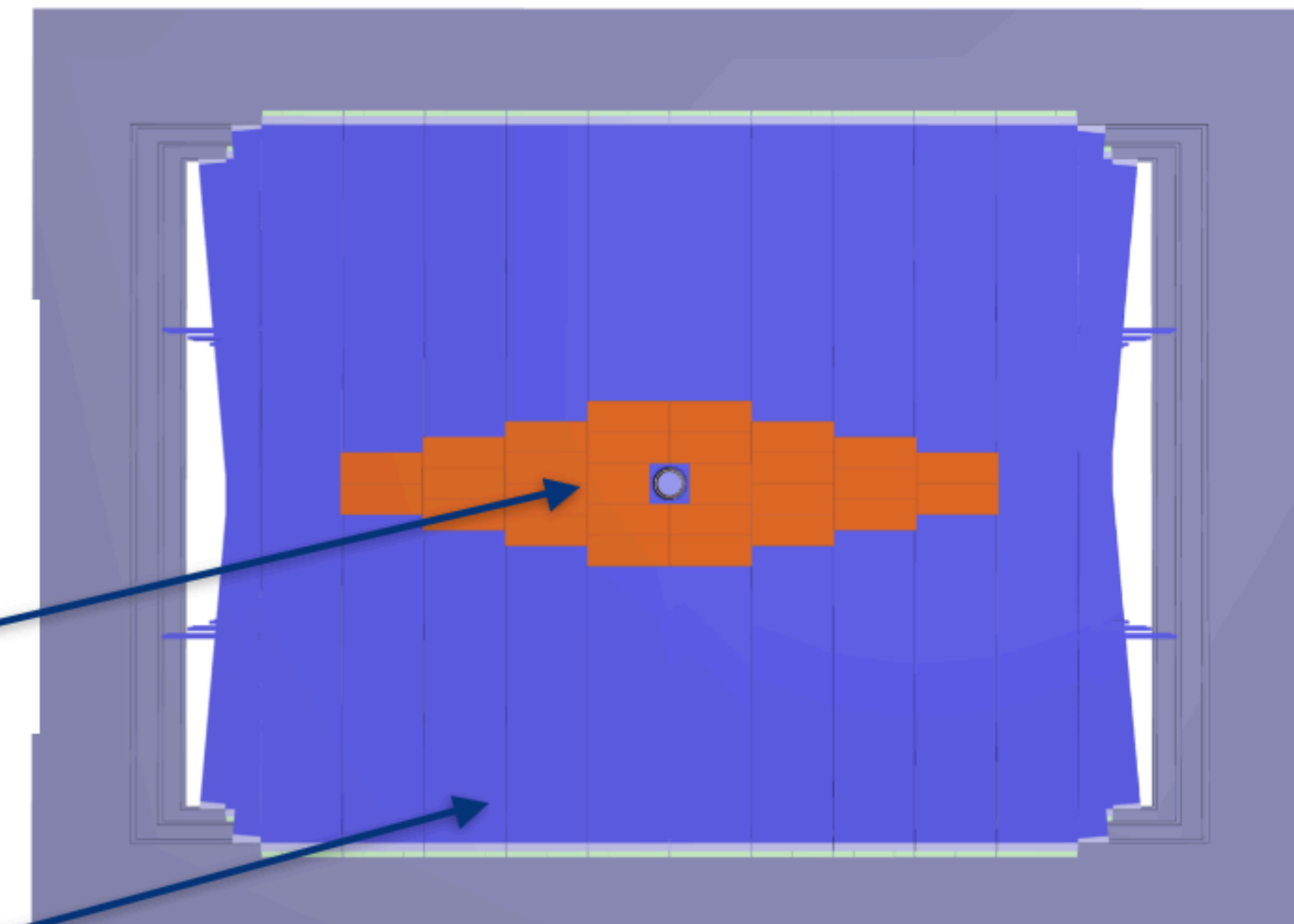
- >99% efficiency within 25 ns
- 3 ns Timing resolution
- Power < 150 mW/cm2
- Pixel size 100 x 300 μm^2
- Radiation tolerance $3 \times 10^{14} 1 \text{ MeV } n_{eq}/cm^2$

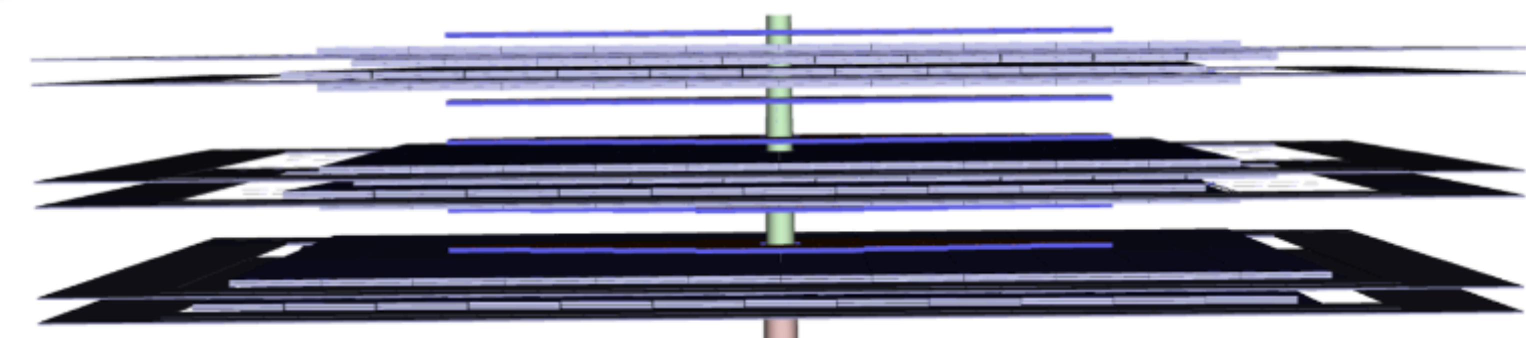
Blake Leverington

- Geometry visualisation in DD4HEP
  - SciFi + Mighty Pix









~13/10x26 Chips arranged into modules

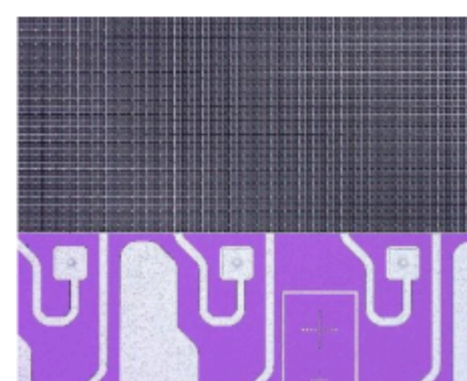
Modules arranged into layers

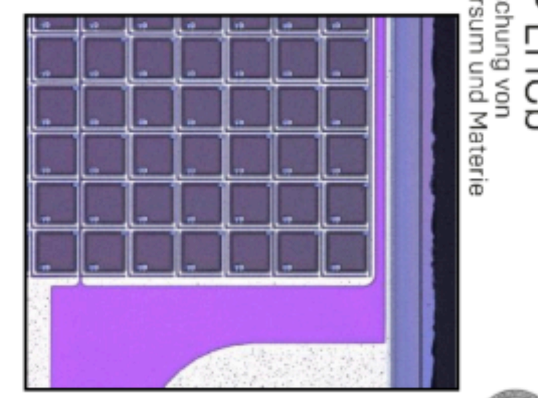
6 tracking layers

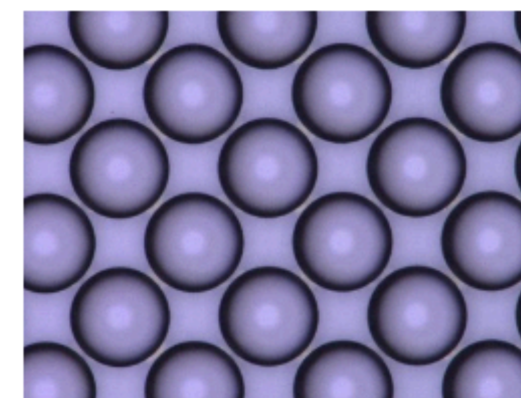
Fibre tracker, (standard fibre), new SiPM

- 42 and 50 um pixels
- NO dead region between Channels
- Tight dicing, 50 um
- Cryo optimized

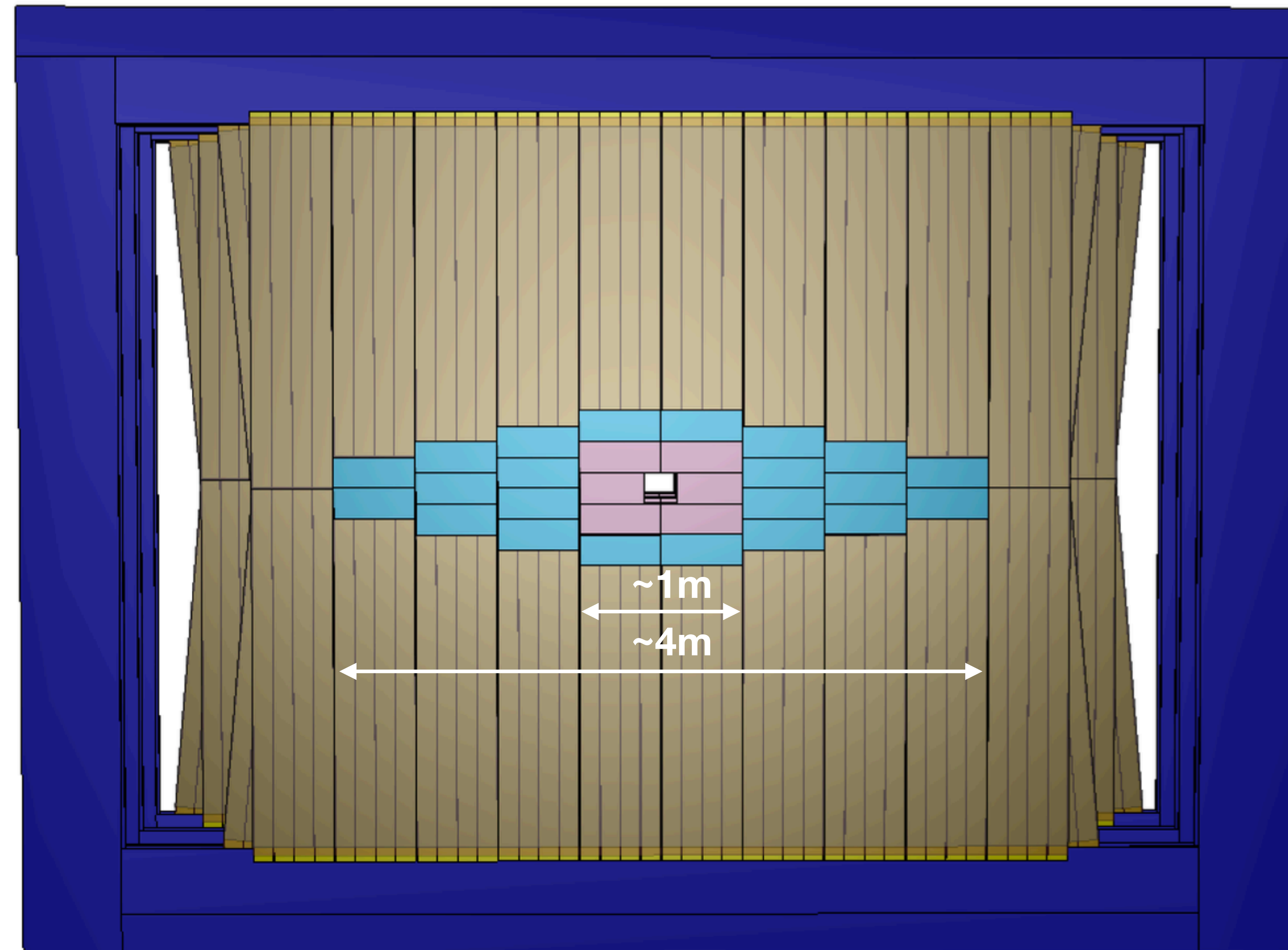
Microlenses may increase light yield

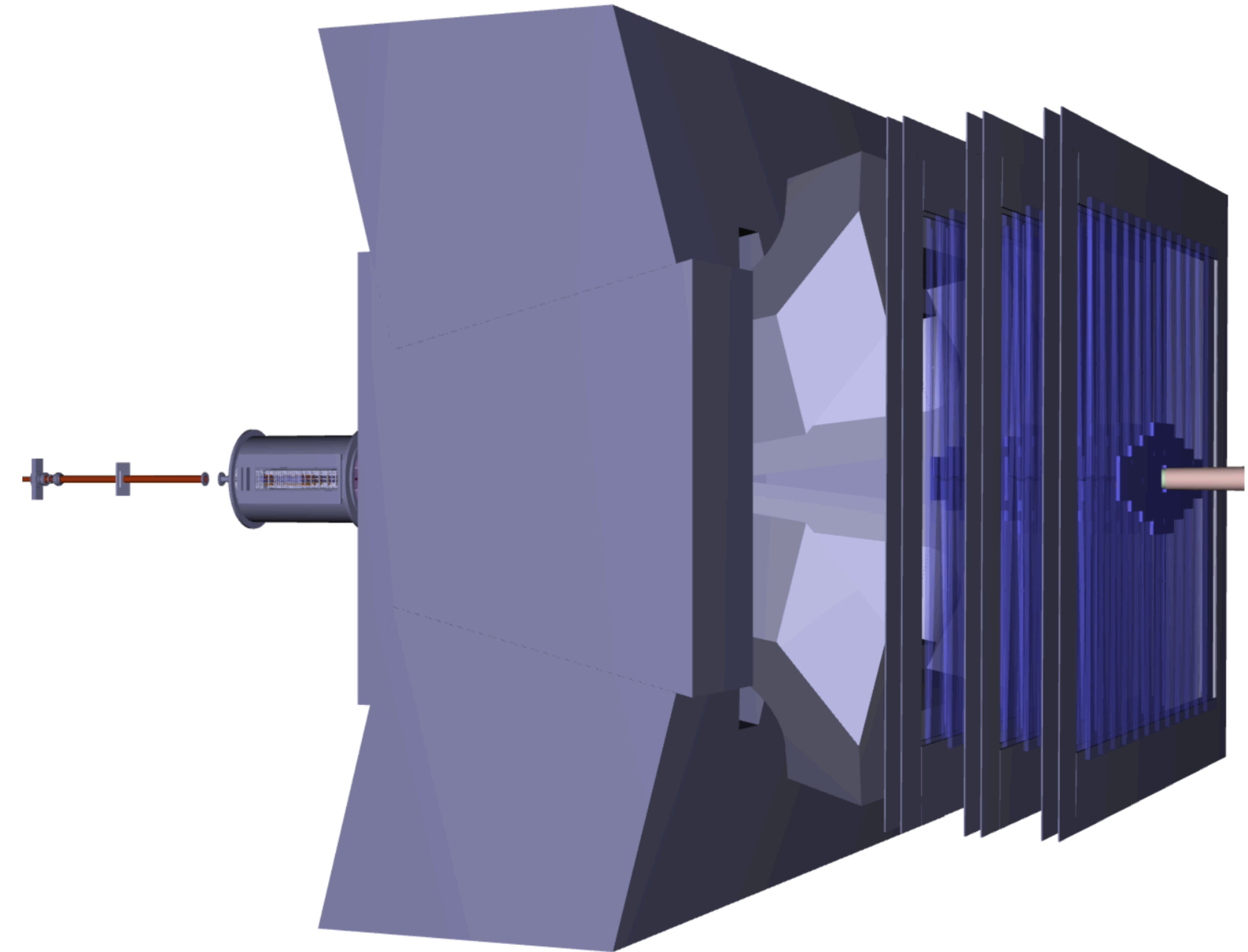

No channel gap


Tight dicing tolerances

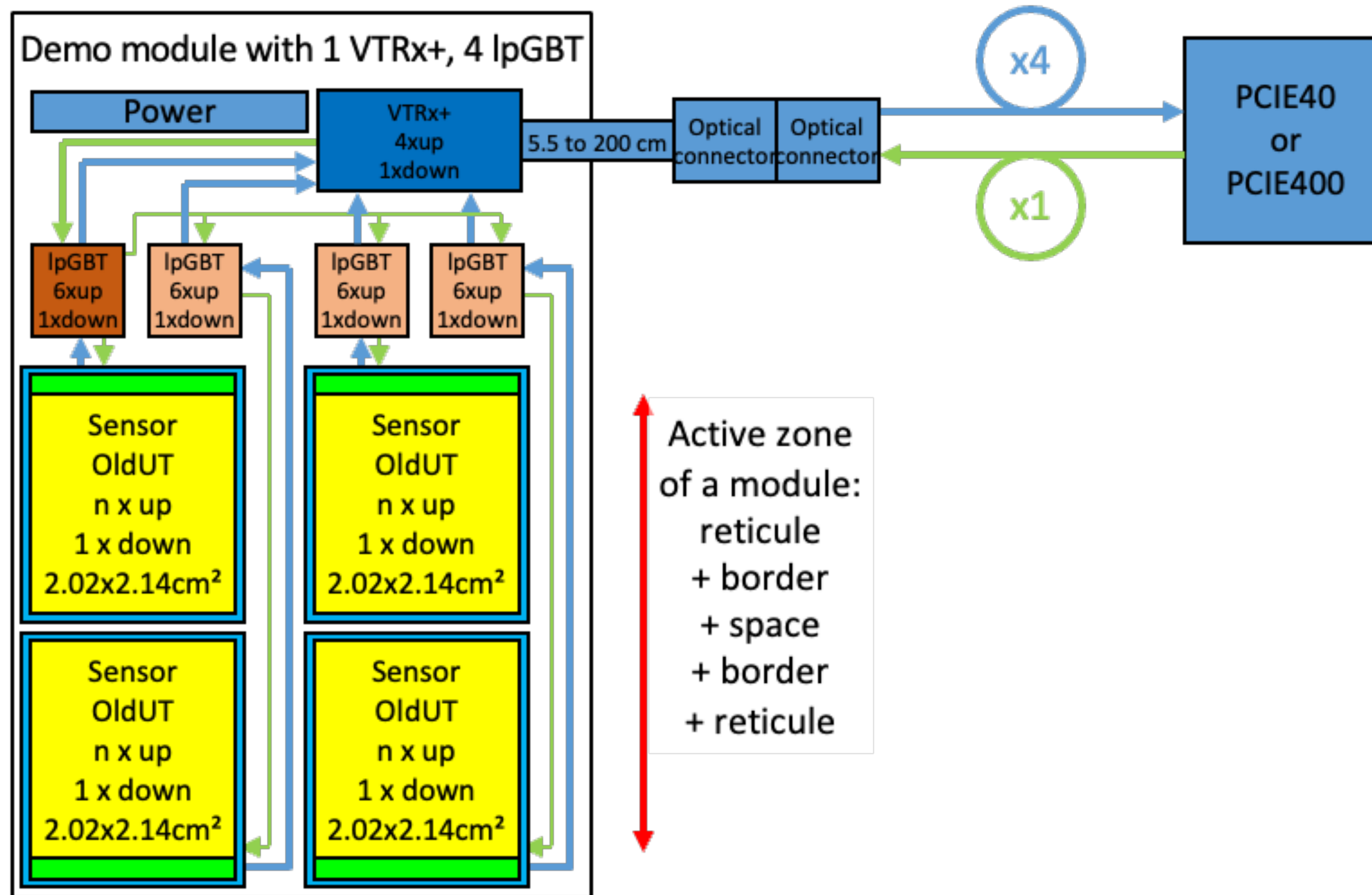


Mighty Tracker preliminary design



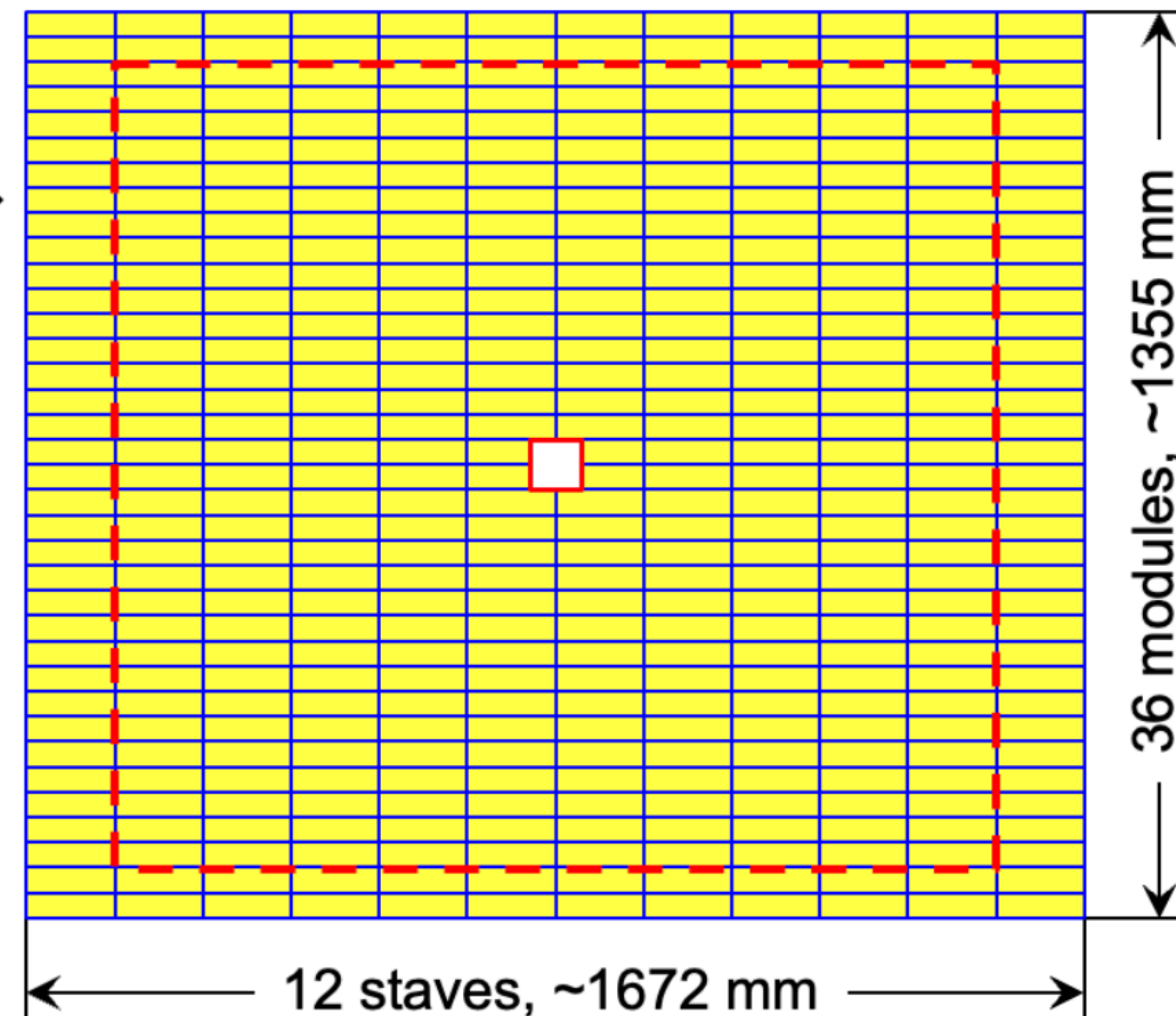


UT module readout scheme design



Descoping scenarios

1) Reduced coverage: **(12→10)** staves × **(36→32)** modules
   - Reduce 26% detection area at the outer ring
   - The overall budget decreases from 9.6 MCHF to 7.9 MCHF by this de-scoping alone



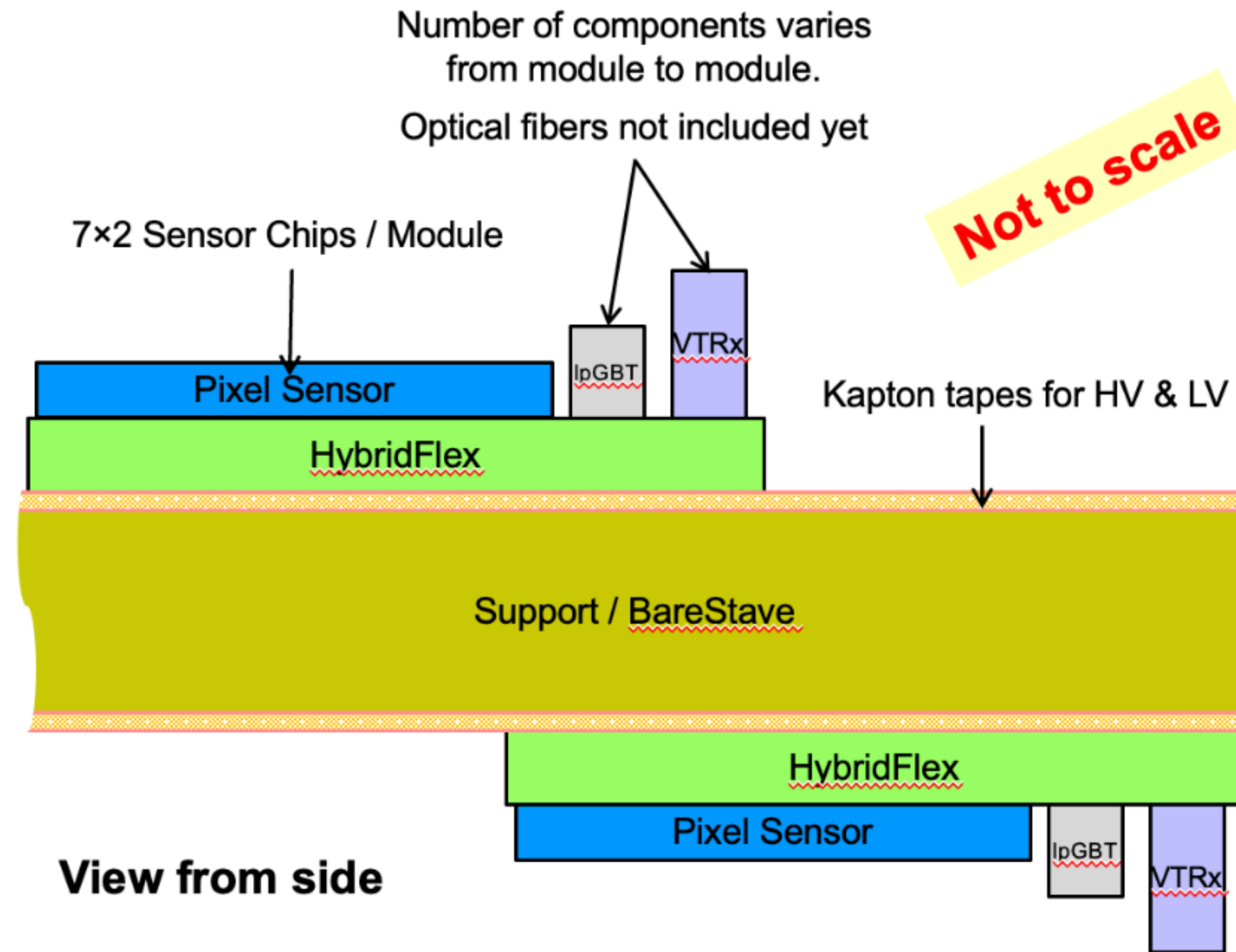
2) Reduced peak luminosity (**1.5→1.3→1.0**)×10^{34} cm^{-2} s^{-1}
   - Designs of sensor chip & detector module are less difficult, even though the cost reduction is not very significant
   - Save 156 kCHF for (**1.5→1.3**)×10^{34} cm^{-2} s^{-1}, or 143 kCHF on top of the coverage reduction
   - Save 389 kCHF for (**1.5→1.0**)×10^{34} cm^{-2} s^{-1}, or 358 kCHF on top of the coverage reduction

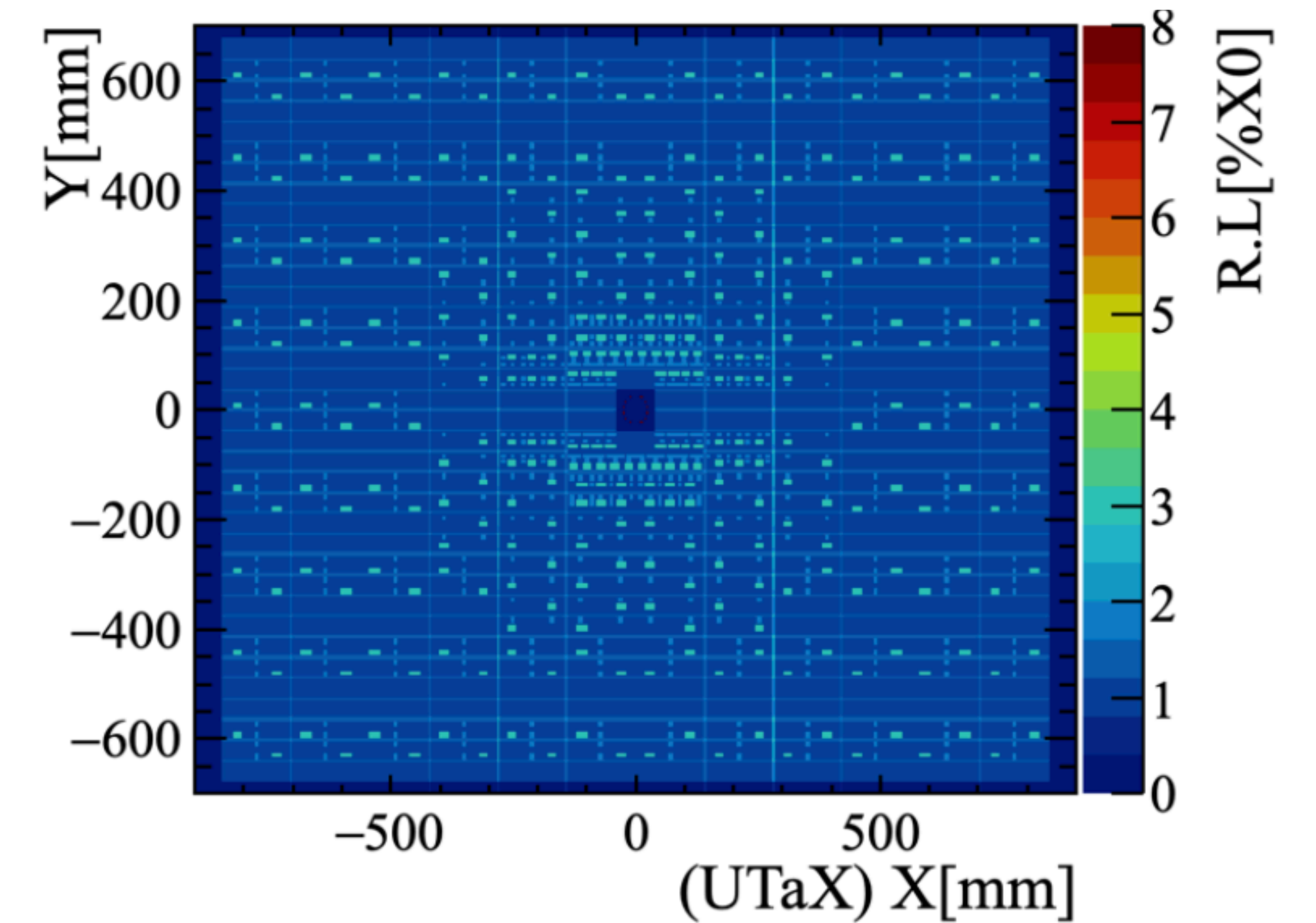
3) Improve the yield of sensor chip: **(40→60)%**
   - It may be feasible to optimize the sensor chip production and wafer test procedure and improve the yield
   - It could reduce the baseline budget by ~10%

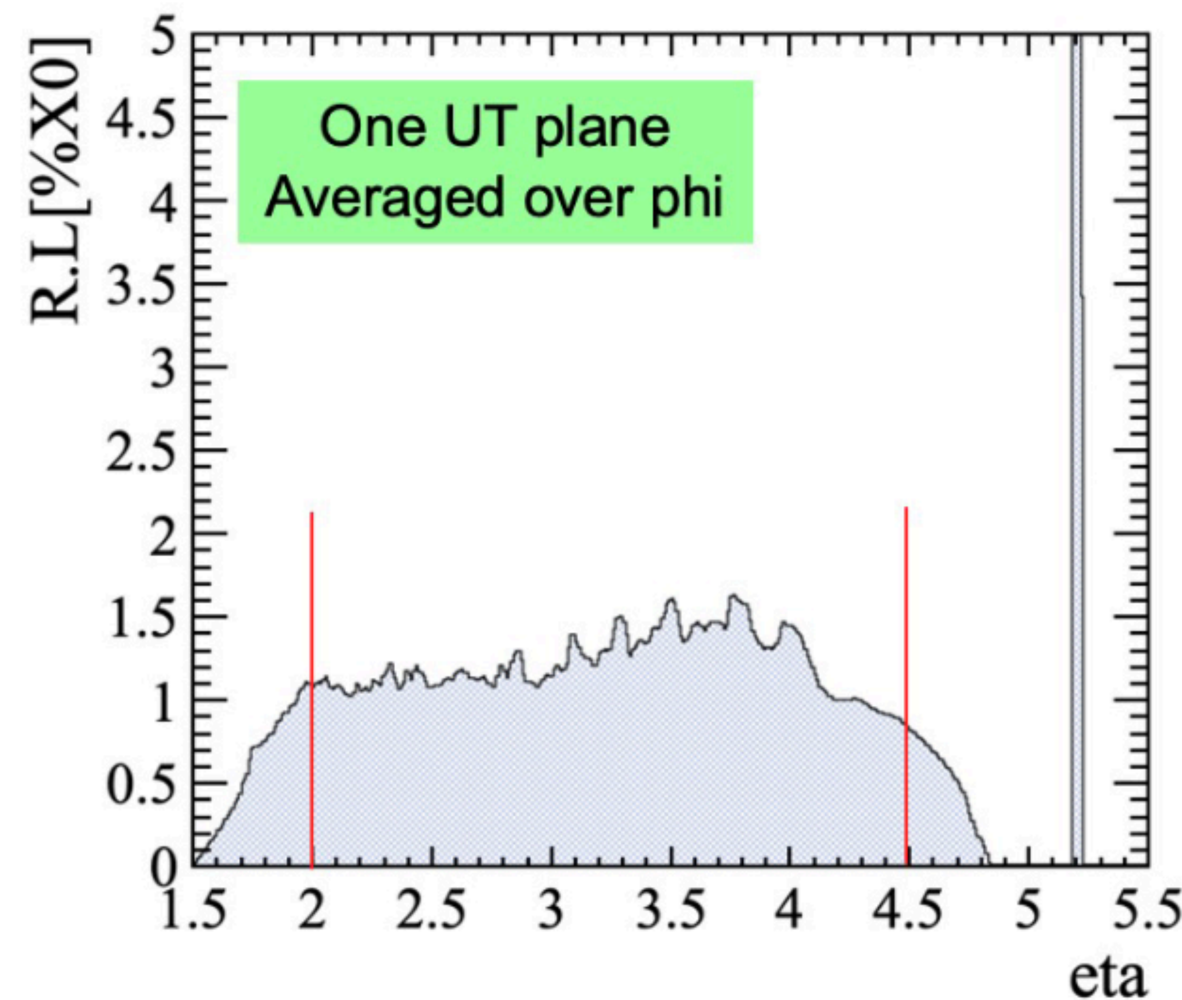
Other options under study but not considered in the cost descoping:
- Reduce the number of planes (4→3)
- Increase central hole (η: 4.8→ 4.5)

Material budget studies

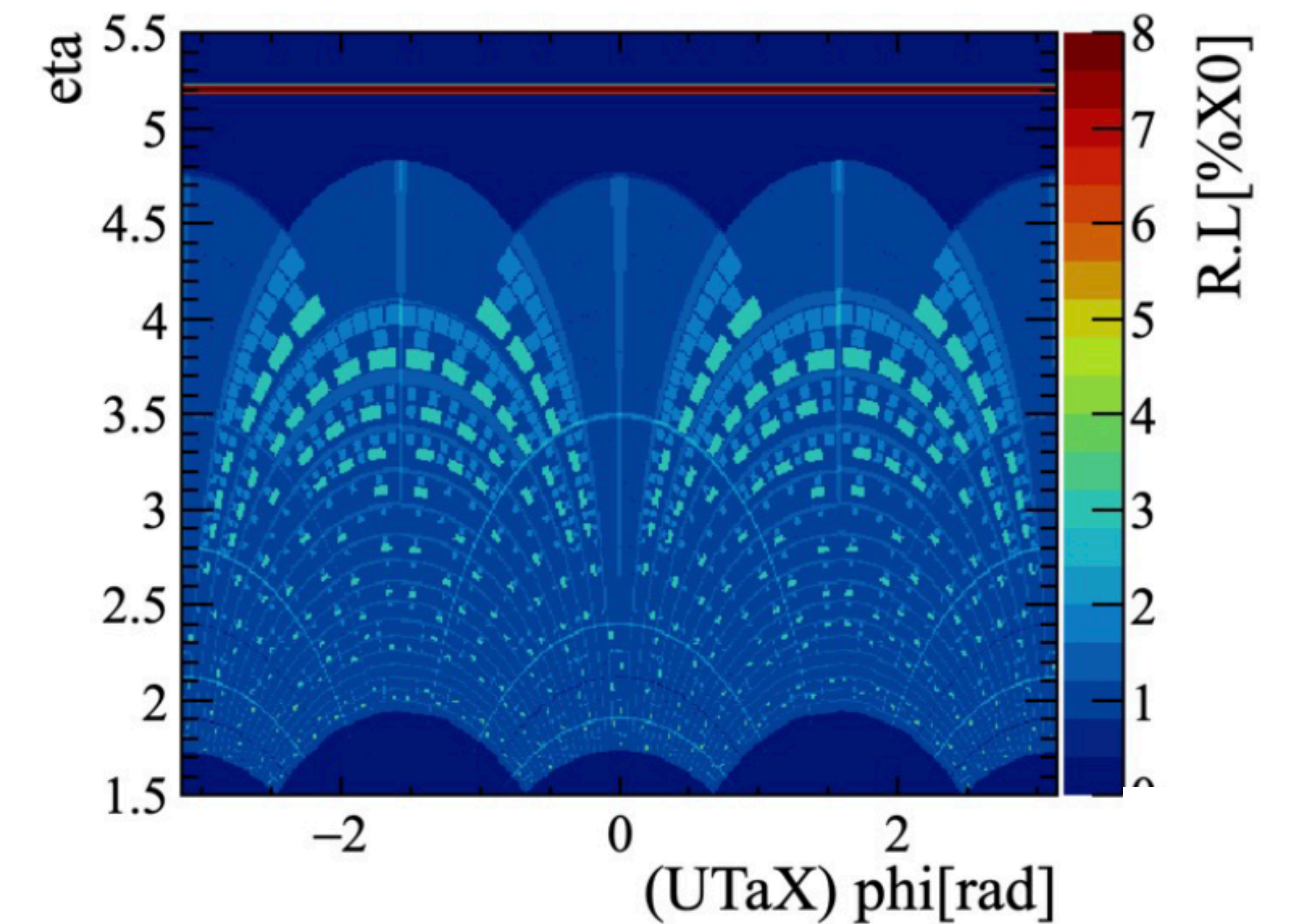
(Unit: mm)	Thickness	W×L
Pixel Sensor	0.200	20.2 × 21.4
lpGBT	1.250	9 × 9
VTRx+	4.000	20 × 10
HybridFlex	0.200	142.16 × 59.18
Kapton Tape	0.100	142.16 × 1357.72
BareStave	4.000	142.16 × 1600.28







	Thickness [mm]	RL ($2<\eta<4.5$) [% X_0]
Pixel Sensor	0.200	0.24
lpGBT	1.250	0.07
VTRx+	4.000	0.13
HybridFlex	0.200	0.28
Kapton Tape	0.100	0.27
BareStave	4.000	0.21
One plane	**-**	**1.20**



Material budget studies

C. Renard

If we optimise the use of the lpGBT e-links

Front modules:
InShrt:0.775435%X_0
InLong:0.749611%X_0
MidIn:0.706341%X_0
MidOut:0.697616%X_0

Distance from centre: 2mm

Back modules:
InShrtInv:0.775435%X_0
InLongInv:0.749611%X_0
MidInInv:0.706341%X_0
MidOutInv:0.697616%X_0

Next sensor:
Border: 0.08 mm
Daq: 1.845 mm
Reticule: 19.8x18.6 mm²
Thickness 200µm

Module:
Space: 0.1 mm
Bonding: 0,4 mm
2x7 sensors

Plane:
Overlap: 0 pixel
Beam pipe diam: 70 mm

Flux:
6.0 hit/cm2/Bxcol

PCB:
Double sided flex with copper under all components
4 more copper layers under lpGBT and VTRx+

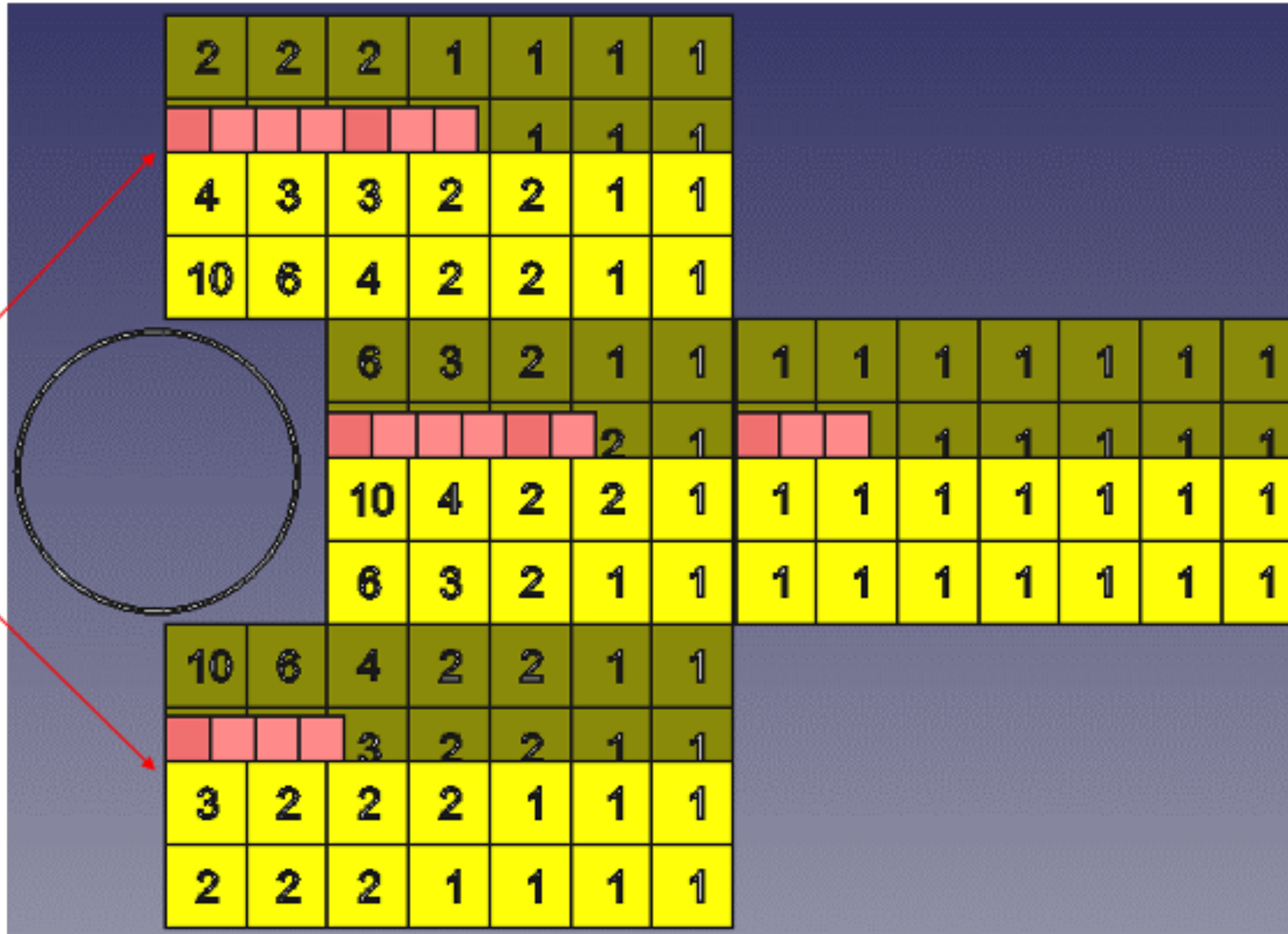
Material budget studies removing components

C. Renard

Front modules:
InShrt:0.634240%X_0
InLong:0.622079%X_0
MidIn:0.595904%X_0
MidOut:0.587179%X_0

Distance from centre: 2mm

Back modules:
InShrtInv:0.634240%X_0
InLongInv:0.622079%X_0
MidInInv:0.595904%X_0
MidOutInv:0.587179%X_0



Next sensor:
Border: 0.08 mm
Daq: 1.845 mm
Reticule: 19.8x18.6 mm²
Thickness 200µm
Module:
Space: 0.1 mm
Bonding: 0,4 mm
2x7 sensors
Plane:
Overlap: 0 pixel
Beam pipe diam: 70 mm
Flux:
6.0 hit/cm2/Bxcol
PCB:
Double sided flex with copper under all components
4 more copper layers under lpGBT

Material budget studies removing components

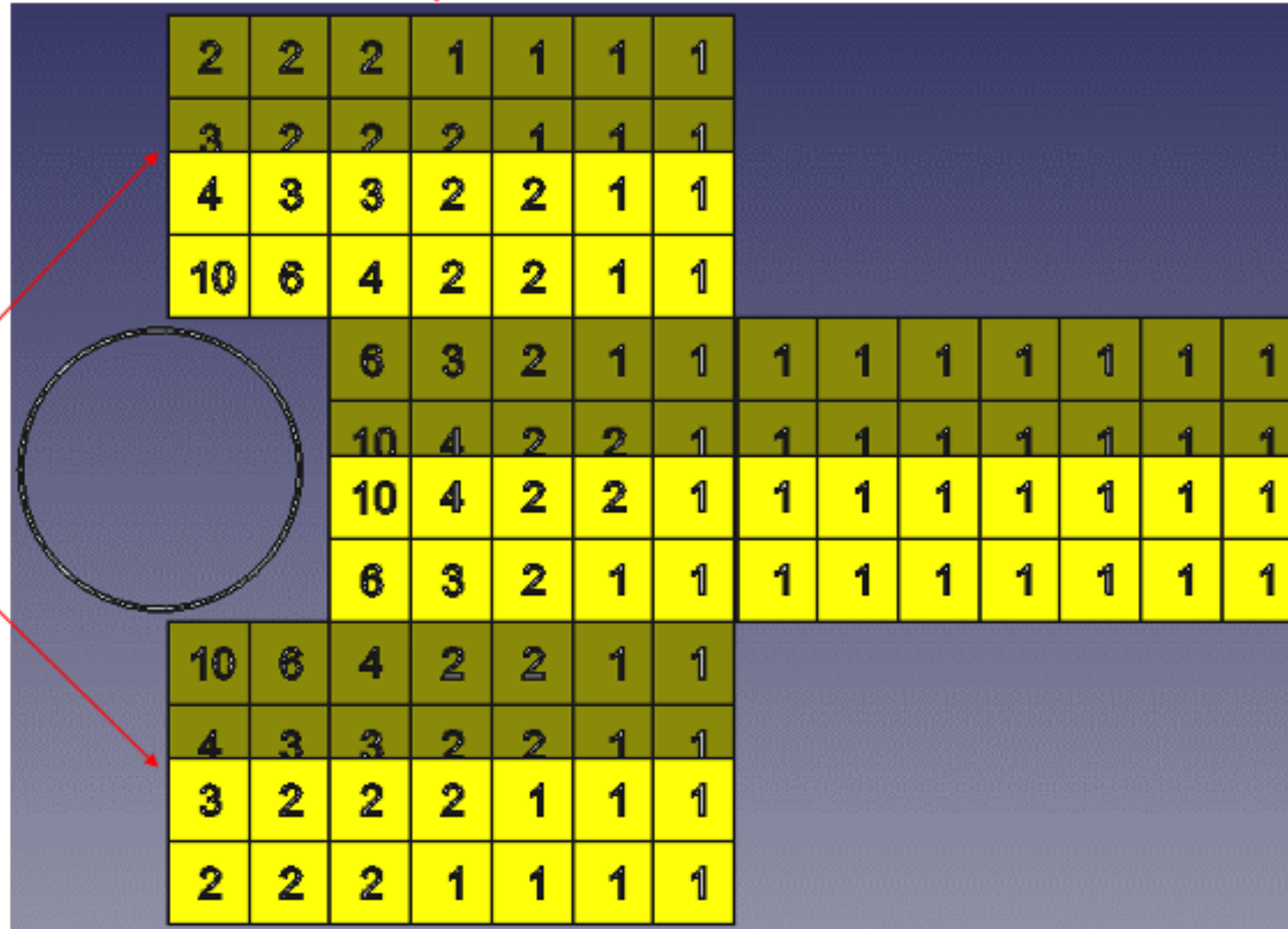
C. Renard

Front modules:
InShrt:0.467630%X_0
InLong:0.467663%X_0
MidIn:0.467663%X_0
MidOut:0.467663%X_0

Distance from centre: 2mm

Back modules:
InShrtInv:0.467630%X_0
InLongInv:0.467663%X_0
MidInInv:0.467663%X_0
MidOutInv:0.467663%X_0

No lpGBT and no VTRx+ in modules



Next sensor:
Border: 0.08 mm
Daq: 1.845 mm
Reticule: 19.8x18.6 mm²
Thickness 200µm

Module:
Space: 0.1 mm
Bonding: 0,4 mm
2x7 sensors

Plane:
Overlap: 0 pixel
Beam pipe diam: 70 mm

Flux:
6.0 hit/cm2/Bxcol

PCB:
Double sided flex with copper under all components

Material budget studies thiner chips

C. Renard

No lpGBT and no VTRx+ in modules

Front modules:
InShrt:0.409254%X_0
InLong:0.409271%X_0
MidIn:0.409271%X_0
MidOut:0.409271%X_0

Distance from centre: 2mm

Back modules:
InShrtInv:0.409254%X_0
InLongInv:0.409271%X_0
MidInInv:0.409271%X_0
MidOutInv:0.409271%X_0

2 2 2 1 1 1 1
3 2 2 2 1 1 1
4 3 3 2 2 1 1
10 6 4 2 2 1 1
6 3 2 1 1 1 1 1 1 1 1 1
10 4 2 2 1 1 1 1 1 1 1 1
10 4 2 2 1 1 1 1 1 1 1 1
6 3 2 1 1 1 1 1 1 1 1 1
10 6 4 2 2 1 1
4 3 3 2 2 1 1
3 2 2 2 1 1 1
2 2 2 1 1 1 1

Next sensor:
Border: 0.08 mm
Daq: 1.845 mm
Reticule: 19.8x18.6 mm²
Thickness 100µm

Module:
Space: 0.1 mm
Bonding: 0,4 mm
2x7 sensors

Plane:
Overlap: 0 pixel
Beam pipe diam: 70 mm

Flux:
6.0 hit/cm2/Bxcol

PCB:
Double sided flex with copper under all components