Serveur avec accélérateur FPGA sur la plateforme ACP au LLR

- Dell 7425 2 x (AMD/EPYC 7551 32 cœurs), 256Go

- carte accélérateur FPGA Xilinx Alveo U280

- CentOS 7.6.1810

- Vivado Design Suite + SDAccel 2019.1

Ressources FPGA utilisées pour RDFT: C5GT

HLD FPGA Reports (Beta) View reports...

Area analysis of system
(area utilization values are estimated)
Notation *file:X* > *file:Y* indicates a function call on line X was inlined using code on line Y.

Collapse All | Expand All

	ALUTs	FFs	RAMs	DSPs	Details
Kernel System (Logic: 8%)	**70690 (31%)**	**73328 (16%)**	**467 (38%)**	**6 (2%)**	
Board interface	51152	45420	366	0	• Platform i...
Global interconnect	9588	10682	0	0	• Global int...
rdft	**9950 (4%)**	**17226 (4%)**	**101 (8%)**	**6 (2%)**	• **Number of ...**
Function overhead	1618	1596	0	0	• Kernel dis...
Block0	132 (0%)	0 (0%)	0 (0%)	2 (1%)	
Block1	7362 (3%)	11687 (3%)	69 (6%)	4 (1%)	
Block2	838 (0%)	3943 (1%)	32 (3%)	0 (0%)	

LS = 256

ALUT = adaptive look-up-table

31% = 70 690 ---> **228 000** ALUT for 301 000 LEs ---> 1.3 LEs / ALUT

ALM (adaptive logic module) = 113 560 ---> 1 ALM = 2 - 3 ALUT

FF = flip-flop (6% of **458 300**)

RAM = internal memory block (38% of **1229**)

DSP = internal digital signal processor (2% of **300**)

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Block0	132 (0%)	0 (0%)	0 (0%)	2 (1%)	
Computation	132	0	0	2	
rdft_lut_scal_c5gt.cl:19	132	0	0	2	
Block1	7362 (3%)	11687 (3%)	69 (6%)	4 (1%)	
Block2	838 (0%)	3943 (1%)	32 (3%)	0 (0%)	

rdft_lut_scal_c5gt.cl

```
1  //__attribute__((reqd_work_group_size(512,1,1)))
2  __kernel void rdft(__global float* restrict x, __global float* restrict lutrsin, __global float*
       restrict lutrcos) {
3
4     int N = (get_global_size(0)-1)*2;
5     int num_vectors = N;
6
7     float X_real = 0.0f;
8     float X_imag = 0.0f;
9
10    float lutcos, lutsin;
11
12    int ilut, n = get_global_id(0);
13
14    for(int i=0; i<num_vectors; i++) {
15
16       if (i == 0) {
17         ilut = 0;
18       } else if (i < n) {
19         ilut = n*(n-1)/2+n+i;
20       } else {
21         ilut = i*(i-1)/2+i+n;
22       }
23
24       lutcos = lutrcos[ilut];
25       lutsin = lutrsin[ilut];
26
27       X_real += x[i] * lutcos;
28       X_imag -= x[i] * lutsin;
29    }
30
31    barrier(CLK_GLOBAL_MEM_FENCE);
32
33    if(get_global_id(0) == 0) {
34       x[0] = X_real;
35    }
36    else if(get_global_id(0) == get_global_size(0)-1) {
37       x[1] = X_real;
38    }
39    else {
40       x[get_global_id(0) * 2] = X_real;
41       x[get_global_id(0) * 2 + 1] = X_imag;
42    }
43 }
44
45
```

ressources par ligne de code du noyau OpenCL

Ressources FPGA utilisées pour RDFT: U280

```
==========================================================
Version:    xocc v2019.1 (64-bit)
Build:      SW Build 2552052 on Fri May 24 14:47:09 MDT 2019
Copyright:  Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
Created:    Wed Oct 30 10:09:44 2019
==========================================================

----------------------------------------------------------
Design Name:                bin_rdft_lut_scal_c5gt_hw
Target Device:              xilinx:u280:xdma:201910.1
Target Clock:               300.000000MHz
Total number of kernels: 1
----------------------------------------------------------

Kernel Summary
Kernel Name  Type  Target                OpenCL Library
-----------  ----  ------------------    -------------------------
rdft         clc   fpga0:OCL_REGION_0    bin_rdft_lut_scal_c5gt_hw

Compute Units
-------------
1                  =  one working group with 256 working elements
```

Ressources FPGA utilisées pour RDFT: U280

```
--------------------------------------------------------------------------------
OpenCL Binary:      bin_rdft_lut_scal_c5gt_hw
Kernels mapped to: clc_region

Timing Information (MHz)
Compute Unit  Kernel Name  Module Name  Target Frequency  Estimated
------------  -----------  -----------  ----------------  ---------
rdft_1        rdft         rdft         300.300293        411.015198

Area Information
Compute Unit  Kernel Name  Module Name  FF    LUT   DSP  BRAM  URAM
------------  -----------  -----------  ----  ----  ---  ----  ----
rdft_1        rdft         rdft         5408  5201  17   20    0
--------------------------------------------------------------------------------
```

```
> platforminfo /opt/xilinx/platforms/xilinx_u280_xdma_201910_1/
                                    xilinx_u280_xdma_201910_1.xpfm
```

```
Resource Availability
  Total
    LUTs:  1 203 870      vs. 228 000, C5GT
    FFs:   2 472 213      vs. 458 300, C5GT
    BRAMs: 1 816          vs. 1 229, C5GT
    DSPs:  9 020          vs. 300, C5GT
```

Les étapes de la simplification du noyau

Area Information

Compute Unit	Kernel Name	Module Name	FF	LUT	DSP	BRAM	URAM
rdft_1	rdft	scaled_fixed2ieee_29_1_s	336	483	0	0	0
rdft_1	rdft	generic_sincos_float_s	2756	3495	11	0	0
rdft_1	rdft	rdft	11798	14296	42	24	0

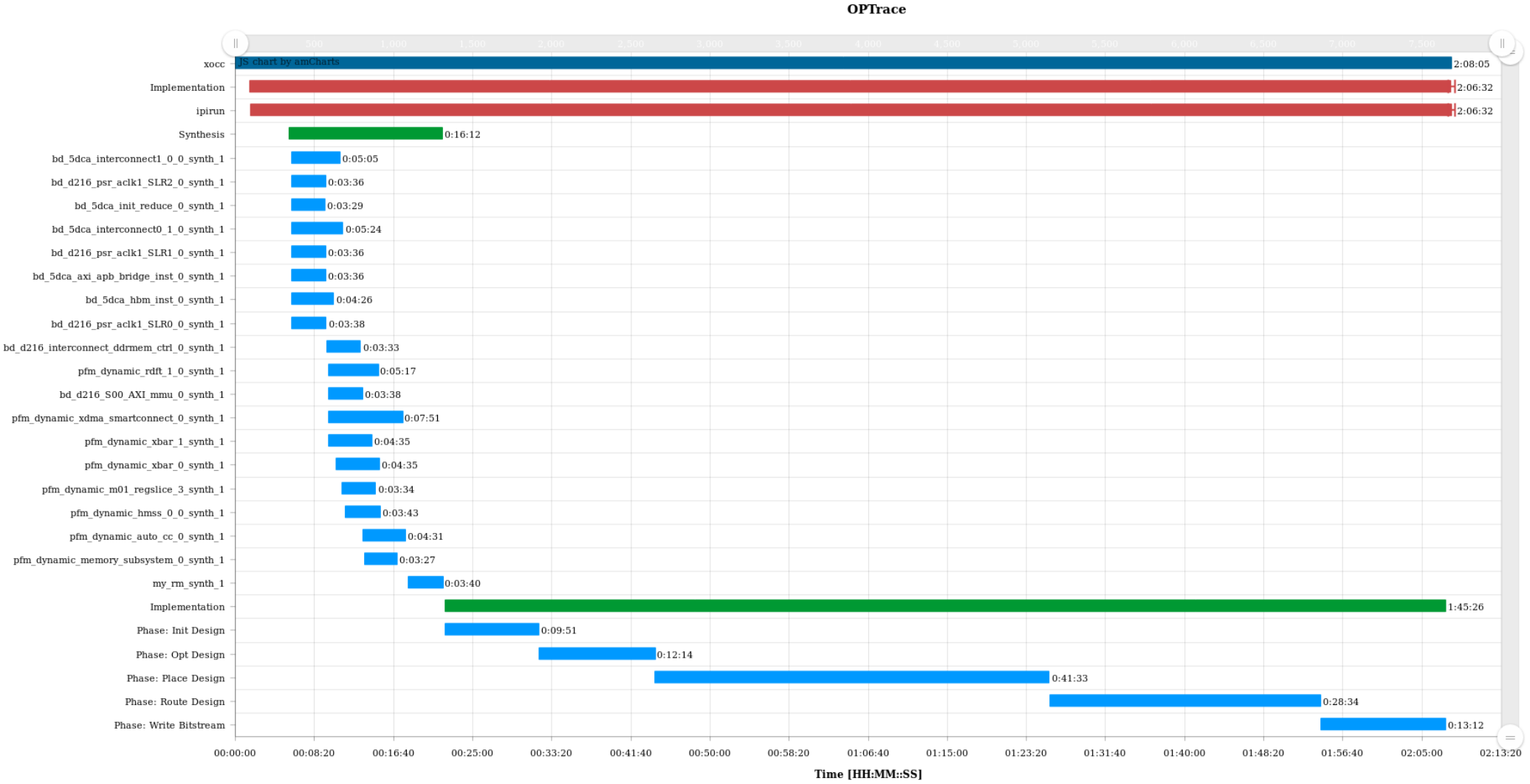
LUT sin/cos

rdft_1	rdft	rdft	8220	8840	29	20	0

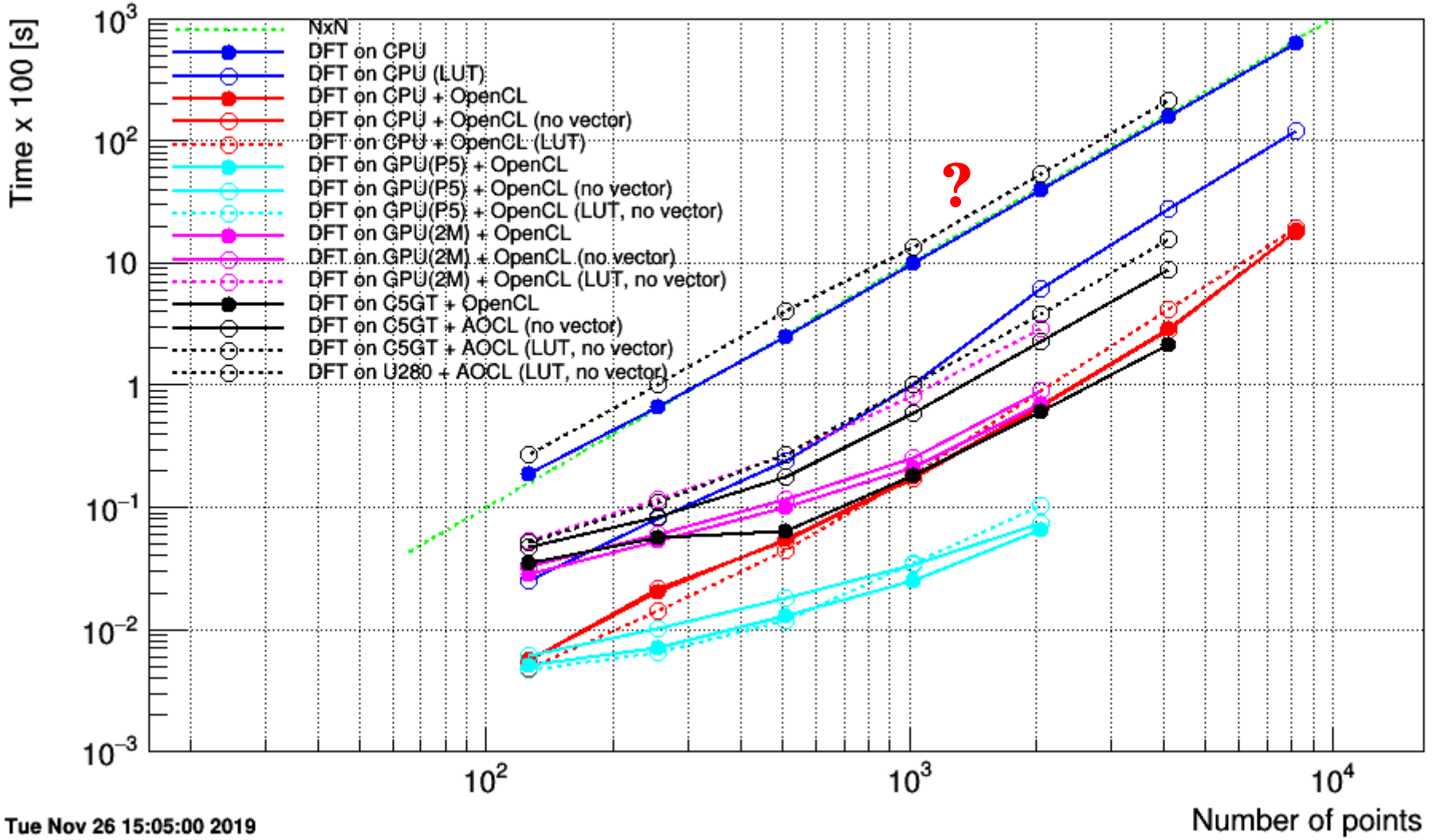
LUT sin/cos + scalar

rdft_1	rdft	rdft	5408	5201	17	20	0

Compilation U280



Temps d'exécution pour RDFT



Au LPC en 2020

On reste sur Intel:

MUSTANG-F100-A10-R10

Enlarge

Images are for reference only
See Product Specifications

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Mouser No:	458-MSTANGF100A10R10
Mfr. No:	MUSTANG-F100-A10-R10
Mfr.:	IEI
Customer No:	Customer No
Description:	Networking Modules PCIe FPGA Highest Performance Accelerator Card with Arria 10 1150GX support DDR4 2400Hz 8GB, PCIe Gen3 x8 interface
Lifecycle:	NEW **New Product:** New from this manufacturer.
Datasheet:	MUSTANG-F100-A10-R10 Datasheet
ECAD Model:	Build or Request PCB Footprint or Symbol

Download the free Library Loader to convert this file for your ECAD Tool. Learn More.

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Stock:	18 Can Dispatch Immediately
On Order:	0
Factory Lead Time:	3 Weeks
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2	1 638,00 €	3 276,00 €