28 nm electronics developments for future pixel detectors

Marlon Barbero, Roua Boudagga, Denis Fougeron, Eva Joly, Mohsine Menouni

CPPM - Aix-Marseille Univ, France

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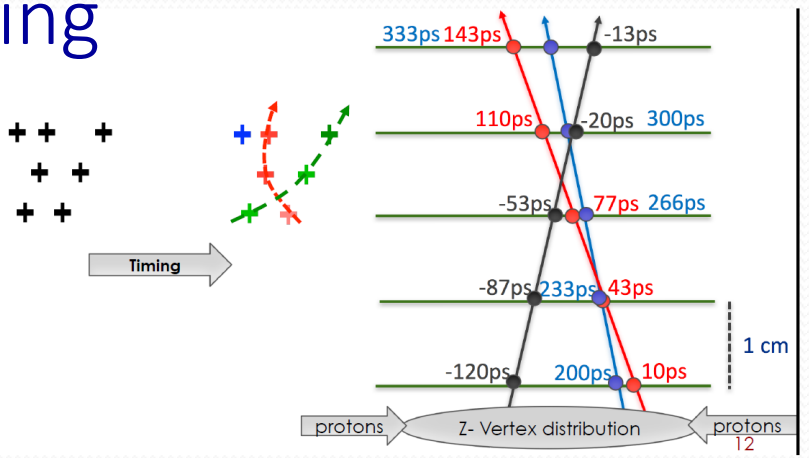
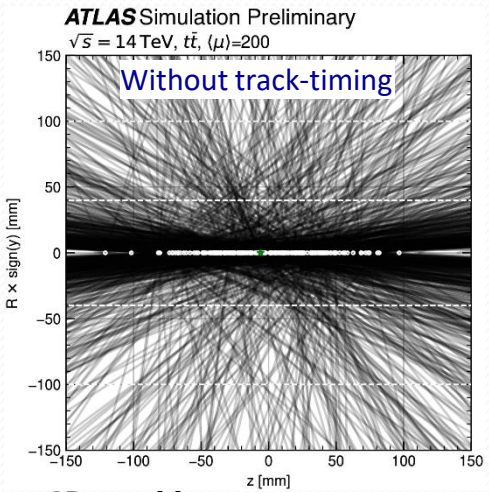
Outline

- Introduction: Timing effect
- 4D tracking in the future experiments
- Electronics and sensor requirements for 4D tracking
- R&D activities at CPPM
  - 28 nm chip design
  - SEE/SET Testing
  - Ring Oscillator Design
  - Analog FE pixel array design and simulations
  - Preliminary test results
- Conclusion and perspectives

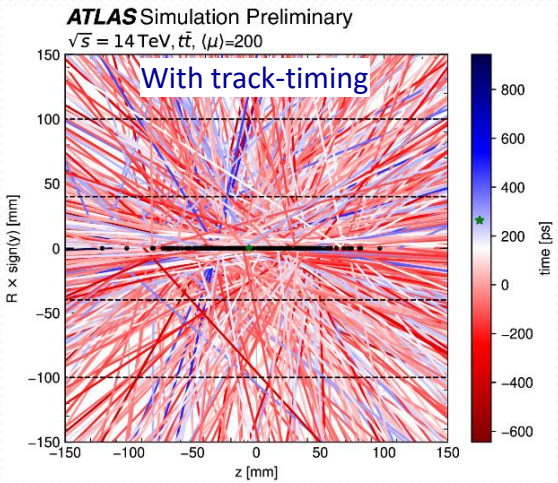
The effects of timing

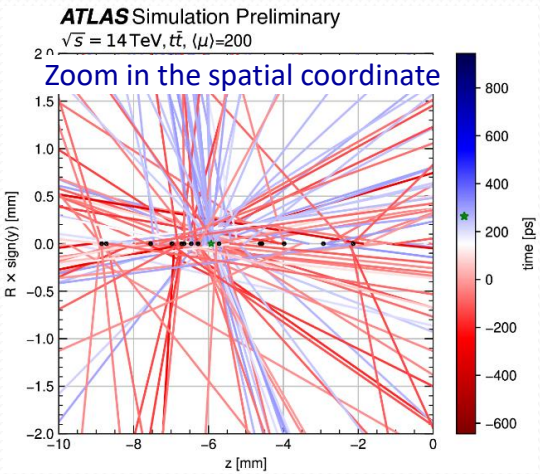
- **Pile-Up (PU)** level increase for the **HL-LHC**
  - PU average of 200 during HL-LHC (5-10 × LHC)
  - PU adds a new level of ambiguity to the reconstruction process
  - When **timing information is available for the tracks**, the association of track to vertices becomes less ambiguous





timing





- **4D tracking**
  - Using **timing at each layer** along the tracks
  - For the rate of 200 PU events/BC
    - Timing **resolutions of 30 ps** is expected to **reduce by a factor of 5** the number of pileup tracks per primary vertex

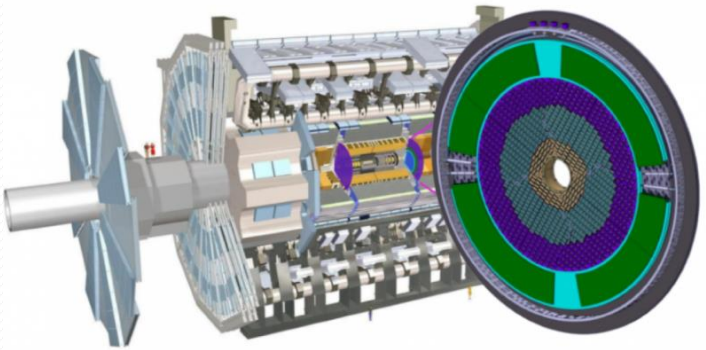
Investigating the impact of 4D Tracking in ATLAS Beyond Run 4, Tech. rep., CERN, Geneva (2023), ttps://cds.cern.ch/record/2870326

Timing information will be more important at future high-energy, high-luminosity hadron colliders with much higher levels of pileup

4D tracking in future experiments

Hadron colliders

- Timing layers (HL-LHC) Run 4
  - CMS and ATLAS are building **silicon-based timing detector** layers that will timestamp each track with **a precision of 30 ps**
  - ATLAS High Granularity Timing Detector (**HGTD**) and the CMS Timing Detector (**MTD**) placed in the forward regions ($2.4<|\eta|<4.0$)
  - Based on novel Low Gain Avalanche Detectors (**LGADs**)
  - The readout chip HGTD is an array of 15×15 channels of 1.3×1.3 mm²
- The ATLAS and CMS tracker Run 5
  - The two innermost pixel layers will need to be replaced after 5 years (LS4)
  - **Pixel time resolution of 50 ps** is needed to boost the tracking performances
- Future Circular Collider tracker (FCC-hh)
  - Efficient reconstruction of charged particle tracks in an environment of high pileup density (1000 pileup)
  - Position < 10 µm, Time resolution < 10 ps
  - Radiation levels: 40 Grad and 6×10^{17}neq/cm² (40 × HL-LHC)
  - A big challenge in sensor and ASIC design



ATLAS High Granularity Timing Detector (HGTD)

Electron colliders

- Linear colliders (ILC, CLIC) and Circular colliders (FCPC, FCC-ee)
  - High spatial precision is required for physics measurements -> **Pixel size < 25 µm x 25 µm**
  - Time resolution at the **ns level is sufficient**
  - Potential applications of timing at the ps level

Electron Ion Collider (EIC)

- 4D detectors based on AC-LGADs are planned to provide timing capability
- **Time resolution of 30 ps** is required
- Spatial resolutions of 15 µm to 150 µm depending on the location.

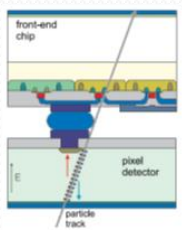
Muon Collider

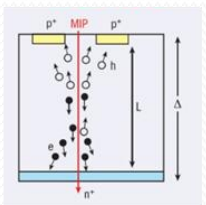
- Initial studies indicate that single hit resolutions of **20-30 ps** are sufficient to reduce the **Beam-Induced Background (BIB)** to a manageable level

Pixel design for 4D tracking

- For the next upgrades or next generation of hadron collider :
  - ATLAS, CMS and LHCb trackers upgrades (Run5), or for FCC–hh -> Very long-term
  - High **spatial resolution** and high **time precision**
  - Very high **radiation tolerance**
  - **Hybrid pixels** with a dedicated ASIC bonded to the sensor is the best suited to these applications

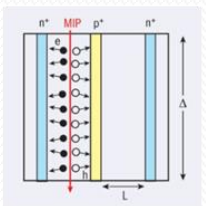
Rad-hard





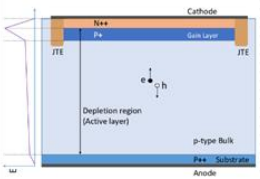
Planar sensors

Very rad-hard



3D sensors

Precise timing

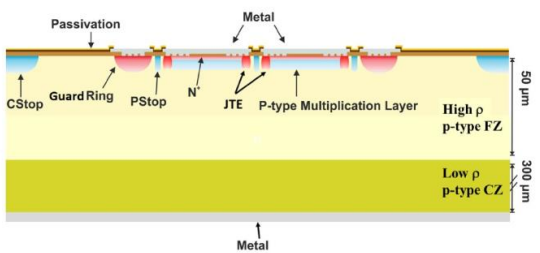


LGAD sensors

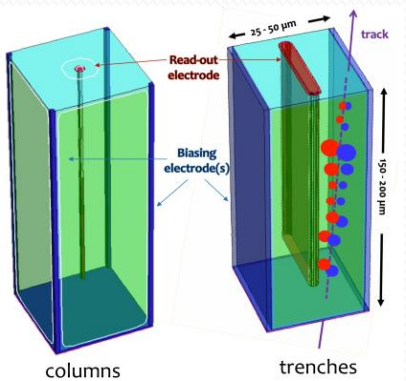
ATLAS/CMS inner layers upgrades

Pixel size	25µm × 25 µm
Sensor capacitance	< 50 fF
Time resolution	< 50 ps RMS
Consumption (pixel)	<5 µA
Threshold	<600 e-
Hit rate	8 GHz/cm²
Hit rate (pixel)	5 kHz
TID	> 1 Grad

- Sensor candidates currently being considered for 4D tracking
  - **LGAD sensors** with modification of the gain implant profile
    - Not yet satisfying a fluence > 2-3 × 10^{15} MeV neq/cm²
  - **3D-trench sensors** developed and tested within the TimeSPOT project
    - No performance loss up to fluences of 2.5 × 10^{16} MeV neq/cm²



M. Ferrero et. Al : Nuclear Inst. and Methods in Physics Research, A 919 (2019) 16–26



Doug Berry:FERMILAB-CONF-22-284-PPD1

- Front end electronics
  - Need of **higher density** and **higher speed** regarding the RD53 chip designed with the 65 nm process
  - **28nm CMOS technology** is considered as the next node for highly integrated chips such as pixel readout chips

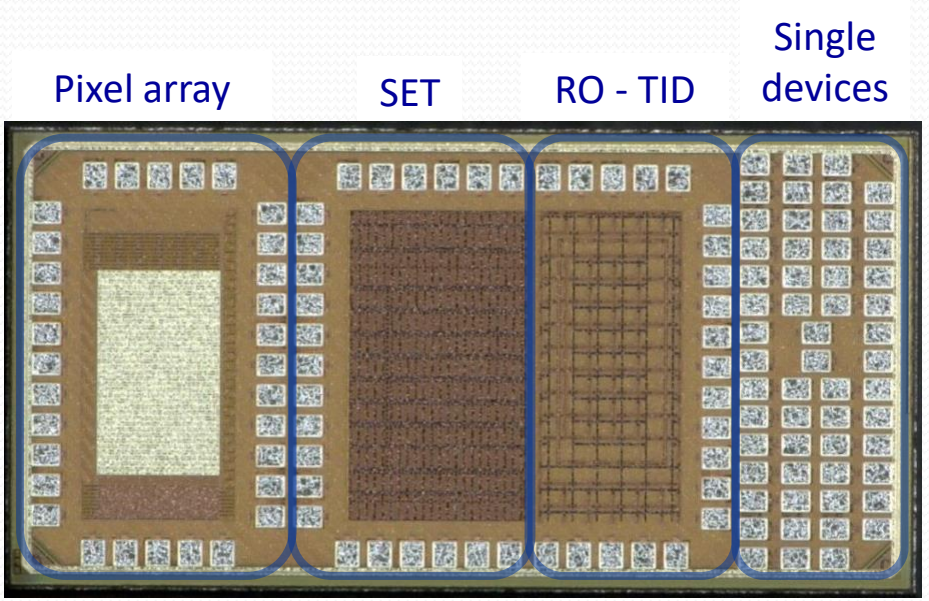
CPPM activities

R&D activities at CPPM

- R&D around **hybrid pixels** for **future upgrades and future colliders** with the 28nm CMOS technology
  - The **radiation tolerance** of the 28nm process up to 1-2 Grad
  - **Time measurement** with a resolution better than 50ps
  - Small pixel size -> **25µm × 25µm**
- Context
  - RD53 collaboration shows a strong interest in these developments for the future upgrades of ATLAS and CMS trackers
  - The project is part of the R&D project DEPHY and can be extended to the other IN2P3 labs interested in the 28 nm process
  - This work is done with the **CERN R&D Program** on technologies for **Future Experiments**
  - CPPM is a member of two working groups within the DRD (ECFA) projects
    - **WG 7.3a** (4D and 5D techniques) to develop front ends with **high temporal resolution**
    - **WG 7.4b** (Advanced and hardened CMOS nodes) to study the **effects of radiation** on highly advanced processes

28 nm chip design

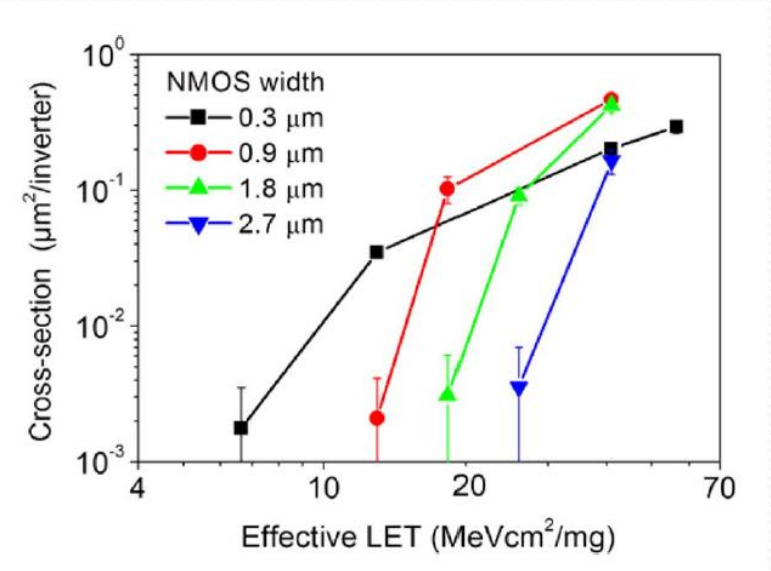
- R&D on hybrid pixels
  - Process qualification in terms of performance for analog, low-power and low-noise circuits
  - Architecture studies
  - Fast charge amplifier array
- Study of Single Event Effects (SEE)
  - Measure the **SET cross-section**
  - Measure the **SET pulse width** with a good resolution < 20 ps
  - Measure the effect of the std cell size
- TID tests and qualification
  - Compatibility with typical dose levels for future projects
  - 28 nm process device qualification
  - **Gate delay** evolution with TID and the effect of the std cell size
  - TID Effects modeling → Analog and digital simulations with TID effects



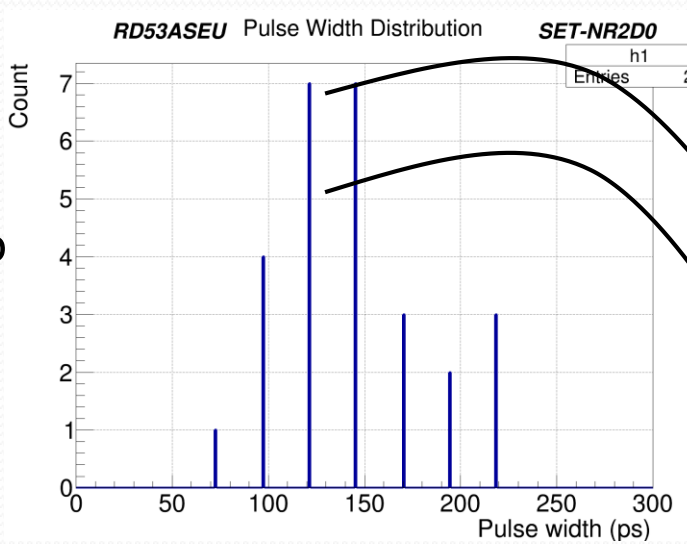
- Mini@sics of 2×1 mm2 received June 2023, consisting of 4 main blocks
  - Analog pixel array (25×25 µm2) with Fast charge amplifiers for high time resolution
  - SET test structures
  - Ring Oscillators for TID tests on digital standard cells
  - Test structures for TID tolerance studies

SEE/SET Testing

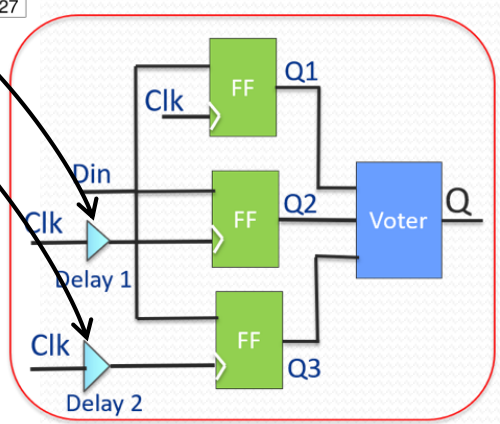
- Single Event Transient (SET) sensitivity increases with process advance
  - Propagation through combinatorial logic and generate SEU in memories
  - Sensitivity to SET increases with speed
- Implementation of test structures to characterize the 28 nm process for SET tolerance



- Objectives :
  - Measure the SET cross-section
  - Measure the SET pulse with a **good resolution < 20 ps**
- Allows as an example to define the delay to be used for the triplication with time delay mitigation

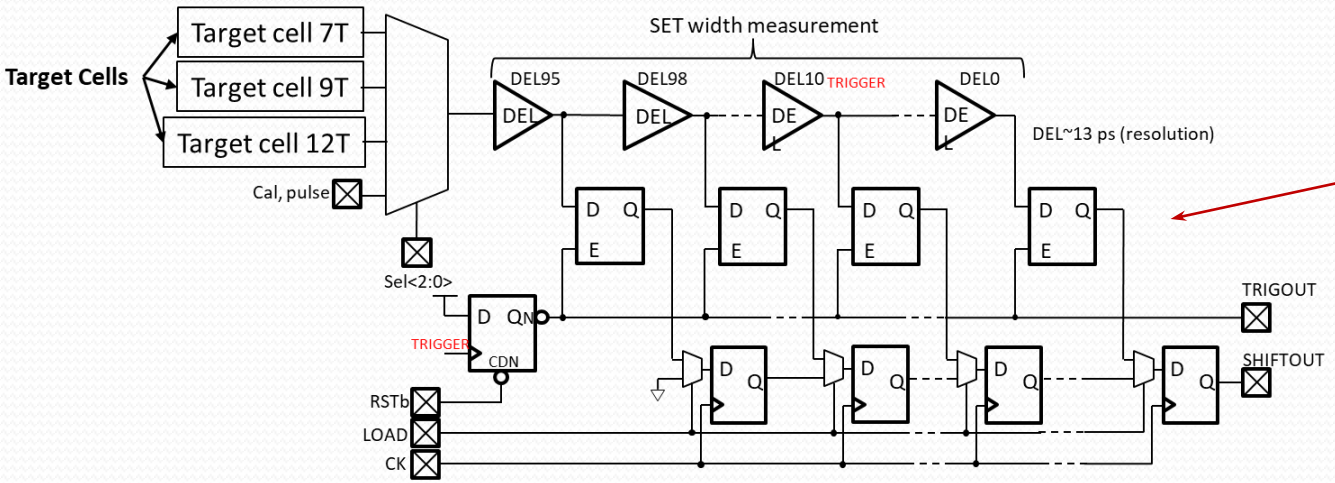


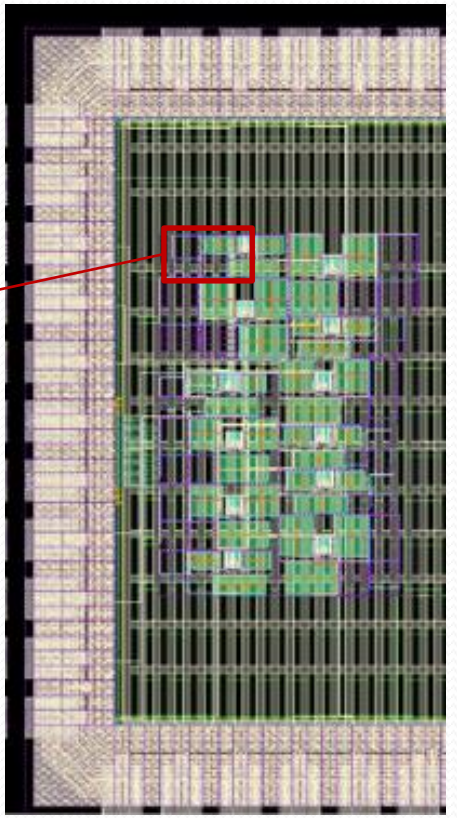
SEU tolerant design with temporal Mitigation



SET chip design

SET sub-bloc synoptic

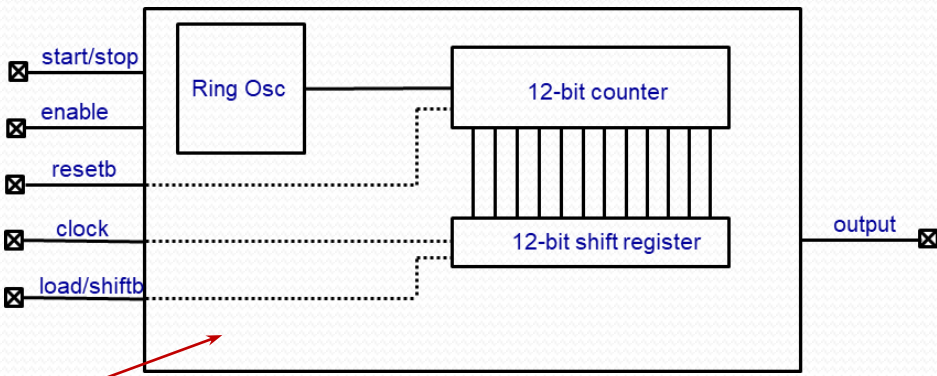




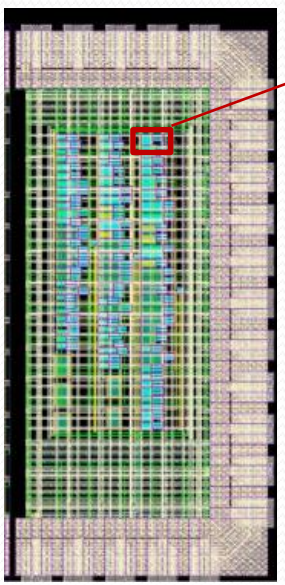
- Each sub-bloc contains
  - 3 target cells made up of thousands of basic cells + 1 calibration input
  - Circuit for SET width measurement 96 delay cells (13ps/cell) -> from a few ps to 1 ns
  - Shift register to send the data to the output when a trigger signal occurs
- 31 SET sub blocs
  - 24 uses SVT target cells (7T, 9T, 12T) -> **Effect of the cell size**
  - 7 uses LVT or HVT target cells -> Effect of **the device options**
- The whole bloc contains 6 inputs / 13 outputs
- In addition to SET testing, this constitutes a sub-block of the TDC required in the pixel front end design

Ring Oscillator chip design

- Study of the effect of TID on the performance of digital standard cells
- Timing of combinatorial or sequential cells
- Leakage currents and static power
- Effects of device size on TID tolerance
- Design based on the digital flow
- 96 Rosc sub-bloc
  - Cell size (7T, 9T,12T)
  - Driving (D0, D2, D4)
  - SVT, LVT, HVT

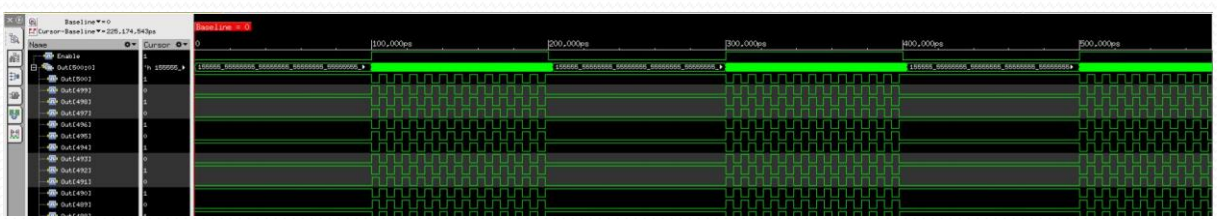


ROsc sub-bloc synoptic



Basic cells	Frequency (MHz)
INVD0	154
INVD2	222
NAND0	118
NAND2	143
NOR0	111
NOR2	139

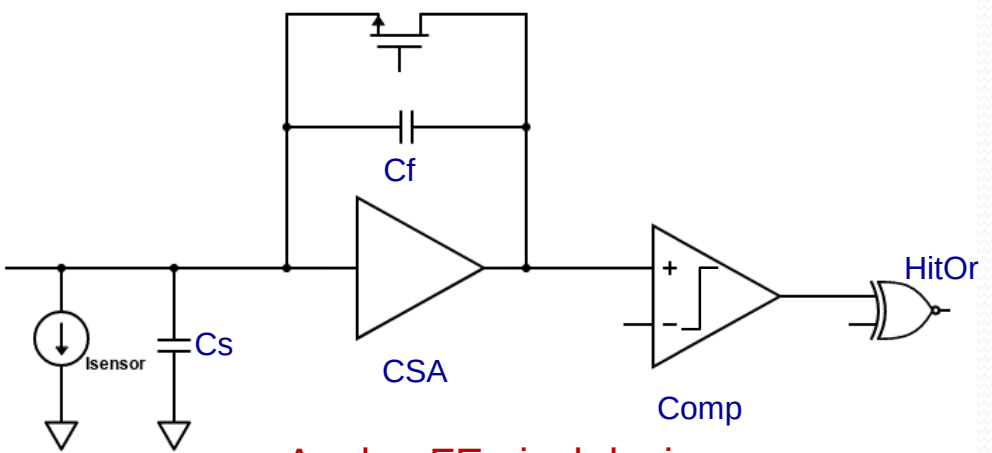
Simulation



Fast amplifier design

- Study the limits to **time resolution** in the analog front- end designed with the **28 nm CMOS** process
  - Effects of the Current bias, power supply, Bandwidth, Noise …
- Design and test a **pixel array of 36 × 12 cells** where only the analog part is considered and implemented
- The time resolution of the pixel:

$$\sigma^2_{total} = \sigma^2_{jitter} + \sigma^2_{timewalk} + \sigma^2_{Landau} + \sigma^2_{TDC}$$



Analog FE pixel design

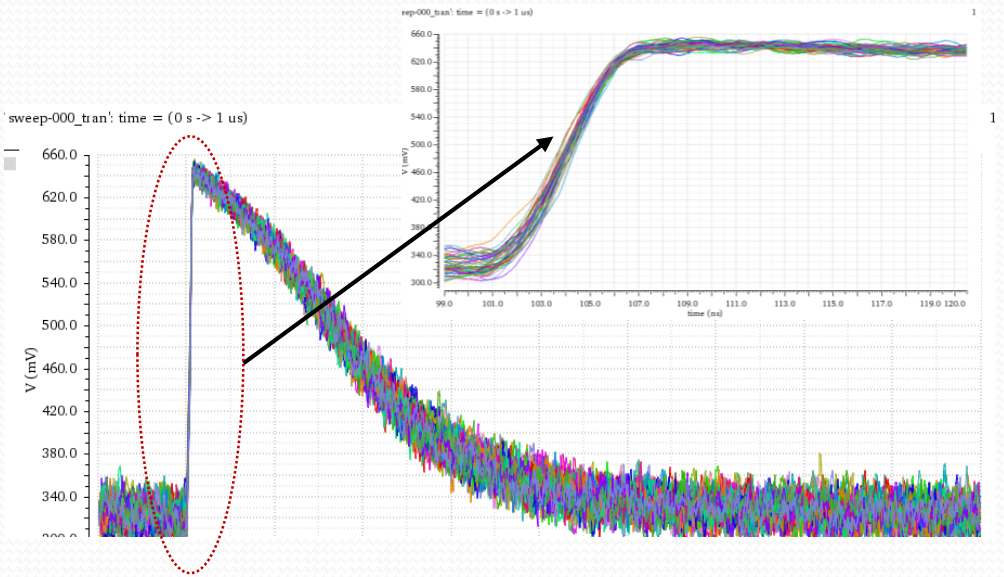
Minimizing the front-end jitter corresponds to :

- Low RMS noise of the charge amplifier (CSA)
- High output voltage
- Small rise time → High bandwidth

$$\sigma_{jitter} = \frac{\sigma_{noise}}{dV/dt} = \frac{t_r}{\left(\frac{S}{N}\right)}$$

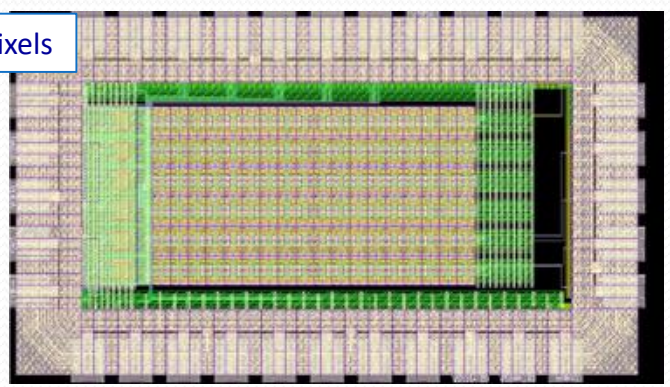
Analog FE pixel prototype

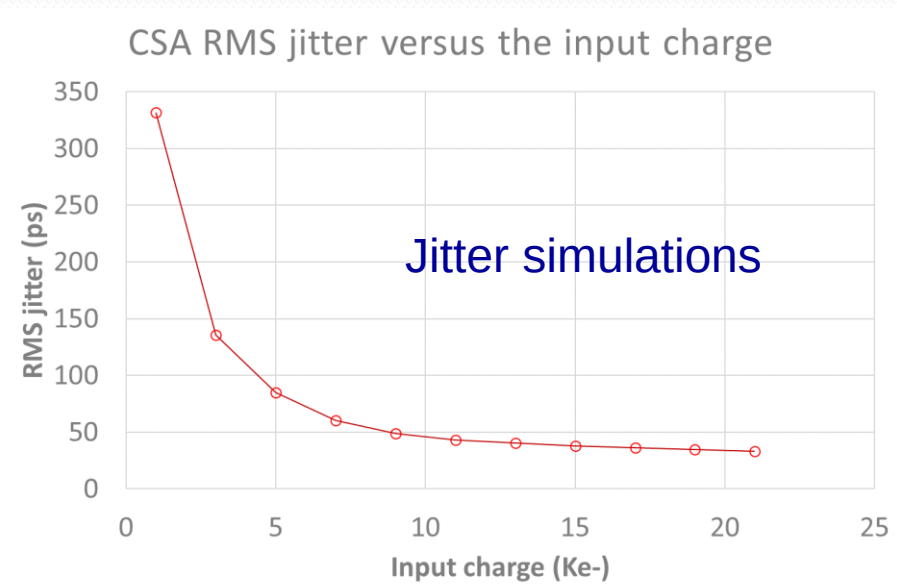
- For each pixel :
  - The charge amplifier current bias can be set in the range of 2µA-20µA
  - MOM capacitance connected to each preamplifier input -> test for different input capacitance values
- Large bandwidth buffers (> 1GHz) implemented and connected for a few pixels for direct jitter measurement
- Simulations for I_{CSA} = 5 µA
  - dV/dt = 100 mV/ns
  - RMS noise = 97 e- RMS for Cin = 100fF
  - Jitter < 100 ps RMS for input charge > 4 ke-
  - Jitter < 40 ps RMS for charge > 10 ke-
- Each pixel contains : CSA + Discriminator + 6 bit DAC
  - Size : 20 µm × 12 µm



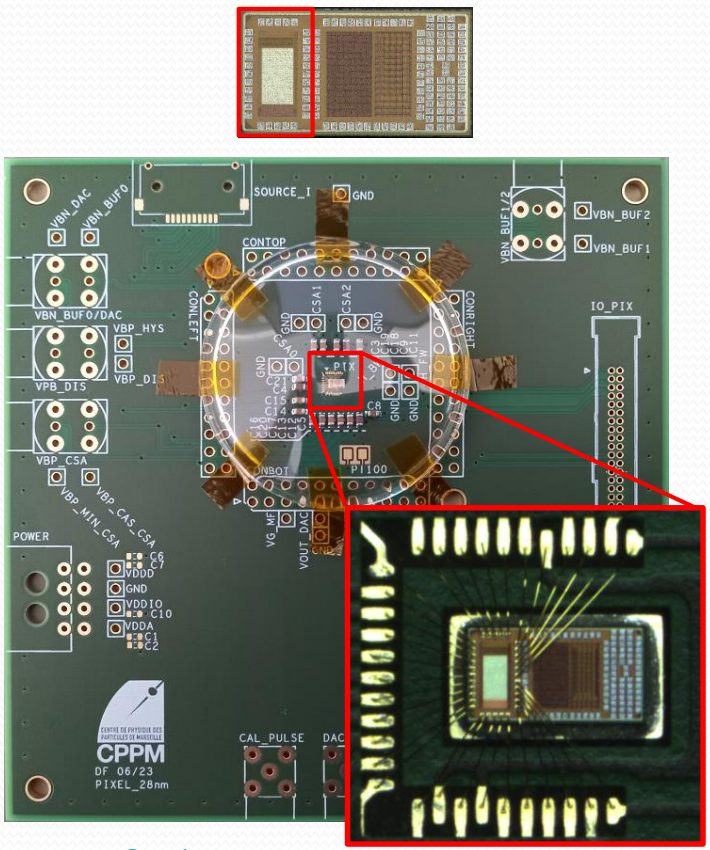
50 superimposed transient noise simulations

Pixel array of 36 × 12 pixels

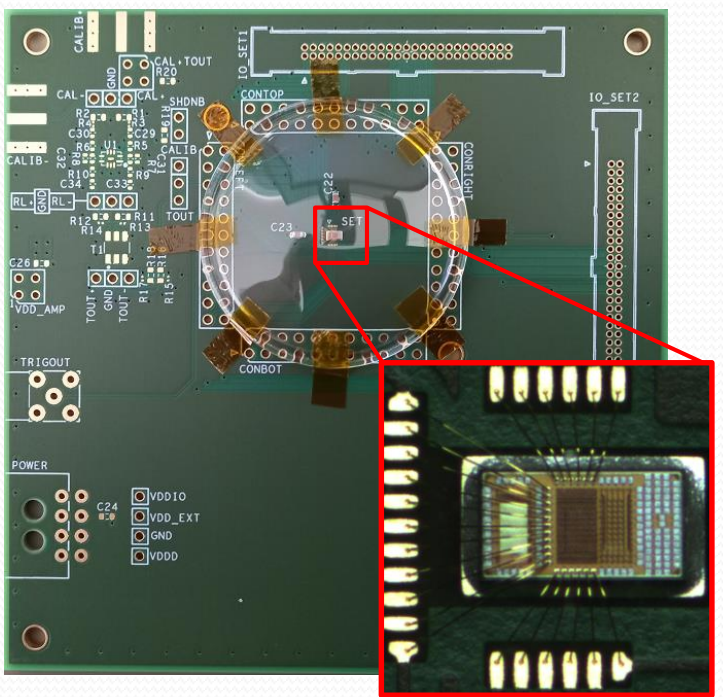




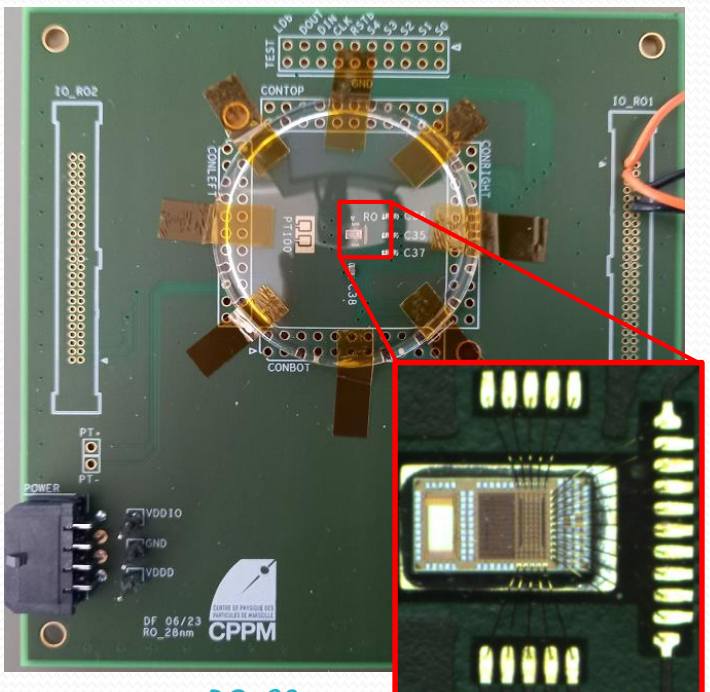
Prototypes 28nm sur PCB



Pixel_28nm



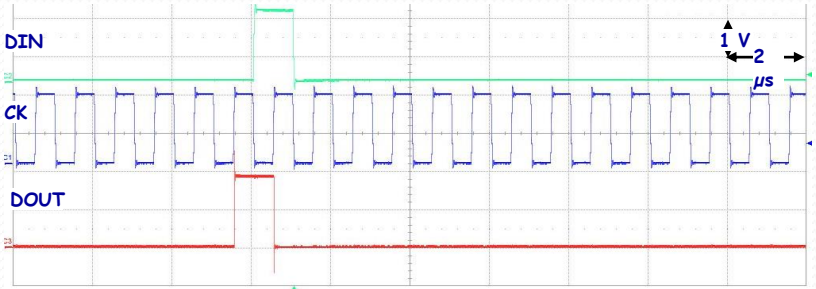
SET_28nm



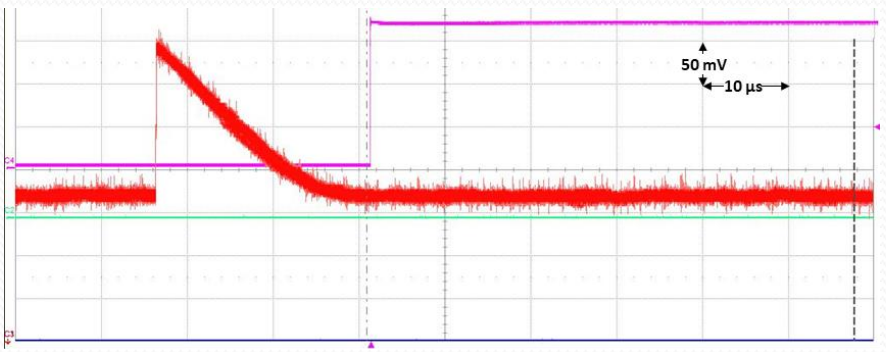
RO_28nm

Preliminary results

- The pixel array prototype is working properly
  - The 3456 registers can be configured correctly
  - The output signal of the test pixel is consistent with simulations
  - intensive testing under way
- Ring oscillators
  - Minor configuration issue but should not prevent testing of the various blocks
- SET block
  - To be tested soon
- Devices characterization
  - Waiting for the PCB with wire bonded block



Configuration SR chip Pixel_28nm (EN_INJ = '1' pixel 36)



Sortie CSA pixel 36

Conclusion and perspectives

- 28nm prototype test boards received the beginning of 2024
  - Testing has started and first results are quite promising
  - 4 different design to be tested and characterized
  - Existing test-setup based on a beagle-bone board to be used

- Continuation of the project
  - The project is part of the IN2P3 R&D DEPHY project
  - Functional tests to be done in Q2 2024
  - Irradiation tests (TID and SEE) in Q3-Q4 2024
  - A new 28 nm design focused on larger size pixel array
    - Implementation of TDC related to ToA and ToT
    - The possibility to bump bond the FE array with sensor array
  - Use of CERN PDK makes the design more manageable
  - Prototype submission scheduled for Q4 2024

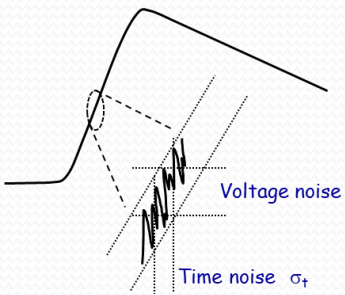
Thank you for your attention

Time resolution

The time resolution of a detector can be expressed as follows: $\sigma^2_{total} = \sigma^2_{jitter} + \sigma^2_{timewalk} + \sigma^2_{Landau} + \sigma^2_{TDC}$

σ_{jitter}

- Due to the noise of the electronic front-end including the sensor
- The jitter is proportional to the rise time and inversely proportional to the S/N ratio.
- The rise time depends on the FE bandwidth and is proportional to the drift time of charge in the sensor



$$\sigma_{jitter} = \frac{\sigma_{noise}}{dV/dt} = \frac{t_r}{\left(\frac{S}{N}\right)}$$

$\sigma_{timewalk}$

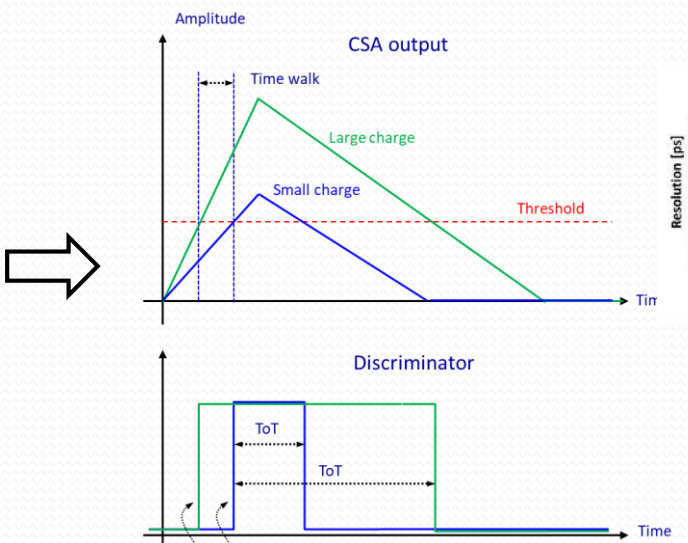
- Related to the variation of the deposited charge event-by-event
- Variation of the time of arrival (TOA)
- Time walk is corrected by :
  - variable threshold → Constant fraction discriminator (CFD)
  - constant threshold correction
    - Correct the time of arrival (TOA) with a calibration based on the time over the threshold (TOT)

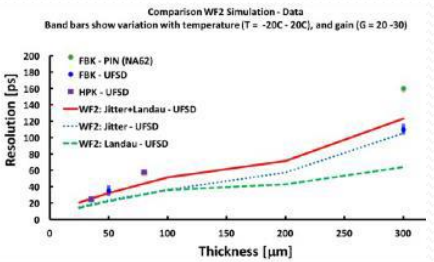
σ_{Landau}

- Due to the Landau distribution of the deposited charge
- Represents the spatial variation of the deposited charge along the path
  - Charges from different depths are collected at different times.
- The effect is small for thinner devices or sensors with short drift times
  - Absent in 3D detectors
  - Not negligible in LGAD sensors

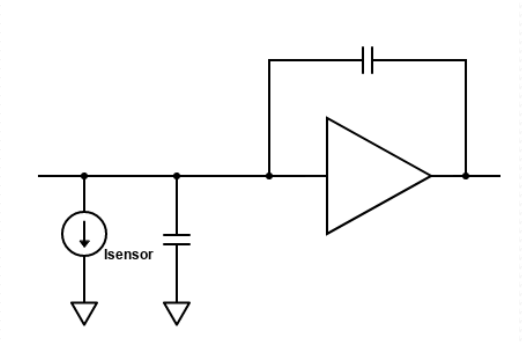
σ_{TDC}

- Due to the Time to Digital Converter (TDC) binning
- Bin size divided by $\sqrt{12}$ which is in general small





Front-end electronics and ASIC R&D

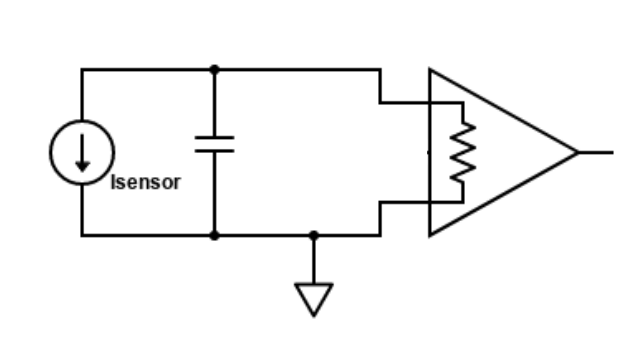


Charge amplifier (CSA)

Vout = CF×Qsensor

Slow slew rate

Less noise



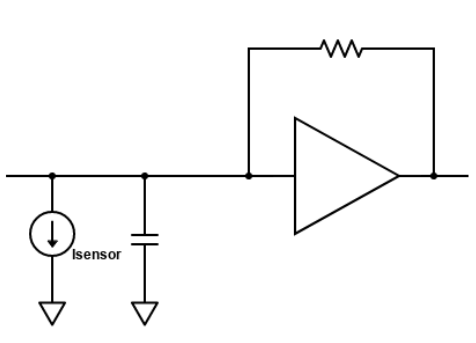
Current amplifier

Iout = A×Isensor

Fast

slew rate

High noise



Transimpedance amplifier

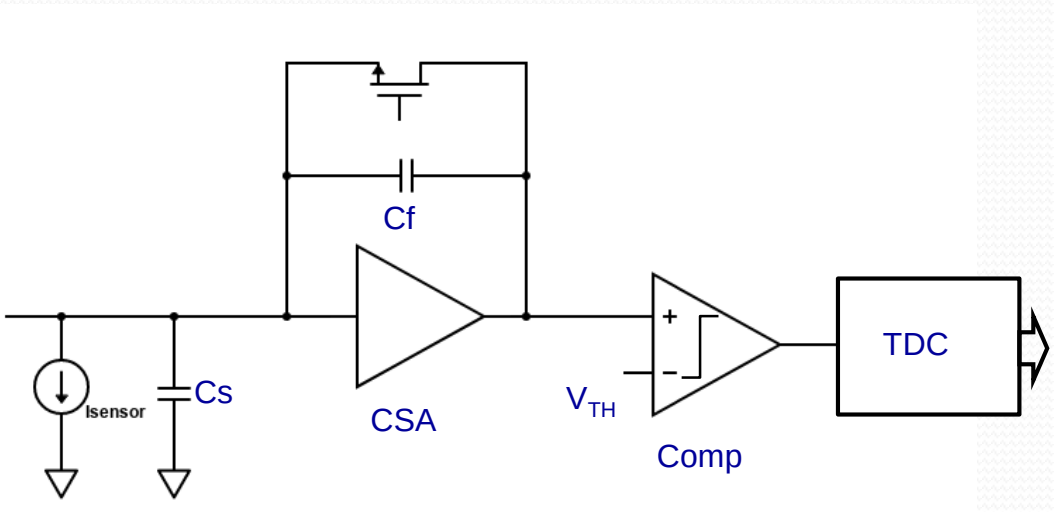
Low Rin

Vout = RF×Isensor

High bandwidth

High noise

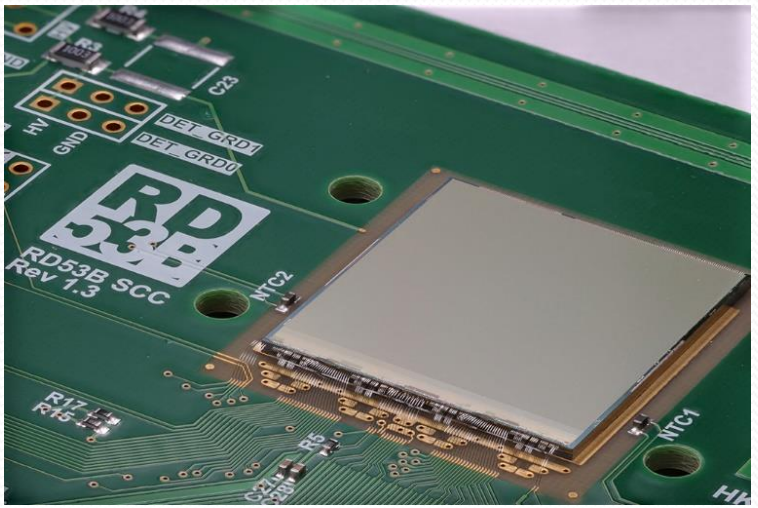
- The choice of the fast amplifier depends on the timing specifications and the sensor bandwidth

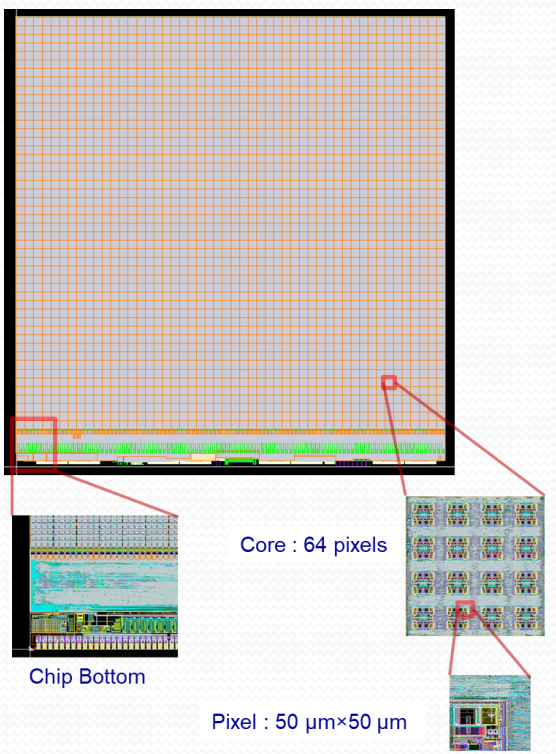


- Front end based on charge amplifier (CSA)
- High-resolution TDC
  - 1 TDC can be shared by several FEs
- TOA and TOT measurements

Circuit de lecture du détecteur

- ITkPixV2 : puce de lecture de production pour les pixels de ATLAS ITk
  - Process CMOS 65nm
  - Taille : 20.054 mm × 21.022 mm
  - Zone sensible :384 x 400 pixels de 50 x 50 µm²
  - 153 600 pixels organisés en 2400 noyaux
- Tolérance au rayonnement jusqu'à une dose ionisante totale de 1Grad
- Préamplificateurs de charge
  - Faible bruit (<100 e)
  - Faible consommation (<5 uW) par pixel
- Traitement d'un taux de hits de 3 GHz/cm2
- Mise en mémoire tampon des données pendant une durée maximale de 12.5 µs
- Lecture des données déclenchée à 1MHz
- Nécessite des liaisons de données jusqu'à 5 Gbit/s

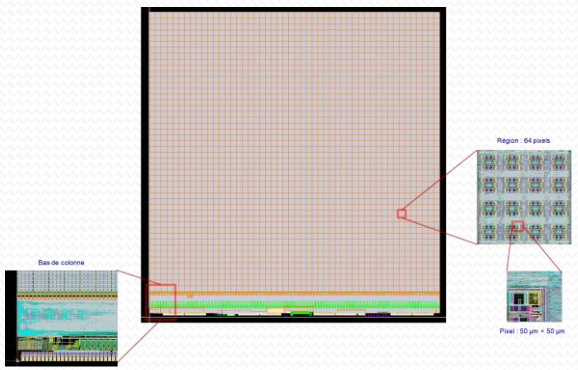




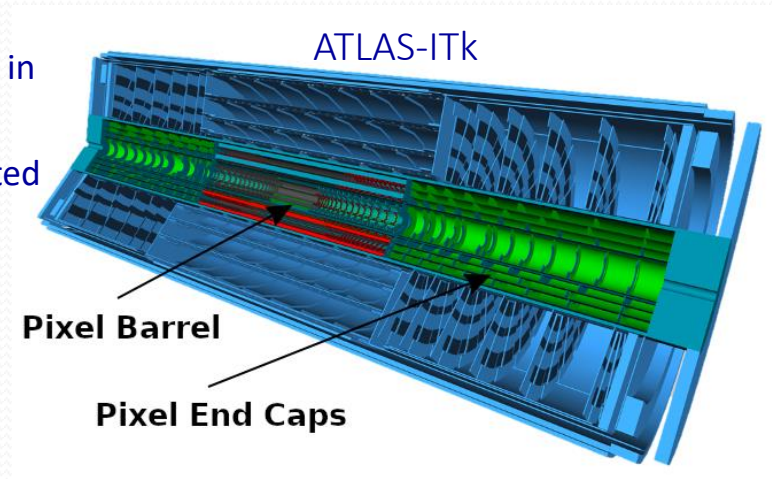
Introduction

- **Since ~1993:** Pixel detectors for tracking and vertexing in the LHC and HL-LHC environments
- **FE-I3 readout chip:** (250nmCMOS process)
  - 2880 pixels of 50µm × 400µm
- **FE-I4 chip the IBL** (130 nm CMOS process)
  - 26880 pixels of 50µm × 250µm
- **RD53 chip for ATLAS/CMS HL-LHC upgrades (65 nm CMOS process)**
  - Size: 20 mm × 21 mm
  - 153 600 pixels of 50µm × 50µm
  - Time over Threshold (ToT) measurement implemented in the pixel (resolution of 6.25 ns)
  - **Precision ToT and ToA** (resolution of 1.5 ns) implemented per each core column
  - Radiation levels : **1 Grad and 2 × 10^{16} (1 MeV neq) /cm^2**

RD53 readout chip



ATLAS-ITk



Analog FE pixel prototype

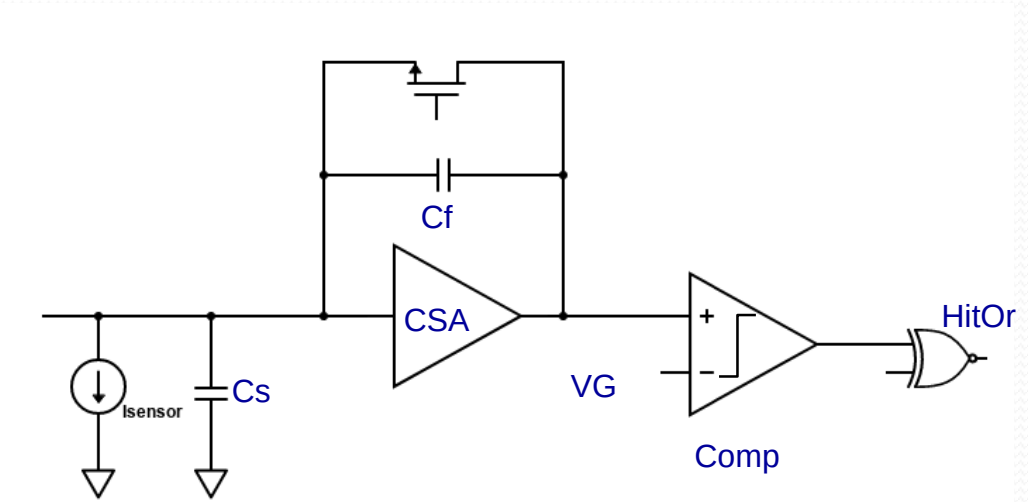
- Pixel array of 36 × 12 pixels
  - Only the analog pixel is considered and implemented
  - Design done for Sensor capacitance of 100 fF (50µm × 50 µm)
- The goal of this pixel matrix design is to study the limits to time resolution in analog front designed with the 28 nm CMOS process
  - Bandwidth, Noise, Current bias, power supply
- The time resolution of the FE is defined by the total jitter of the pixel FE

$$\sigma_{FE} = \frac{t_r}{\left(\frac{S}{N}\right)}$$

- Minimizing the jitter corresponds to :
  - Low RMS noise of the charge amplifier
  - High output voltage
  - Small rise time → High bandwidth

	High granularity	Ultra high granularity
Pixel size	50µm × 50 µm	25µm × 25 µm
Sensor capacitance	100 fF	< 50 fF ?
Time resolution	< 50 ps RMS	< 50 ps RMS
Consumption (pixel)	<20 µA	<5 µA
Threshold	< 600 e-	<600 e-
Hit rate	8 GHz/cm²	8GHz/cm²
Hit rate (pixel)	20 kHz	5 kHz
TID	2-4 Grad	2-4Grad

2 options for ATLAS/CMS inner layers upgrades

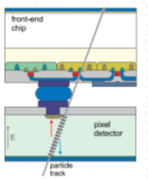


Analog FE pixel design

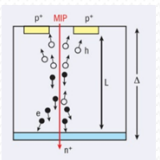
Semi-conductor pixel detectors

- Hybrid devices with a dedicated ASIC bonded to the sensor
  - R&D driven by LHC
  - Still solution for the HL-LHC pixel detector upgrade (Planar and 3D sensor, LGAD ??)
- Monolithic Active Pixel Sensors (MAPS)
  - Integrating the sensor and the readout electronics
  - Compromise between charge collection and signal read-out speed
- Depleted Monolithic Active Pixel Sensors (DeMAPS)
  - High radiation hardness and read-out speed

Hybrid Pixels

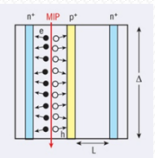


Rad-hard



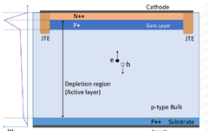
Planar sensors

Very rad-hard



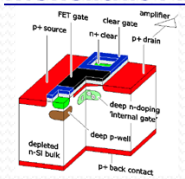
3D sensors

Precise timing

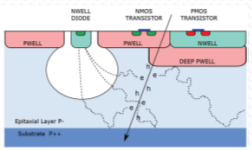


LGAD sensors

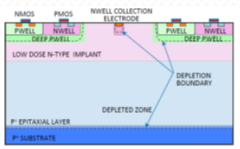
Monolithic Pixels



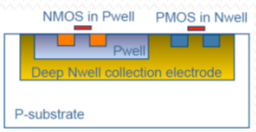
DEPFET in Belle



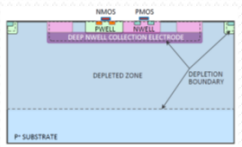
MIMOSA28 (ULTIMATE) in STAR



ALPIDE in ALICE



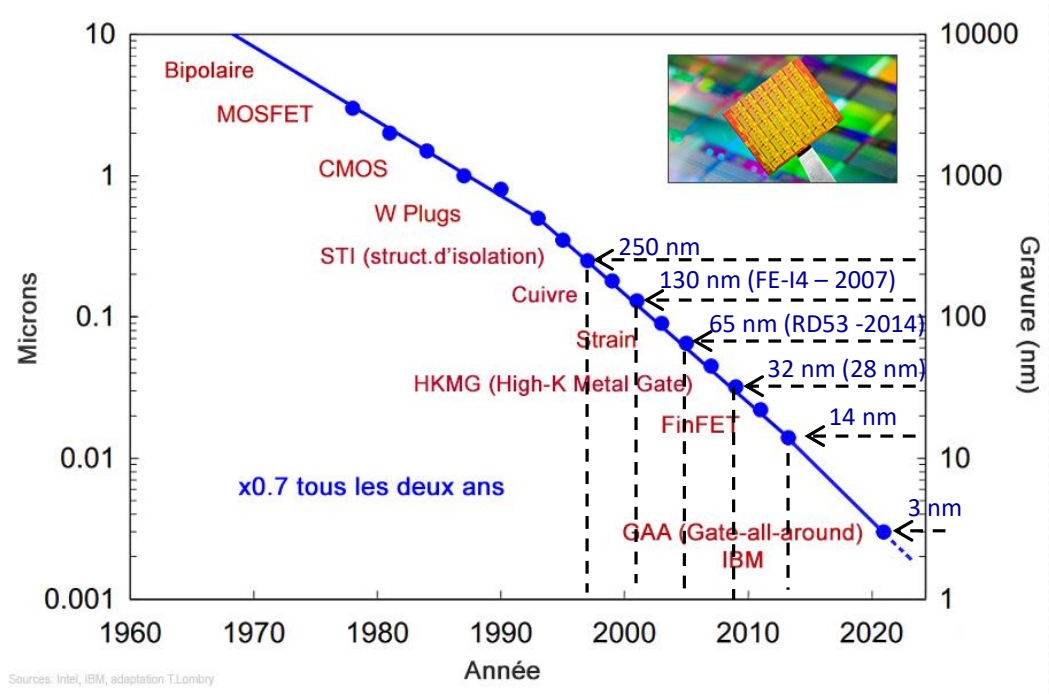
HV/HR-CMOS



DEPLETED MAPS for better time resolution and radiation tolerance

BiCMOS HBT

Technology choice and ASICs evolution

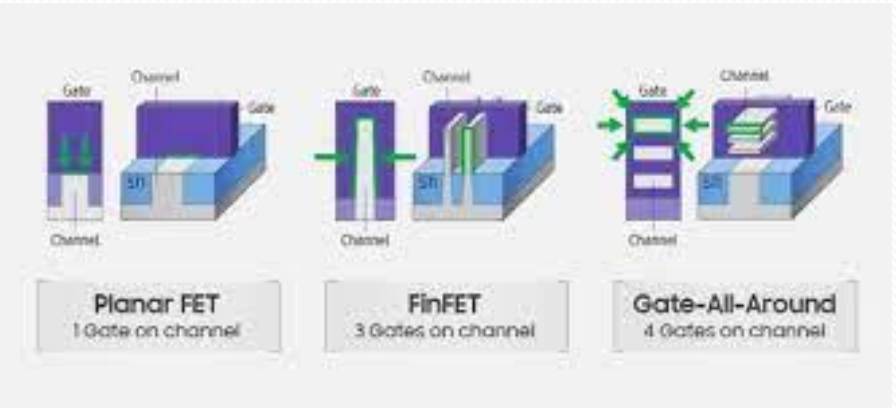


- The CERN community is lagging behind in the use of the new processes
  - Cost and accessibility
  - Take years to design our complex chips
  - Risk of technology aging (factory can abandon the node)

- Most of the designs for CERN experiments are based on 65 nm and 130nm CMOS
  - Qualified by CERN for radiation-hardness
- HL-LHC : Over 40 front-end ASICs have been developed in 130 and 65nm CMOS technology for detector readout
  - Access to foundry and design tools run centrally from CERN
  - Common projects for the specific developments like data links or power conversion
  - Collaborative developments across experiments (RD53 or Medipix)
- 130 and 65nm CMOS technologies are already fifteen to twenty years old
- 28nm CMOS technology is considered as the next node for highly integrated chips such as pixel readout
- A cheaper process should be preserved for less dense/demanding applications
- The requirements of lepton and heavy-ion colliders seem to be mostly within reach of technologies from HL-LHC
- CMOS Imaging Sensors (CIS) variant should be

Technology choice and ASICs evolution

- FCC-hh or a muon collider
  - Electronics can become a facilitator, but also a potentially limiting element
  - Access to some of the required technologies and tools
  - The R&D strategy will be driven by what is feasible and not just by the requirements of experiments
- CMOS nodes below 28nm need to be qualified
  - Potential use in future applications requiring extreme miniaturization, High speed and low power
- High performance CMOS image sensors are based on stacked active layers to reduce pixel pitch and increase functionality
- Commercial CMOS image sensors are a good example, stacking two or three device layers fabricated in different technologies
  - Integration of different technologies: sensor/analogue/digital/photonic functions
  - R&D in TSVs and bump-less techniques is needed



- For ASICs, the microelectronics industry has reached nanoscale CMOS nodes (< 5nm), based on new transistor structures
  - FinFETs devices
  - GAA devices