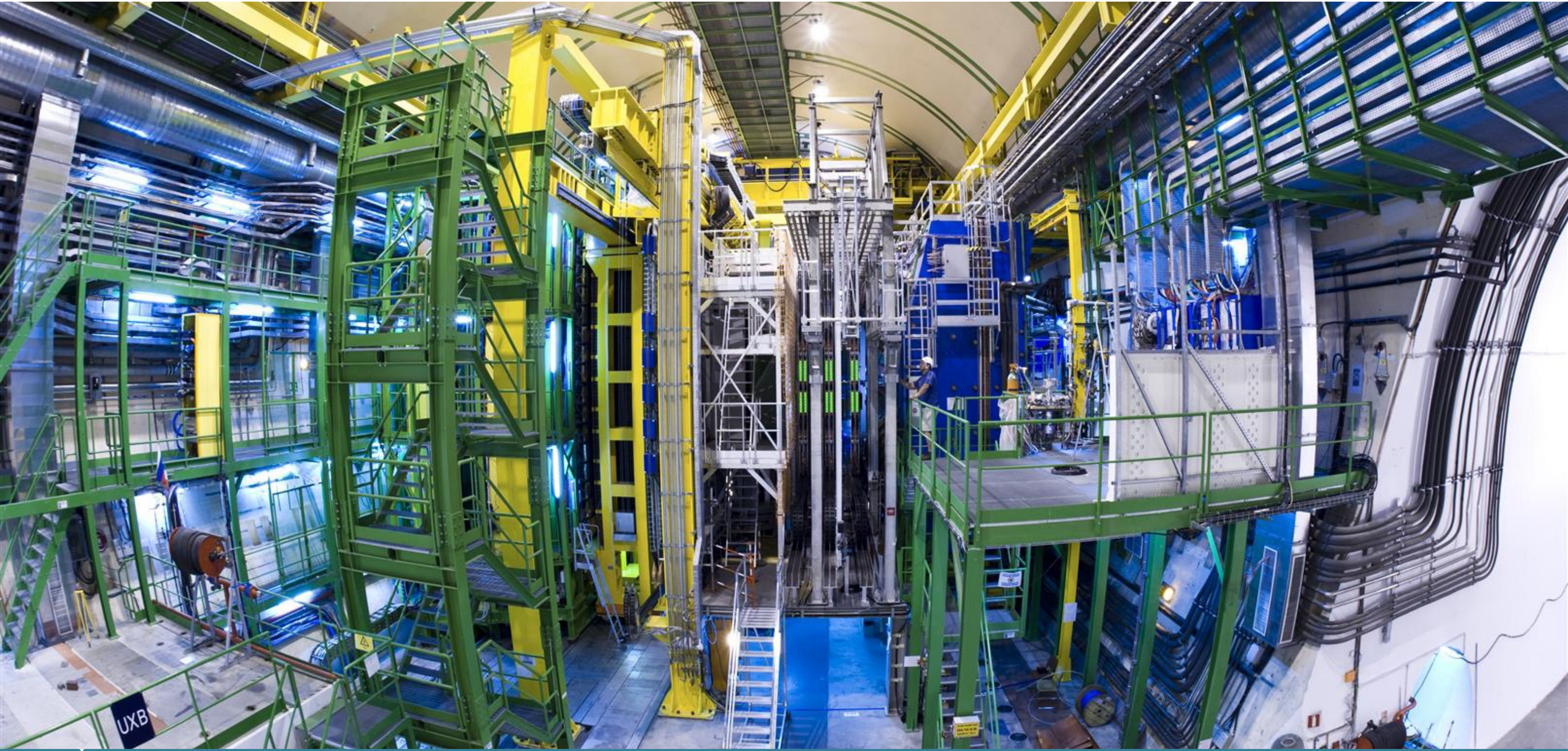
8-11 Apr 2024, Marseille, France

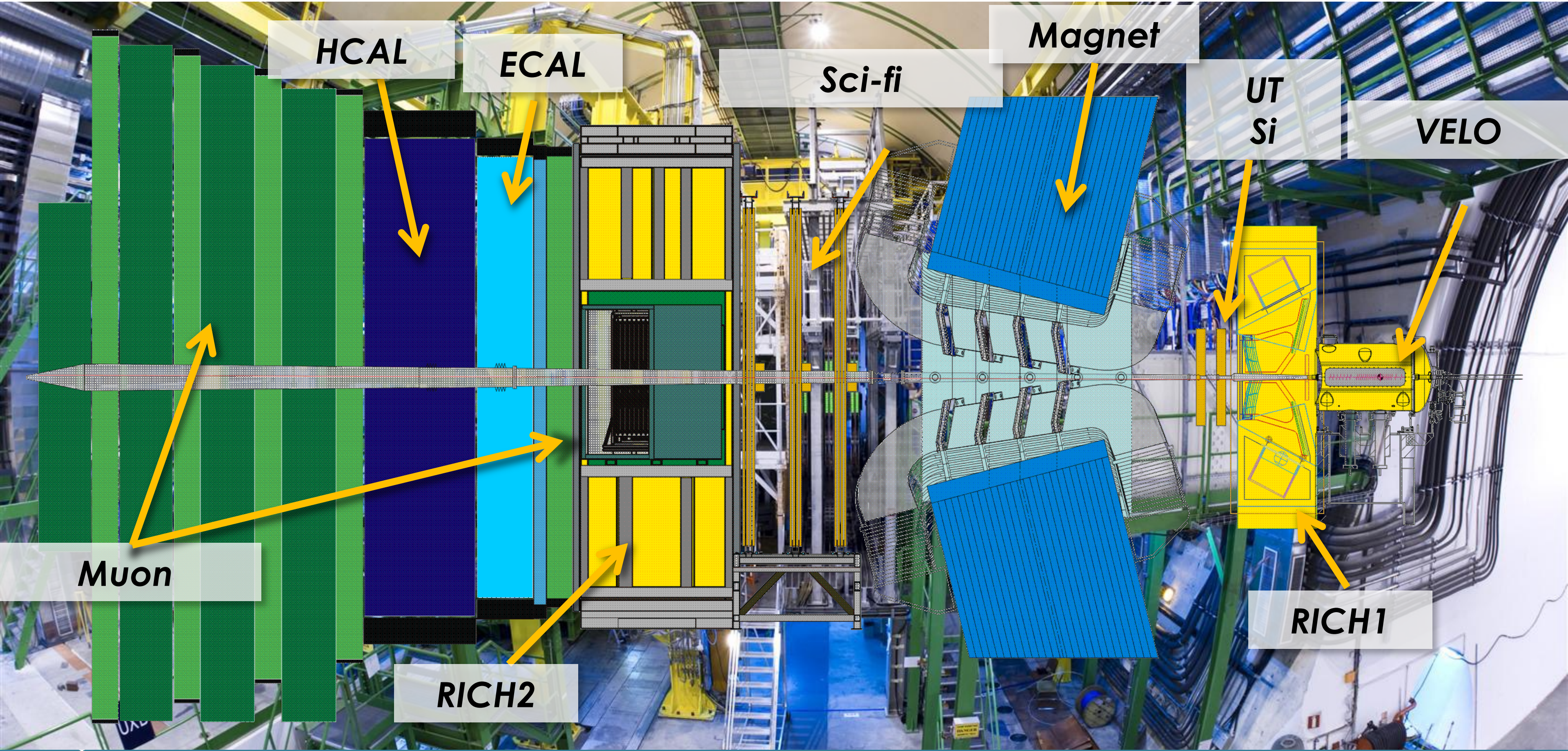
The Future of the Vertex Locator: Towards 4D tracking

Kazu Akiba

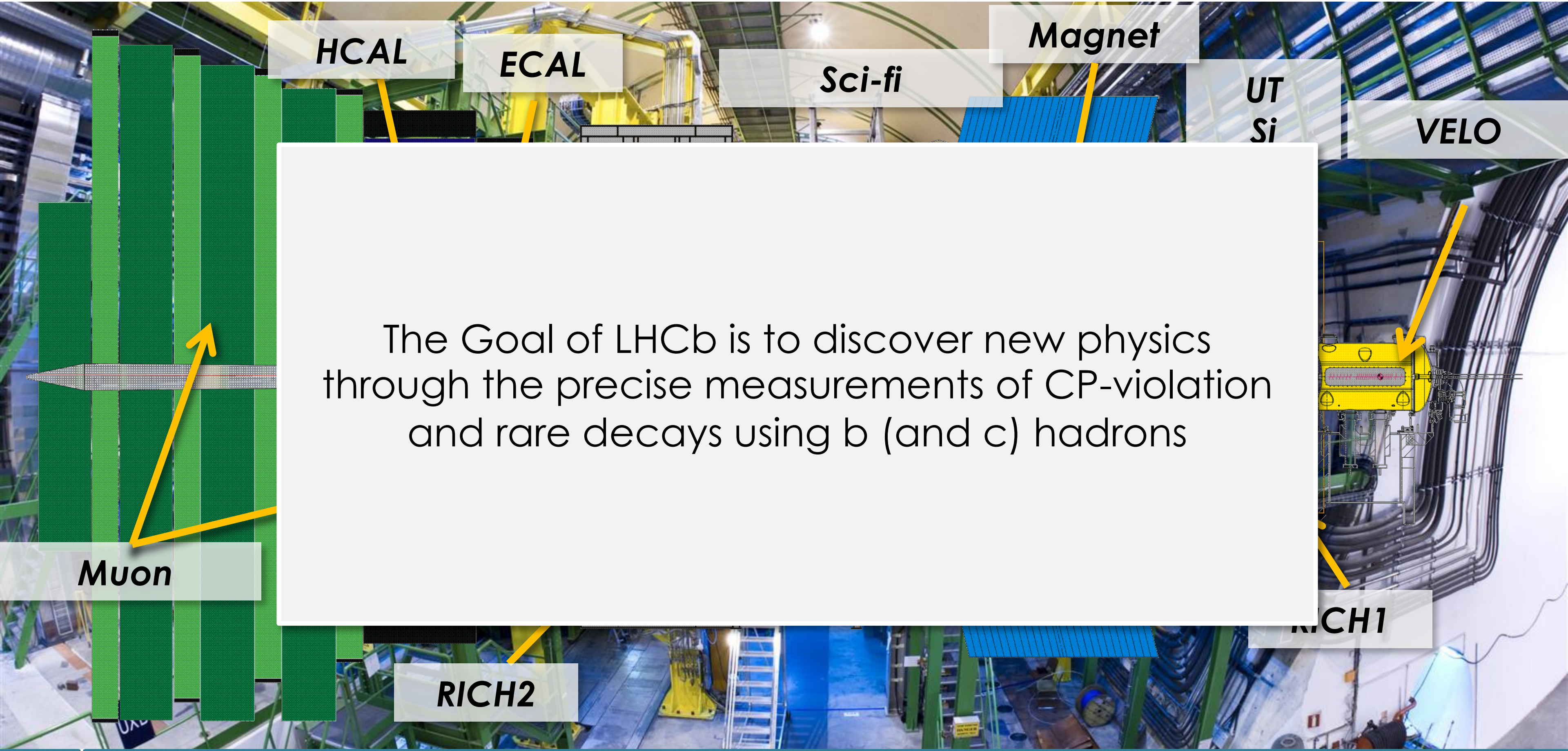
The LHC*b* Experiment Upgrade1 (LHC run3)



The LHCb   Experiment Upgrade1 (LHC run3)



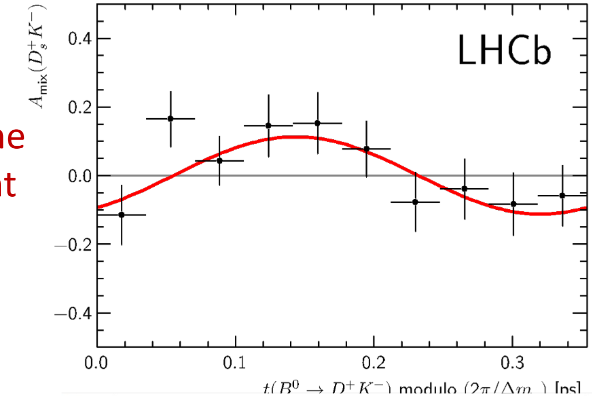
The LHC*b* Experiment Upgrade1 (LHC run3)



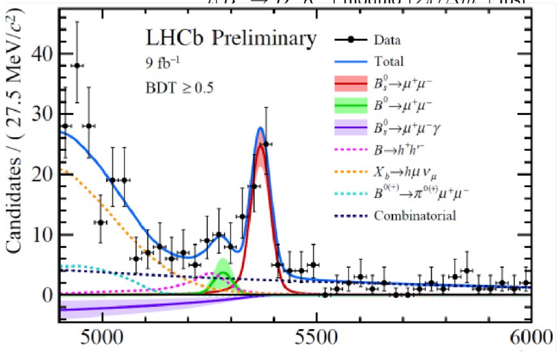
The Goal of LHCb is to discover new physics through the precise measurements of CP-violation and rare decays using b (and c) hadrons

LHCb Physics: General purpose forward detector

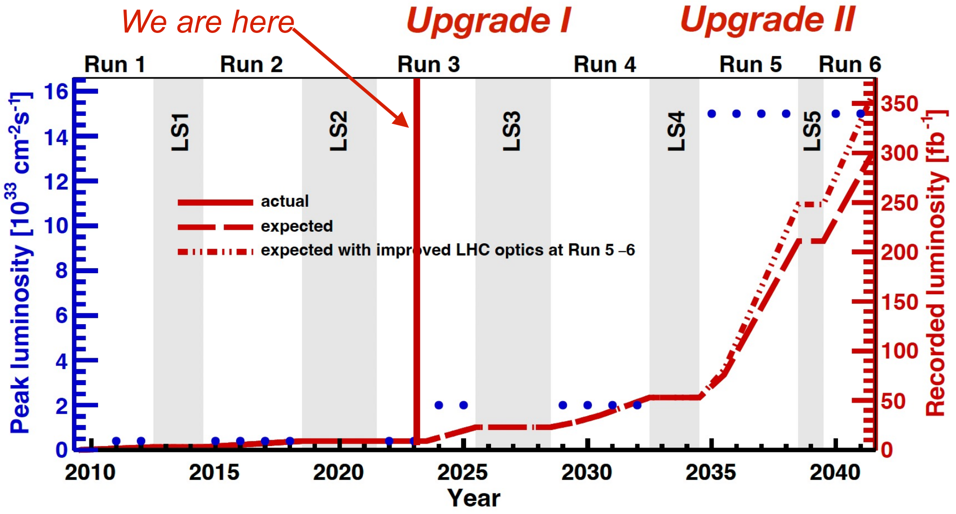
Decay Time dependent CPV



Very Rare decays



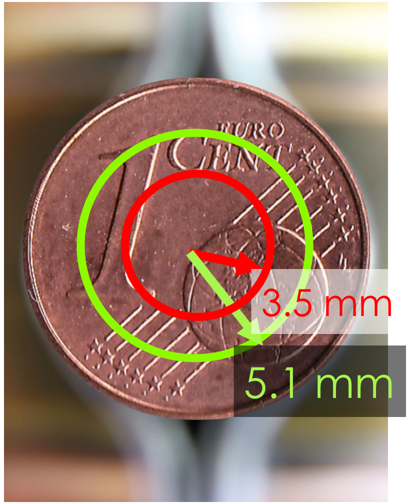
Limited by the detector, not accelerator

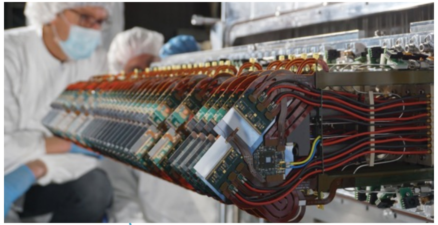


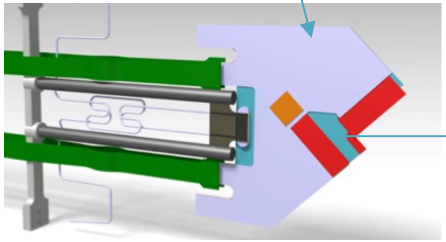
Can acquire 6 times more luminosity than current detector by the end of Run5

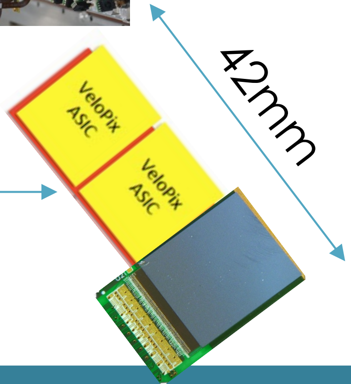
Overview of the Current VELO

- 52 modules, 55 μm pitch sensors
- 40M pixels
- Data driven readout
- 5.1 mm sensitive distance to beam.
- Operate in Vacuum
- Innovative micro-channel cooling (-20 °C)
- Separated from the beam by a milled Al box (250 μm)



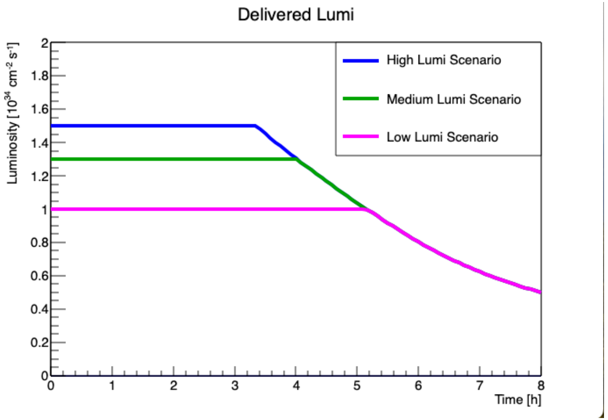


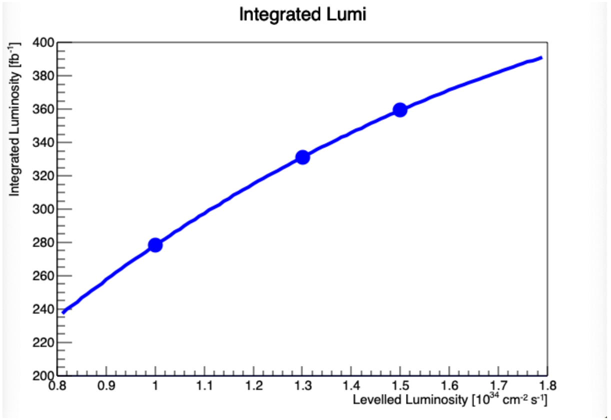




Luminosity Scenarios for LHCb

levelled L_{peak} $(cm^{-2}s^{-1})$	$1.0x10^{34}$	$1.3x10^{34}$	$1.5x10^{34}$
total recorded Run 1-6 *ROUND* (fb^{-1})	263	291	300
total recorded Run 1-6 *FLAT* (fb^{-1})	290	336	359





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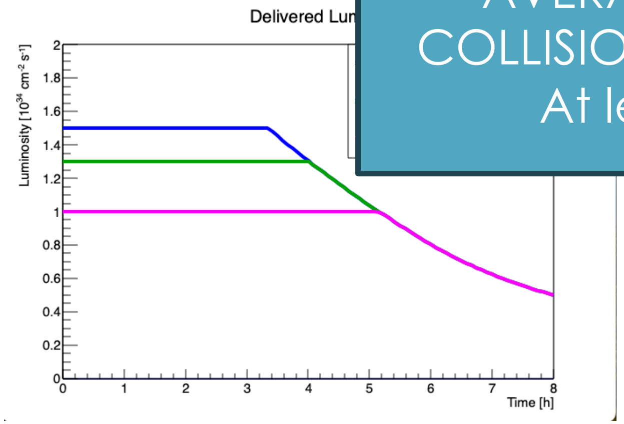
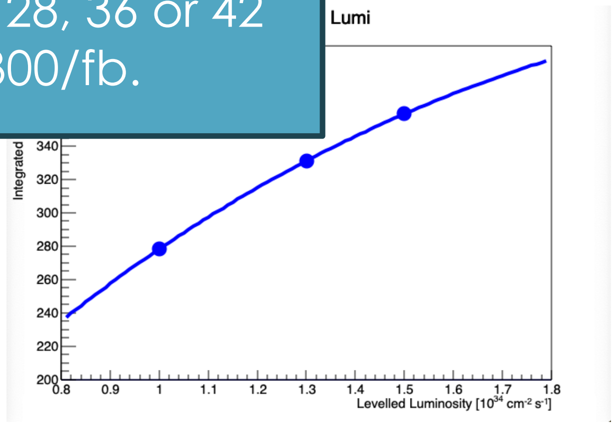
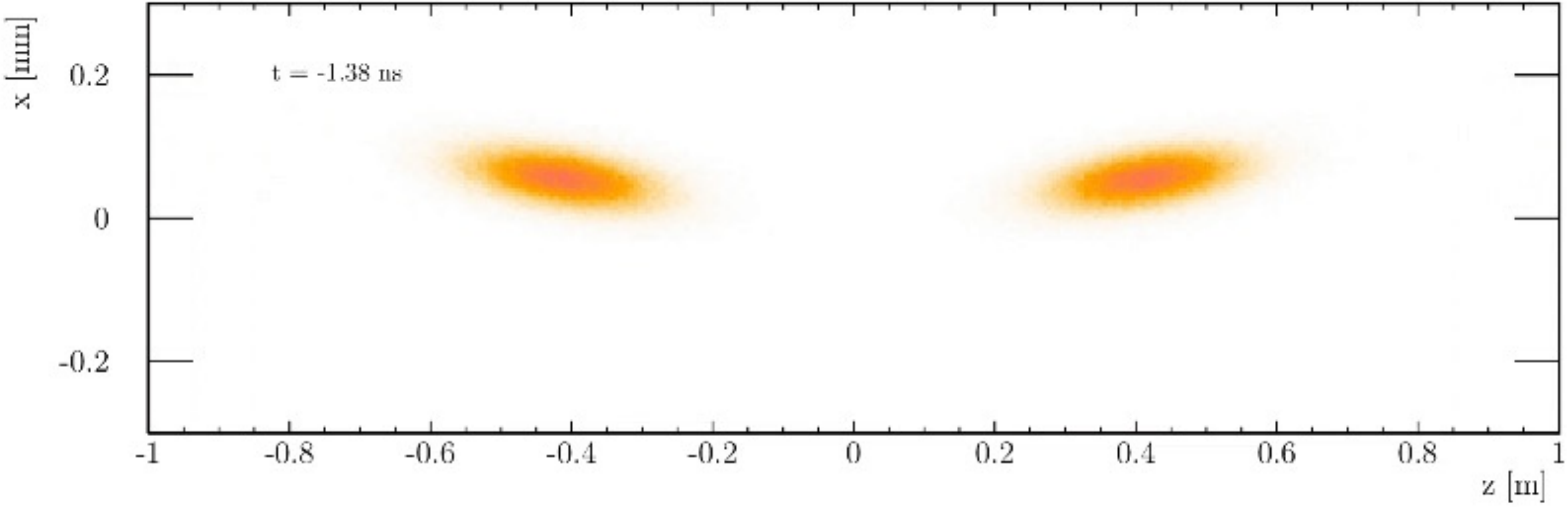


AVERAGE NUMBER of COLLISIONS OF 28, 36 or 42
At least ~300/fb.

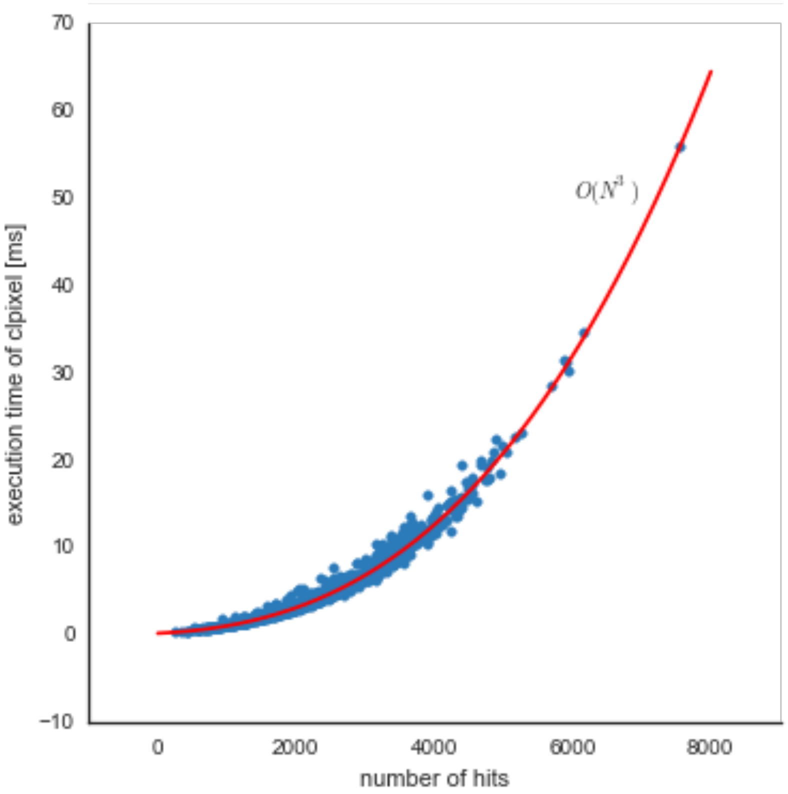


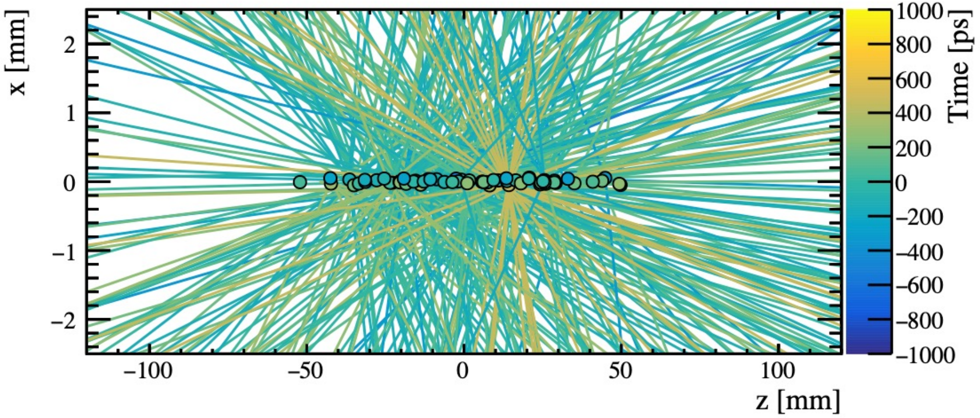
Bunch crossings

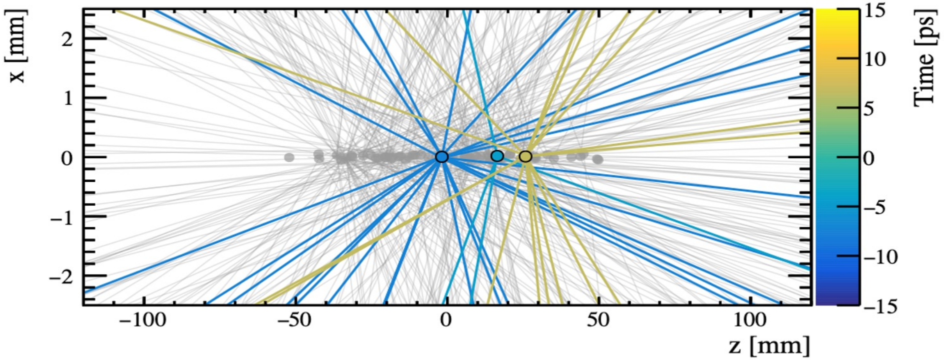
$$\sigma_z^{RMS} \approx 44.7 \text{ mm}$$
$$\sigma_t^{RMS} \approx 186 \text{ ps}$$
$$\sigma_t^{comb} \approx 240 \text{ ps}$$



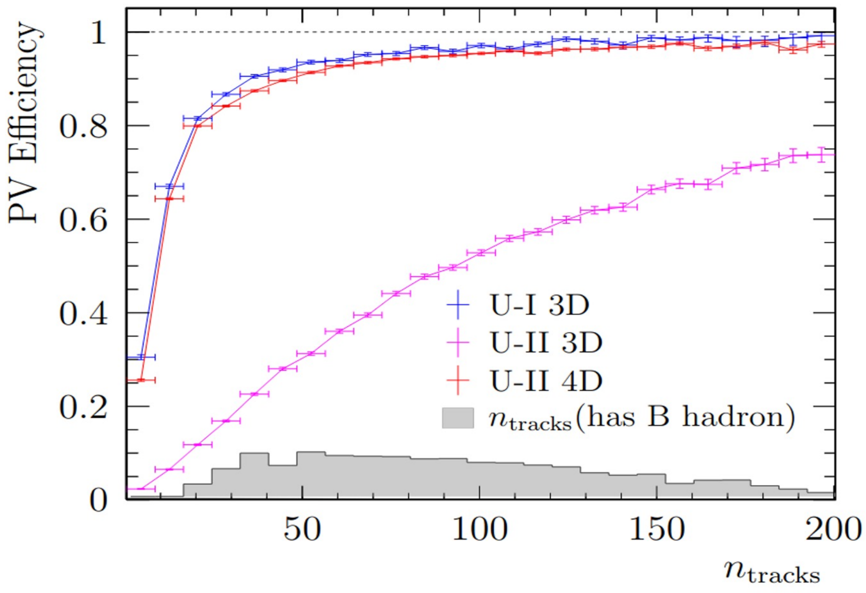
Maintain same performance: Fast Timing

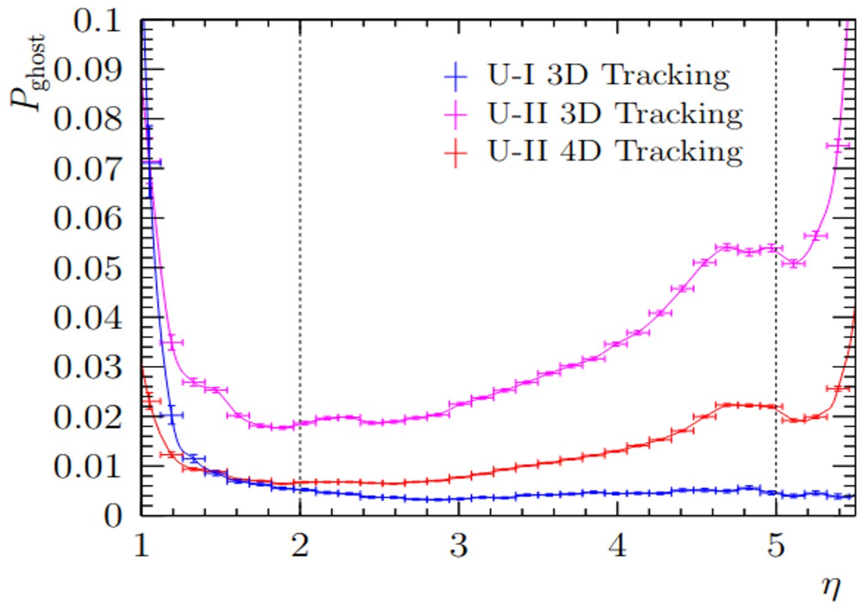






Can we really use that in our favour?





Timing recovers PV efficiency and reduces fake tracks.

https://cds.cern.ch/record/2800144

A successful LHCb @ 1.5×10^{34} cm^{-2}s^{-1}

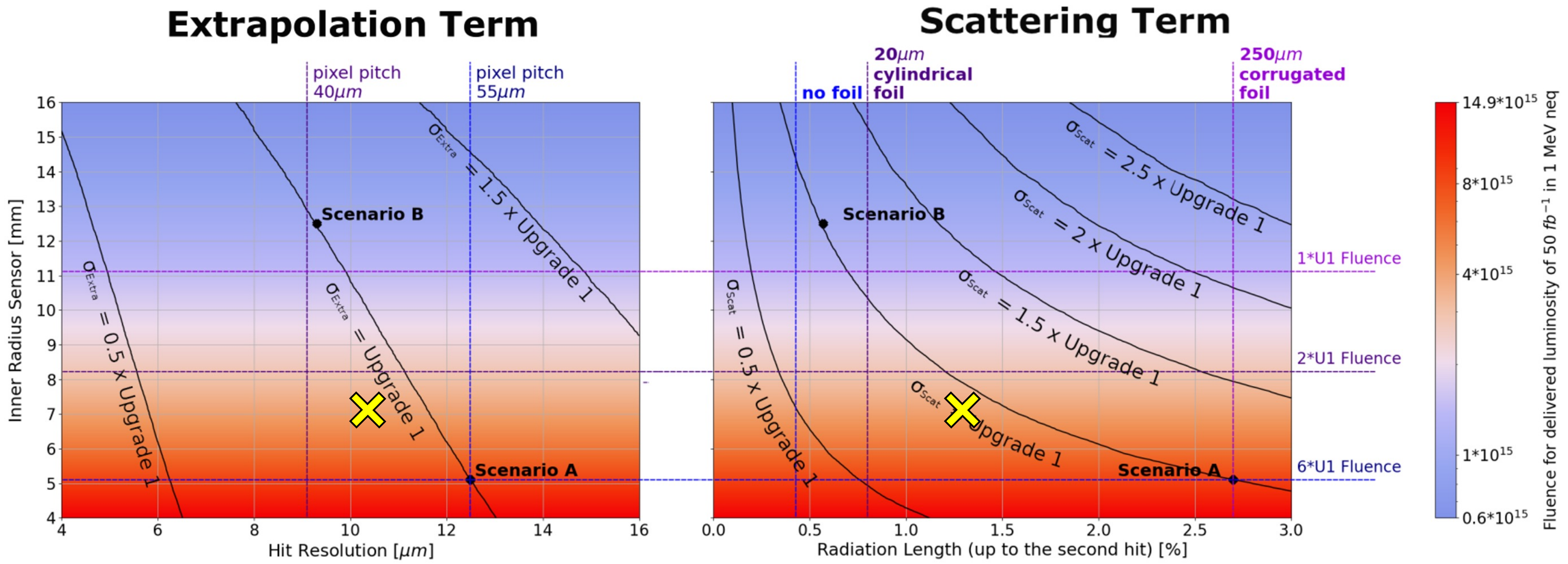
Assumption: U1 Impact Parameter Resolutions
will yield same signal selection performance
IF timing resolution of **20 ps/track** is achieved.

Timing of 50 ps/hit is a global requirement.

Radiation Hardness could be up to 6 times larger than current

An extensive R&D program was launched to find the achievable limits

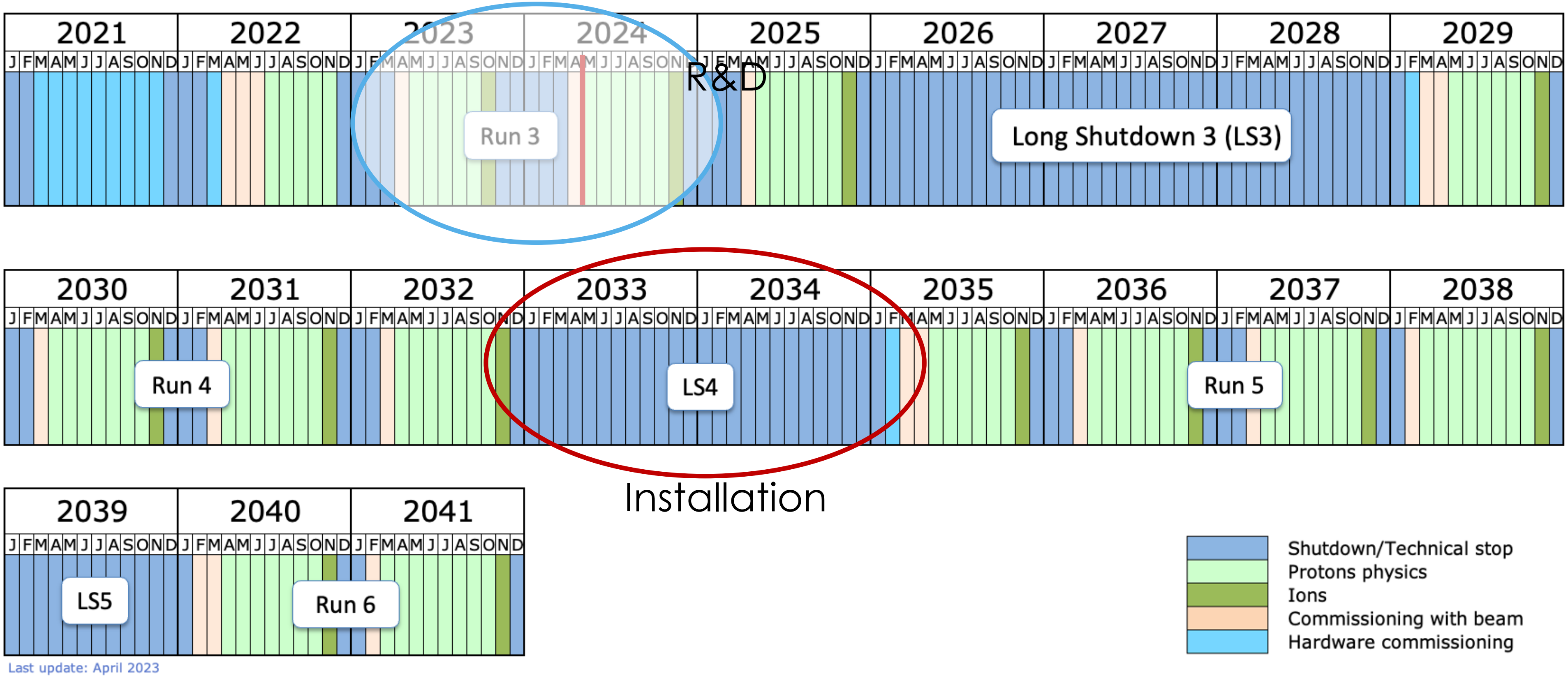
Using IP resolution as detector construction requirement



Basic detector requirement becomes: <u>hit resolution</u> better than 10-11μm

And <u>detector material</u> minimised per station. RF-foil < 75 μm Al.

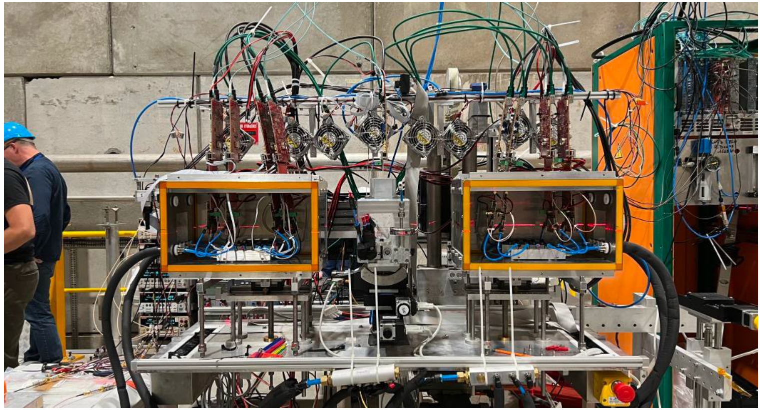
LHC schedule

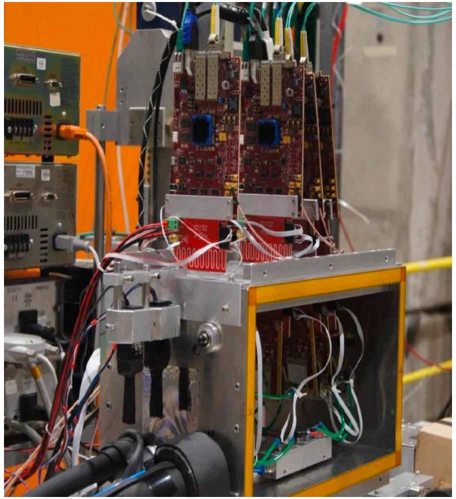


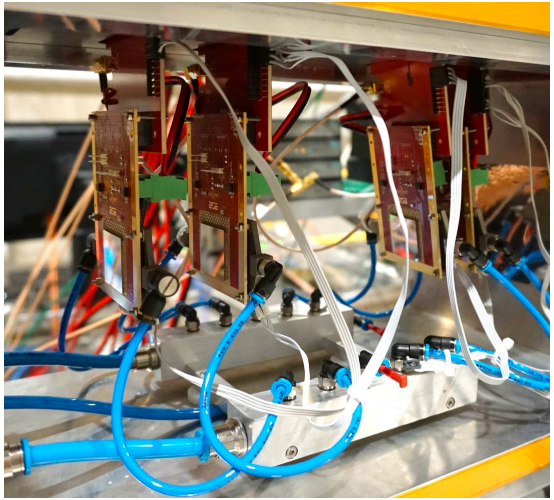
A FEW R&D RESULTS

Timepix4 Telescope

- The telescope aims to be a high rate (> 10 MHz) high resolution in space (~2 μm) and time (<20ps).
- Proof-of-principle in 4D tracking.
- Composed of spatial planes (300 μm thick) and timing planes(100 μm), plus Cherenkov-MCPs.







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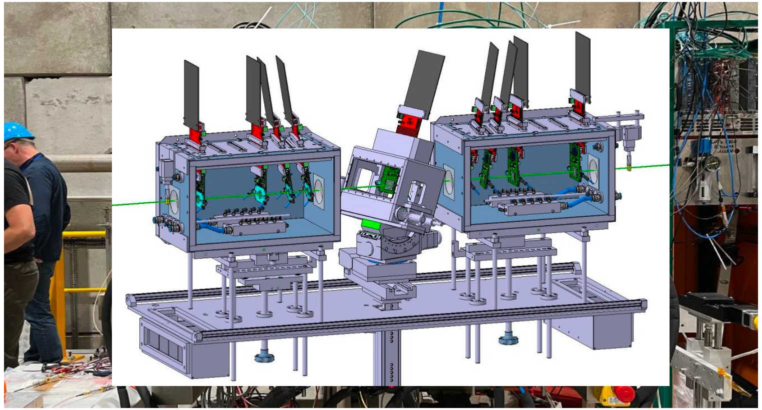
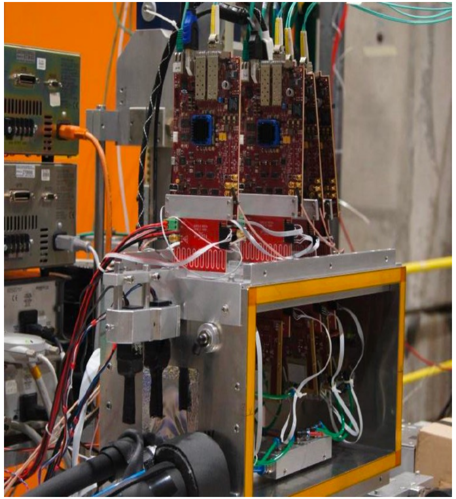
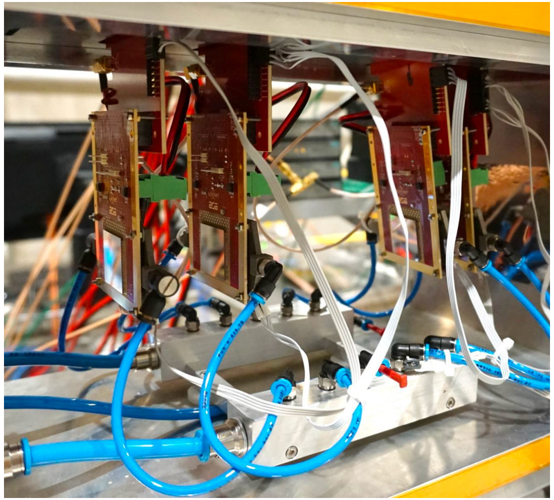
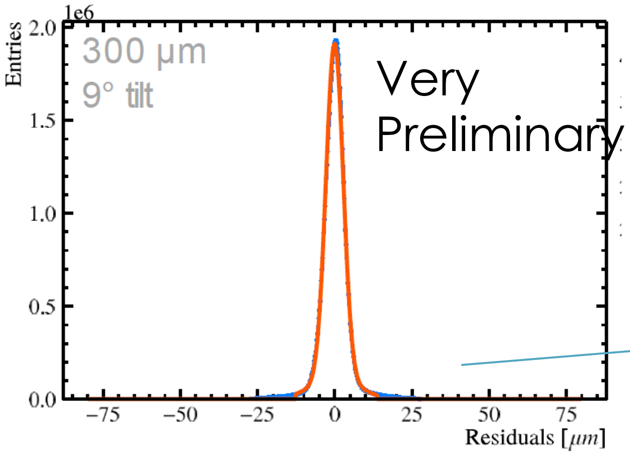
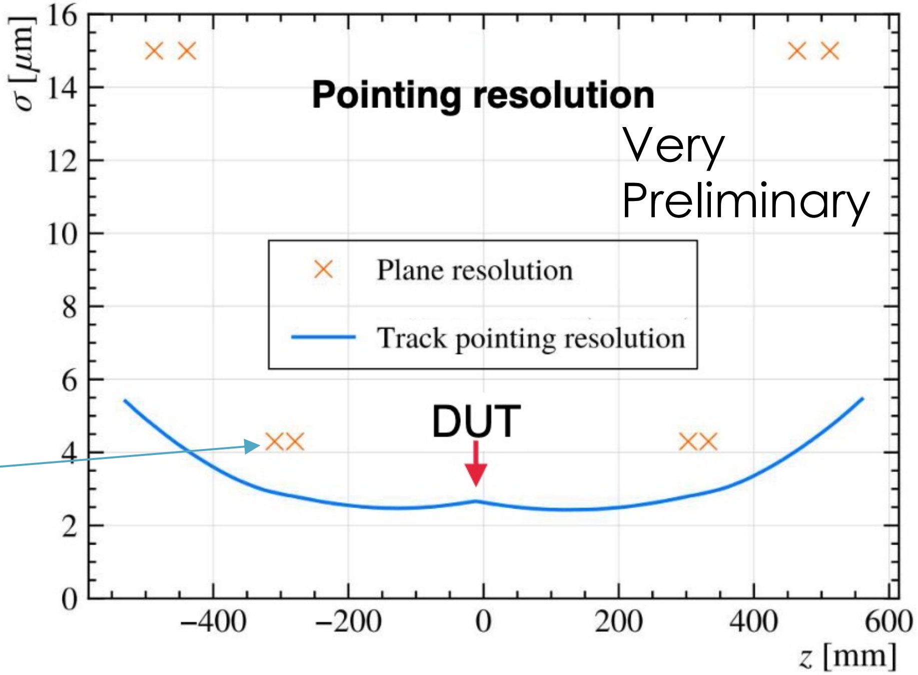




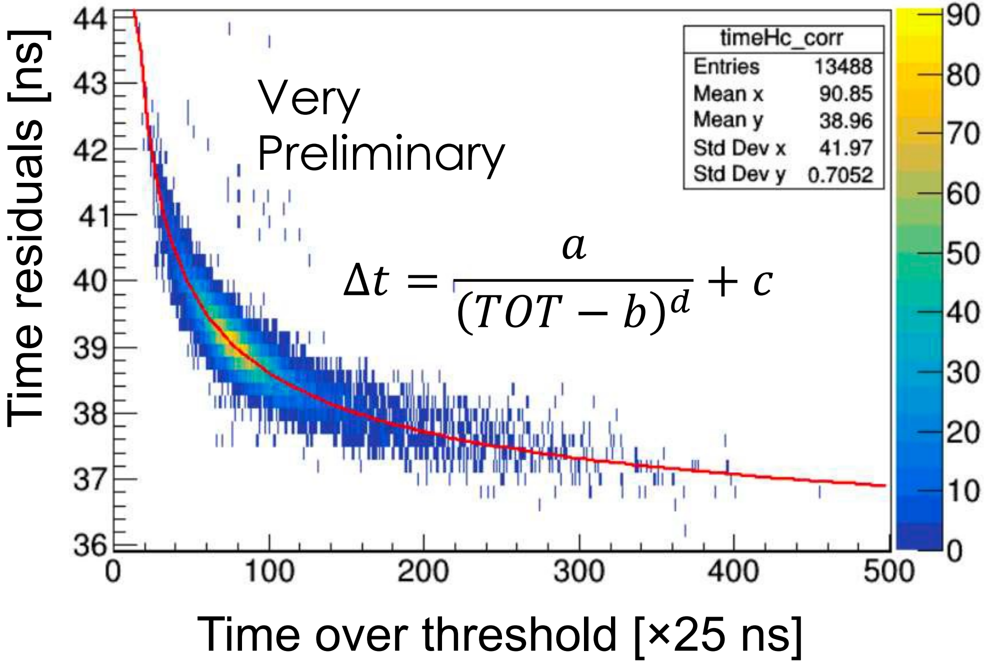


Telescope Spatial Resolution



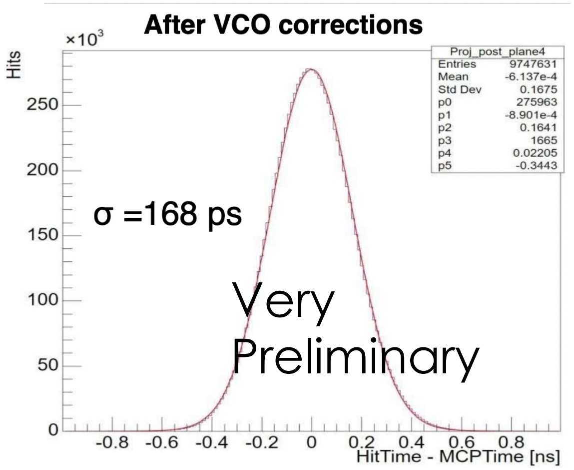


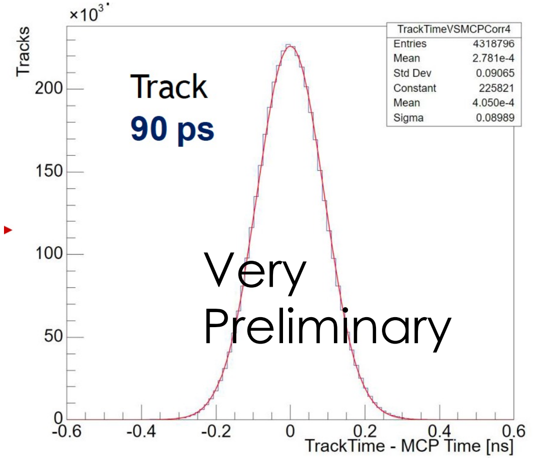
Telescope Timing



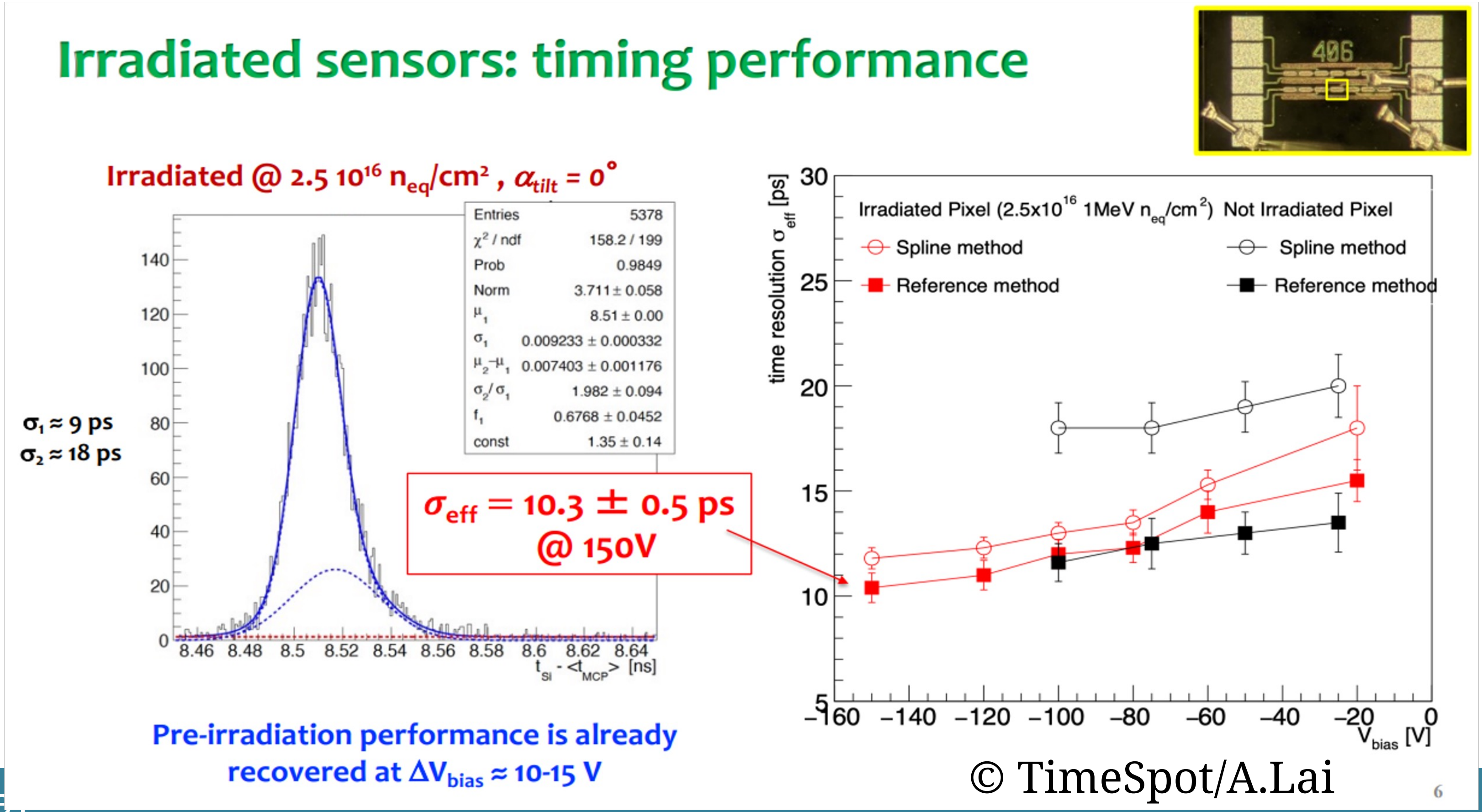
$$\Delta t = \frac{a}{(TOT - b)^d} + c$$

Timewalk curve – Small charge signals have lower temporal

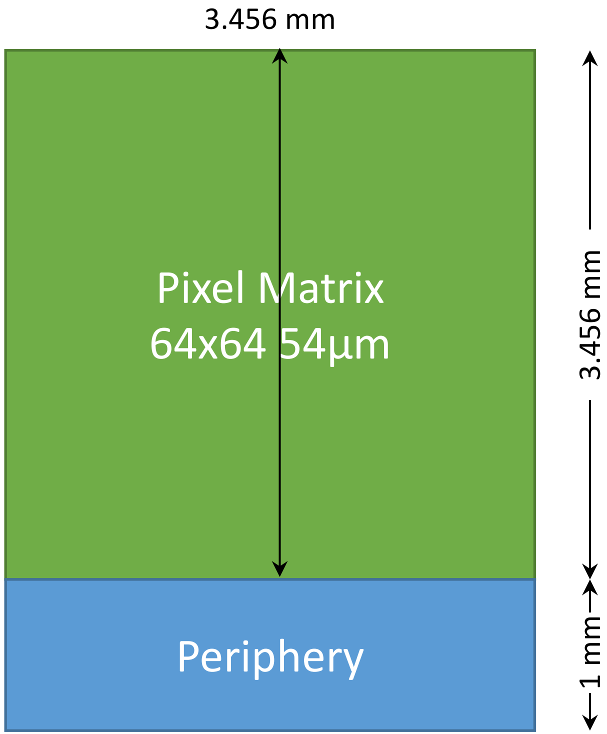




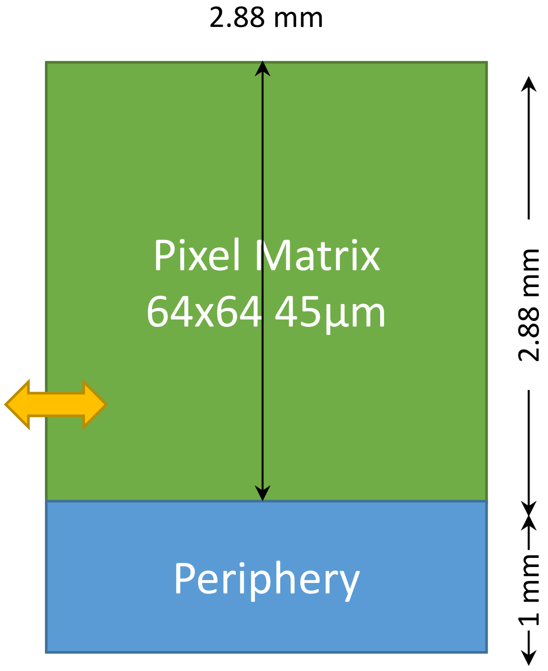
3D trench sensors from Timespot



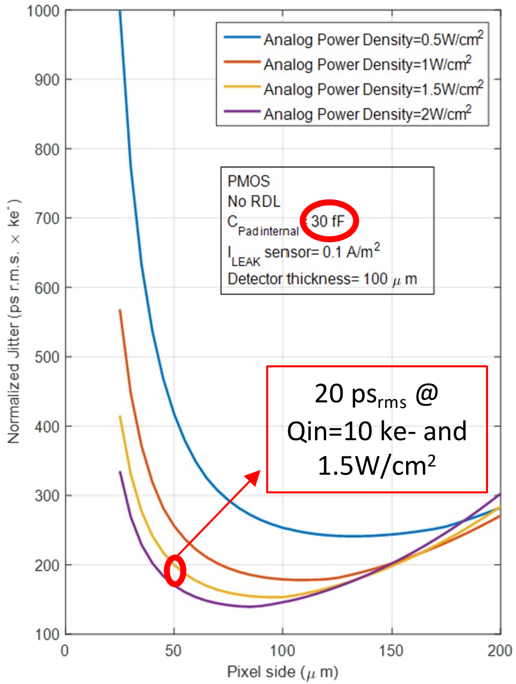
Picopix – a 28 nm ASIC prototype



~120 K$



~75 K$



R.Ballabriga, The Timepix4 analog front-end design: Lessons learnt on fundamental limits to noise and time resolution in highly segmented hybrid pixel detectors
https://doi.org/10.1016/j.nima.2022.167489

Future ASIC challenges

- Cope with increase in Radiation damage
- Analog front-end does not scale much -> about the same size as VeloPix/Timepix4 (25% of pixel)
- Cope with hit pile up:
  - @Upgrade I, MIP discharge time ~300 ns for 1% max pileup.
  - Upgrade II would need 10 times faster rate.
- Per pixel TDC with time resolution < 50 ps.
- More information in output and higher hit rate.
- Time-walk correction?
- Clock distribution effects?

	VeloPix (2016)	Timepix4 (2019)	Velopix2 (202?)
technology	130 nm	65 nm	**28 nm**
Pixel size	55x55 μm^2	55x55 μm^2	**45x45 μm^2?**
Sensitive area	2 cm^2	7 cm^2	**2 cm^2?**
Packet size	24 bit	64 bit	**64 bit?**
Max rate	400 Mhits/cm^2/s	180 Mhits/cm^2/s	**4000 Mhits/cm^2/s**
Time resolution	25 ns	200 ps	**35 ps?**
Output data rate	20 Gb/s	81 Gb/s	**250 Gb/s?**

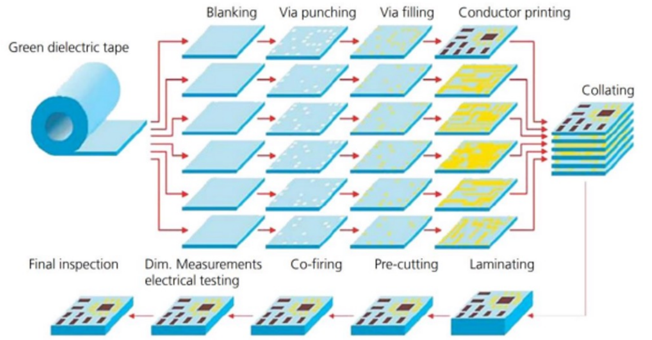
- Fruitful collaboration with the Medipix group has yielded the VeloPix ASIC for the LHCb Upgrade I.

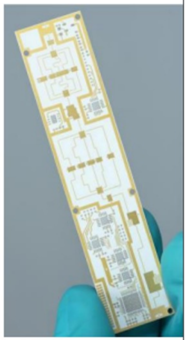
Minimizing material

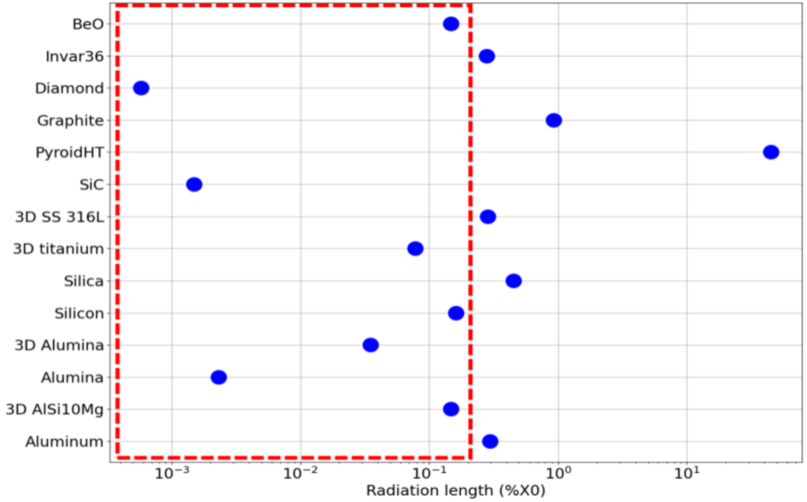
Several different approaches ongoing to minimize module substrate material.

Combining functions on Ceramics and, for example, Low voltage could be implemented using ceramic tape with embedded copper channels.

Many ceramic materials can have low X_0 but low Thermal conductivity.

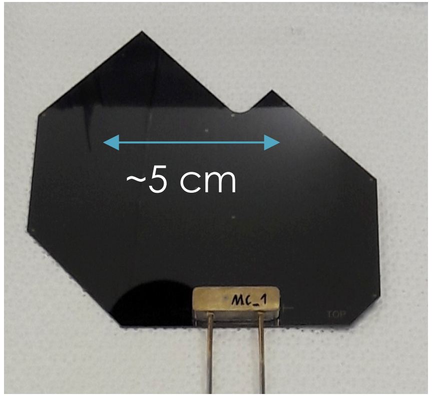


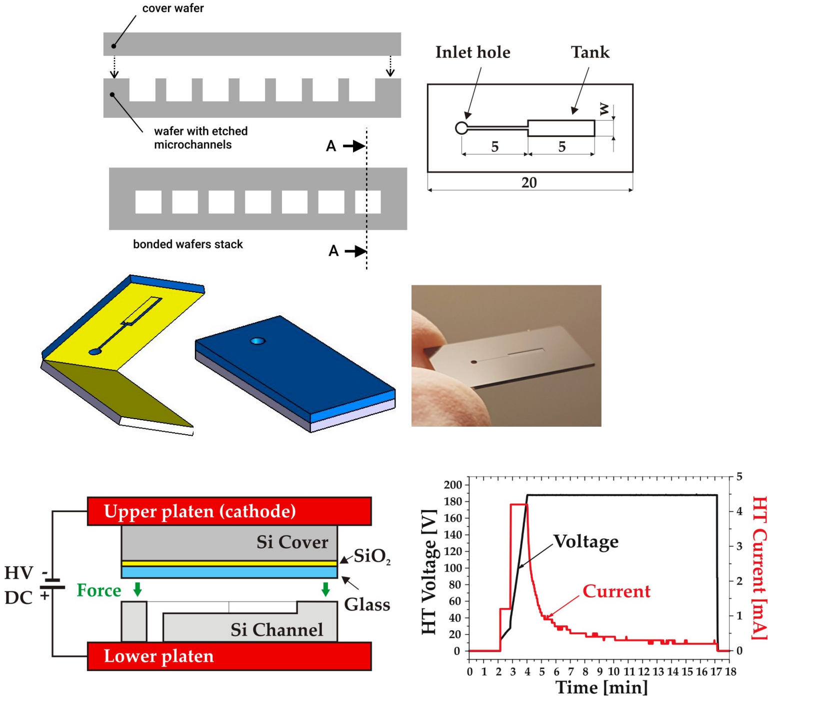




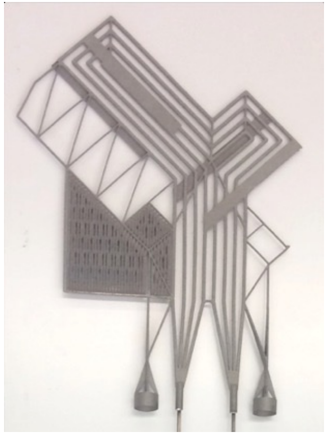
Cooling for next upgrade

- Operation in vacuum demands active cooling.
- Needs to be very light weight
- Studying the possibility to operate at lower temperatures < -40°C
  - Avoid runaway at high radiation damage
  - Requires the R&D of different cooling fluids and technologies …





R&D performed by the CPPM group in Marseille

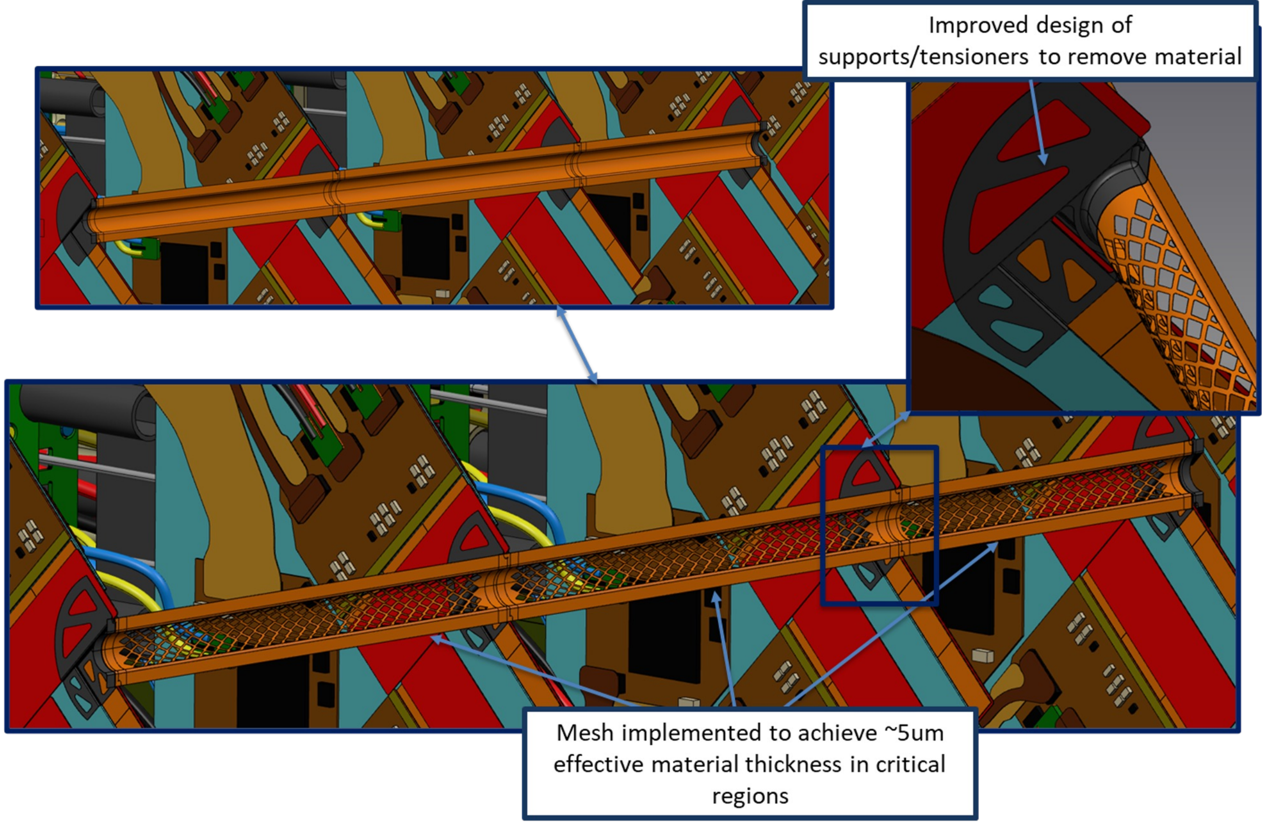


3d printed Titanium substrates, already prototyped for Upgrade I

RF shield

Current ideas revolve around a cylindrical shield

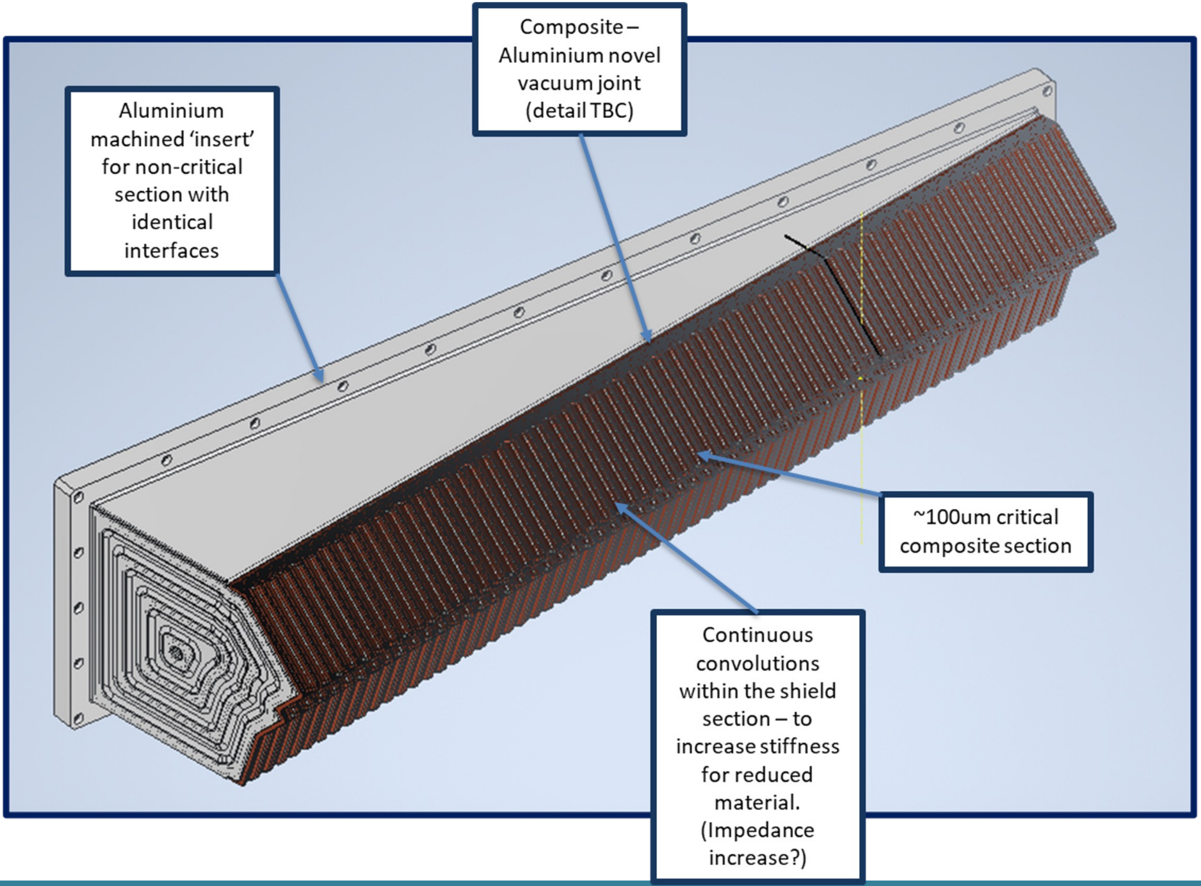
This implementation has critical consequences on module design and implementation -- no outgassing harmful materials to LHC.



However, the main consequence is the reconstruction of the vacuum tank and all associated systems (motion, vacuum, cooling etc.) -- Also critical for maintenance periods.

RF shield

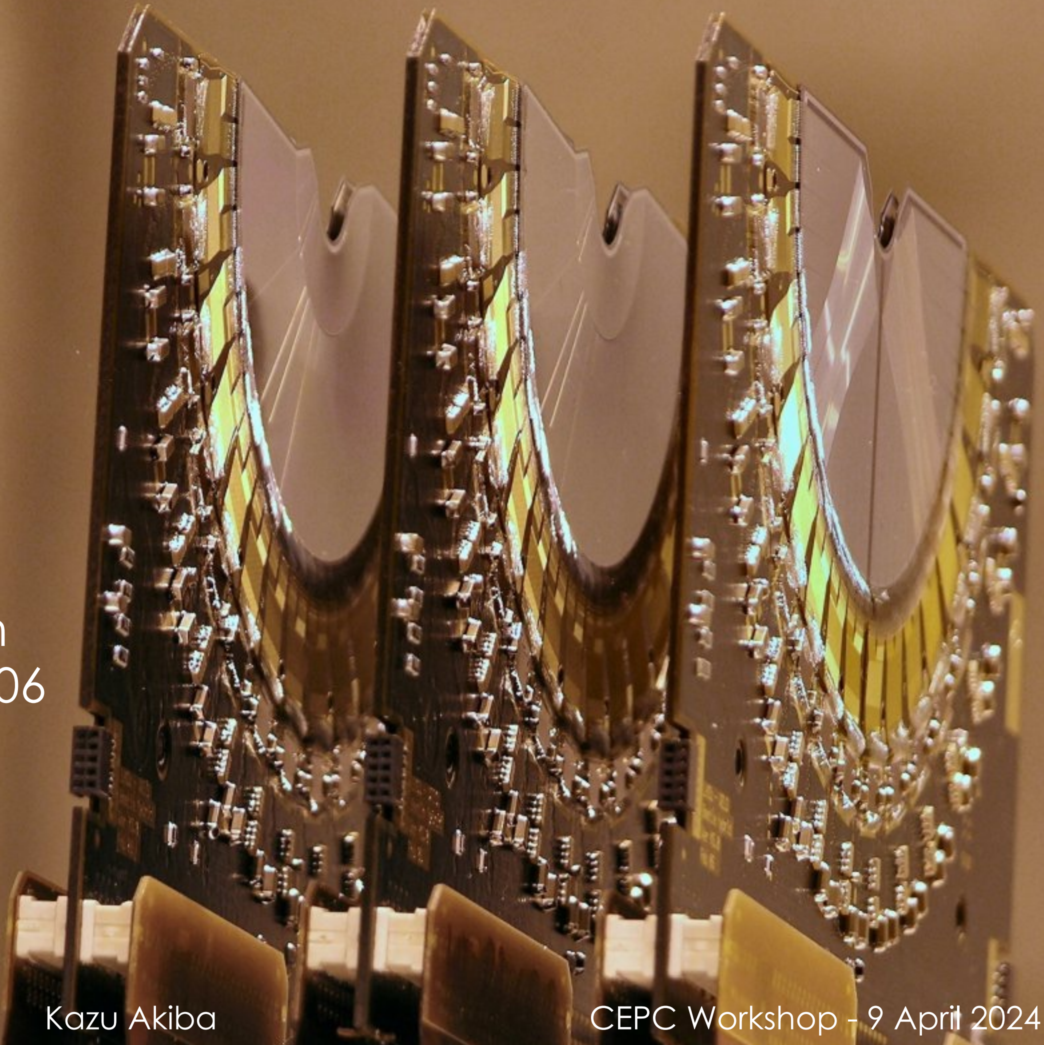
A more conservative solution could yield a light interface to the beam, but 100μm still to be proven/achieved.



Summary

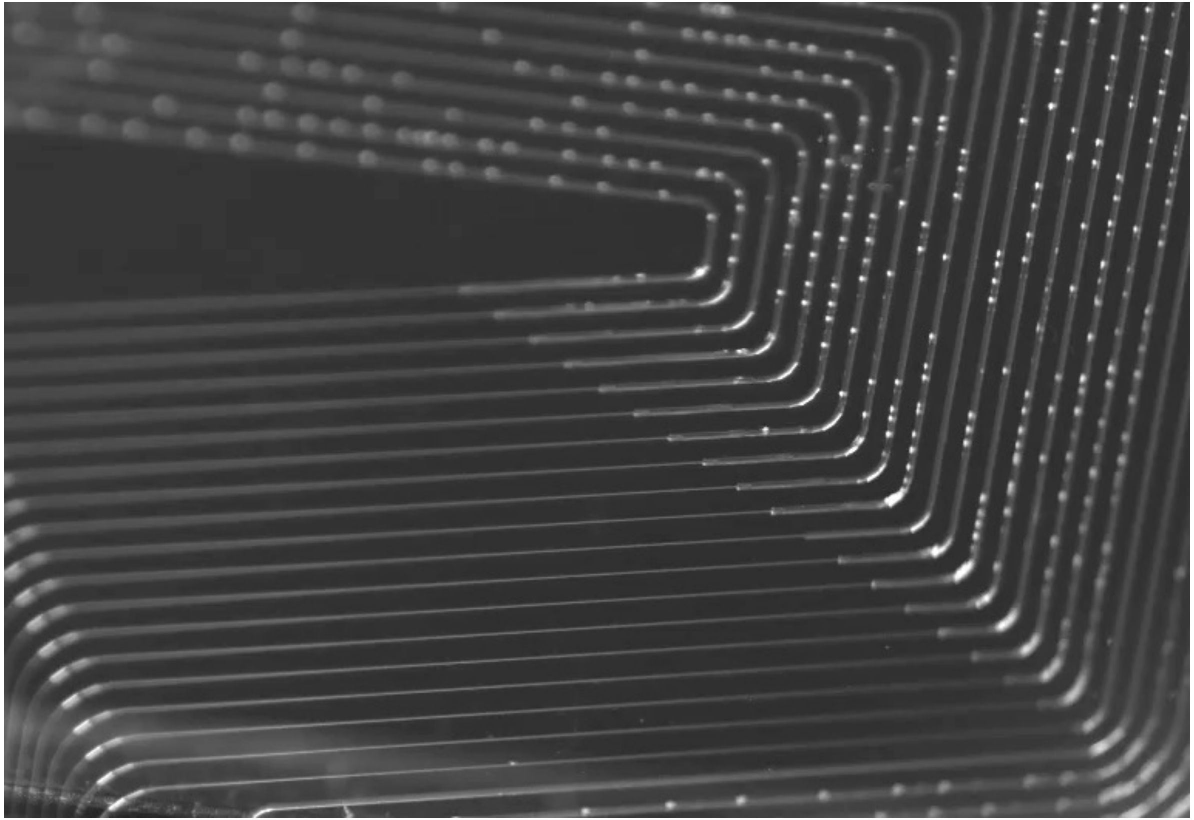
- We are planning a next upgrade to run at up to **7.5 times higher** instantaneous luminosity.
- The high Primary Vertex density motivates a Vertex detector with **high resolution timing**.
- The **Secondary Vertex** reconstruction and **association** to its origin **PV** require precise Impact Parameter. Fast timing can allow this matching at the high pile up regime.
- Fast timing shows promising results in the **pattern recognition** as well.
- An ultra **high radiation** resistant **sensor** and **ASIC** technology is required to operate through the whole lifetime.
- The VELO project welcomes new collaborating teams!

Back up

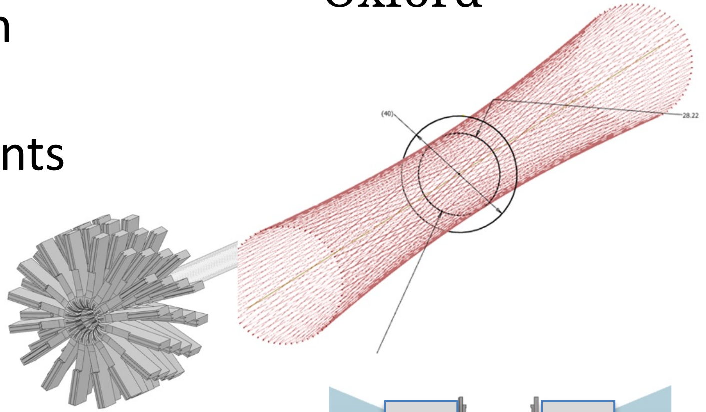


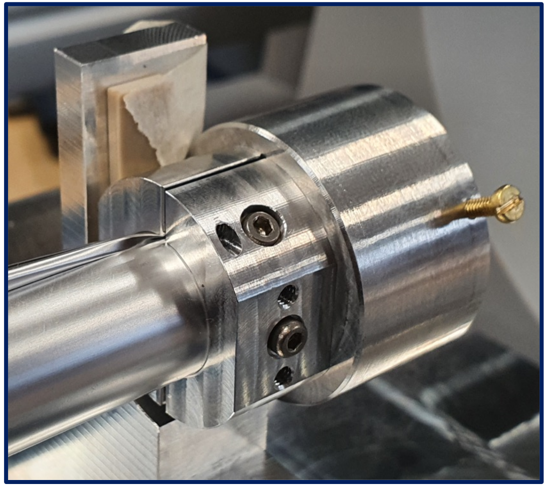
First test beam with final modules in 2006

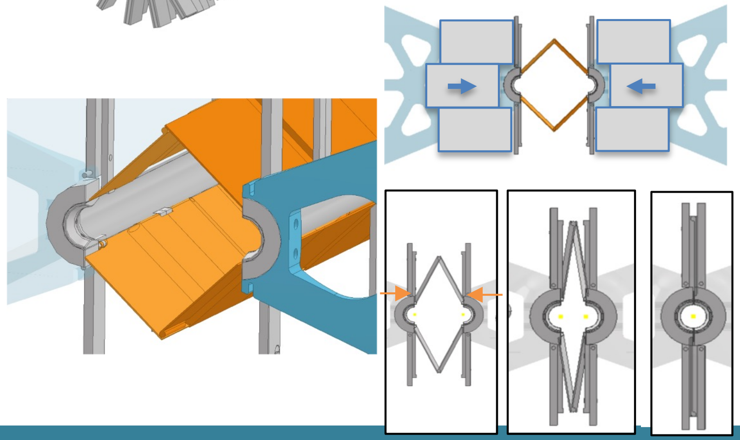
Silicon on pyrex



- Thin-foil Shield
  - Tension tests, conclusions & possible next steps
- Wire/Fibre Shield
  - Proposed layout, feasibility & prototyping option
- Open/Closed Position Mechanics
  - Concept mechanism, linkage & setup requirements

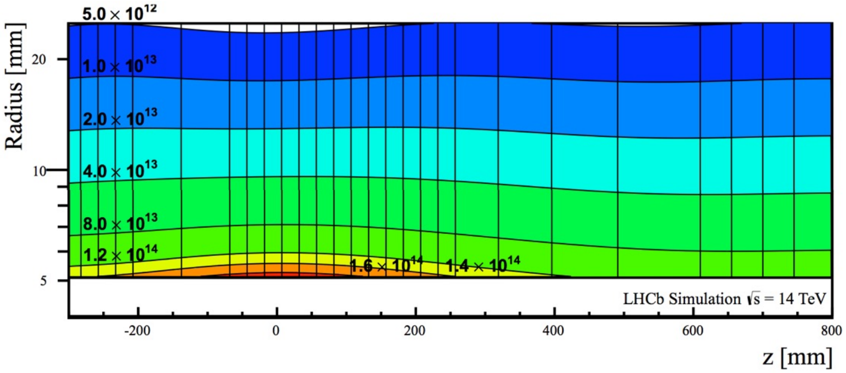






Design considerations – Radiation and data rates

- At 5 mm, fluence translates to :
  1.6×10^{14} 1MeV n_{eq}/fb.
  after 300/fb➔ ~5×10^{16} n_{eq}
- Very challenging constraint for fast timing devices.
- At that distance, pixel hit rates are estimated to be close to 350 kHits/s
- Estimated data rates can be as high as 250 Gbits/s

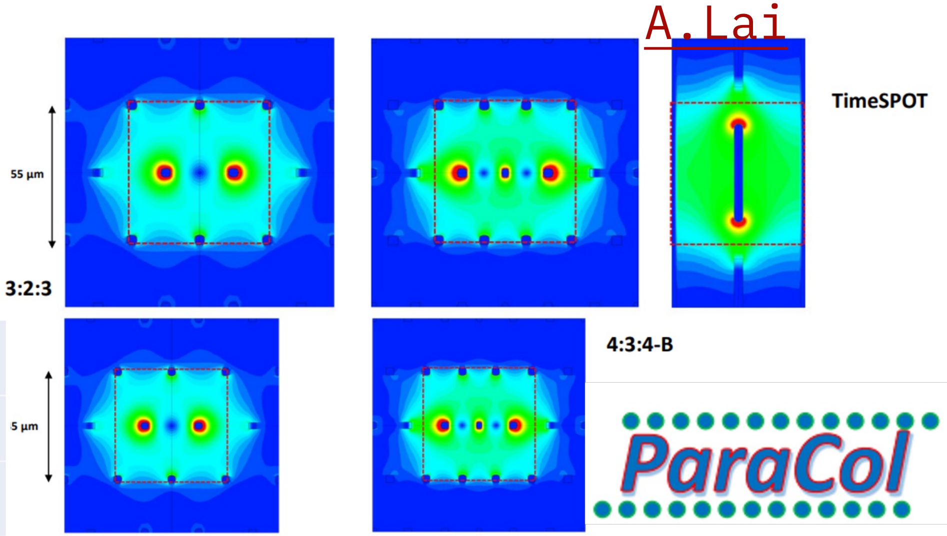


3D Sensors

Progress on 3D sensors from Timespot → Ignite/Paracol.

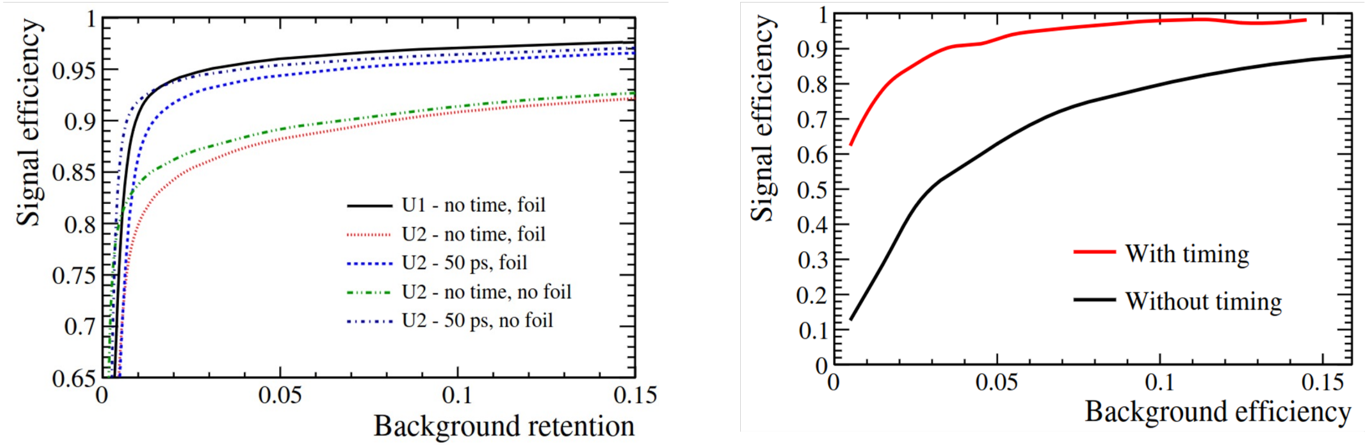
Joint effort with CERN/Cagliari/Nikhef starting for 3D sensor production.

Still need to prove operability under non-uniform irradiation to up to 2.5e16 1MeV n_{eq}

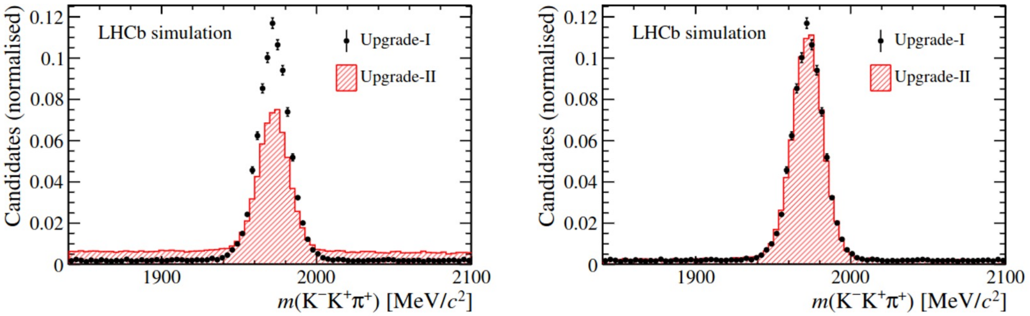


Sensor:	CCT	Std.Dev. CCT	Centroid	Std.Dev. (Centroid)	Time Res. IC-CSA
TimeSPOT	293.3 ps	54.95 ps	108.2 ps	30.89 ps	27.5 ps
ParaColl 3:2:3-45	329.1 ps	52.74 ps	115 ps	29.77 ps	26.3 ps
ParaColl 3:2:3-55	406.3 ps	76.73 ps	148.1 ps	39.55 ps	38.3 ps
ParaColl 4:3:4-45	301.6 ps	52.42 ps	100.9 ps	27 ps	26.2 ps
ParaColl 4:3:4-55	368.6 ps	65.06 ps	130.5 ps	33.61 ps	32.1 ps

Smaller pitch will help getting to 10 µm.
(55µm → ~14 µm res,
50 µm 3d → 12 µm res @ 0 deg)



Timing improves trigger efficiency



https://cds.cern.ch/record/2800144

And eventually signal purity

ASICs - PicoPix

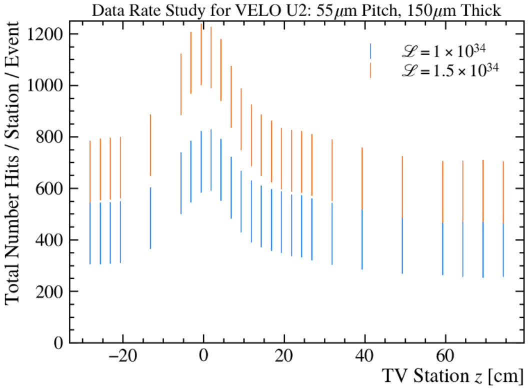
Huge data rate poses severe constraints the ASIC design.

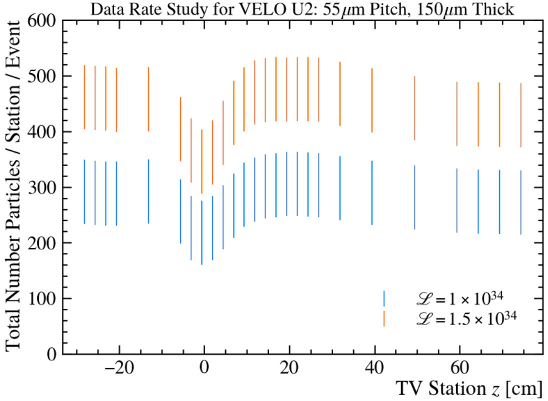
On pixel data processing to compress d

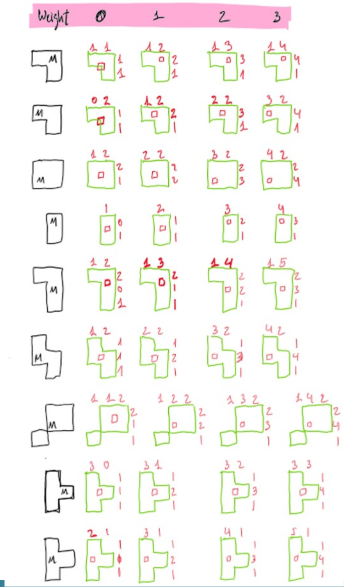
Cluster events in X and Y in a single data output packets:

- 1 data packet per cluster
- Main (M) pixel found using arbitration circuitry as in Medipix4
- TOA and TOT only on Main (M) pixel
- Hitmap of pixels around Master (M)

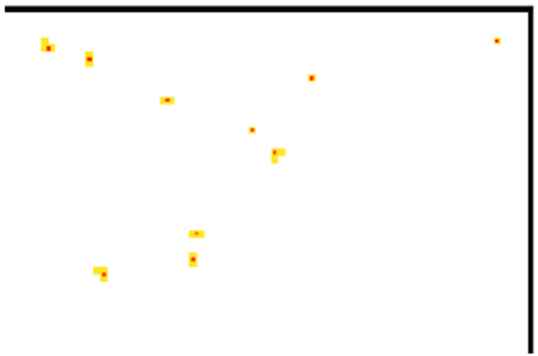
Potentially resolution can be better than simple binary, but requires off-ASIC cluster processing.







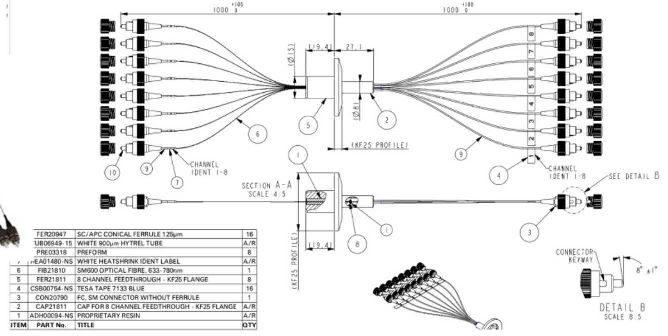
Data rate due to long clusters can be extreme!

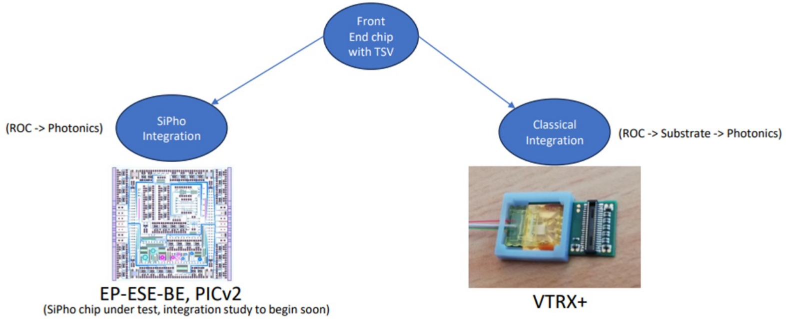


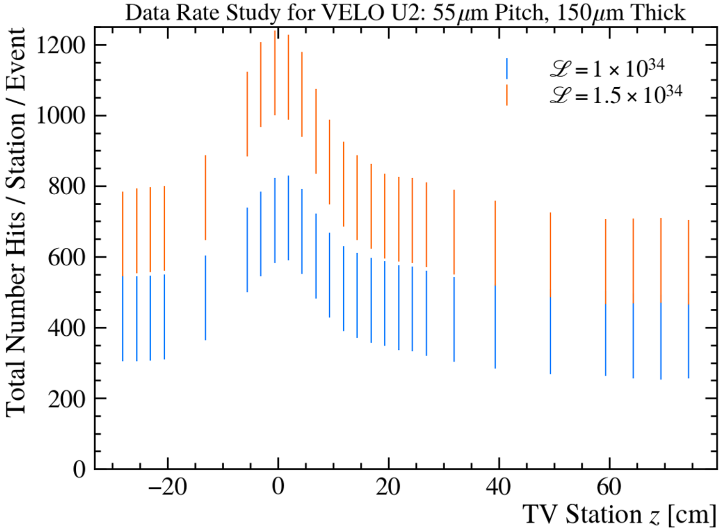
Optical links → feed-throughs

Estimated AVERAGE Number of optical links (inside vacuum!): 82/module

- Actual number varies by up to 80%.
- <u>Expensive Feedthroughs (20k€ each station)</u>: High rate modules will need to share feedthroughs (and TELL400s) with "low rate ones"
- Si-Pho could half these costs.

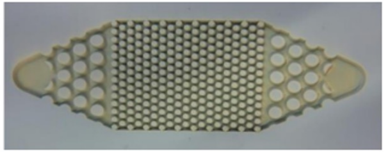




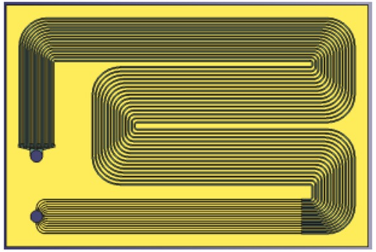


3D printed Ceramics or metals

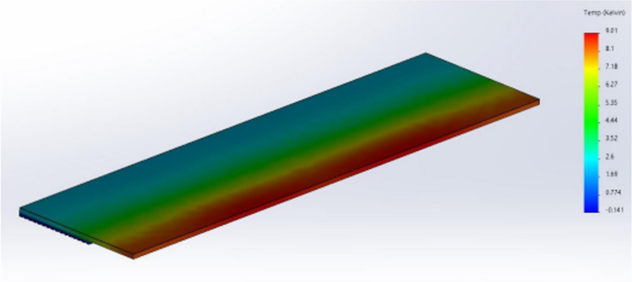
Substrate composed of very little material must also provide sufficient heat extraction and a low operating temperature



©Fraunhofer IKTS

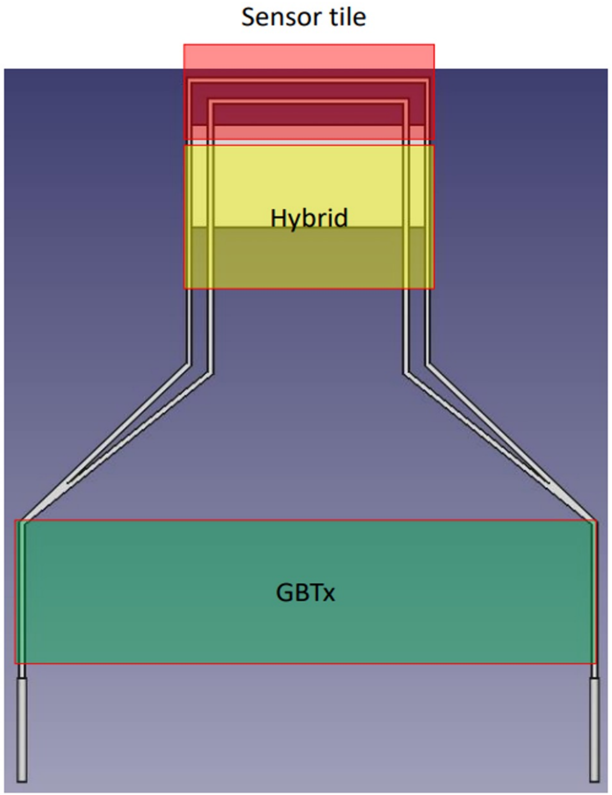


SNAKEI based design to optimize printing parameters/test feasibility

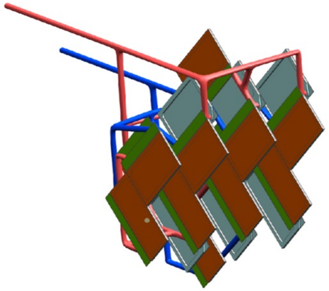


© Oscar Augusto

Simplified FEA focusing on the 5 mm overhang. Substrate in alumina and heat conduction on one side of the cooling plate and Stycast (100um). For $2W/cm^2$, $\Delta T \sim 9$ C.

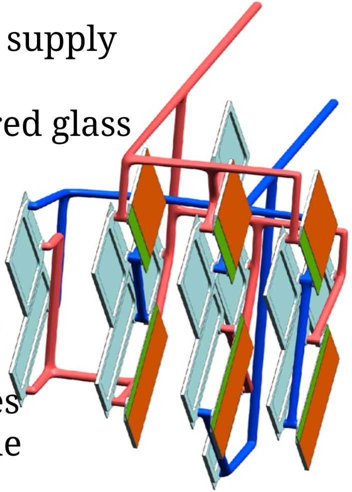


Combining functions in the module
co



A single set of modules:
- Design can change depending on location inside detector
  - Modules can be replaced
  - 1 set of LV/cooling connection

Multi functional support:
- 3d printed aluminium
- Hollow tubes, for cooling supply
- Low voltage supply.
- If more stiffness is required glass fiber-epoxy can be added



3d printed support gives option to create extreme layouts, like the onion shape

Limited hit efficiency coming from electronics

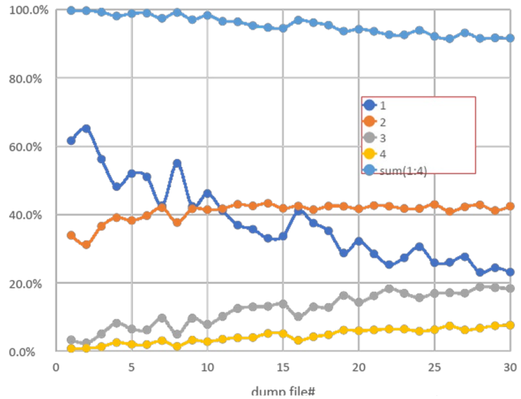
Clustering Efficiency ~97.2%

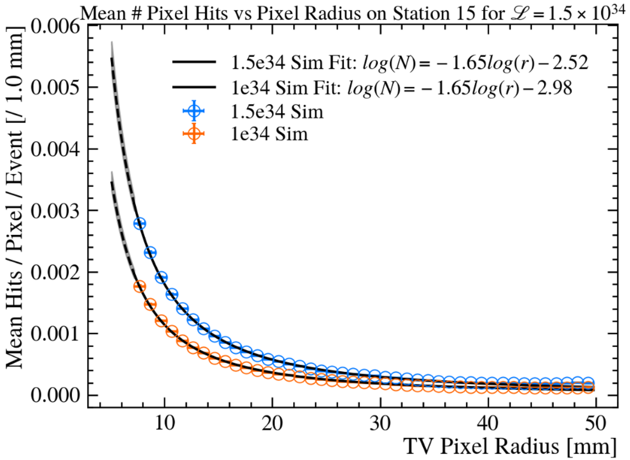
X. Llopart (13/Feb)

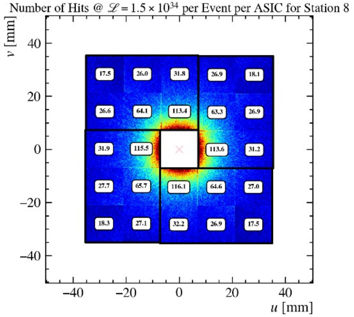
Dead pixels due to spillover of about 3%

Compound "design" hit efficiency as low as

Increasing these efficiencies is a main R&D point!







Baseline Detector layout

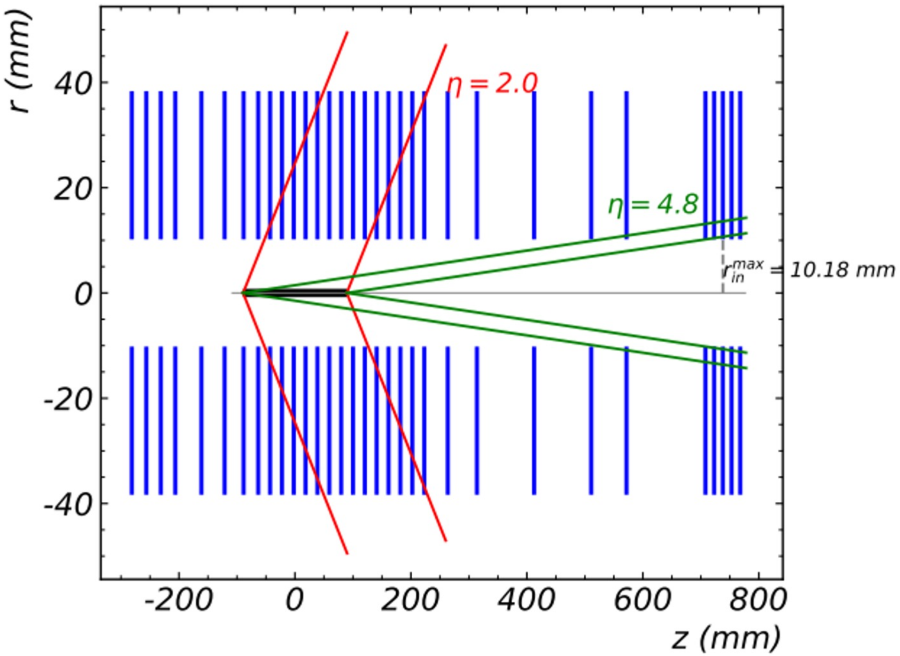
Acceptance optimisation taking into account:

- 2σ luminous region
- At least <u>5 planes in acceptance.</u>
- Eta max of 4.8 for 100% acceptance

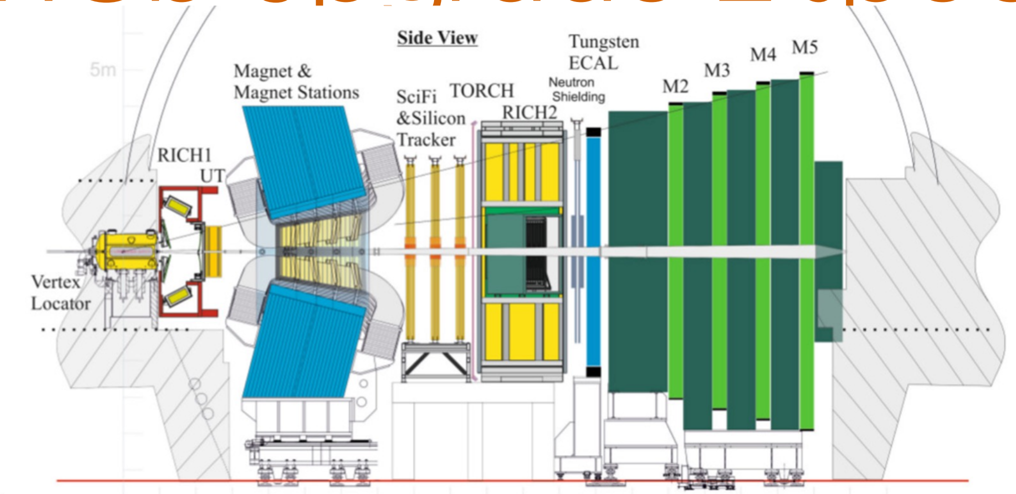
Also assuming that we can achieve ~10 μm spatial resolution ⇒ smaller pitch implied

Currently optimistic Baseline simulation, with **150 μm thick sensors**, **50 μm ASICs**, **400 μm Cooling substrate**, **75 μm RF-shield cylinder**

32 stations!



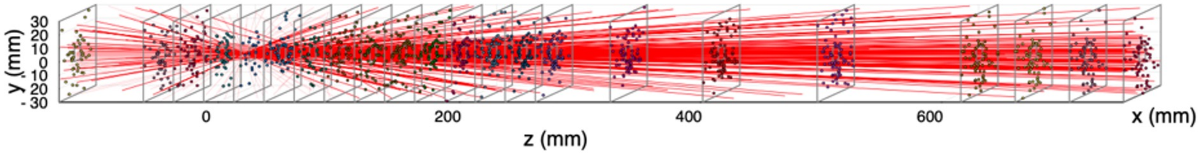
LHCb Upgrade-2 spectrometer



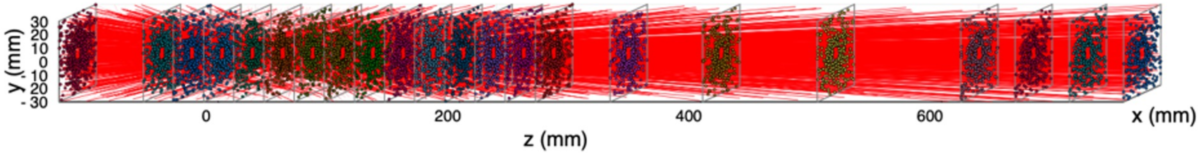
- Spectrometer layout to be further optimised
  - Key ingredient: fast timing in tracking, PID, and calo's
- Innovative technology for detector and data processing
  - Key ingredient: (sustainable) heterogeneous computing

Experimental goal: maintain similar efficiencies for much higher occupancies

Velo Run3 pileup ~6 :

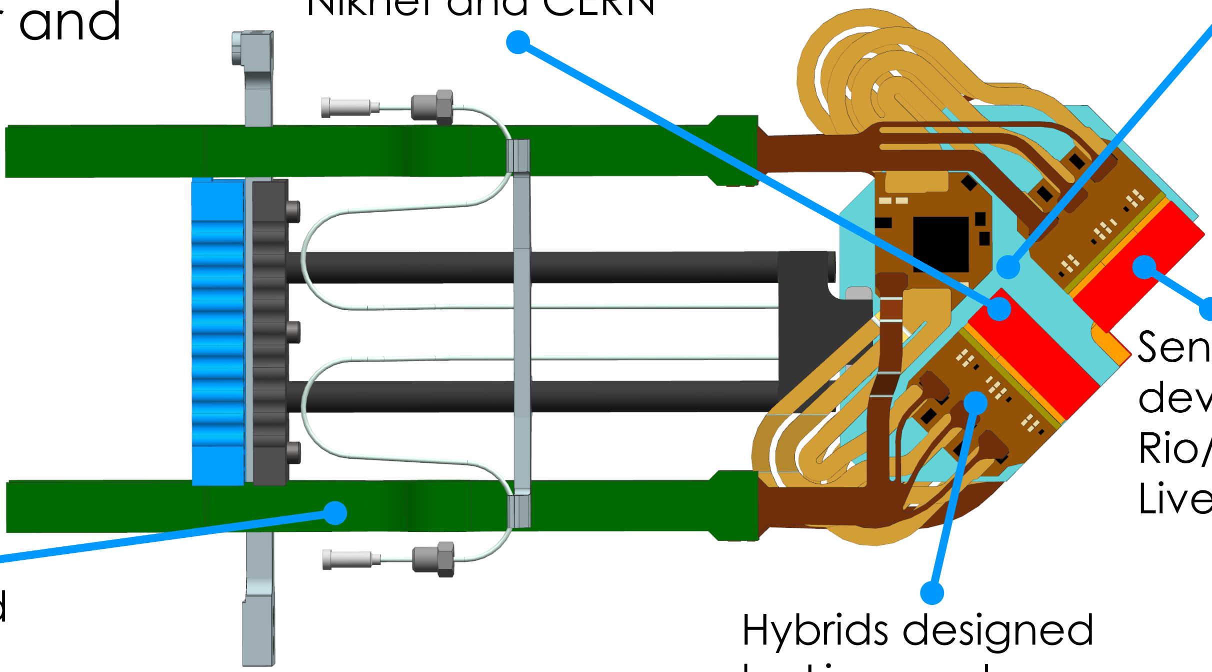


Upgrade 2 pileup ~42 :



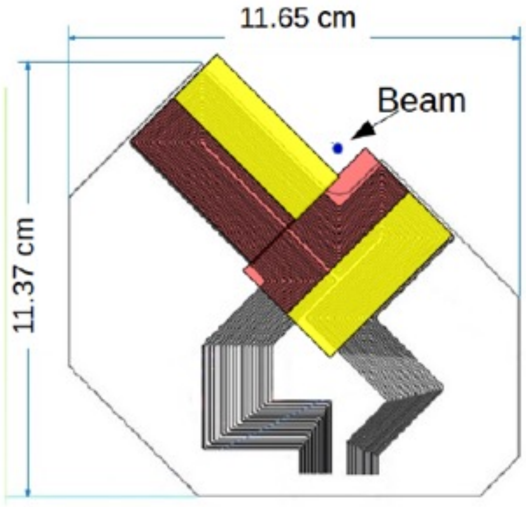
Modules

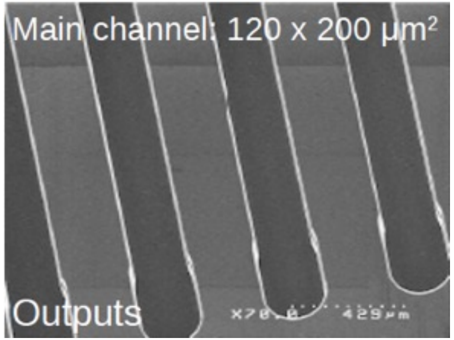
Modules to be built in Manchester and Nikhef

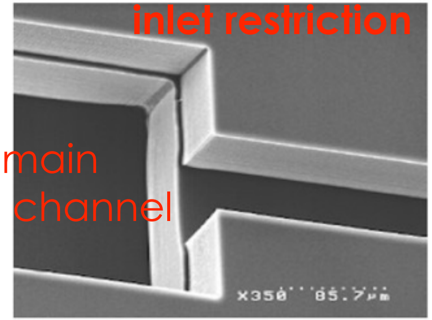


Microchannel cooling

- Efficient cooling solution is required to maintain the sensors at < -20°C
- No CTE mismatch
- This is provided by the novel technique of evaporative CO_2 circulating in 120 µm x 200 µm channels within a silicon substrate.

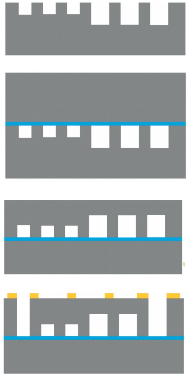






SEM images of etched wafer before bonding

Manufacturing and assembly

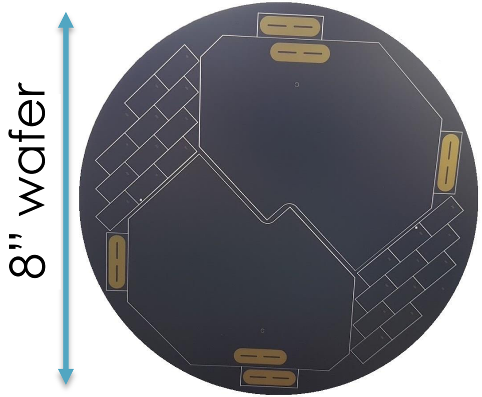


Channel etching

Cap wafer bonding

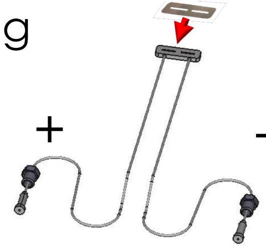
Thinning (both sides)

Inlet/Outlet etching



Silicon pre-tinning

+



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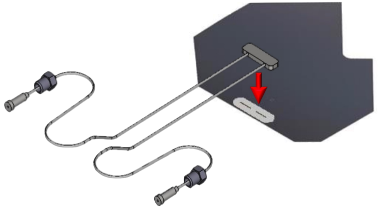
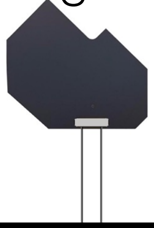
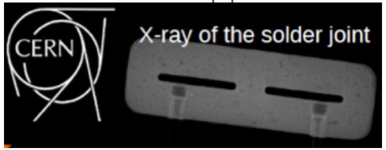
Alignment



Soldering

+





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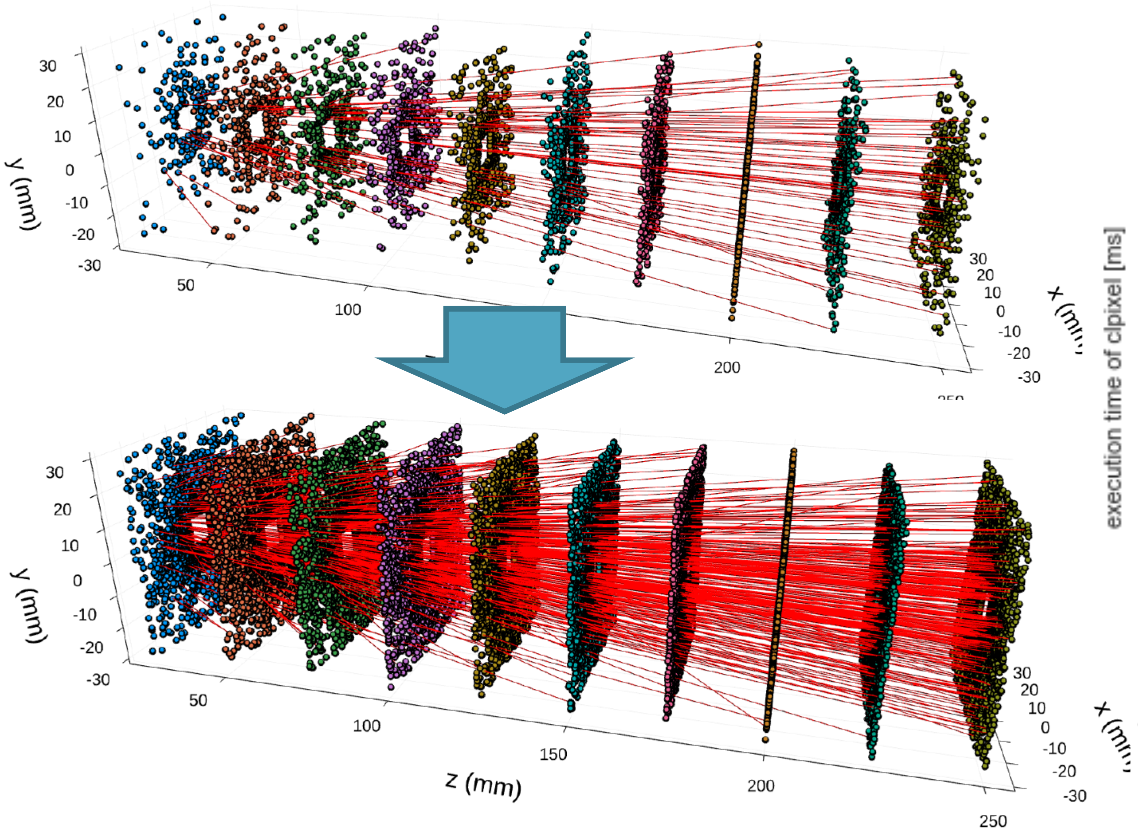
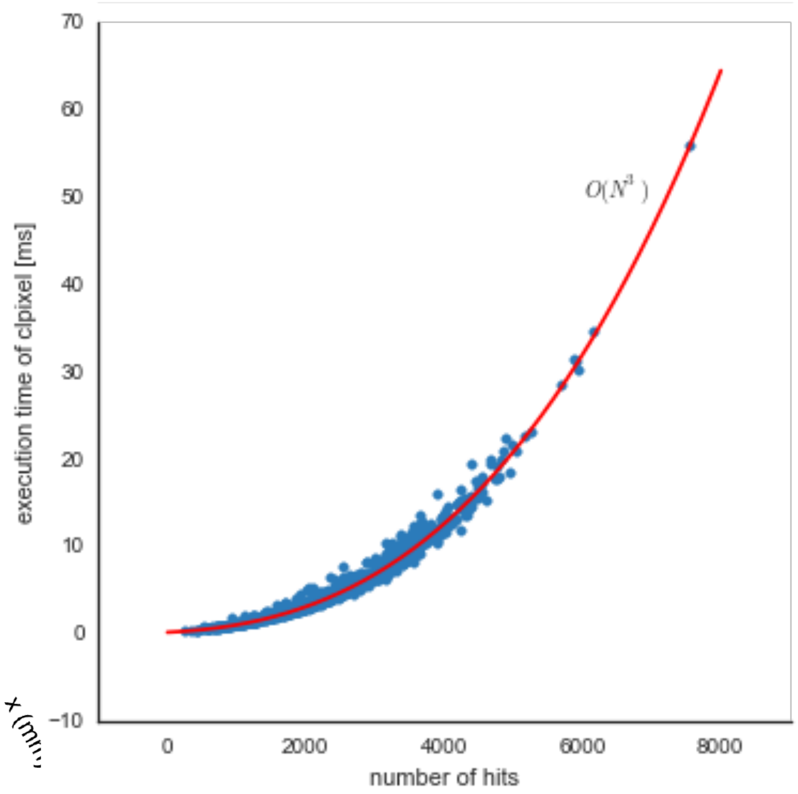
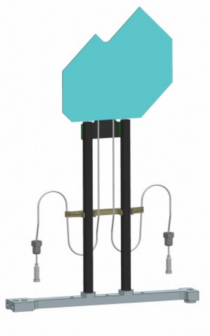
Final assembly can Withstand 200 bar

Pattern recognition

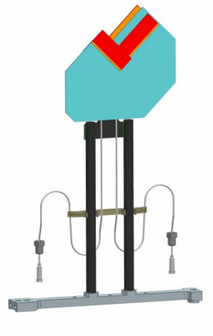




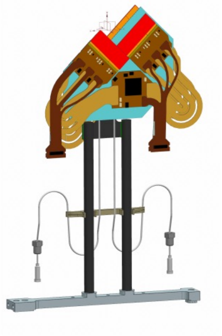
Module Production



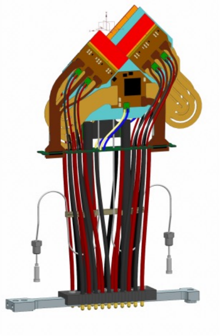
Mechanical construction



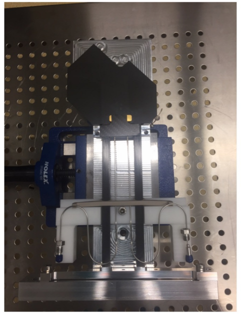
Precision tile placement to 10 µm

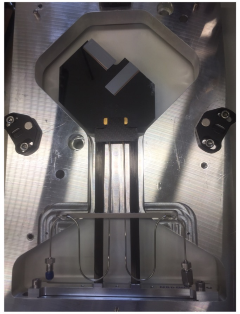


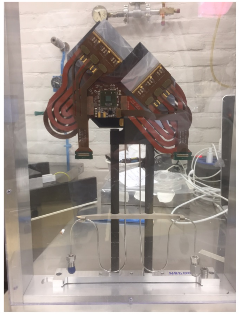
Flex circuit placement

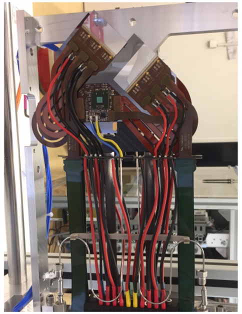


wire bonding and HV/LV/data cable attachment









Three modules in SPS test beam