OBELIX sensor for the upgrade of the Belle II Vertex Detector

Roua BOUDAGGA – CPPM, Aix Marseille Université, CNRS/IN2P3, Marseille, France

on behalf of the Belle II VTX collaboration

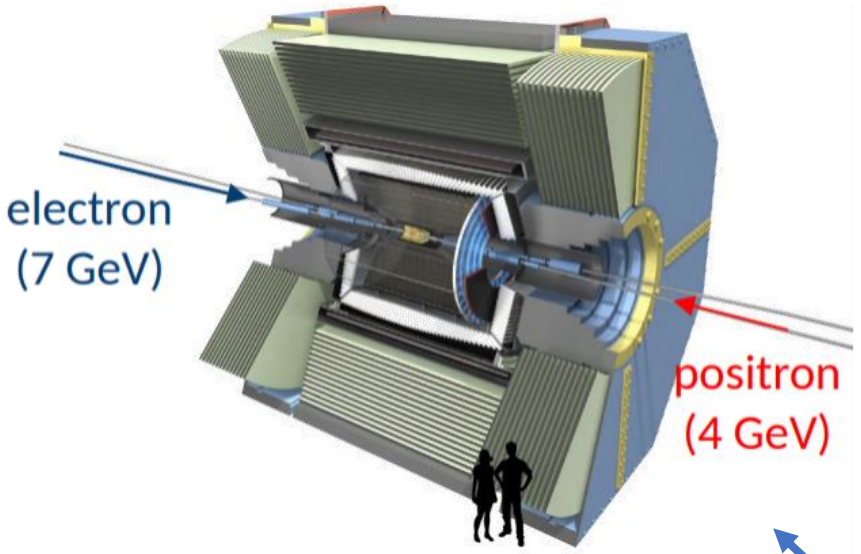
boudagga@cppm.in2p3.fr

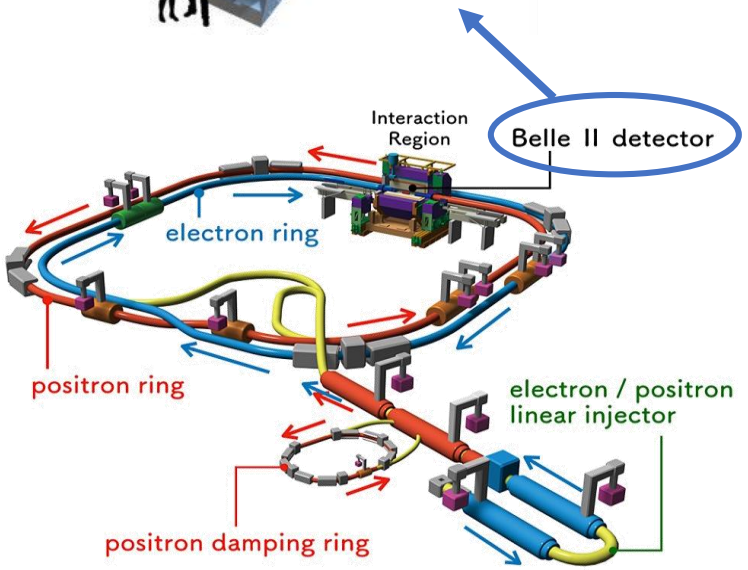
Outline

1. The BELLE II Experiment
2. The current Vertex Detector (VXD)
3. The VTX Upgrade Proposal
4. The Tower Jazz-Monopix2 chip
5. The OBELIX sensor : **O**ptimized **BEL**LE2 p**IX**el sensor
6. Conclusions

The Belle II Experiment

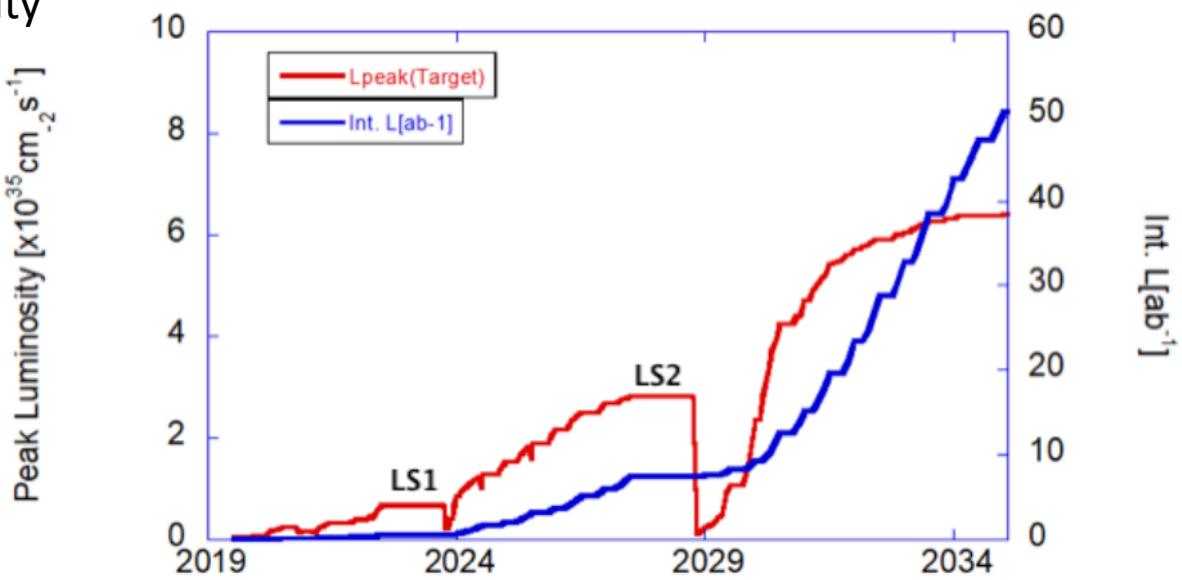
- Located at the SuperKEK-B collider in Tsukuba,Japan
- Asymmetric e^+- e^- collider at 4 / 7 GeV and √s = 10.58 GeV
- Luminosity frontier experiment, exploring new physics
- Restart beam operation in 2024 after a **long shutdown (LS1)**
- World luminosity record : $\mathbf{L_{max} = 0.47x10^{35}\ cm^{-2}\ s^{-1}}$ in June 2022
- Target instantaneous luminosity of $\mathbf{6x10^{35}\ cm^{-2}\ s^{-1}}$, currently $\mathbf{0.47x10^{35}cm^{-2}s^{-1}}$
- Target integrated luminosity of $\mathbf{50\ ab^{-1}}$, currently $\mathbf{0.43\ ab^{-1}}$
  - Machine related beam background will increase with high luminosity
  - Efficiency, resolution and performance of data tracking could degrade with higher occupancy from background
  - Extrapolation to this target luminosity has large uncertainty and limited safety margins





The Belle II Upgrade Motivations

- An upgrade of the machine elements and the detector's **interaction region (IR)** is required :
  - To cope with the higher luminosity provided by the SuperKEK-B accelerator
  - To improve detector robustness against high backgrounds
  - To provide larger safety factors for running at higher luminosity
  - To increase longer term subdetector radiation resistance
  - To improve overall physics performance
- A **long shutdown (LS2)** is foreseen around 2028 and provides the opportunity to install an upgraded detector



➡ **A new vertex detector concept VXD is proposed**

The Current Vertex Detector (VXD)

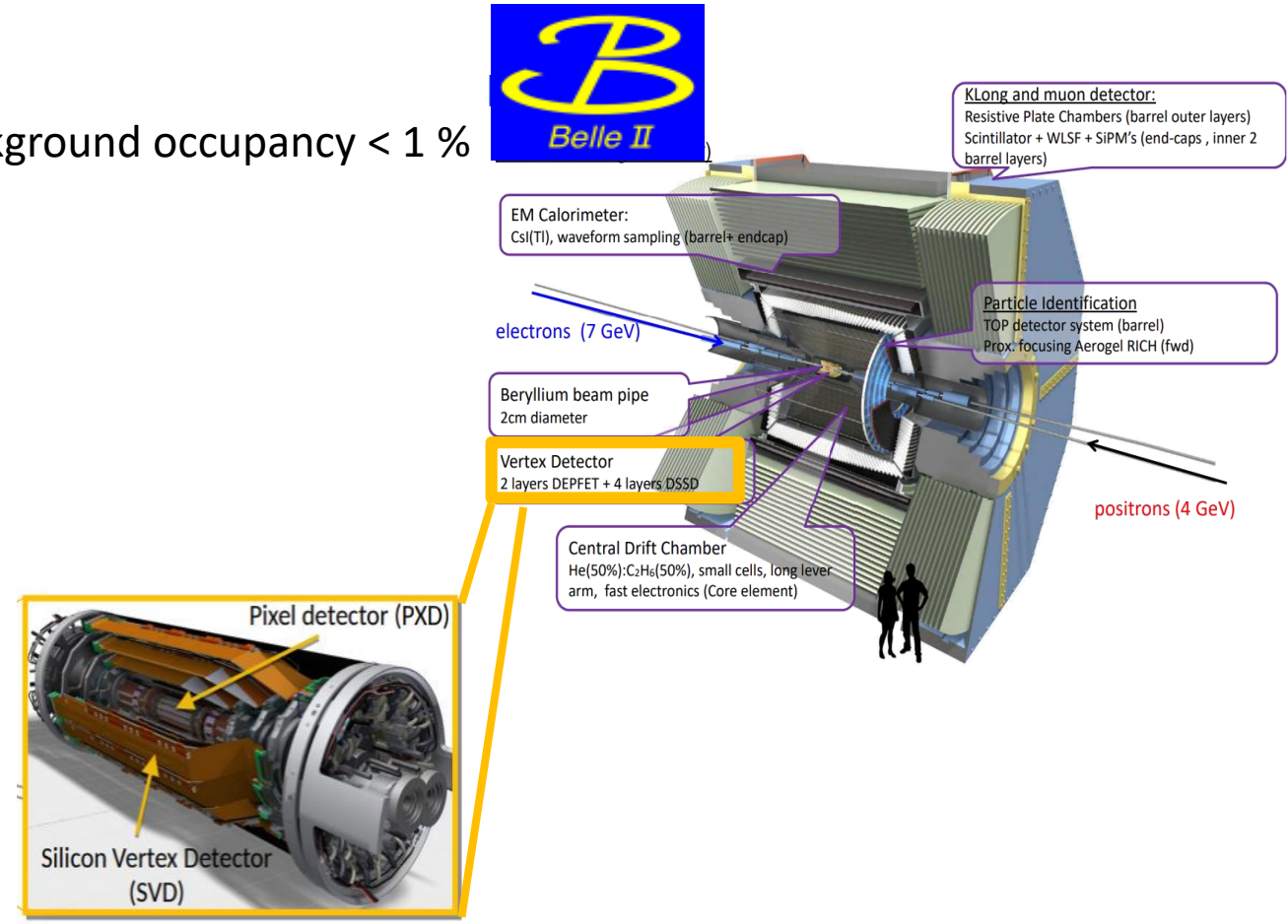
- The main tracker device is the central drift chamber (CDC), which is complemented by the Vertex Detector (VXD)

- Its main task is the reconstruction of decay vertices in addition to low momentum track finding

- Current VXD performance good and operating with low background occupancy < 1 %
  - Well below limits : PXD ~ 3%, SVD ~ 5%

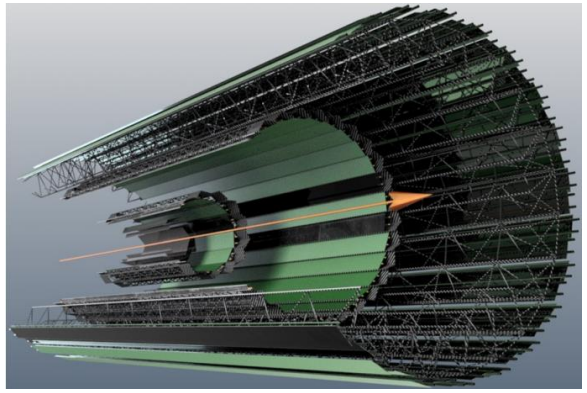
- Two different technologies compose the VXD :
  - Pixel Detector (**PXD**)
    - Two layers of DEPFET pixel sensor
    - 50 to 75 µm pixel pitch
    - 20 µs integration time

  - Silicon Vertex Detector (**SVD**)
    - Four layers of double sided silicon strip sensor
    - 6 cm long strips
    - Expected occupancy ~ 3% after LS2

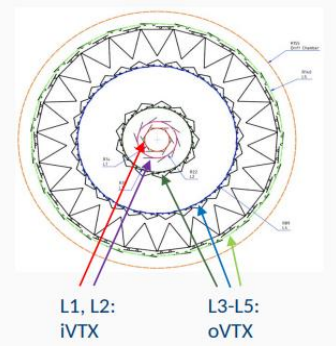


boudagga@cppm.in2p3.fr

The VTX Upgrade proposal



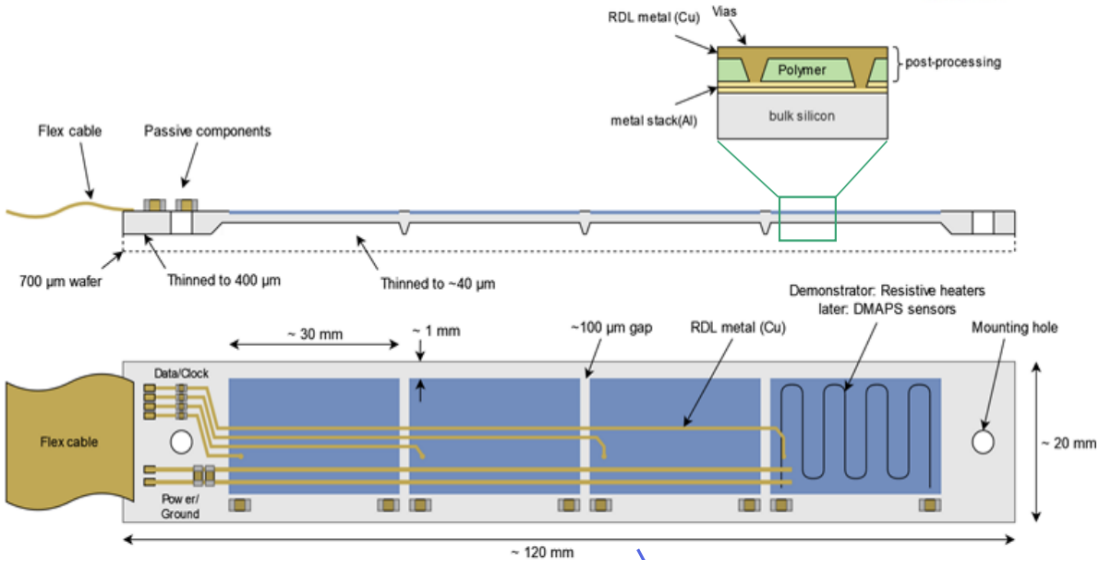
- A new fully pixelated CMOS detector to replace the VXD ➡ VTX
- Improved tracking resolution and space-time granularity
- Reduced material budget less than 2%X0 instead of 3.8%X0 (sum of all layers)
- 5 straight layers with **D**epleted **M**onolithic **A**ctive CMOS **P**ixel **S**ensors (**DMAPS**) process
- L1 and L2 (iVTX)
  - All silicon ladders
  - Air cooling (constrains power)
- L3 to L5 (oVTX)
  - Carbon fiber support frame
  - Cold plate with liquid cooling



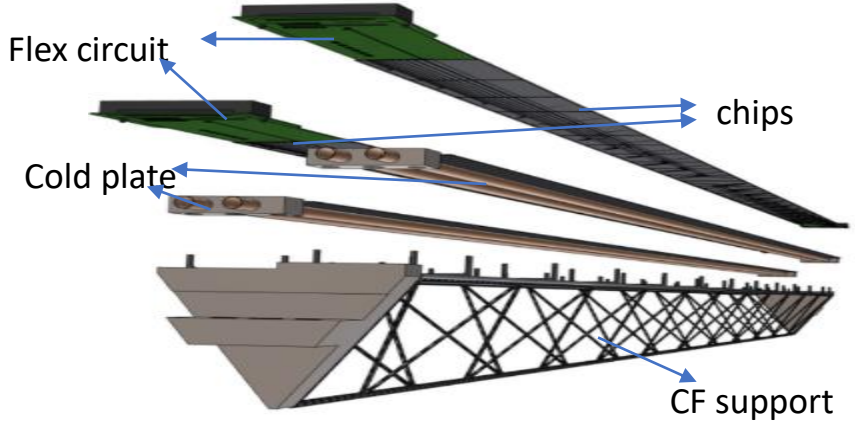
	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	8	18	26	
# Sensors	4	4	8	16	48	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.1	0.1	0.3	0.5	0.8	% X_0

The VTX detector mechanics

- Ladder structure design inspired by ALICE ITS2, composed of:
  - Carbon Fiber support structure
  - Cold-plate with pipes for liquid coolant circulation
  - Chip and Flex circuit for power and signal glued on top



Schematic view of the iVTX ladder design

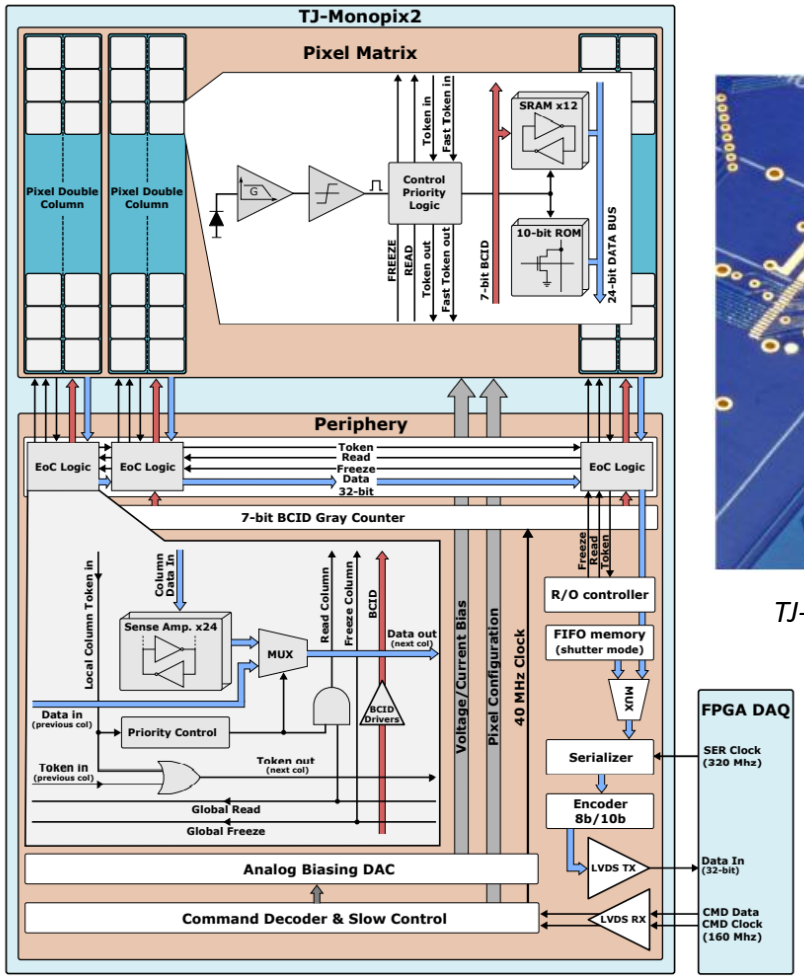


Exploded view of the oVTX

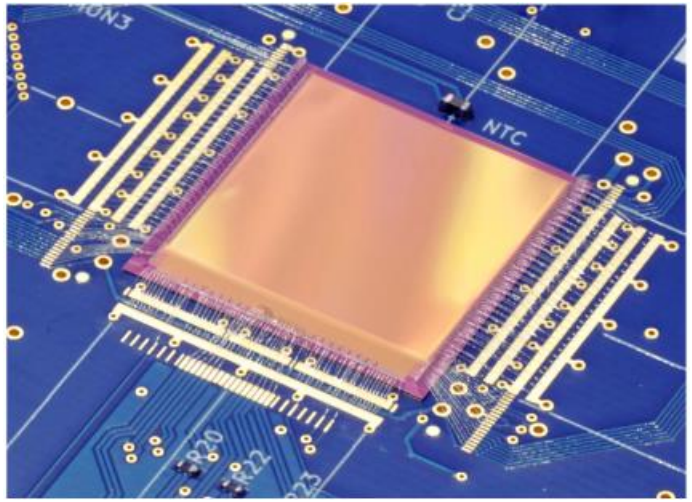
- iVTX Inner Layer Concept :
  - 4 contiguous sensors diced as a block from the wafer
  - Flex print cables
  - Redistribution layer for interconnection
  - Heterogeneous thinning for thinness and stiffness

- A same monolithic CMOS pixel sensor chip for all layers : **Optimized BELLE II pIXel sensor (OBELIX)**

The Tower Jazz-Monopix2 as prototype



Chip architecture of TJ-Monopix2



TJ-Monopix2 sensor bonded on a test board

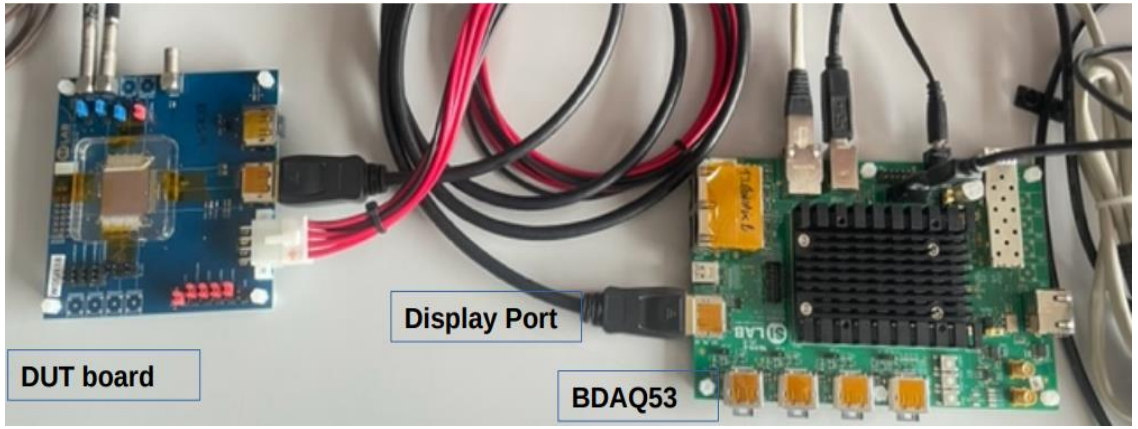
- Developed for ATLAS experiment
  - FE derived from ALPIDE
  - 4 FE flavors
  - Column-drain R/O architecture
- DMAPS **Tower Jazz 180 nm** process
- 2 × 2 cm² chip : 512 × 512 pixels
- Pixel pitch: 33.04 × 33.04 µm²
- Expected from design (simulations):
  - ~ 100 e− min. threshold
  - 5-10 e− threshold dispersion (tuned)
  - >97% efficiency at 10^{15} n_{eq}/cm²
  - ~ 5 e− noise
  - Fully efficient with hit rate 120 MHz/cm²
  - Power: ~ 1 µW/pixel

Baseline option for OBELIX design

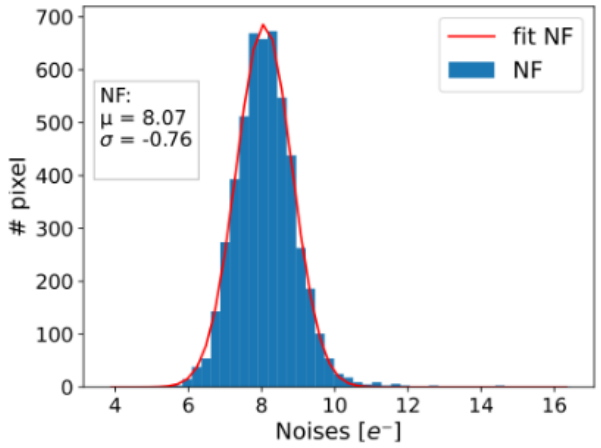
The Tower Jazz-Monopix2 Testing

- **Full characterization** on bench:
  - Threshold scans (lowest value, dispersion)
  - Noise testing
  - ToT (Time Over Threshold) calibration

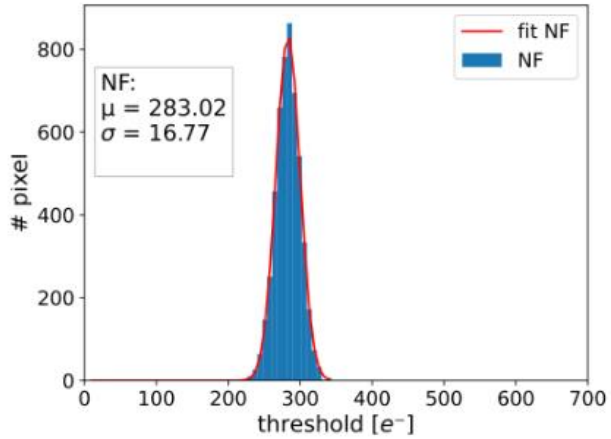
- Control and data acquisition system based on the BDAQ53 setup



Setup for BDAQ53 Test – developed by Bonn



Noise distribution



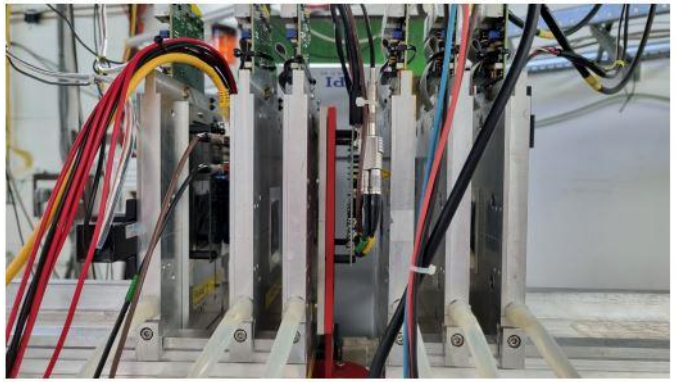
Threshold distribution.

- Typical characterization test results after tuning the matrix :
  - Thresholds between 200 to 300 e−
  - Average noise varies from 7 to 8 e−

- Tests on several chips are on going in different Labs :
  (Bonn, Pisa, HEPHY, CPPM, Gottingen)

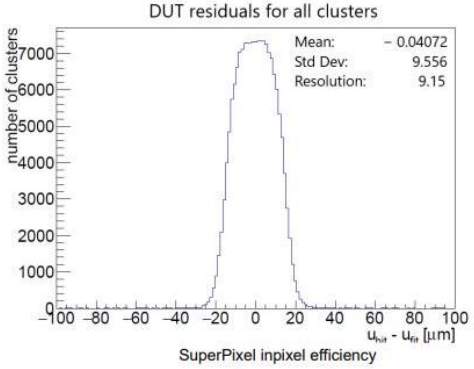
The Tower Jazz-Monopix2 Testing

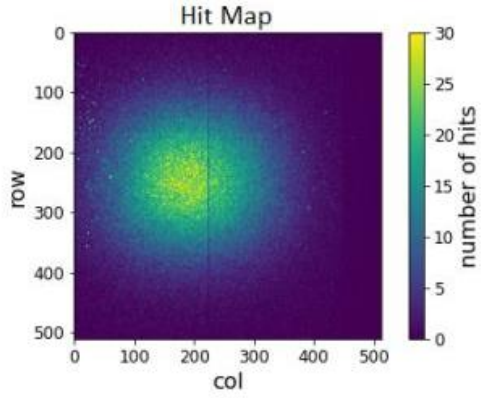
- **Full characterization@DESY**:
  - Efficiency/Resolution measurements
  - Radiation hardness (NIEL and TID irradiation campaigns in progress)



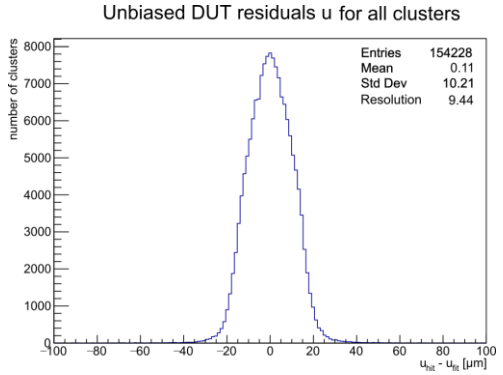
Setup for testbeam – @Desy

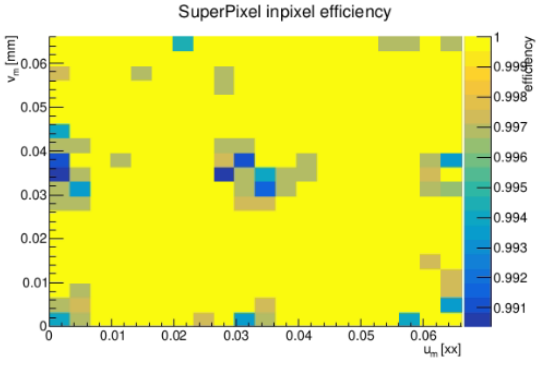
- **Performed at DESY in June 2022**:
  - Unirradiated chips
  - Preliminary settings used, beam e- at around 5GeV
  - Use very high threshold ~ 550 e-
  - Hit efficiency : 99.54 +- 0.04%
  - Cluster position residuals: 9.15 µm





- **New Test beam in July 2023 (**Data analysis on-going):
  - Lower threshold settings ~ 310e$^-$ threshold
  - Irradiated chips
- Some preliminary results shown for the irradiated chip at 5x10^{14} n_{eq}/cm^2
  - Efficiency of 99.79% for irradiated chip, with small inefficiency in the pixel corners
  - Cluster position residuals : 9.44 µm -> about pitch/√12 ~ 9.5 µm binary resolution
  - Decrease in cluster size after irradiation

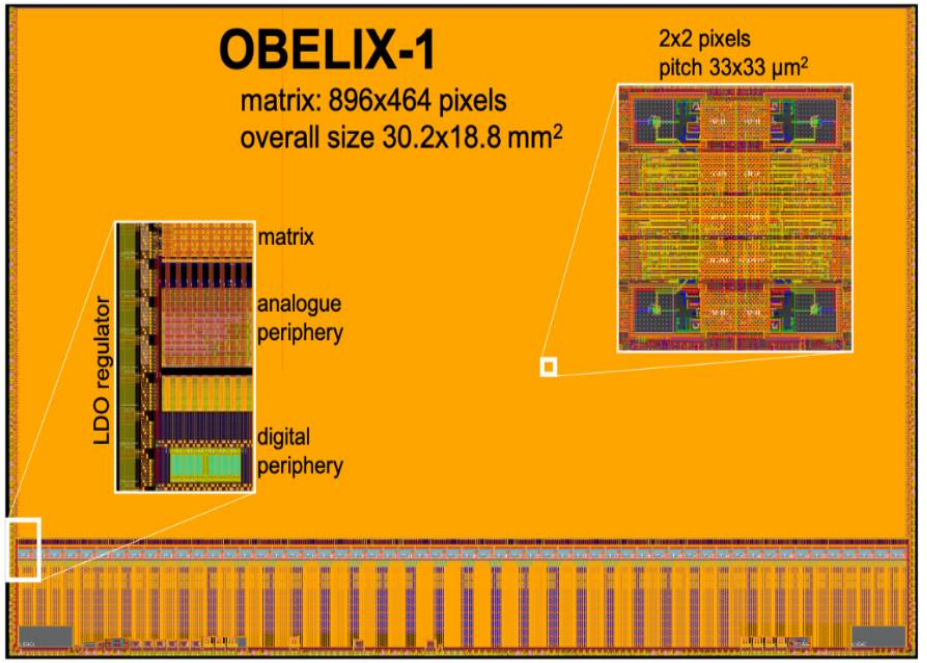




The OBELIX Sensor

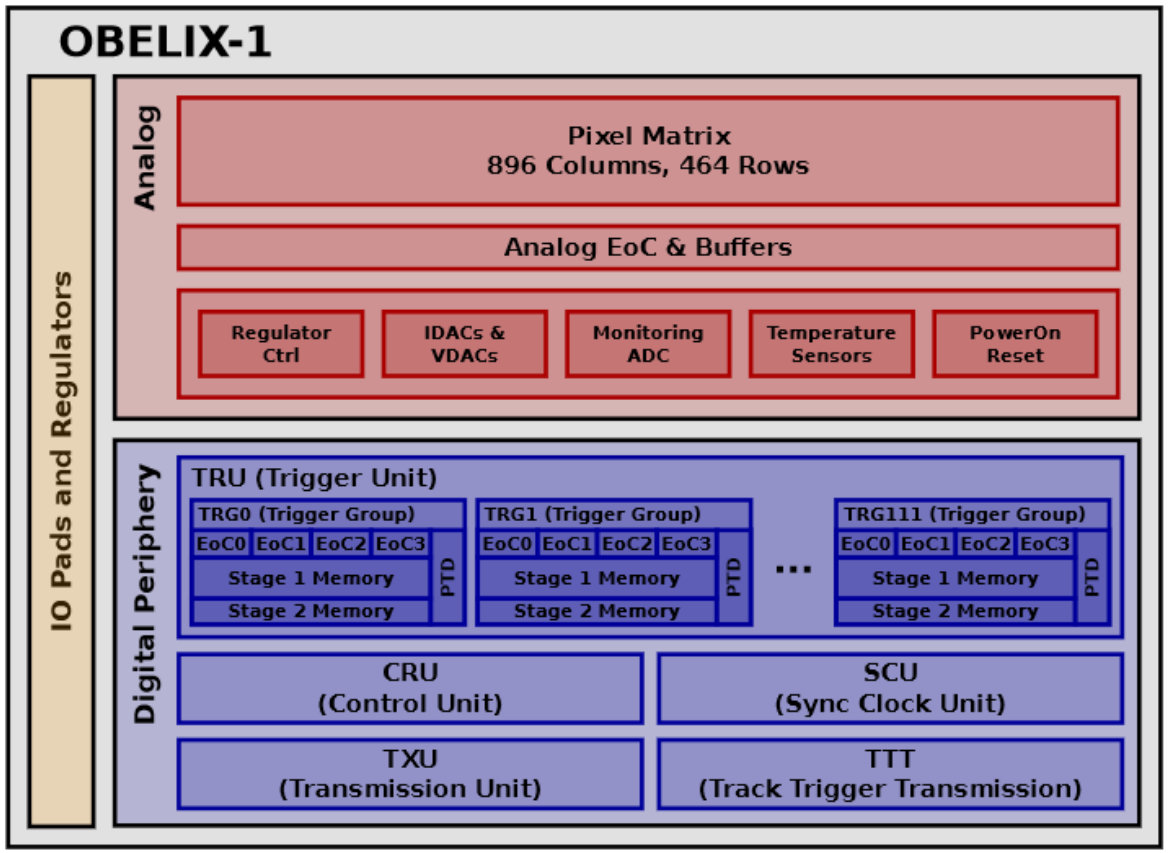
Sensor specifications :

- Tower Jazz 180 nm process
- Hit rate up to 120MHz/cm²
- TID tolerance : 10 MRad / year
- NIEL tolerance : $5x10^{13}$ $n_{eq}/cm^2/year$
- Spatial resolution < 15µm
- Power < 200 mW/cm²
- Time precision < 100 ns
- Trigger at 30KHz average frequency with 5-10 µs latency



- 464 rows and 896 columns
- Overall sensor dimensions around 30.2x18.8 mm²
- Pixel pitch 33x33 µm²
- Main design is based on the **Tower Jazz-Monopix2** chip

The OBELIX Block Diagram



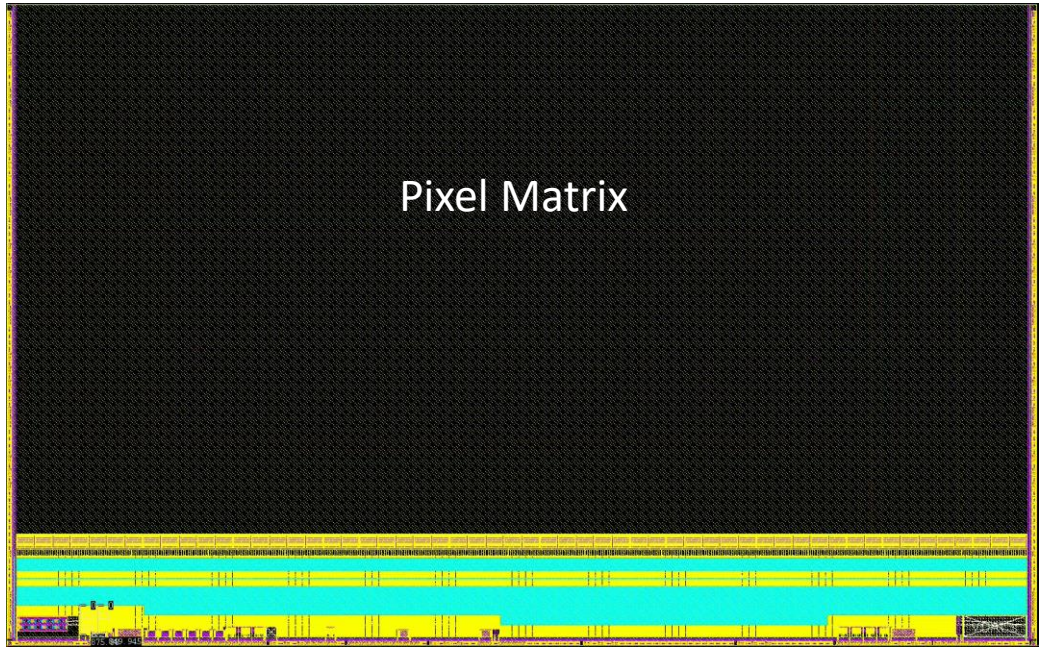
Analog
- Pixel matrix from **TJ-Monopix2**
- Column drain architecture
- Monitoring ADC
- Temperature sensors

Power pads
- Power regulators added
- Simplified system integration

Digital Periphery
- Main clk-in : 160MHz
- New end-of-column adapted to Belle II trigger
- Timestamped hits stored in memories
- Read-out when timestamp matched with trigger
- Single output at 320 MHz average bandwidth
- RD53 control/readout protocol

The pixel matrix of OBELIX

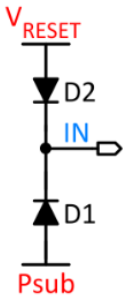
- The OBELIX sensor inherits the performance of the pixel matrix from TJ-Monopix2 sensor.
- The same pitch, 33 × 33 µm², with the same layout for the analog and digital parts
- The Matrix pixel of TJ-Monopix2 is composed of 4 pixel flavors with differences in the Front-End (FE) amplifier and detector input coupling (AC or DC) :
  - Normal FE / Cascode FE
  - HV Cascode FE / HV FE
  - **Based on current characterization results, 2 FE flavors are chosen for OBELIX on equal area :**
    - **Cascode FE**
    - **HV Cascode FE**



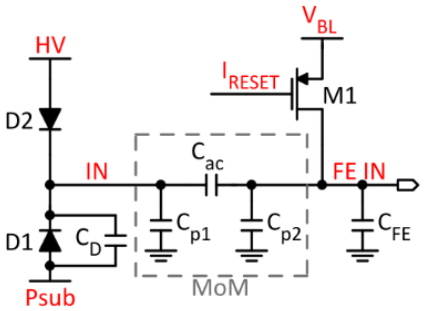
Floorplan of OBELIX (Design on going)

The analog FE design

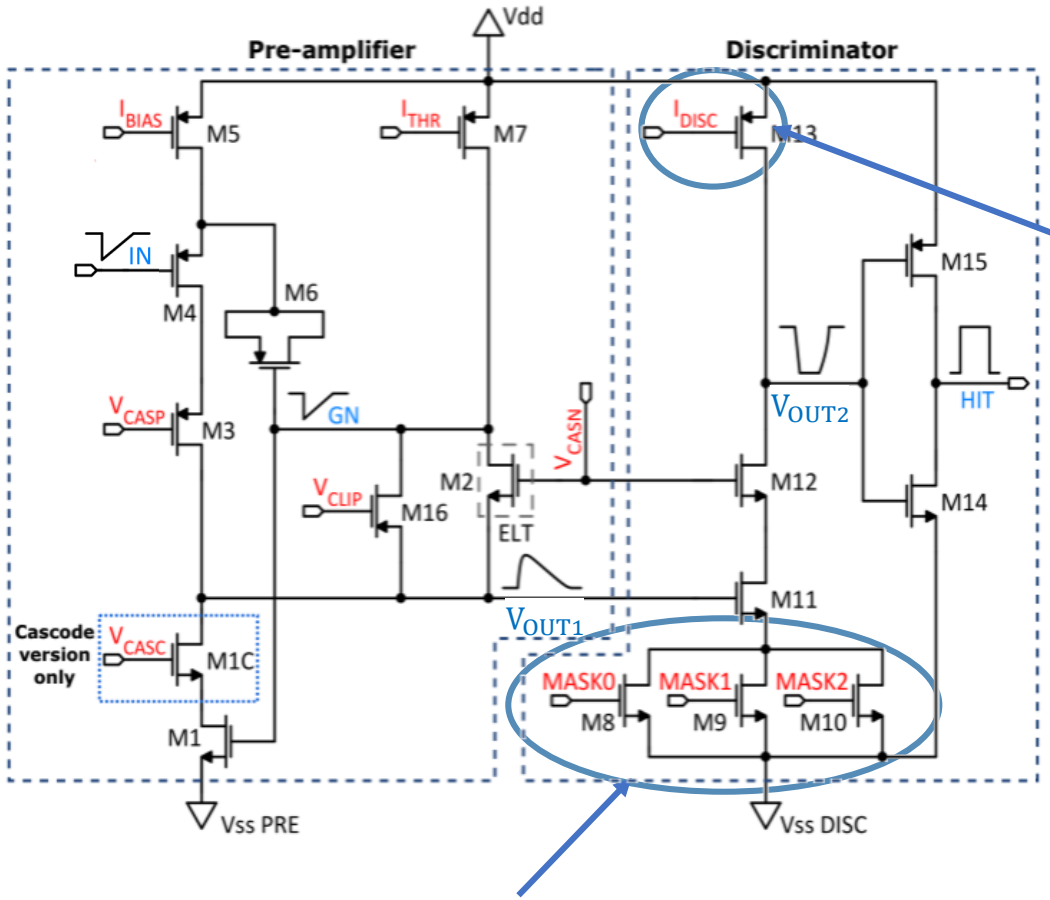
- Two flavors with a cascode pre-amplifier :
  - With an input **DC-coupling** using a forward biased diode **(Cascode FE)**
  - With an input **AC-coupling** allowing higher bias voltage above 30V (**HV Cascode FE)**



Input DC-coupling

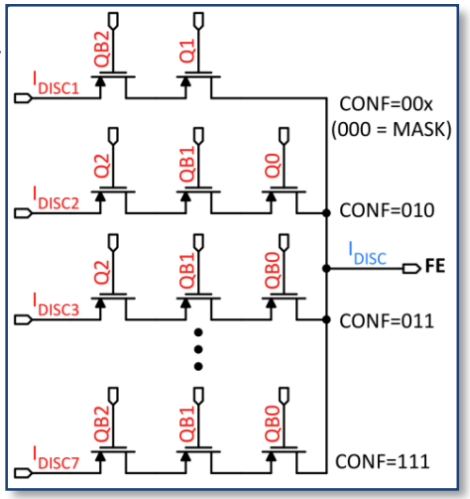


Input AC-coupling



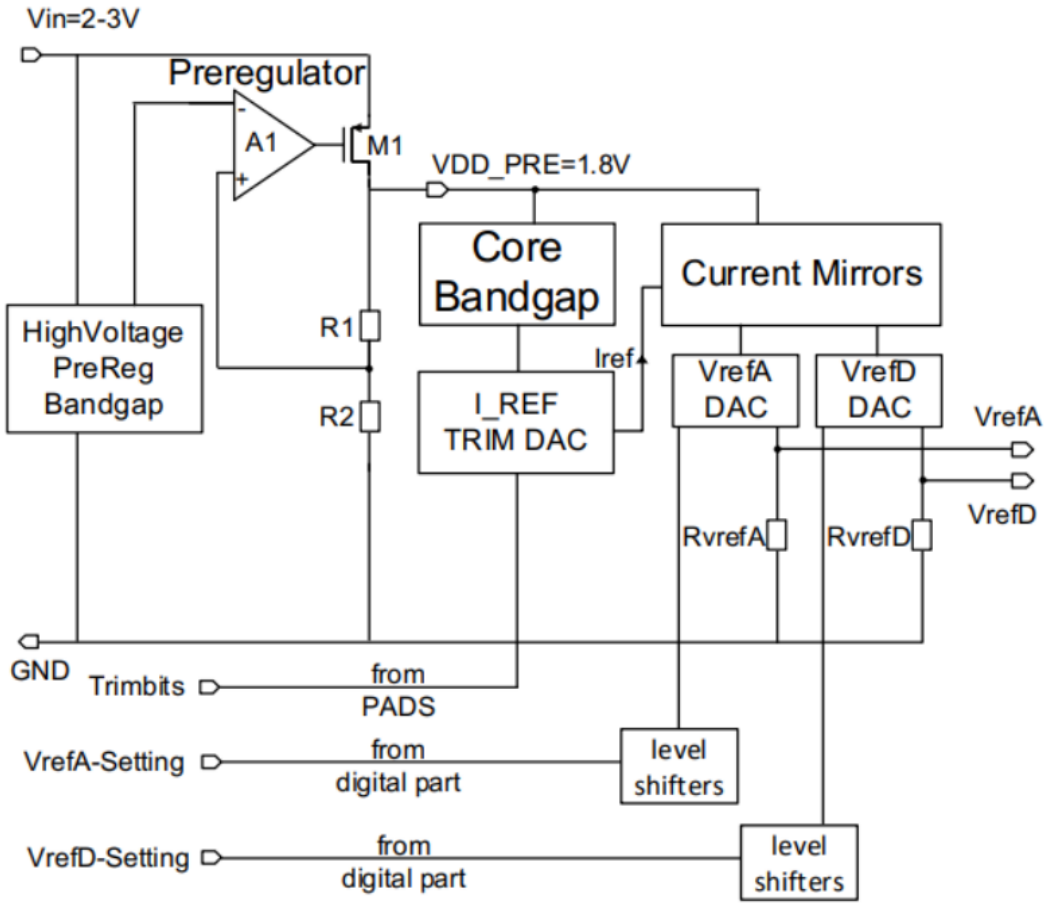
Individual pixel masking

3-bit Threshold Tuning DAC



- A 3 bit threshold tuning is available at the pixel level to reduce the threshold dispersion

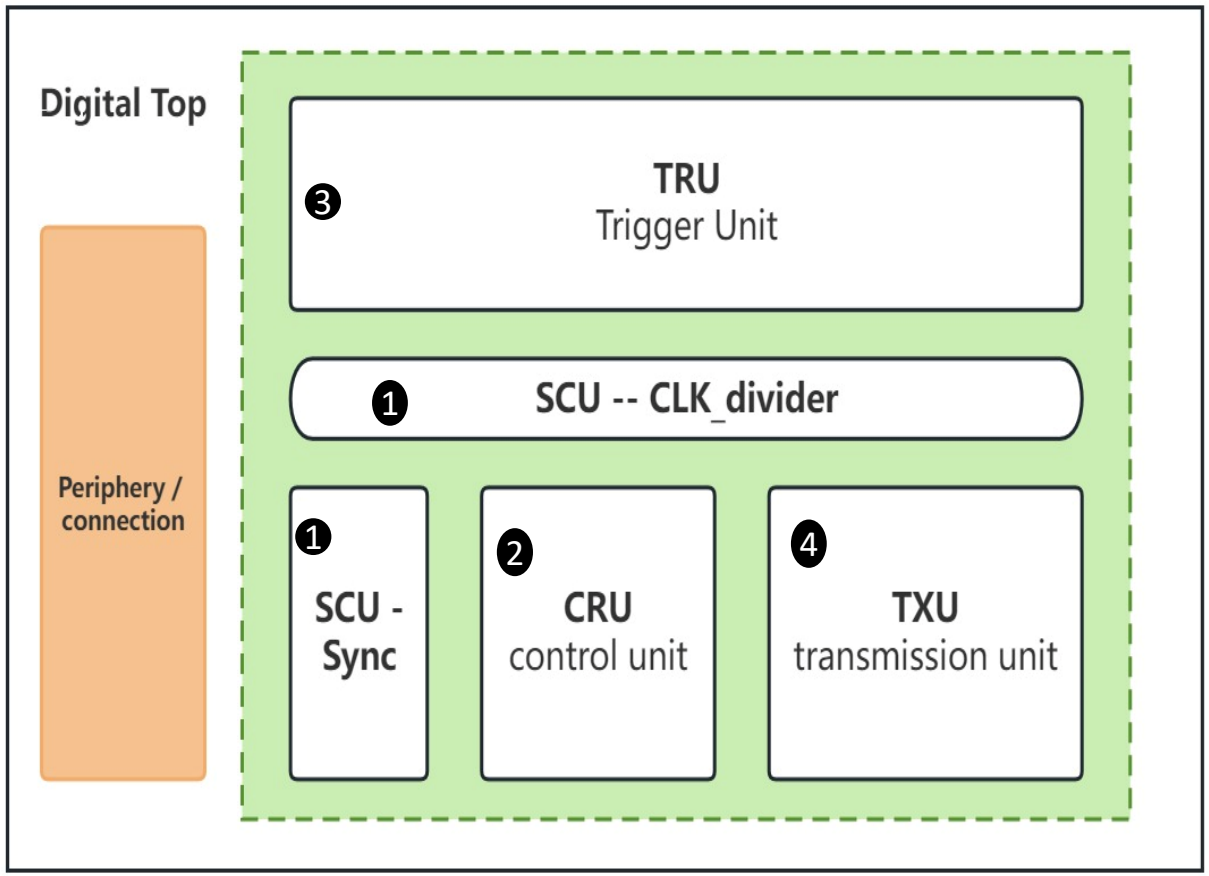
The OBELIX Power management



The LDO regulator architecture

- Power distribution is a major concern as OBELIX is larger than TJ-Monopix2, leading to performance degradation
- Long linear ladders ⇒ voltage drop across ladder
- An on chip regulator is being developed in OBELIX to compensate the voltage drop and minimize the material budget dedicated to power distribution
- Two **LDO (Low Dropout) regulators** will be implemented to supply the matrix from both sides through their pass transistor M1
- The LDO generates the output voltage of 1.8 V ± 10% necessary for the technology to power the chip
- Wide input supply voltage range of 2V to 3 V

The Digital blocs of OBELIX



- Module division : 4 main parts

❶ **SCU – sync & clk divider**: digital clk divider, synchronize circuit & clk divider, RxDat format conversion, main function: clock divider, Rx_data SIPO synchronization

❷ **CRU – Control Unit**: Implementation RD53B interface, which almost keeps the same design as TJ-Monopix2, main functions: command decoder, global configuration

❸ **TRU – Trigger Unit**:Manage pixel data from the matrix-EOC and wait for the trigger to pick them for output

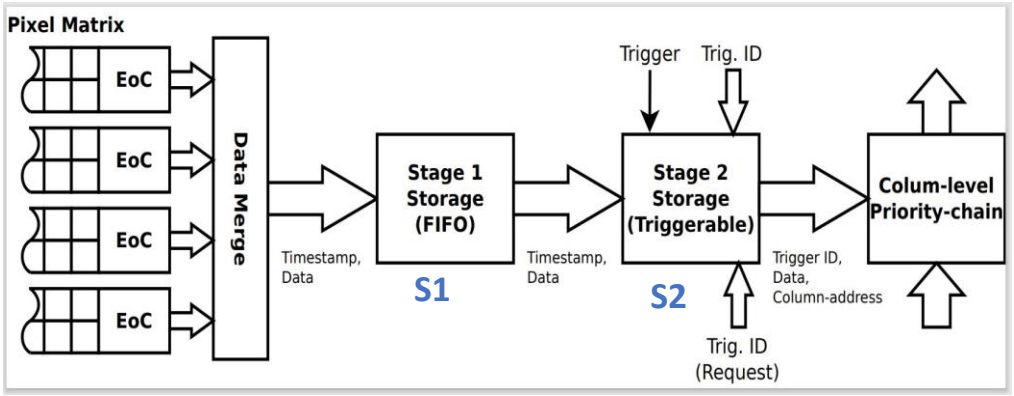
❹ **TXU – TX Unit**: generate output data and sequential output, main functions: data framing, serializer

- Two new modules are related to the Belle II trigger:
  - **TRU :** The Trigger Unit
  - **TTT :** The Track Trigger Transmission

The TRU and the TTT

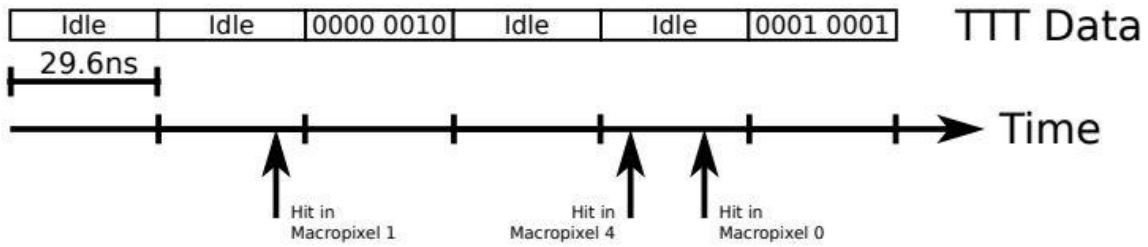
Trigger Unit (TRU):

- New End-of-column adapted to Belle II trigger
- Handle the incoming data from the pixel matrix with two stages of memory (S1 and S2)
  - S1: Buffers the pixel information during the trigger latency
  - S2: Main trigger memory, associates trigger with hitdata
- Timestamped hits stored in memories
- Read-out when timestamps matched with trigger
- Trigger memory organized in 112 Trigger Groups (TRGs), each connected to 4 double columns.



Track Trigger Transmission (TTT):

- Quickly provides the coarse pixel information of all hits to trigger of Belle II
- Allows a Belle II-trigger based on track information
- Divides the matrix into 2 to 8 regions (micropixel)
- Produces a one byte word indicating which of these regions is fired
- 160MHz DDR (Double Data Rate) transmission(320Mb/s, 8b/10b encoded)
- Power constrains this function to the oVTX



Conclusions

- The SuperKEK-B collider is planning a major upgrade to reach a high luminosity
- Reaching the target peak luminosity requires an upgrade of the interaction region and the Vertex Detector
- A new DMAPS VTX is foreseen to improve the performance of the Belle II vertex detector
- The OBELIX sensor based on TJ-Monopix2 chip with TJ180 nm technology is under development with additional features (all on-chip) :
  - Voltage regulators
  - ADC and temperature sensors
  - Trigger logic, up to 10 µs latency at 120 MHz/cm²
  - Precision timing module
  - Fast transmission for trigger contribution
- Development and verification of OBELIX are entering the final stage
- Aiming submission of OBELIX-1 in summer 2024

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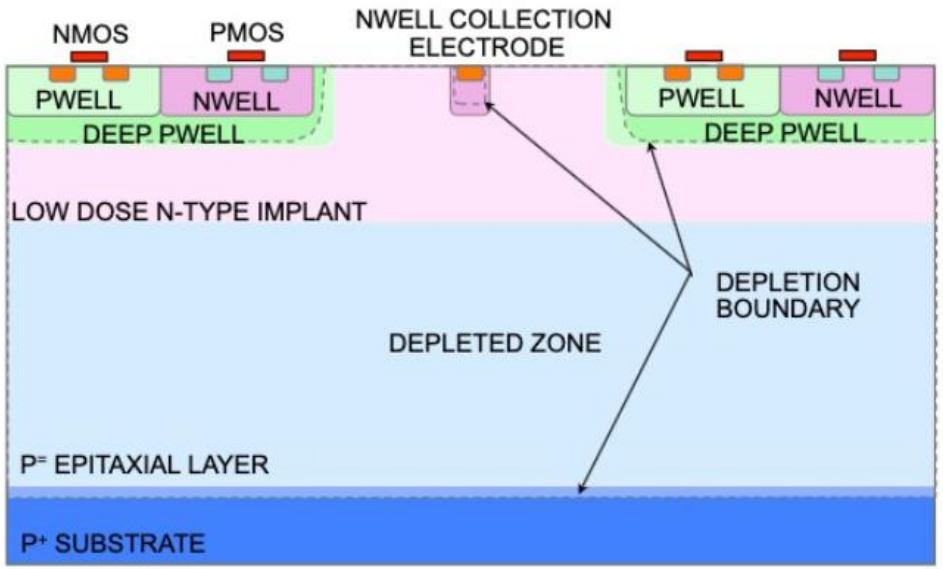
Thanks for your attention

boudagga@cppm.in2p3.fr

Backup slides

Technology: DMAPS

- Monolithic sensor : Combine sensor and readout on the same wafer
- Electronics outside the collection nwell
- Low material budget



- Using an isolated deep well that collects charge and includes both analogue and digital circuits
- Large signal and fast charge collection
- Sensors can be thinned to 50 µm without signal loss
- Sensors can operate in a high rate environment (< 25 ns)
- Good radiation tolerance
- Very small sensor capacitance
- Low noise and power