Timing with Monolithic CMOS
Potential applications to CEPC

CEA/Irfu/DphP and CEA/Irfu/Dedip

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Timing sensor basic ingredients

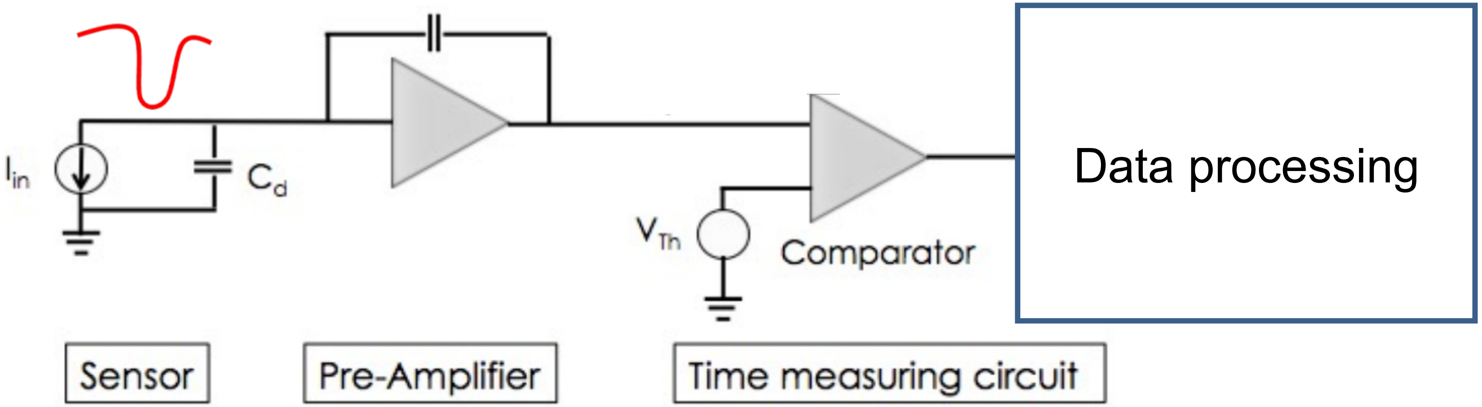


Illustration taken
From N. Cartiglia
(VCI 2022)

- Monolithic sensors : Analog Front-End, Time measuring electronics (typically LE discriminator)
- Data processing (TDC, serializers, PLL, sparsification) can ideally also be on same chip,

but actual development not easy (risk of analog/digital couplings)

Timing oriented sensor families

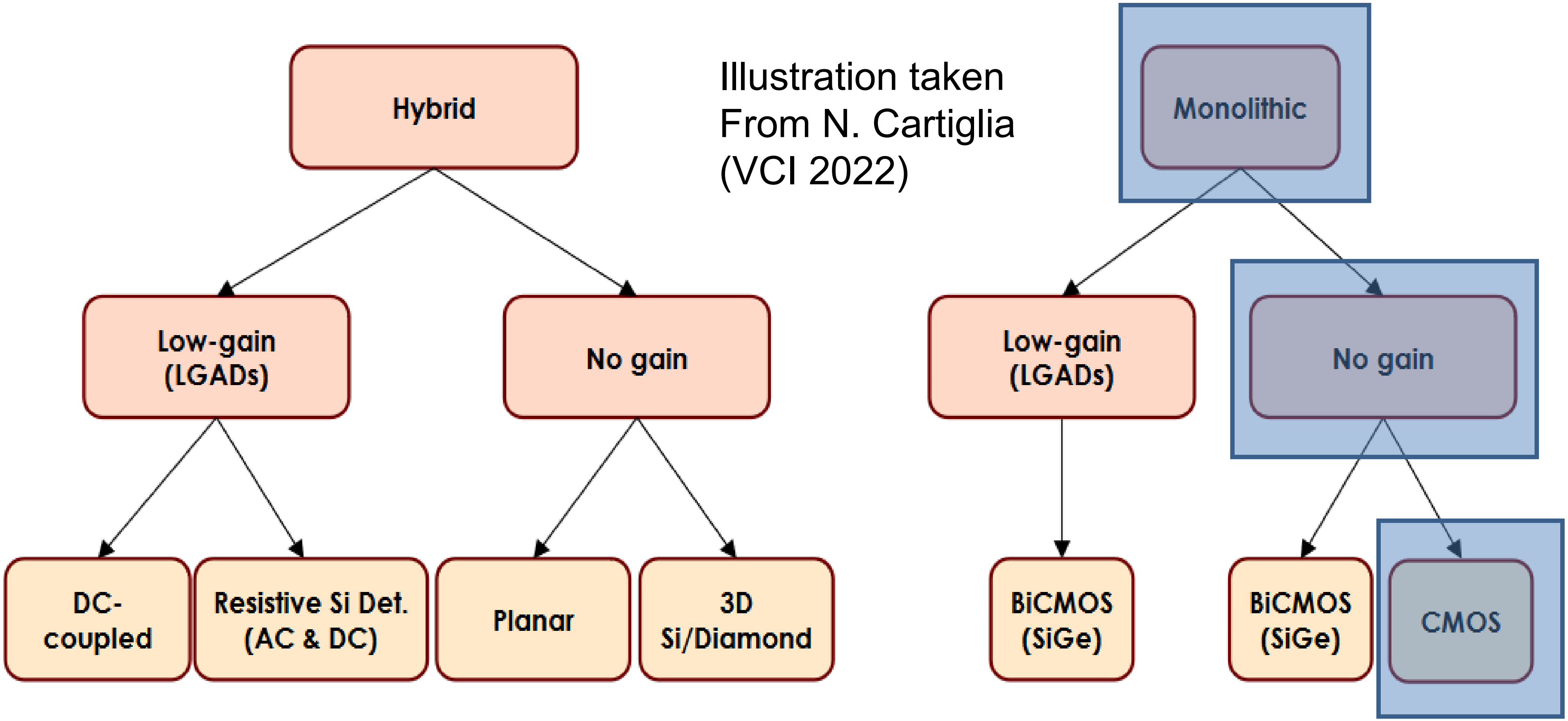
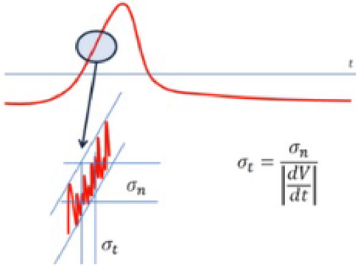


Illustration taken
From N. Cartiglia
(VCI 2022)

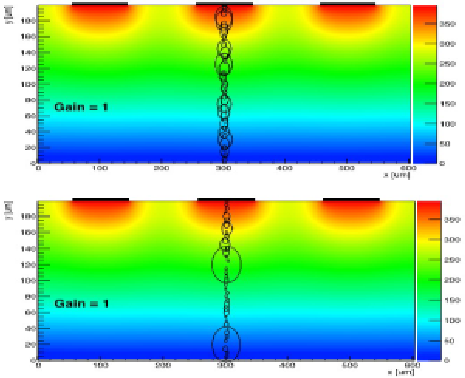
Time resolution

$$\sigma_t^2 = \left(\frac{Noise}{dV/dt}\right)^2 + (\Delta ionization)^2 + (\Delta shape)^2$$



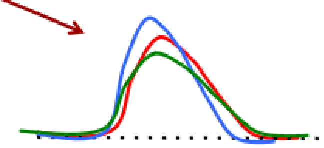
“Jitter” term

Small noise → choice of technology, small detector capacitance
High dv/dt →
High electric field (but Vd saturates around 1 V/µm)
Intrinsic amplification (LGADs)



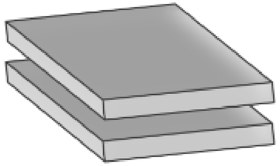
Amplitude variation → Timewalk, corrected offline

Non-homogeneous energy deposition → cannot be corrected, minimized by design



Signal shape is determined by Ramo’s Theorem

$i \propto qvE_w$



Saturated drift velocity in sensor volume → Uniform weighting field

Parallel plate geometry, easier for big pixels

Illustration taken From N. Cartiglia (VCI 2022)

Features of monolithic CMOS sensors

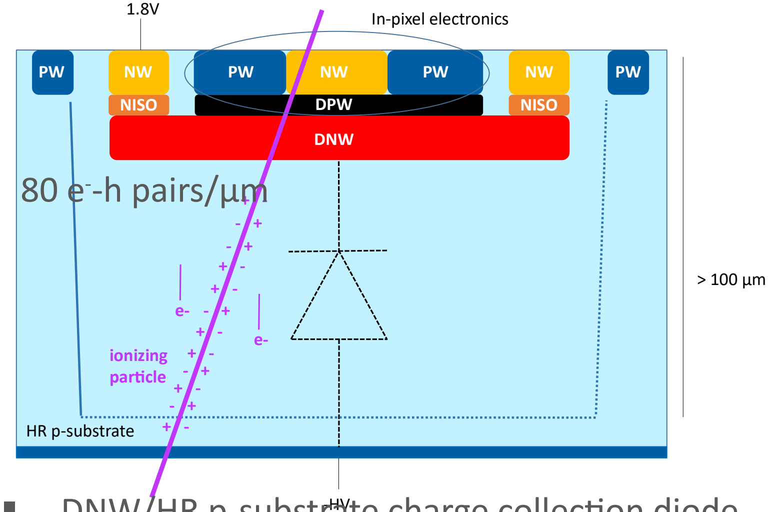
- (Relatively) cheap high volume industrial technology
  - 2-3 k euro/8’’ wafer, post-processing and dicing included → bare sensor cost for 100 m2 : 7-11 M euros
  - Bump bonding operation not needed for fully monolithic architecture
- Stable and easy operation
- HV-HR wafers available, allows charge collection by drift and not only by diffusion → favorable for fast collection and also for radiation hardness
- Can be designed as a complete SoC, from sensor to DAQ interface
- Presently available technologies are known to be rad-hard up to a few 10^{15} 1 MeV neq/cm2
- Can be thinned down to < 100 µ

TIMING WITH HV-CMOS/DMAPS*

*Depleted **MAPS**

- The objective of our R&D is the development of a **monolithic timing sensor** in a **commercial HV-CMOS process** for future high energy physics experiments or for LHC upgrades (timing detectors, after phase 2 upgrades)
- **LFoundry 150 nm** HV-CMOS is one of the CMOS processes studied extensively for the CMOS option of the ATLAS Inner Tracker Upgrade
- Several large size demonstrators already designed and tested for tracking applications (**LF-CPIX**, **LF-MONOPIX1**, **LF-MONOPIX2**) in this process with proven **radiation hardness** (Bonn, IRFU and CPPM coll.)

HV-CMOS Sensor Pixel

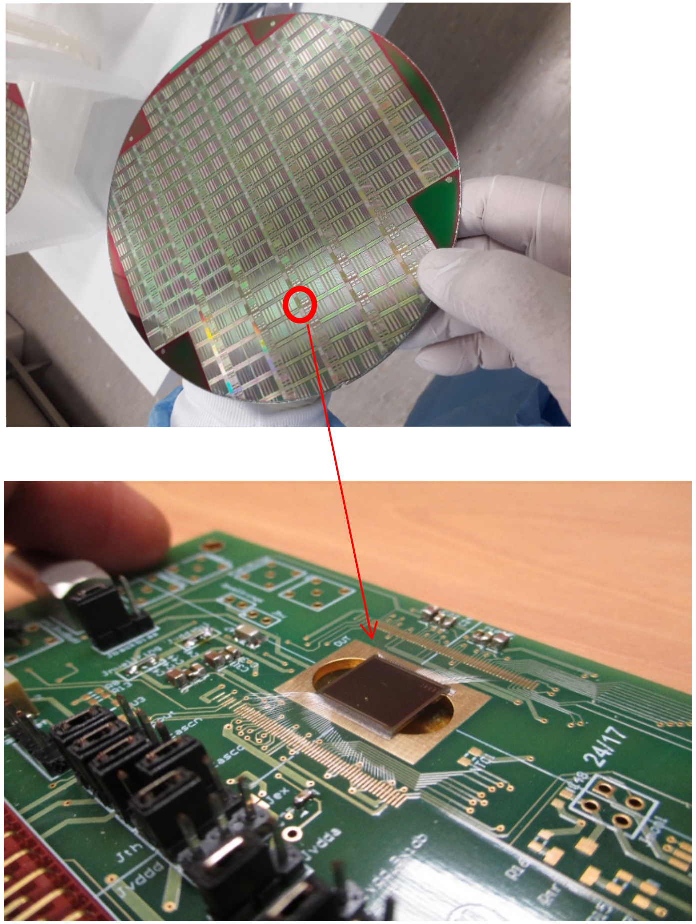


- DNW/HR p-substrate charge collection diode
- HV (≥ 300 V) applied on the substrate (from top or back)
- Large depletion depth (≥ 300 µm)
- **Charge collection by <u>drift</u> (fast)**
- **No internal amplification**
- Electronics can be integrated inside charge collection diode

CACTUS* DEVELOPMENT

*CMOS **AC**tive **T**iming **µS**ensor

- The first demonstrator called **CACTUS** for timing in LF 150 nm process designed in 2019
- The front-end in CACTUS is based on an **in-pixel fast preamplifier** followed by a **leading edge discriminator**
- Time walk corrections done off-line by **ToT measurement**
- Expected timing resolution from Cadence & TCAD simulations: 50-100 ps



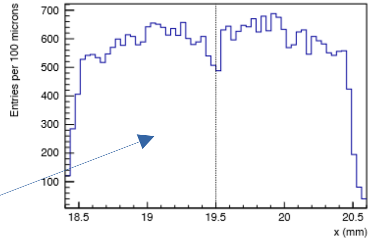
The CACTUS demonstrator on PCB (chip size : 1 cm x 1 cm)

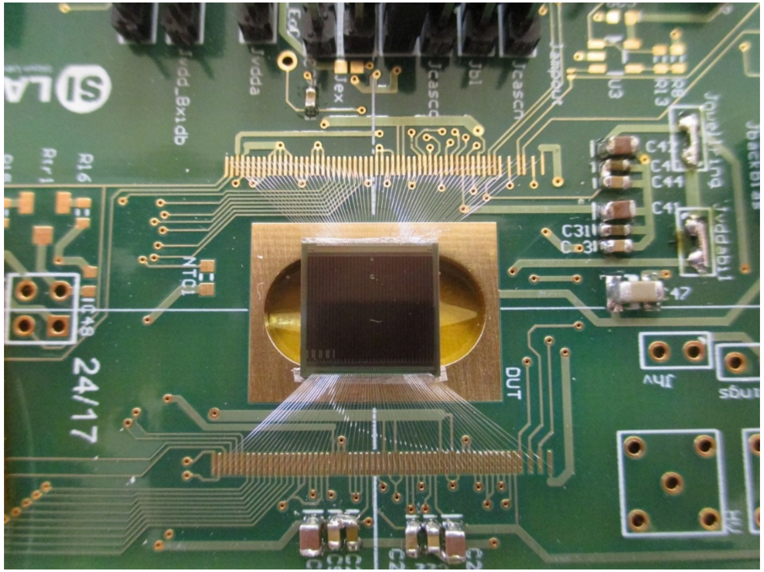
Cactus (Irfu) : Timeline and results

We started around 2017 after being involved into LF-CPIX and MONOPIX strip detector for ATLAS-ITK outer layers (possible backup solution).
CACTUS was designed in parallel, reusing blocks and concepts from LF-CPIX and MONOPIX, adding optimizations towards timing performance

At that time, 2 possible applications for sub-100ps timing detectors:

- ATLAS High η muon tagger (upstream forward calorimeter)
- HGTD in front of ATLAS-LAr



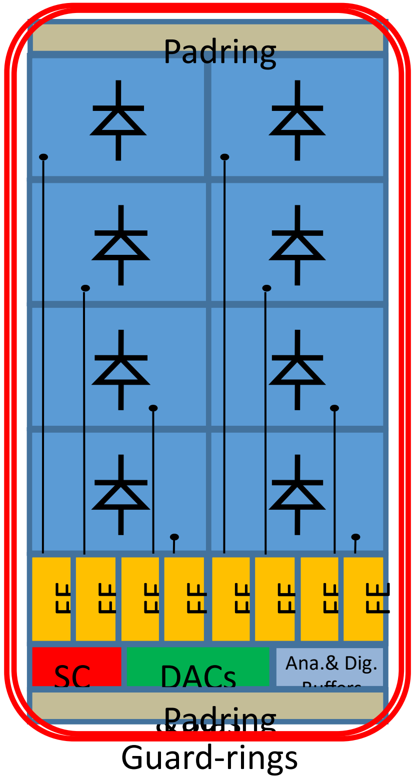


First try with CACTUS:
- Yield correct, High break down voltage, homogenous charge collection, deep depletion depth
- Main problem with CACTUS: underestimation of parasitic capacitance → bad S/N
-Also coupling between analogic and digital part → ringing of digital pulse
→ modest timing performance ~500ps

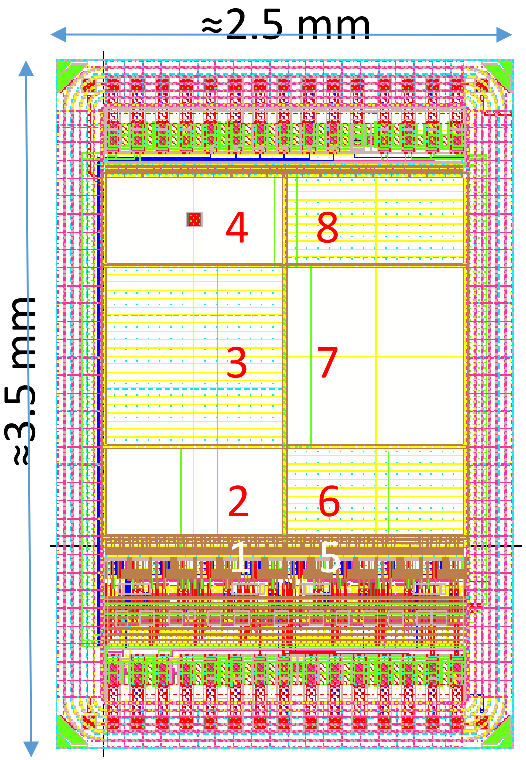
https://arxiv.org/abs/2003.04102

→ Version 2 of CACTUS called Mini-Cactus

MiniCACTUS Sensor Chip



Block diagram of the MiniCACTUS chip (not to scale)



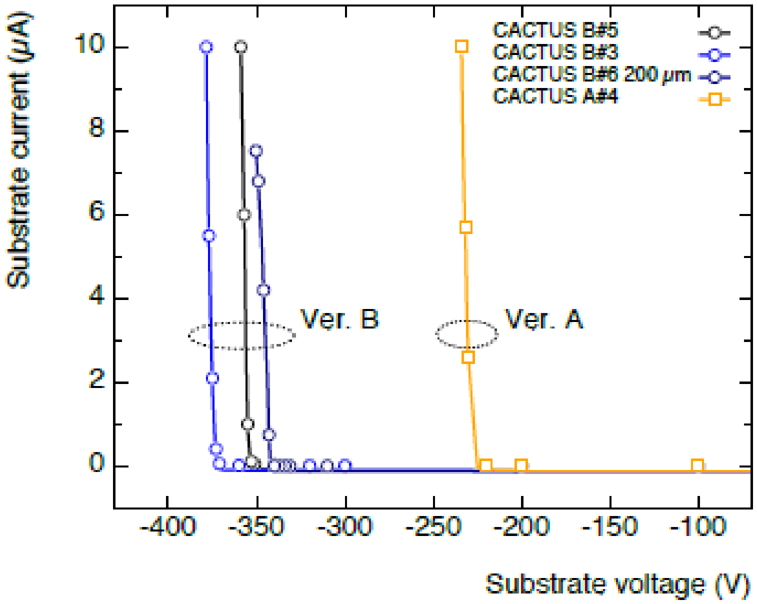
Layout of MiniCACTUS

Pixel Flavors :
Pixels 3 & 7 : 1 mm x 1 mm baseline pixels
Pixels 2, 4, 6 & 8 : 0.5 mm x 1 mm pixels
Pixel 8 : 0.5 mm x 1 mm pixel with in-pixel AC coupling capacitor (20pF)
Pixels 1 : 50 µm x 50 µm test pixel
Pixels 5 : 50 µm x 150 µm test pixel

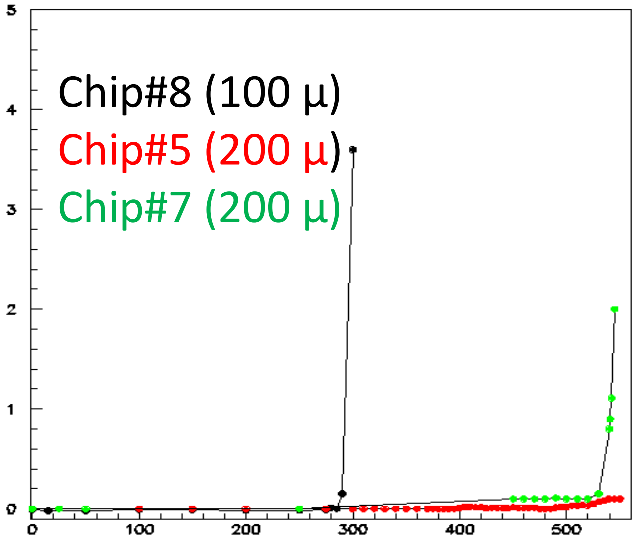
- **MiniCACTUS** is a smaller detector prototype designed in order to address the *low S/N issue* observed on previous CACTUS large size demonstrator
- Main change in MiniCACTUS: FE integrated at column level, pixels mostly passive
- On-chip **Slow Control**, **DACs**, **bias circuitry**
- 2 discrimated digital (LVDS) and 2 analog monitoring (*slower than CSA output*) outputs for 2 columns
- 2 small pixels implemented as test structures to study charge collection (*FEs not power optimized*)
- Some detectors thinned to 100, 200, 300µm and than post-processed for backside polarization after fabrication

BREAKDOWN VOLTAGE MEASUREMENTS

CACTUS



MiniCACTUS



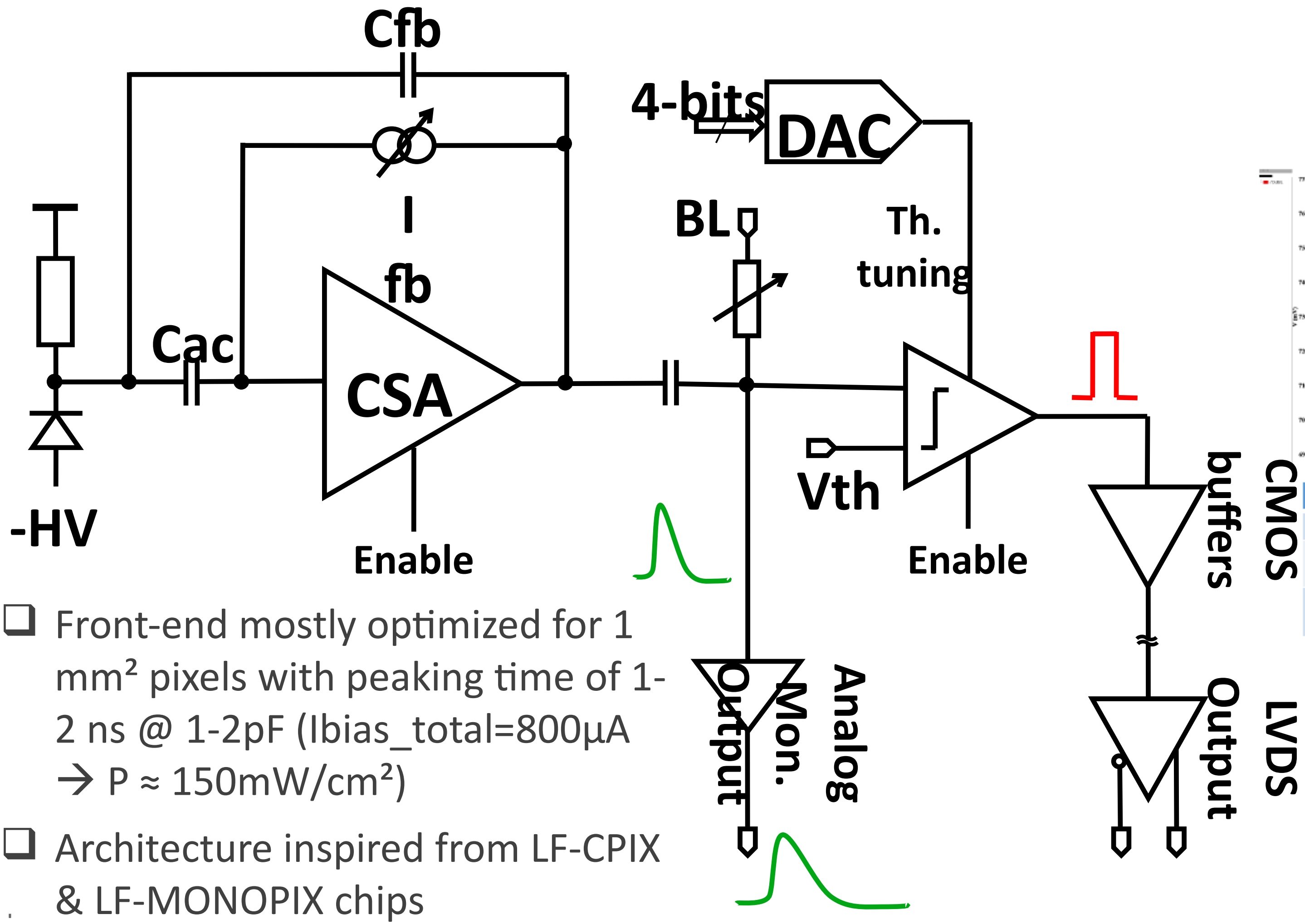
- Same LF15A process used for both chips
- Same guard rings used for both chips (MiniCACTUS uses Ver. B CACTUS rings)
- Same postprocessing for both chips (as far as we know)

- Found similar BV for thinned and unthinned chips
- Version B BV is around 350 V.

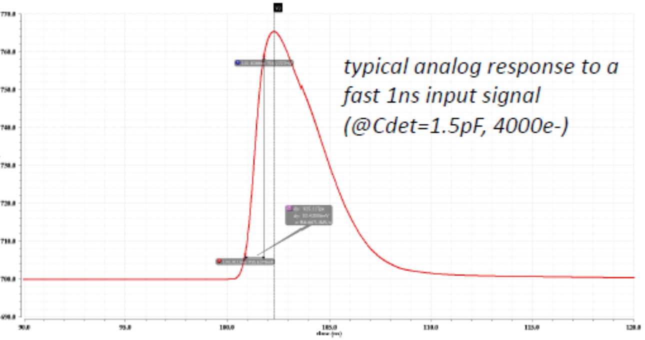
The tested two 200 μ chips break down above 500 V !

Not clear why there is such a difference between 200 μ chips and other thicknesses : post-processing details ? Specific wafer ?

ON-CHIP FRONT-END



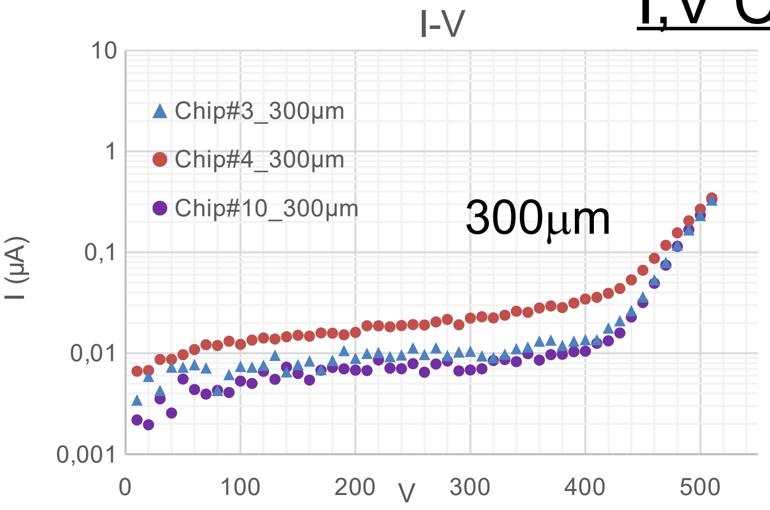
Typical CSA transient simulation result

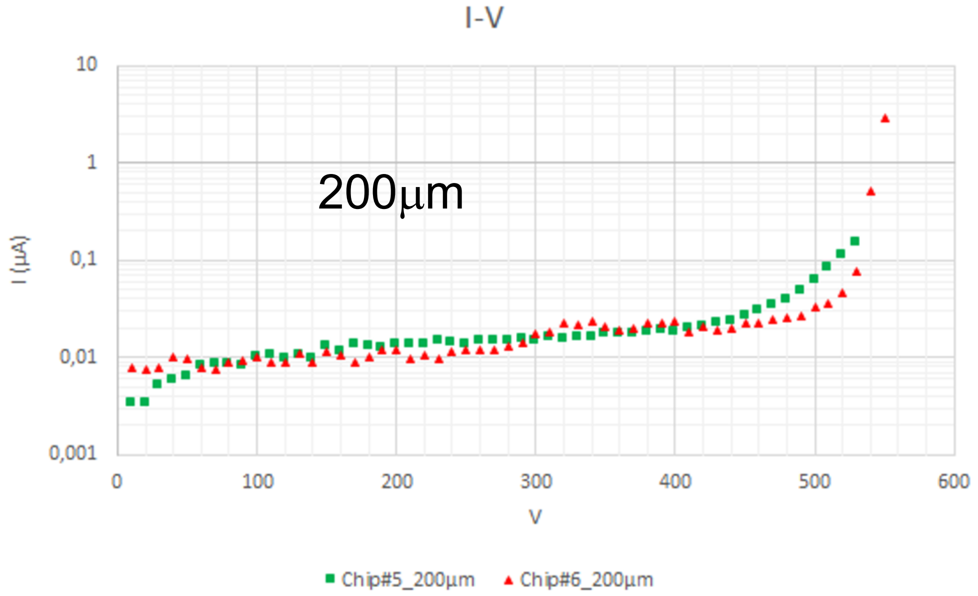

typical analog response to a fast 1ns input signal (@Cdet=1.5pF, 4000e-)

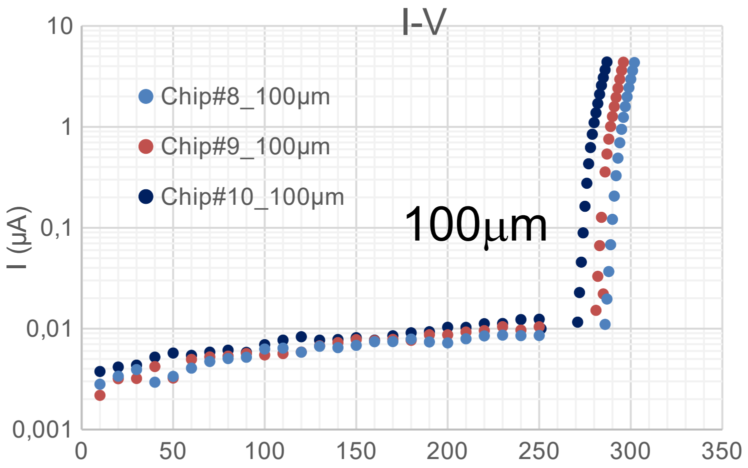
Parameter	1.5 pF	1 pF
Rise Time (from 10% to 90%)	~ 0.9 ns	~ 0.8 ns
Input Referred Noise [estimated from AC simulations]	~ 290 e-	~ 220 e-
Jitter [estimated from $t_r/(S/N)$]	~ 67 ps	~ 44 ps

- ❑ Front-end mostly optimized for 1 mm² pixels with peaking time of 1-2 ns @ 1-2pF (Ibias_total=800µA → P ≈ 150mW/cm²)
- ❑ Architecture inspired from LF-CPIX & LF-MONOPIX chips

I,V Curves of MiniCactus

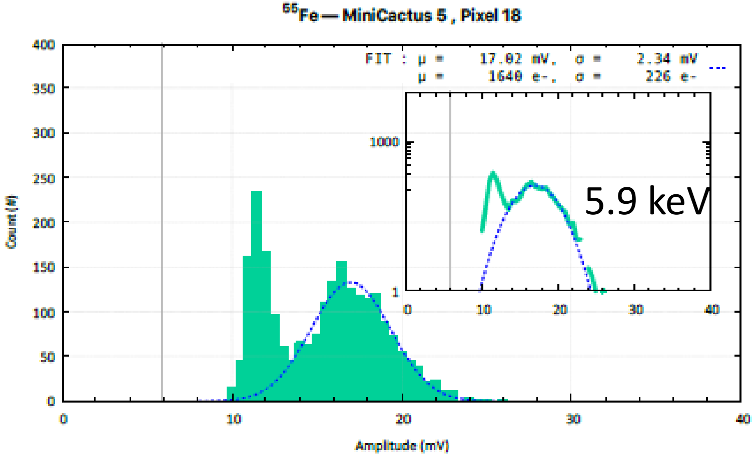


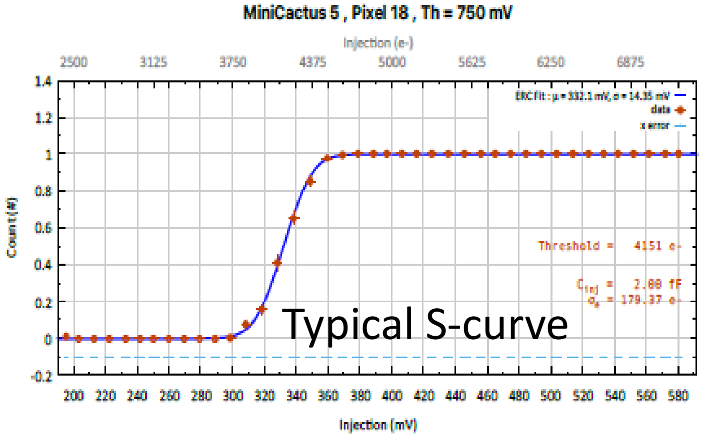


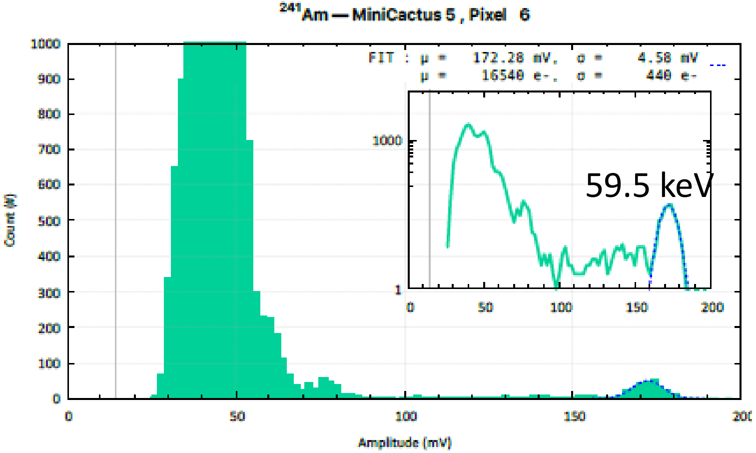


Breakdown voltage from 300 V to 500 V
Variations likely due to posprocessing

IN-LAB TESTS (injection pulse, Gamma-ray sources)

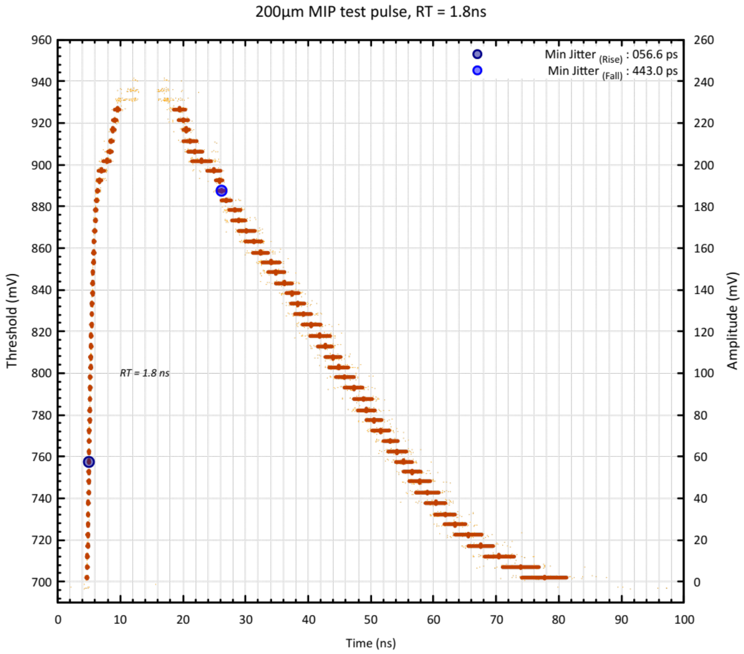


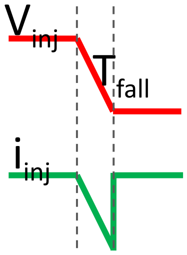


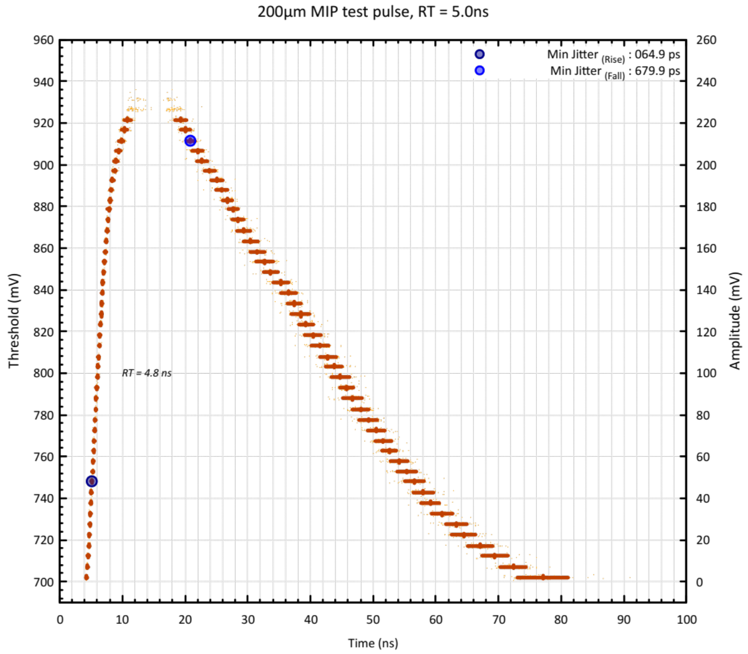


- → Best S/N observed on pixel 8 (0.5mm²) among large pixels
- → Noise$_t$:
  179.4e- (chip#5_200µm)
  155.9e- (chip#8_100µm)

INTERNAL ANALOG PULSESHAPE RECONSTRUCTION FROM DIGITAL OUTPUT







- Charge Injection → Vpeak AmpOut ~ 150 mV

(MPV of MIPs for a 200 µm thick sensor)

- Input injection pulse Rise/Fall Time = 1.8 ns
- FE Internal Pulse Rise Time ≈ 1.7 ns

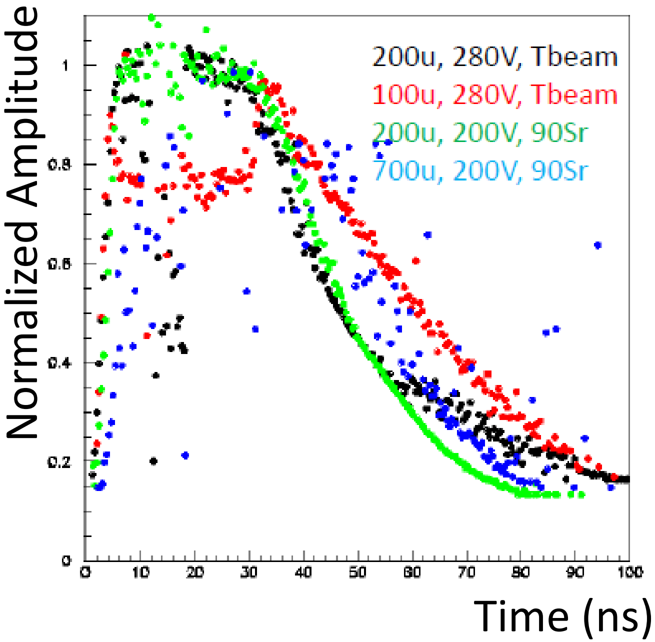
- Charge Injection → Vpeak AmpOut ~ 150 mV
- Input Rise/Fall Time = 5.0 ns
- Pulse Rise Time ≈ 4.8 ns
- Jitter : 64.9 ps

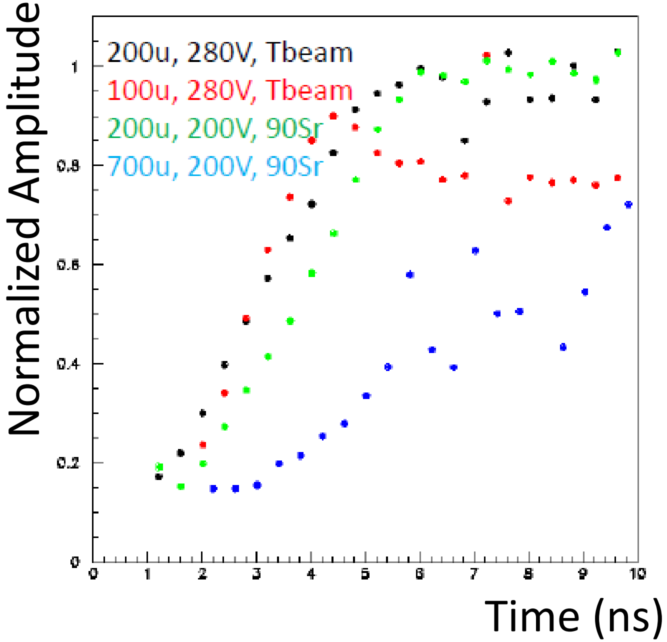
s *(not realistic case)*

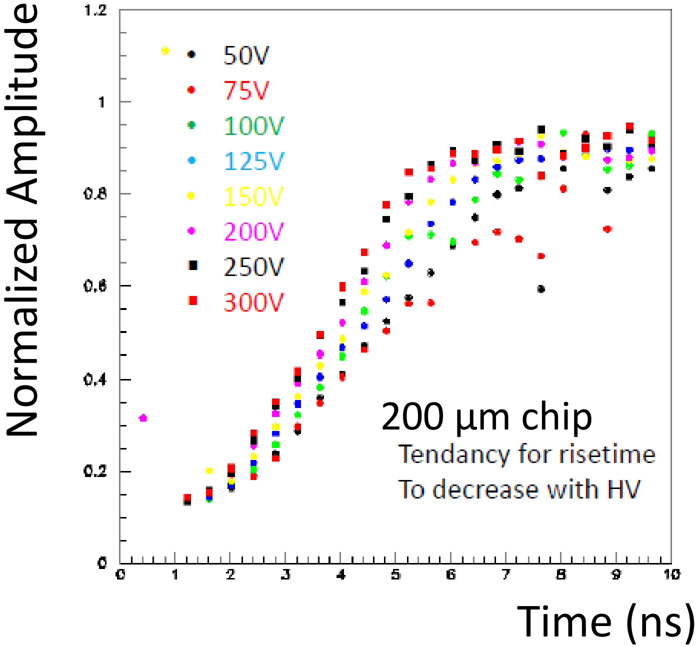
→ The FE follows well a 1.8 ns falling edge digital injection pulse

INTERNAL ANALOG PULSESHAPE RECONSTRUCTION ATTEMPT

Testbeam data

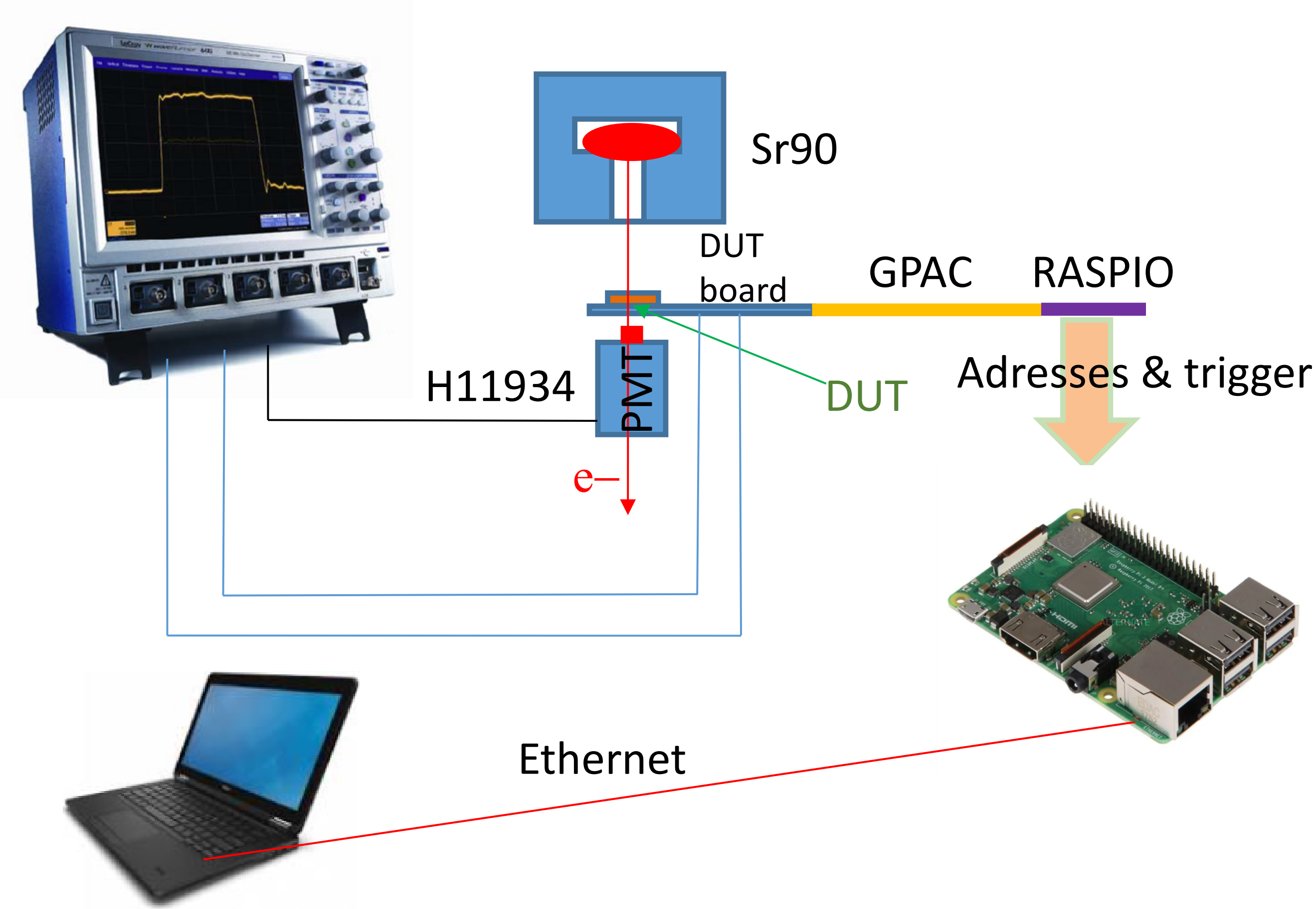






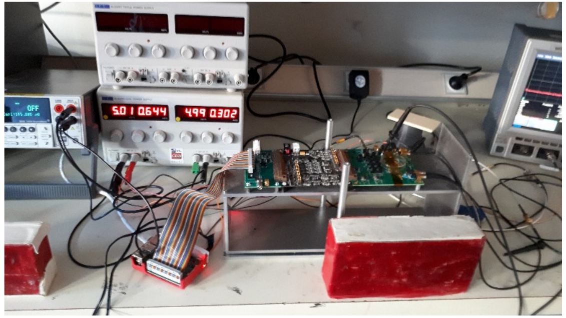
- Internal pulseshape reconstruction not very precise, but enough to get an idea of the shape and the rise time
- Rise time is of the order of **4-5 ns** for 200 µm and 100 µm → need to reoptimize front-end for future iterations
- The unthinned 700 µm chip are clearly slower → post-processing is definitely needed !
- Rise time decreases somewhat with HV (related to drift velocity increase)
- With these results, for a given thickness and bias voltage, **the noise of the FE seems to be the limiting factor of the current timing resolution**

IN-LAB ^{90}Sr TEST SET-UP

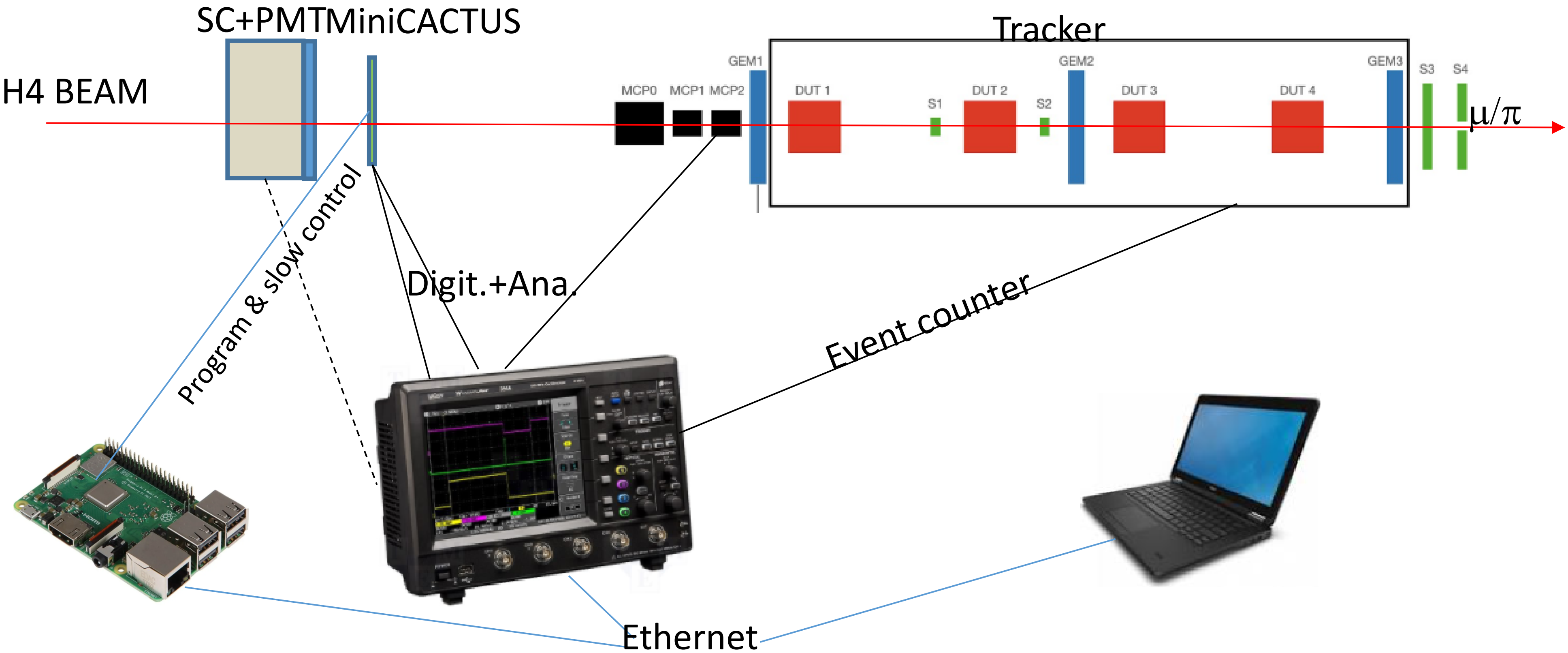


Used for :

- First test and debug
- Calibration
- parameter optimisation studies looking for relative performance improvements

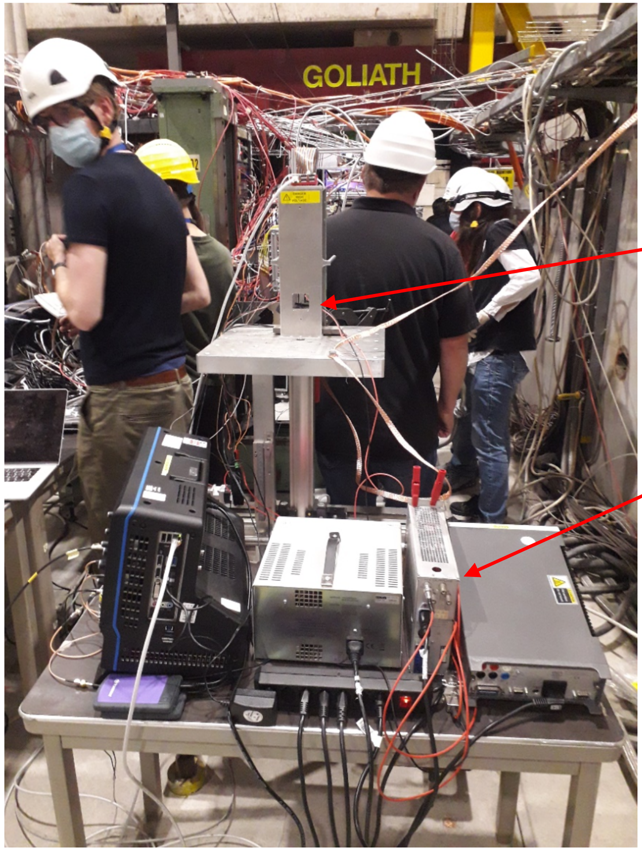


TESTBENCH OF MINICACTUS IN TESTBEAM



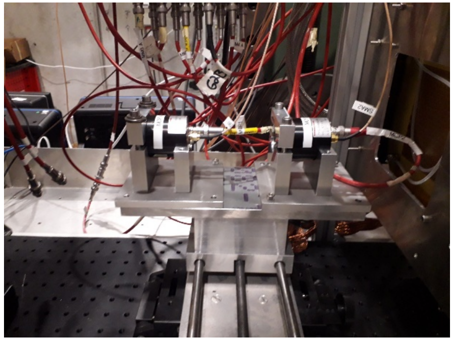
Setup installed on H4 line at SPS-CERN during **RD-51** test-beam periods in **parasitic** mode
(October 2021, April 2022, September 2022)

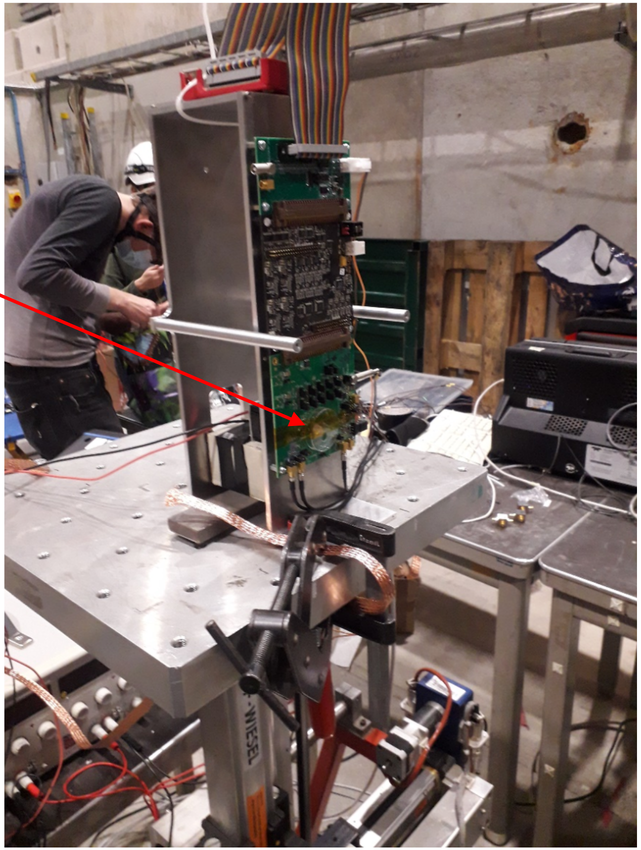
TESTBENCH OF MINICACTUS IN TESTBEAM



MiniCACTUS

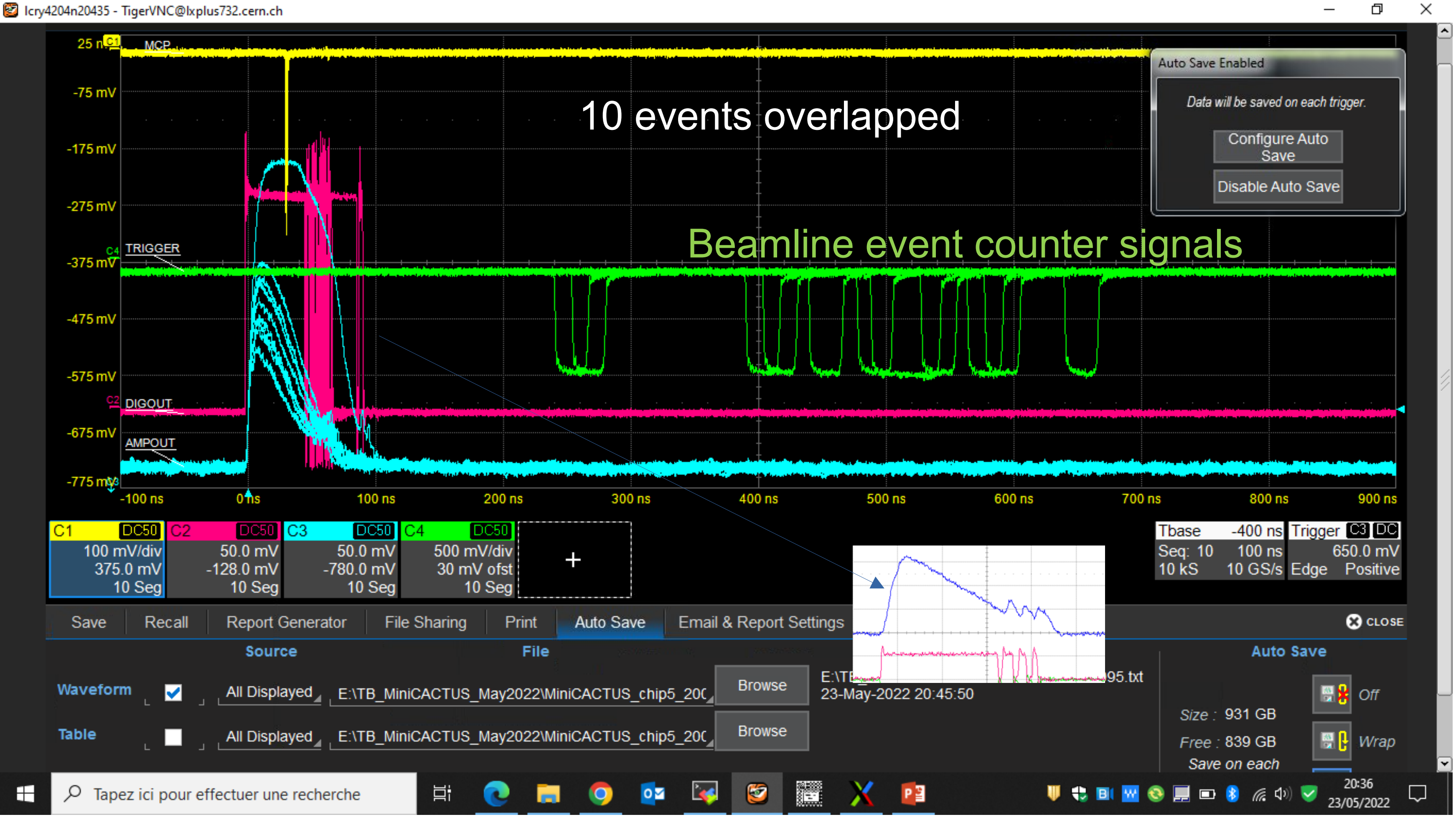
Power Supplies
(LV and HV)





Time reference
RD-51 MCPs (resolution < 10 ps)

TYPICAL WAVEFORMS OBSERVED DURING TESTBEAM



10 events overlapped

Beamline event counter signals

Auto Save Enabled

Data will be saved on each trigger.

C1 DC50	C2 DC50	C3 DC50	C4 DC50
100 mV/div	50.0 mV	50.0 mV	500 mV/div
375.0 mV	-128.0 mV	-780.0 mV	30 mV ofst
10 Seg	10 Seg	10 Seg	10 Seg

Tbase	-400 ns	Trigger	C3 DC
Seq: 10	100 ns		650.0 mV
10 kS	10 GS/s	Edge	Positive

	Source	File
Waveform ☑	All Displayed	E:\TB_MiniCACTUS_May2022\MiniCACTUS_chip5_20(
Table ☐	All Displayed	E:\TB_MiniCACTUS_May2022\MiniCACTUS_chip5_20(

E:\TE…95.txt
23-May-2022 20:45:50

Auto Save
Size : 931 GB
Free : 839 GB
Save on each

20:36
23/05/2022

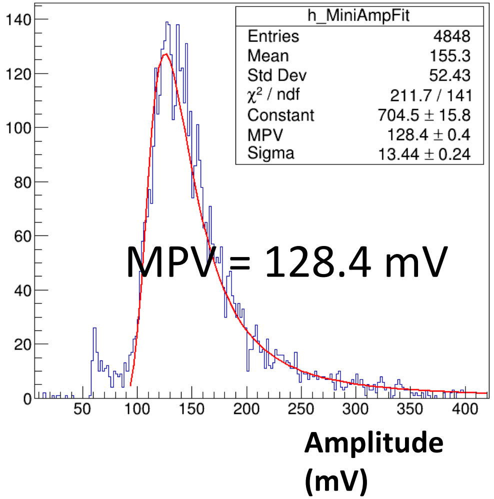
→ Ringing on Digital Output due to coupling from the digital buffers

(known problem from in-lab tests, negative impact on TW corrections from digital ToT)

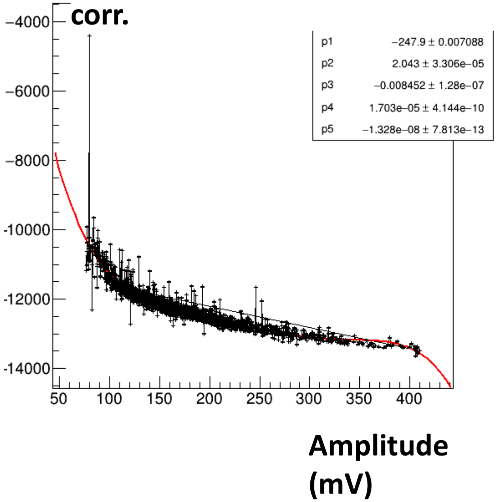
DATA ANALYSIS PROCEDURE

Chip#5, pixel 8**, 0.5 x 1 mm²**, **200 µm**, **-280V** (Back-side pol.)

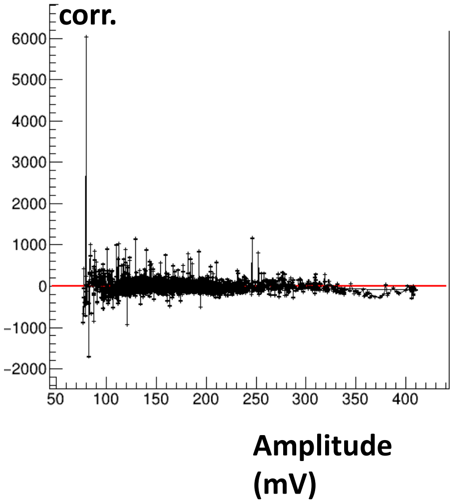
MiniCACTUS Analog Monitoring Output



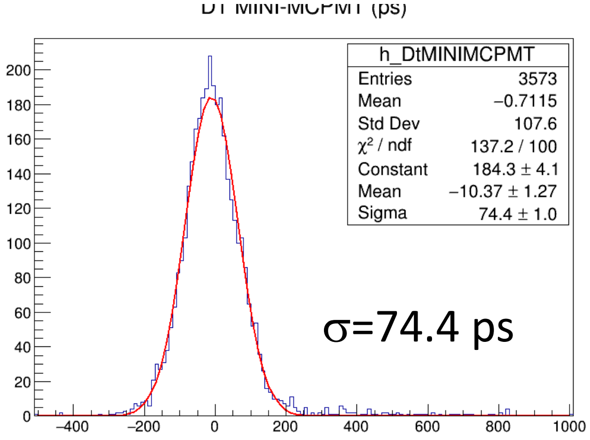
Fit T_MCP – T_DigOut (ns), no corr.



Fit T_MCP – T_DigOut (ns), TW corr.



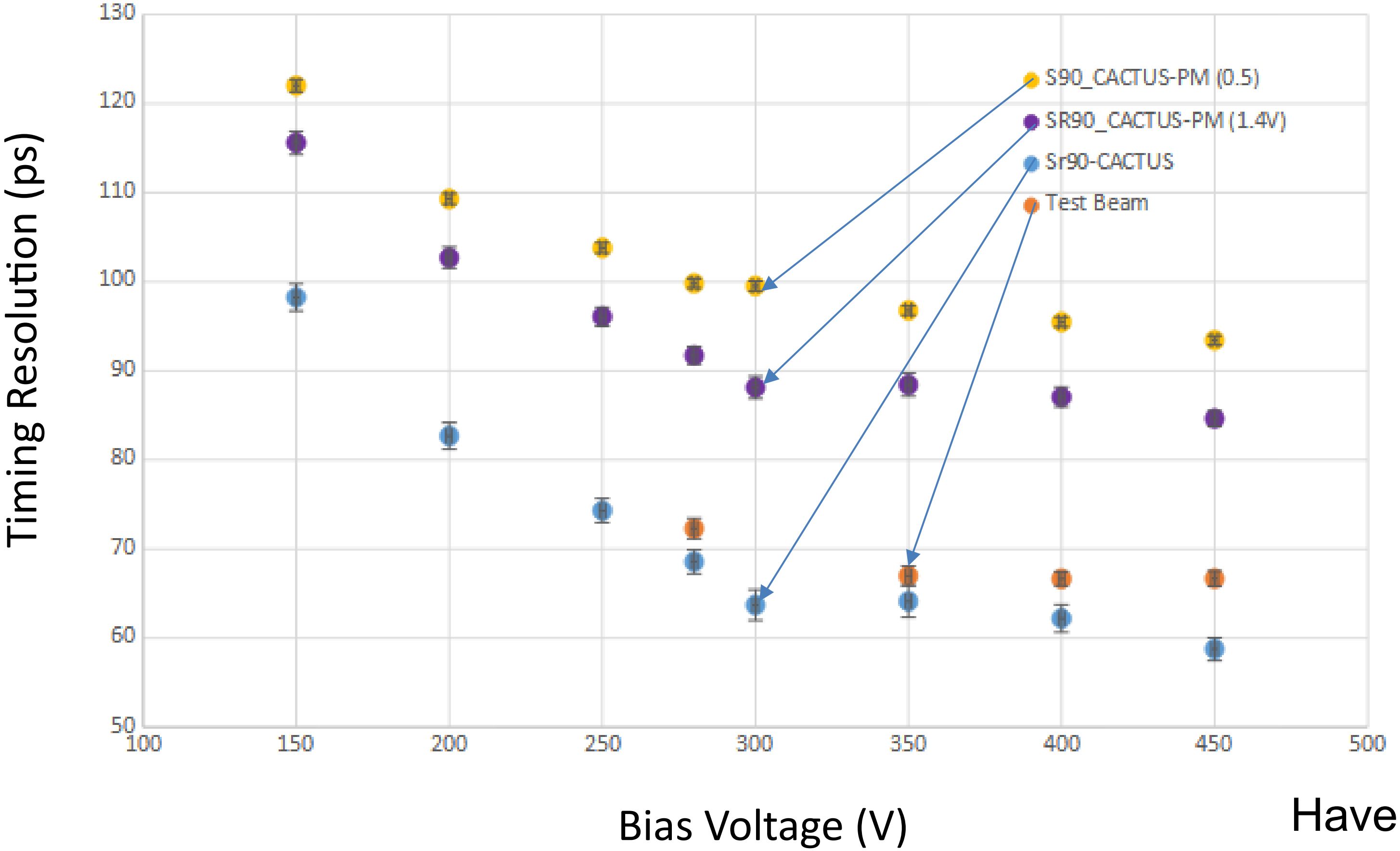
T_MCP – T_DigOut (ps) after TW correction



- Measured timing resolution (-280 V) : **74.4 ps** (MCP resolution negligible)
- Worse timing resolution measured with 100 µm sensor (*lower S/N* and *ringing from digital*)
- Small pixels have worse performance, probably due to charge sharing effects (*pixel 5 tested in testbeam*)

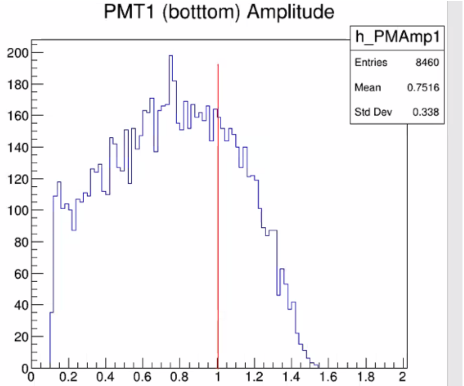
IN-LAB TIMING MEASUREMENTS WITH PMT AND ^{90}Sr SOURCE

Chip#6, pixel 8**, 0.5 x 1 mm^2, 200 µm**



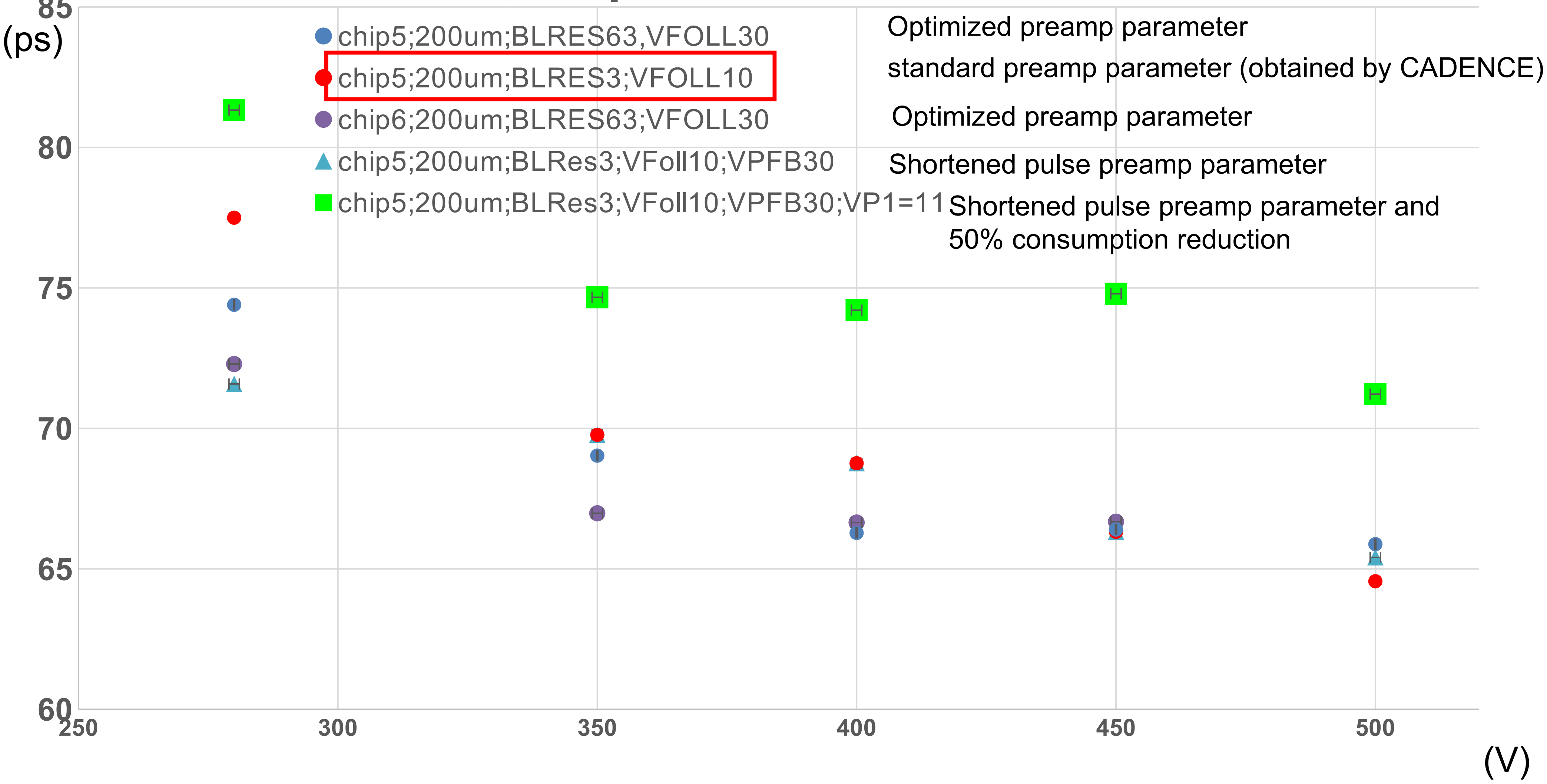
→ In-lab measurements with 90Sr betas

allowed to predict actual performance with MIPs



Have to select MIP-like betas by cutting out low energy deposits in PMT

Pixel 8;200 µm; Resolution versus HV (Test-beam data)



Optimized preamp parameter

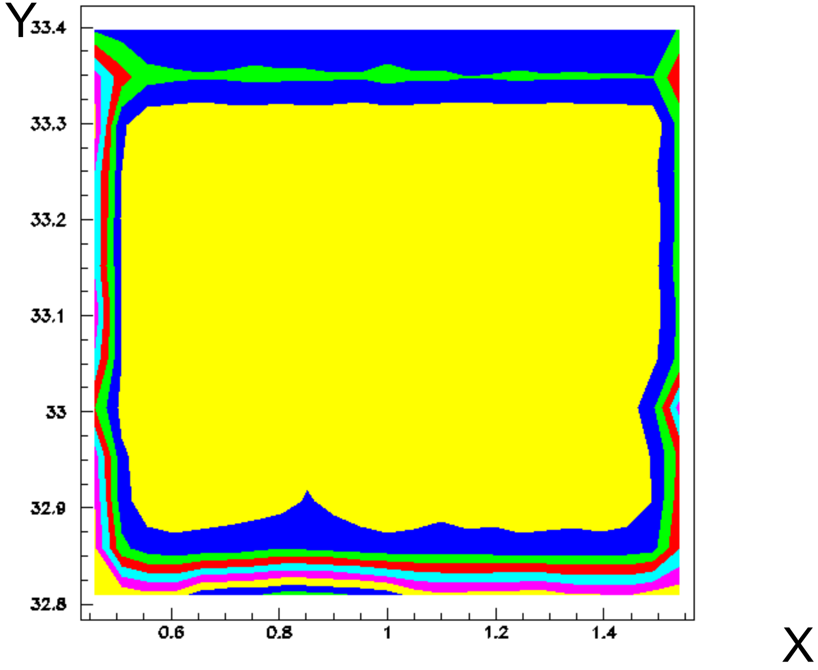
standard preamp parameter (obtained by CADENCE)

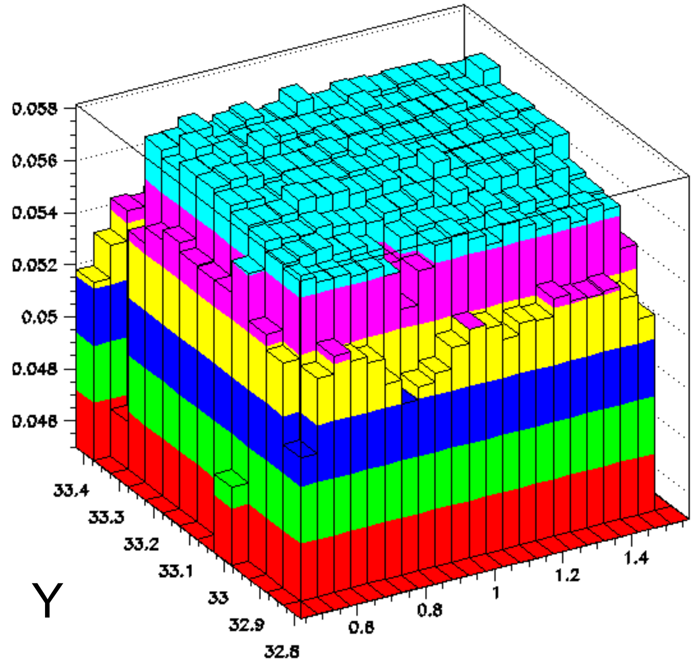
Optimized preamp parameter

Shortened pulse preamp parameter

Shortened pulse preamp parameter and
50% consumption reduction

Pixel position scan at 20 keV with photons (data taken at Synchrotron Soleil)





Pixel has very good uniformity

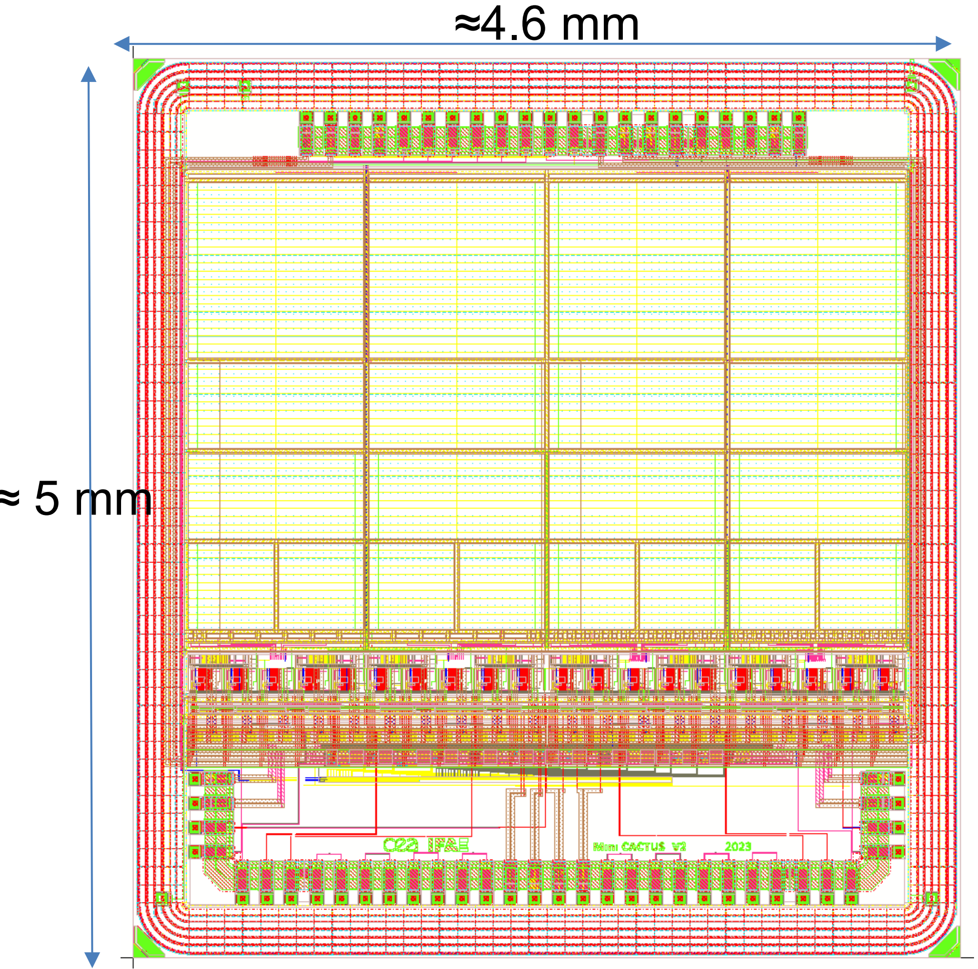
Used a pencil beam (50 microns by 50 microns) to scan pixel surface

No non-uniformity found

Thanks to F. Orsini and A. Dawiec for the Beam line time and help with data taking !

MiniCACTUS_V2 Sensor Chip

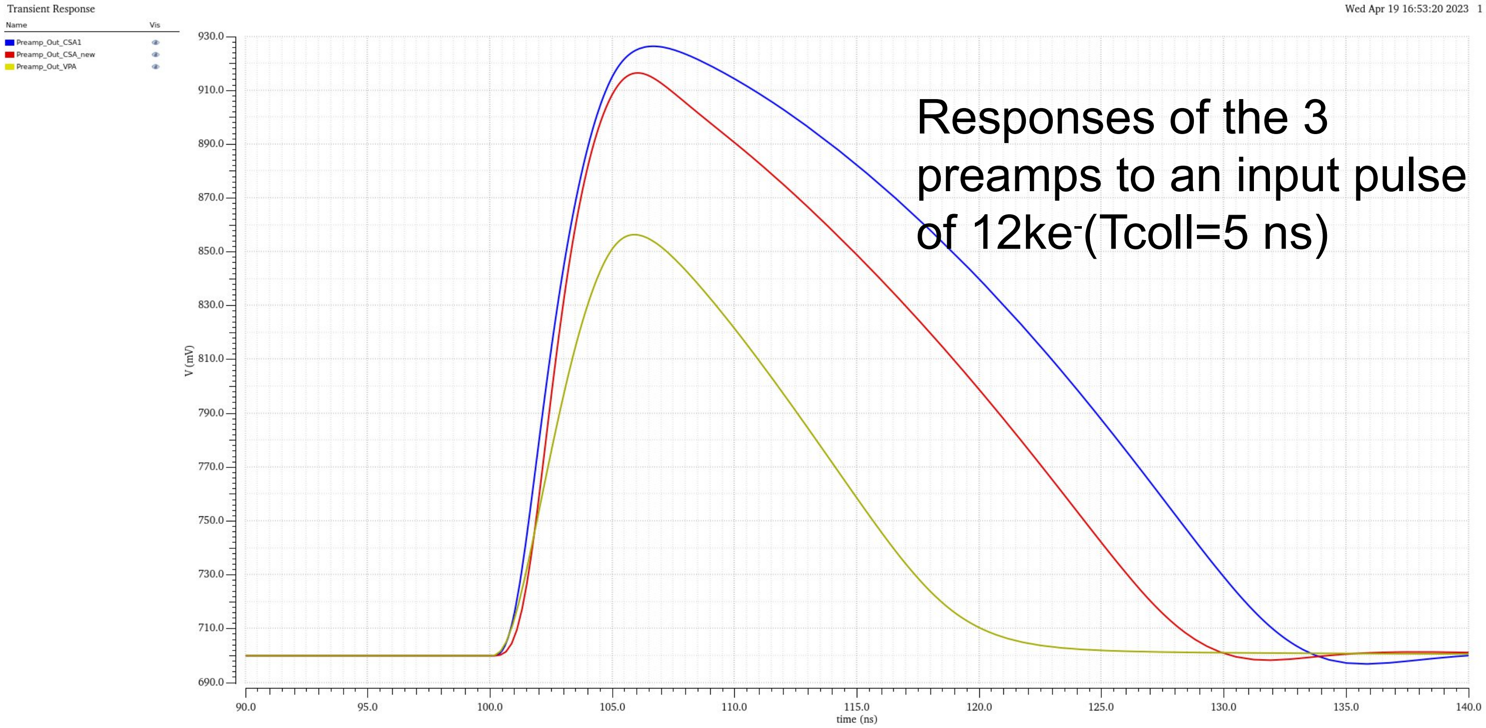
Irfu : Yavuz Degerli, Fabrice Guilloux, Jean-Pierre Meyer, Philippe Schwemling
IFAE : Raimon Casanova, Yujin Gan, Sebastian Grinstein



- ~ 2 times larger than MiniCACTUS
- 0.5 mm x 1 mm (baseline), 1 mm x 1 mm and 0.5 mm x 0.5 mm diodes
- 50 µm x 150 µm and 2 50 µm x 50 µm small test diodes
- 3 different preamps
- New multistage discriminator with **programmable hysteresis**
- Improved layout for better mixed-signal coupling rejection
- **CEA-IRFU** & **IFAE-Barcelona** coll.
- Submitted in May 2023, waiting for samples to
- come back from post-processing

MiniCACTUS_V2 Sensor Chip

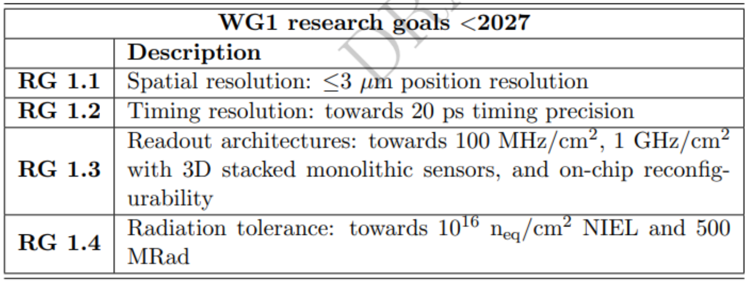
- 3 different preamps implemented in MiniCACTUS_V2
- 2 new preamps (CSA_new and VPA) designed by **IFAE-Barcelona** for better jitter and reduced ToT



Responses of the 3 preamps to an input pulse of 12ke$^-$(Tcoll=5 ns)

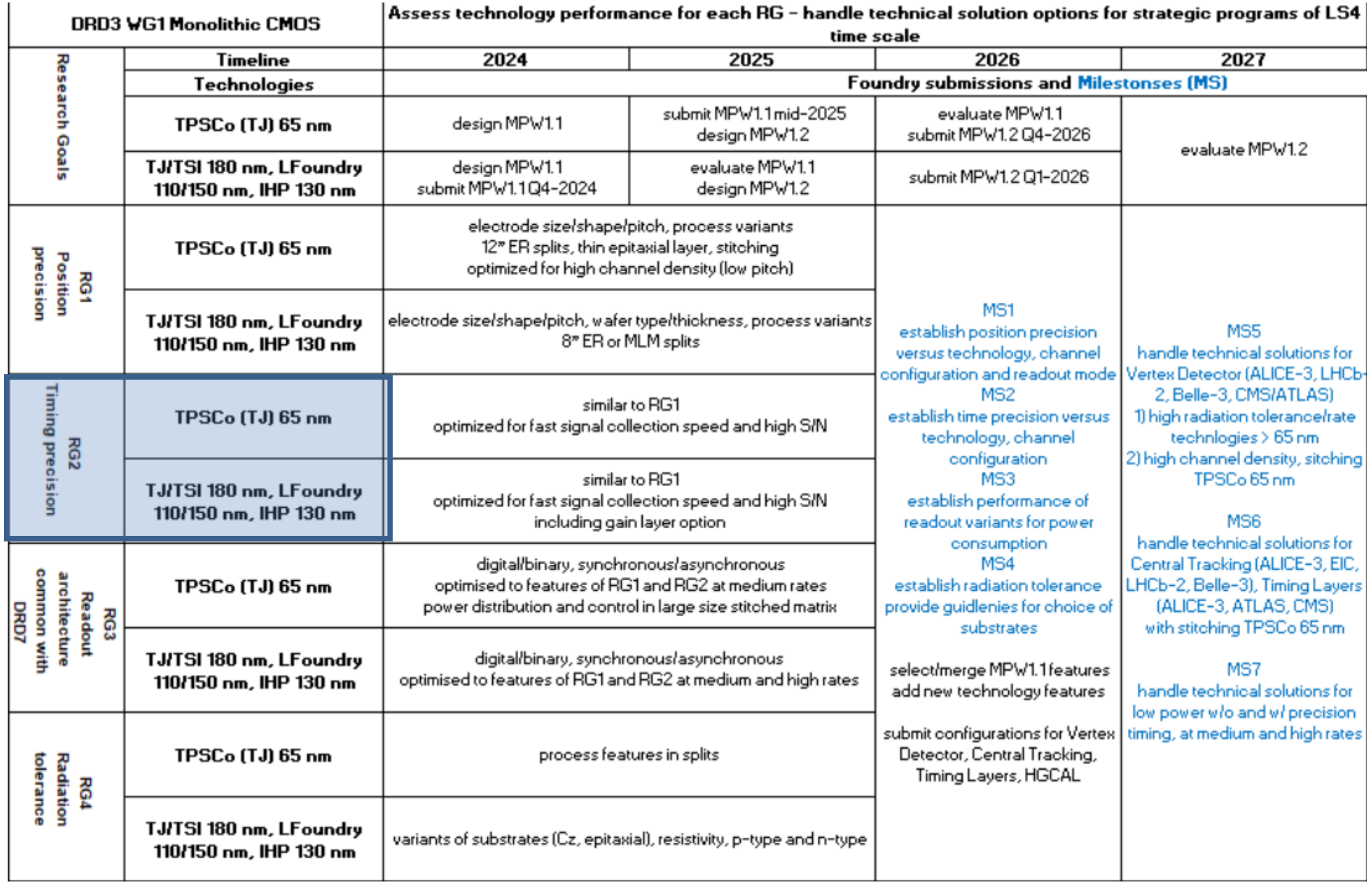
- CSA1 : MiniCACTUS_V1 charge sensitive preamp
- CSA_new : new charge sensitive preamp
- VPA : new voltage preamp

Monolithic CMOS and DRD3



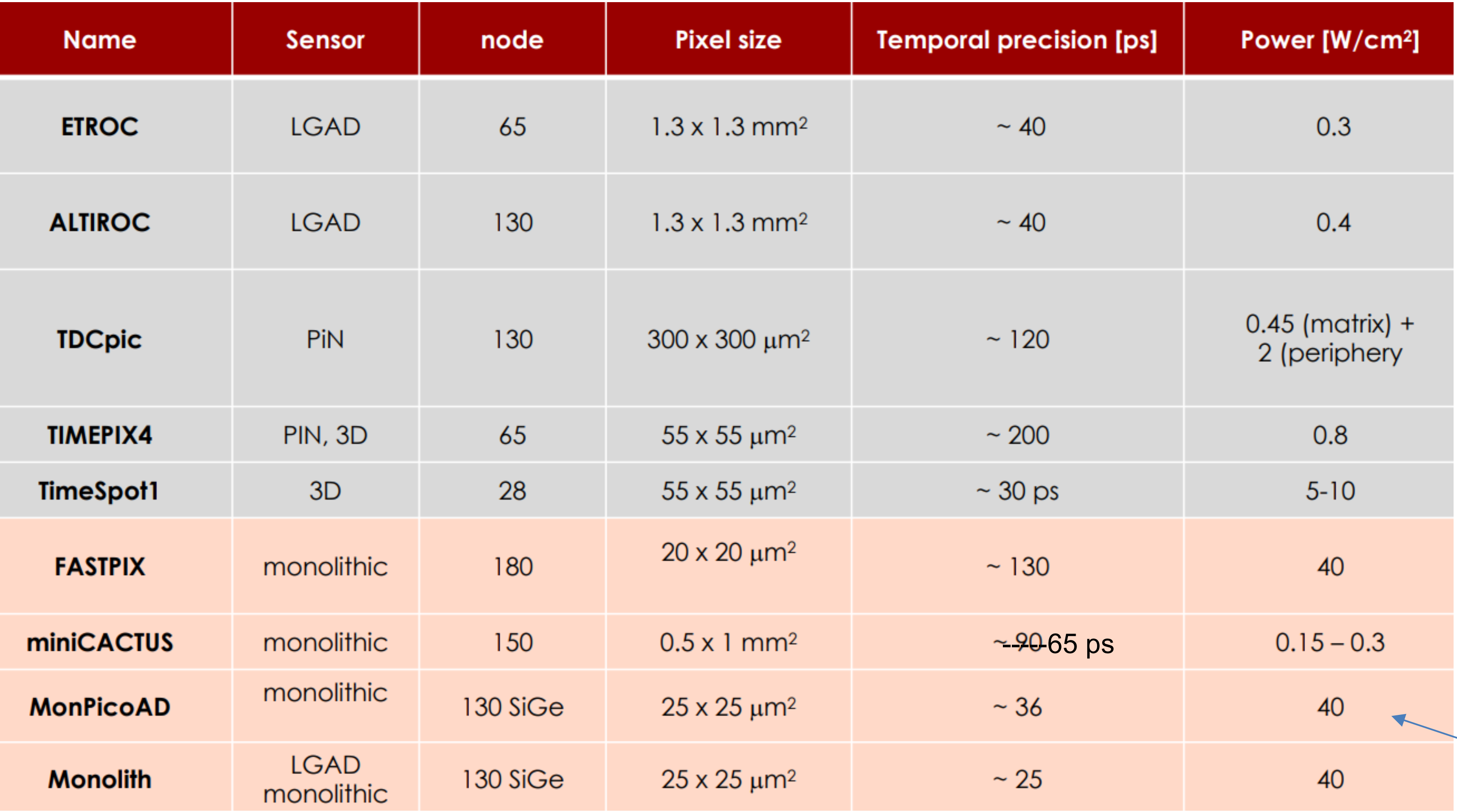
WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: ≤ 3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n$_{eq}$/cm^2 NIEL and 500 MRad

- Ambitious research goals
- Agressive timeline
- Quite some technologies/foundry processes under consideration → no clear choice yet, very likely one given technology will not reach all goals



DRD3 WG1 Monolithic CMOS		**Assess technology performance for each RG – handle technical solution options for strategic programs of LS4 time scale**			
Research Goals	**Timeline**	**2024**	**2025**	**2026**	**2027**
	Technologies	**Foundry submissions and Milestonses (MS)**			
	TPSCo (TJ) 65 nm	design MPW1.1	submit MPW1.1 mid-2025 design MPW1.2	evaluate MPW1.1 submit MPW1.2 Q4-2026	evaluate MPW1.2
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	design MPW1.1 submit MPW1.1 Q4-2024	evaluate MPW1.1 design MPW1.2	submit MPW1.2 Q1-2026	
RG1 Position precision	**TPSCo (TJ) 65 nm**	electrode size/shape/pitch, process variants 12" ER splits, thin epitaxial layer, stitching optimized for high channel density (low pitch)		MS1 establish position precision versus technology, channel configuration and readout mode MS2 establish time precision versus technology, channel configuration MS3 establish performance of readout variants for power consumption MS4 establish radiation tolerance provide guidlenies for choice of substrates select/merge MPW1.1 features add new technology features submit configurations for Vertex Detector, Central Tracking, Timing Layers, HGCAL	MS5 handle technical solutions for Vertex Detector (ALICE-3, LHCb-2, Belle-3, CMS/ATLAS) 1) high radiation tolerance/rate technlogies > 65 nm 2) high channel density, sitching TPSCo 65 nm MS6 handle technical solutions for Central Tracking (ALICE-3, EIC, LHCb-2, Belle-3), Timing Layers (ALICE-3, ATLAS, CMS) with stitching TPSCo 65 nm MS7 handle technical solutions for low power w/o and w/ precision timing, at medium and high rates
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	electrode size/shape/pitch, wafer type/thickness, process variants 8" ER or MLM splits			
RG2 Timing precision	**TPSCo (TJ) 65 nm**	similar to RG1 optimized for fast signal collection speed and high S/N			
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	similar to RG1 optimized for fast signal collection speed and high S/N including gain layer option			
RG3 Readout architecture common with DRD7	**TPSCo (TJ) 65 nm**	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium rates power distribution and control in large size stitched matrix			
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium and high rates			
RG4 Radiation tolerance	**TPSCo (TJ) 65 nm**	process features in splits			
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	variants of substrates (Cz, epitaxial), resistivity, p-type and n-type			

Global trade-offs : time resolution is not everything



Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm²	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm²	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm²	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm²	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm²	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm²	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm²	~~~ 90~~ 65 ps	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm²	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm²	~ 25	40

50 ps @ 0.1W/cm2

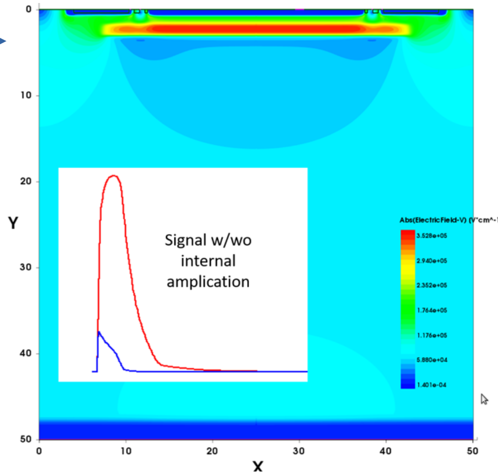
Table from N. Cartiglia (VCI 2022)

Trade off to be found between
- Space resolution,
- time resolution
- power consumption
- Technology availability

Conclusions and perspectives

Short term : evaluation of 10^{15} 1 MeV neq/cm^2 MiniCactus v1 : 10^{14} (1 MeV neq/cm^2 (not shown here) have perf comparable to unirradiated chips if cooled at -15°C

- In-lab and test-beam tests of MiniCactus v2. Hope to correct analog/digital coupling and have improved timing performance !
- Medium term : investigate monolithic pixels with integrated gain layer.
- Possible with standard LF15A process, submission being prepared
  - Intrinsic gain would allow better timing performance and possibility of thinner sensors



- In general, a lot of activity underway on monolithic CMOS timing oriented sensor
- developments
  - Many technologies are being evaluated, see DRD3 WGs and WPs

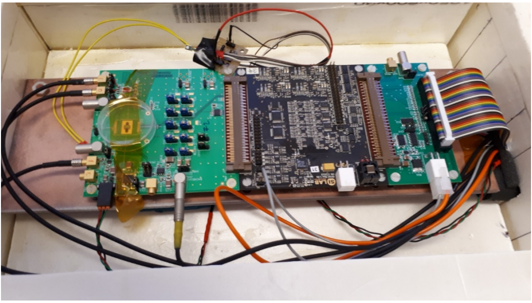
- Present performance not far from what could be needed for a timing layer or a TOF detector

- Integration in an actual experiment needs :
  - Careful trade off evaluation between timing performance, space resolution, power dissipation
  - A lot of work to integrate digital data processing in a fully monolithic design

- Publications :
  - MiniCACTUS: A 65 ps Time Resolution Depleted Monolithic CMOS Sensor (arXiv:2309.08439, NSS 2022 conference)
  - MiniCACTUS: Sub-100 ps timing with depleted MAPS, Nucl.Instrum.Meth.A 1039 (2022) 167022, VCI 2022 conference)
  - CACTUS: A depleted monolithic active timing sensor using a CMOS radiation hard technology (arXiv:2003.04102, JINST 15 (2020) 06, P06011)

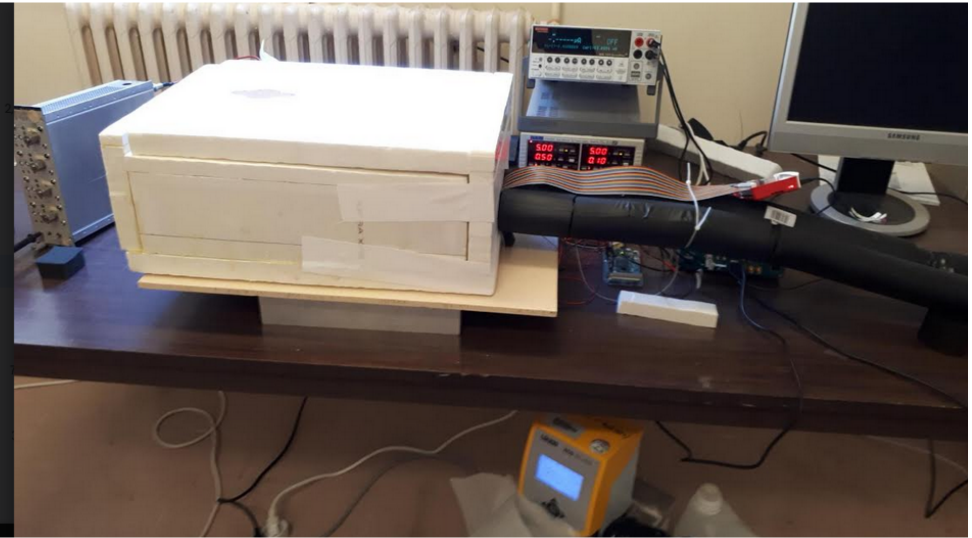
Backup

Development of cold box setup



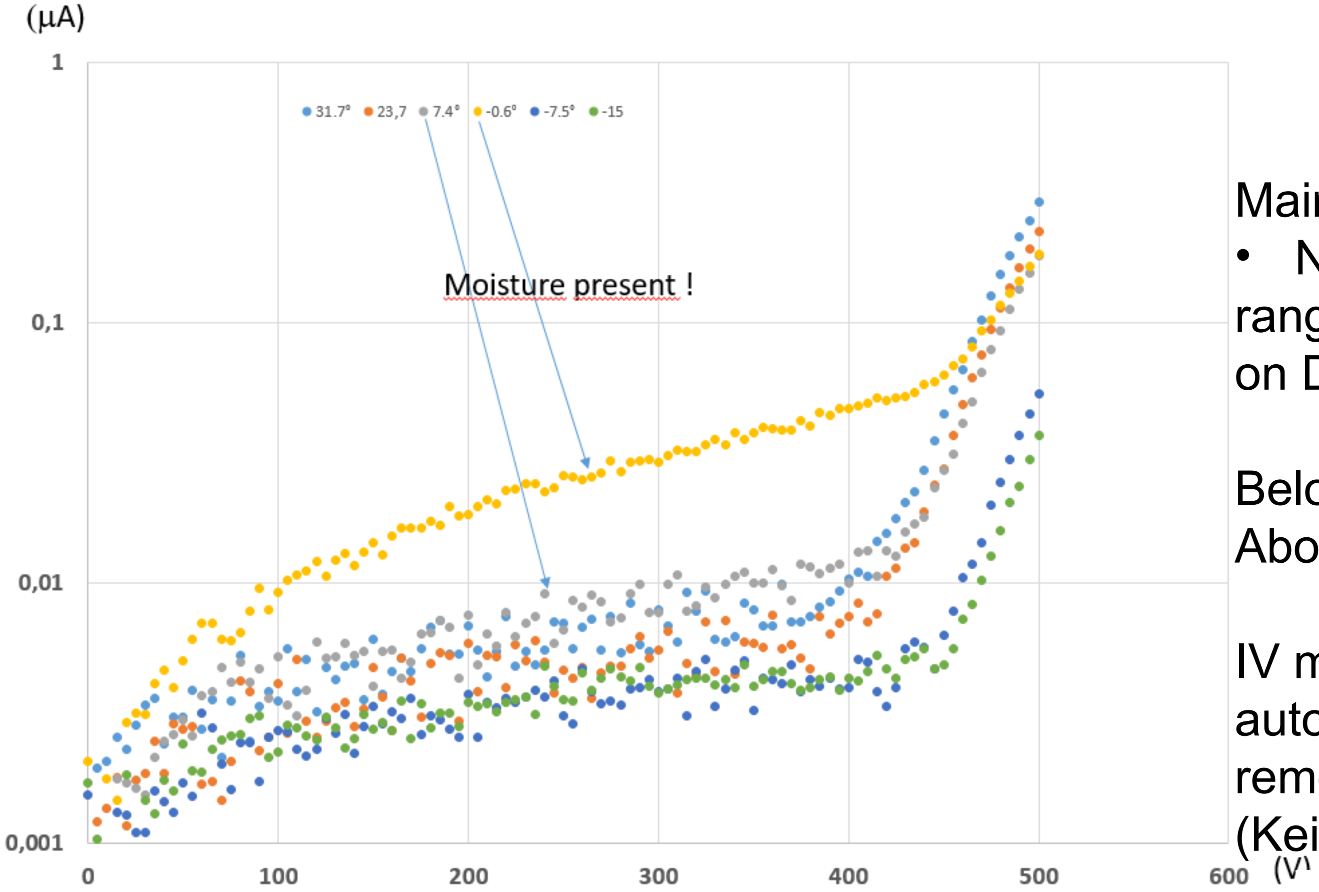
Initial status

After one month of continuous operation at -15°C



- Mostly intended to test irradiated samples
  - We have 100 µ and 300 µ irradiated at 10^{14}, 10^{15}, 10^{16} 1 MeV neq/cm^2
- MiniCactus testbench (DUT board, GPAC, Raspio) in insulating foam box (plus feedthroughs for power and cooling)
- Copper plate with a cooling pipe welded to it plus copper fingers bring cold surface as close as possible to DUT
- Monitoring of temperature and moisture level at various places in cold box
- No moisture control, we just try to minimise water input
- LAUDA chiller, min temp -30°C at chiller output
- Kapton windows allow use of 90Sr beta source (has to stay outside of cold box for safety/regulatory reasons)

IV curves vs temperature (Unirradiated DUT. 300 µ thick)



Main conclusion :

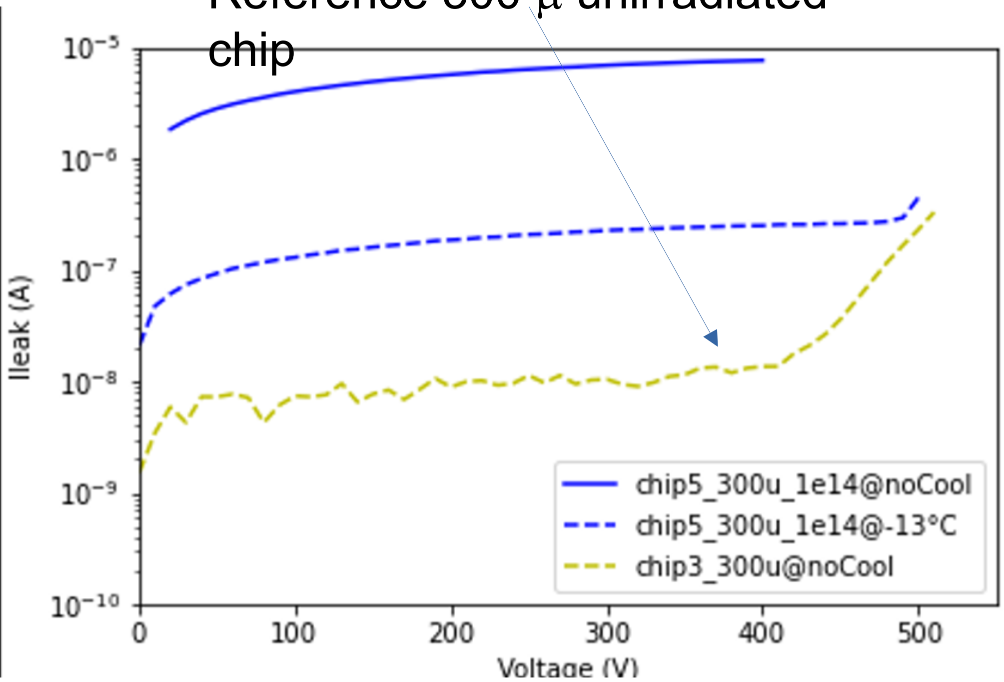
- Need to run avoiding temperature range between 7.5°C and -1°C measured on DUT

Below -1°C all water is frozen → OK
Above 7.5°C all water is vapour → OK

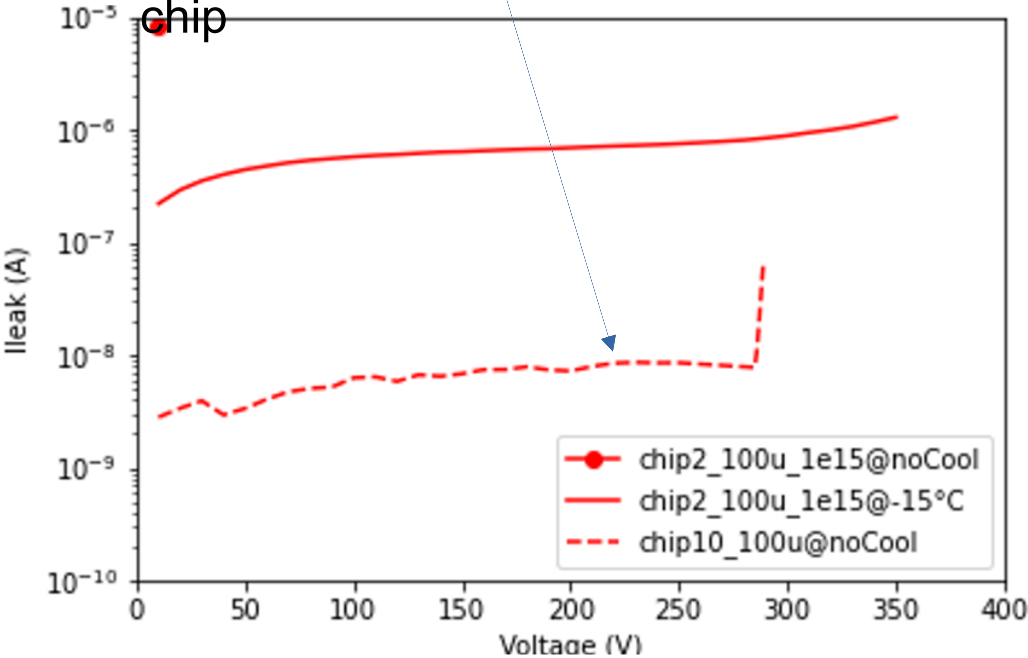
IV measurement done routinely and automatically through
remote control and monitoring of HV PS (Keithley sourcemeter)

IV curves of irradiated MiniCactus v1

Reference 300 μ unirradiated chip

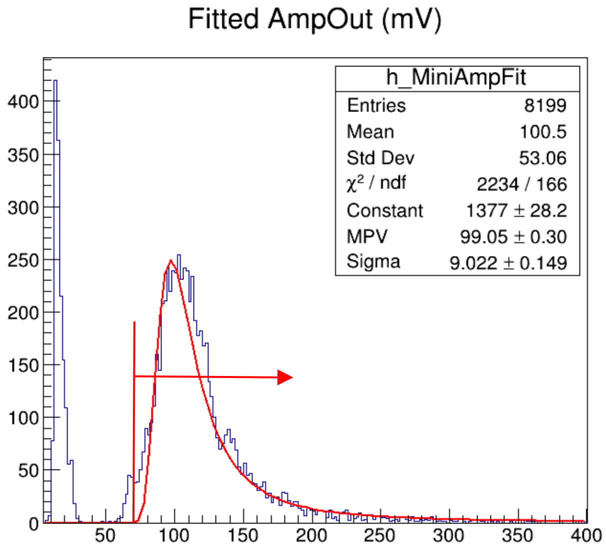


Reference 100 μ unirradiated chip

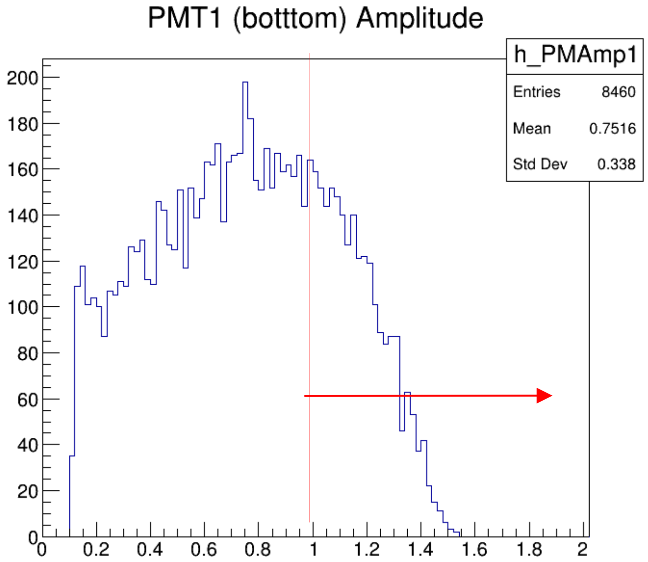


As expected, BV increases with total dose
Cooling is essential to bring leakage current to manageable values

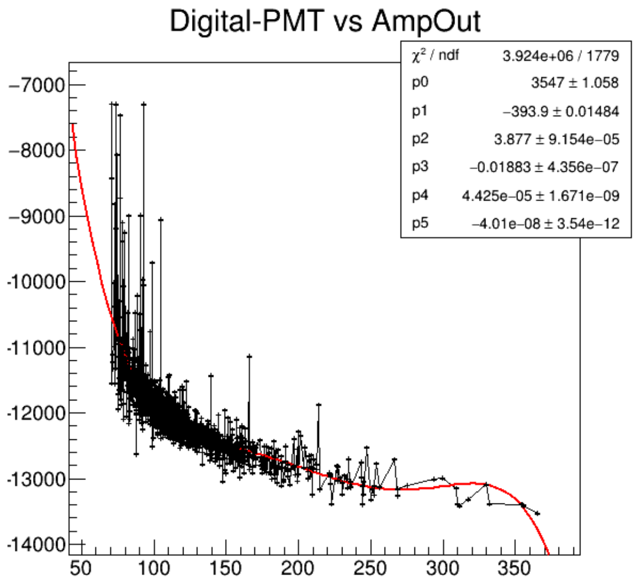
PMT and MiniCactus data
10^{14} 1 MeV neq irradiated DUT, 300 µ thick, 200V



Amplitude
(mV)



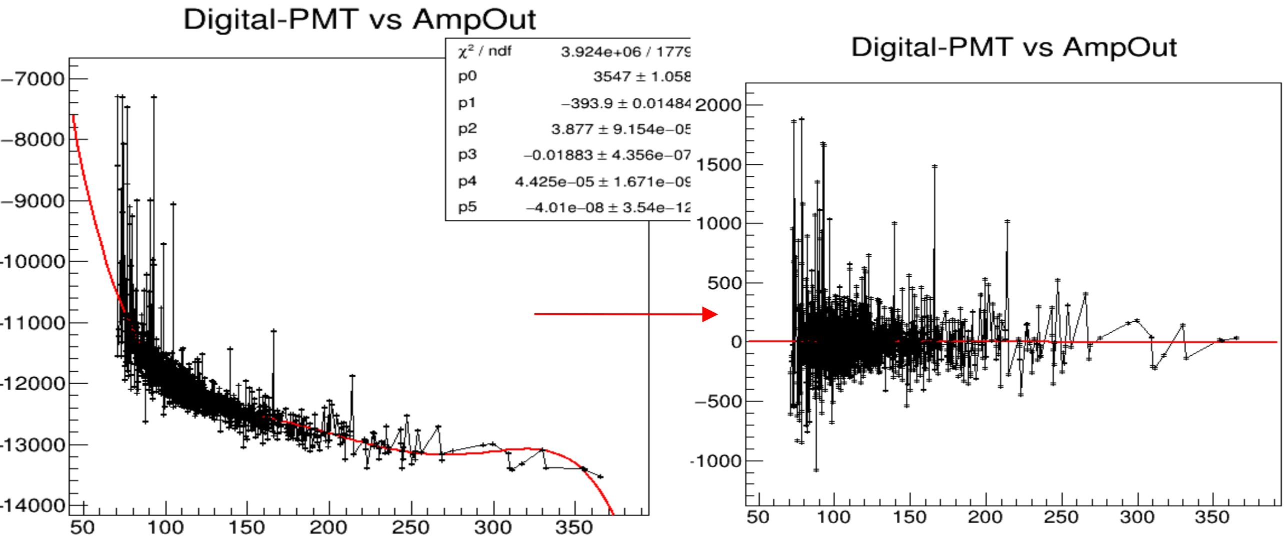
Amplitude
(V)

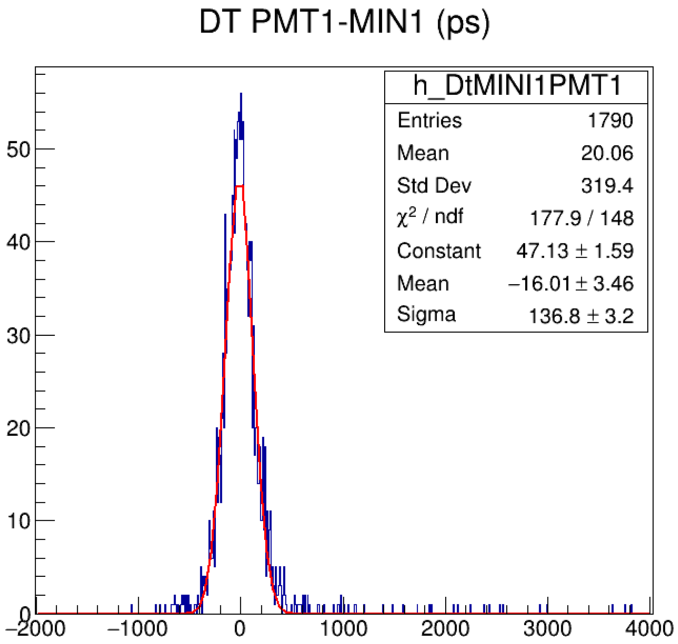


TW correction
As a fct of analog
amplitude

yavuz.degerli@cea.f

PMT and MiniCactus data
10^{14} 1 MeV neq irradiated DUT, 300 µ thick, 200 V

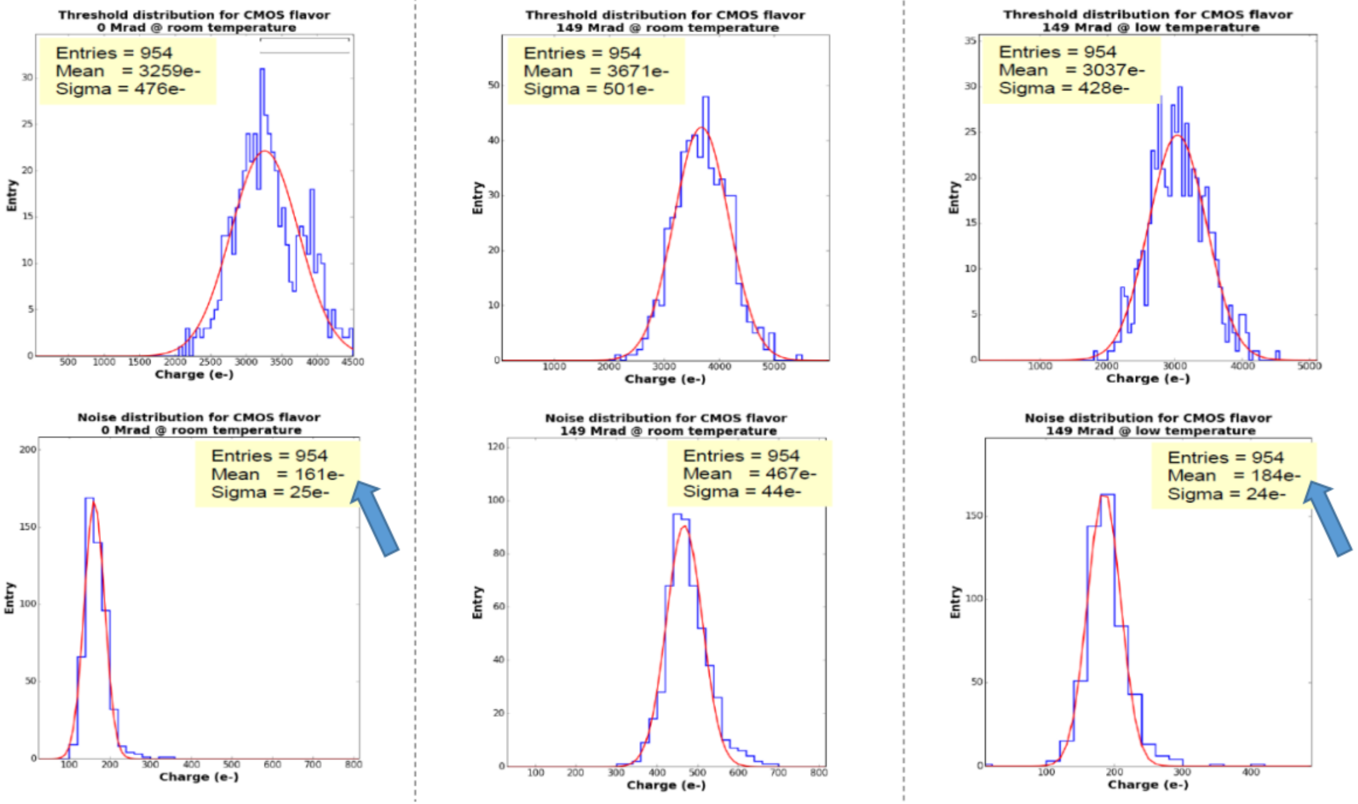


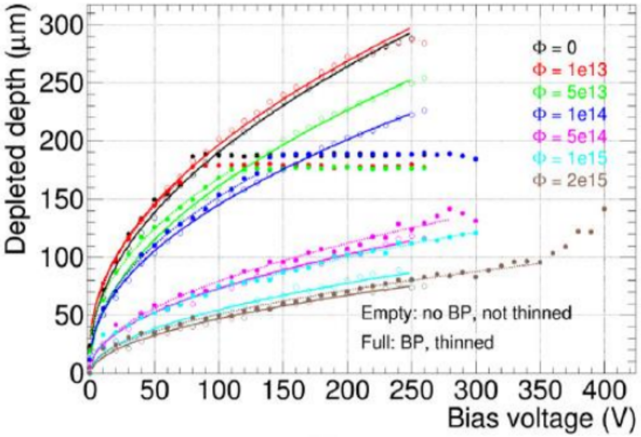


yavuz.degerli@cea.f

LF15A radiation hardness

0 Mrad @Room Temp **149 Mrad @Room Temp** **149 Mrad @Low Temp -15°C**





[I. Mandic et al. NIM A 903, 2018]

→ Radiation tests at CERN-SPS with **proton** beam on **LF-CPIX** chip (**CPPM**)

→ 14% increase of noise after irradiation with cooling

Comparison of time resolution of unirradiated and 10^{14} 1 MeV neq chips

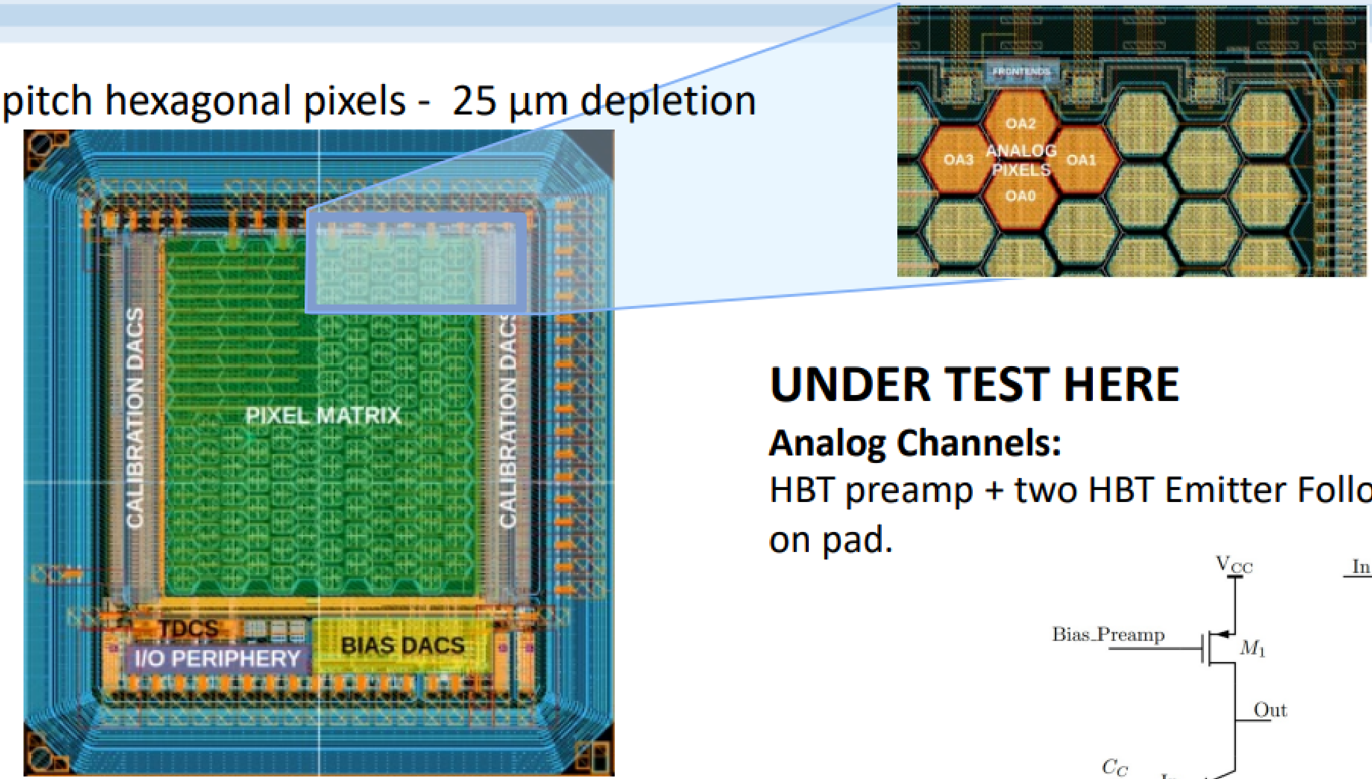
Sensor	HV bias (V)	Conditions	Temp. (°C)	Time res. (ps)	MPV (mV)
Unirradiated 300 u	400	testbeam, MCPMT time reference	room	78.97 ± 1.36	201.9 ± 0.5
Unirradiated 300 u	400	90Sr, PMT time reference*	room	104.5 ± 2.30	195.7 ± 2.3
Unirradiated 300 u	280	testbeam, MCPMT time reference	room	89.11 ± 1.56	200.9 ± 0.5
Irradiated 300 u	280	90 Sr, PMT time reference	20	108.2 ± 3.2 (PMT subt.)	108.2 ± 3.2
Irradiated 300 u	320	90 Sr, PMT time reference	20	132.9 ± 5.0 (PMT subt.)	113.5 ± 0.8
Irradiated 300 u	320	90 Sr, PMT time reference	-15	87.9 ± 4.7 (PMT subt.)	132.7 ± 0.6

Irradiation at 10^{14} n_{eq} worsens time resolution by 18 % w.r.t. unirradiated at 20 °C
Cooling at -15°C brings time resolution more or less back to unirradiated performance (less dark current fluctuations)

*PMT resolution for 90 Sr betas estimated to be 71.3 ps ± 1.7 ps

ATTRACT prototype

100µm pitch hexagonal pixels - 25 µm depletion

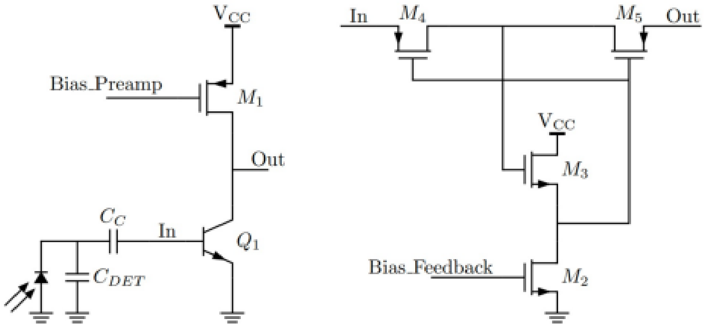


MPW submission in 2019 funded by H2020 ATTRACT

UNDER TEST HERE

Analog Channels:

HBT preamp + two HBT Emitter Followers to 500Ω Resistance on pad.



G. Iacobucci et al 2022 JINST 17 P02019

MONOLITH

UNIVERSITÉ DE GENÈVE

FACULTY OF SCIENCE
Department of Nuclear and Particle Physics

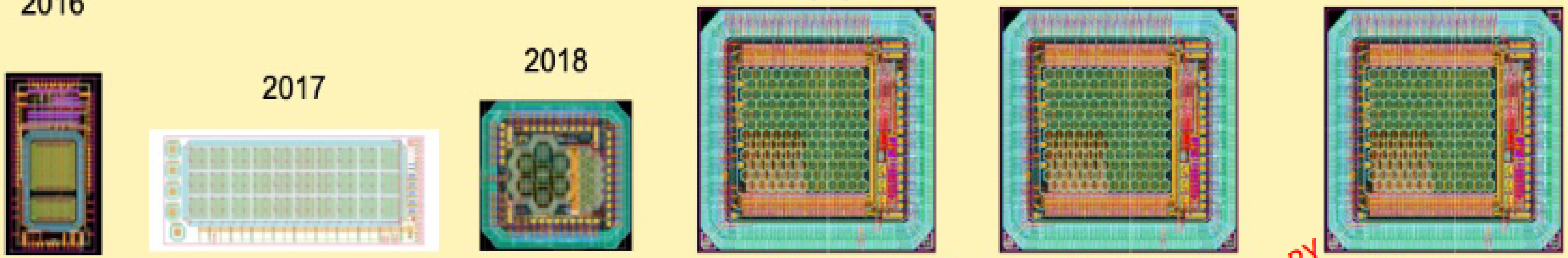
Leading-edge technology: **IHP SG13G2**

130 nm process featuring **SiGe HBT** with

- Transistor transition frequency: $f_t = 0.3\ THz$
- DC Current gain: $\beta = 900$
- Delay gate: **1.8 ps**

innovations for high performance microelectronics

Leibniz-Institut für innovative Mikroelektronik



2016

200ps

- 1 and 0.5 mm² pixels
- Discriminator output

2017

110ps

- 30 pixels 500x500µm²
- 100ps TDC +I/O logic

2018

50ps

- Hexagonal pixels 65µm and 130µm side
- Discriminator output

2019

ATTRACT noGAIN

36ps

- Hexagonal pixels 65µm side
- 30ps TDC +I/O logic
- Analog channels

2021

PicoAD p0

24ps

PRELIMINARY

- Same pixel/Electronics of ATTRACT

2022

PicoAD p1

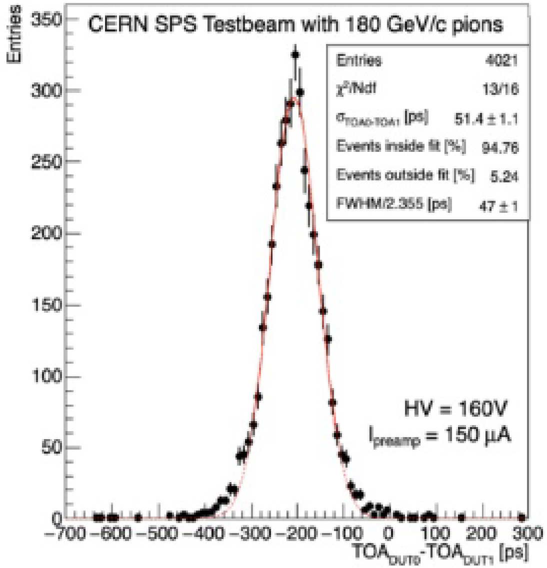
- Hexagonal pixels 65µm side
- 1ps TDC +I/O logic
- New FE, target 10ps

MONOLITH

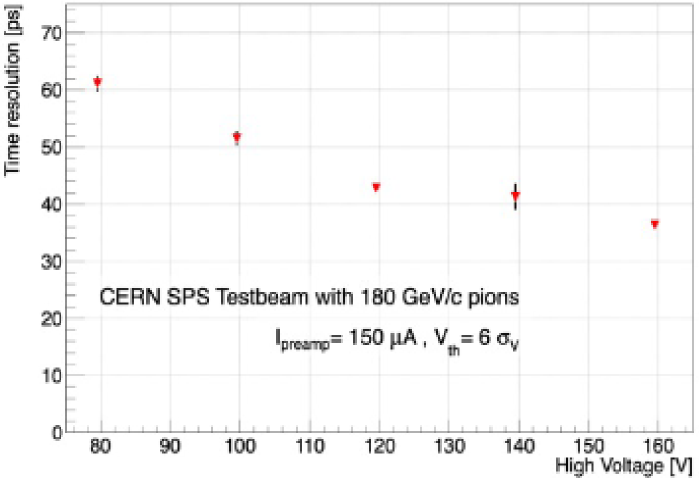
UNIVERSITÉ DE GENÈVE

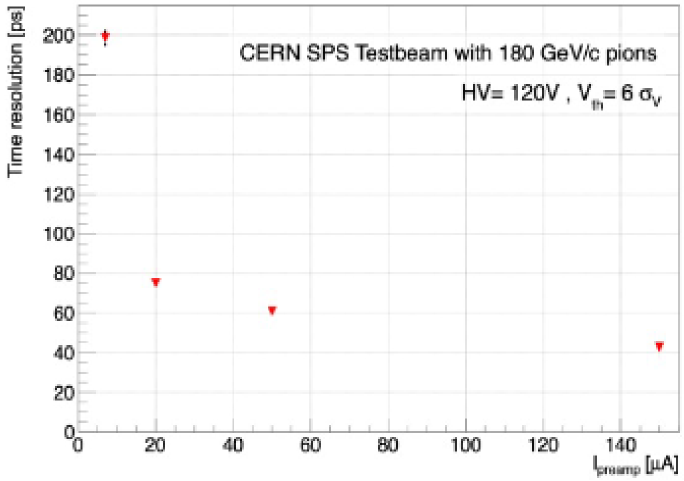
FACULTY OF SCIENCE
Department of Nuclear and Particle Physics

ATTRACT prototype – Time Stamping



Time of flight between DUT0 and DUT1





- 57 ps after 10^{16}
1 MeV neq/cm2
- can be brought back to 40 ps, with
HV and LVPS increase :
Arxiv : 2310.19398

$$\sigma_t = \frac{\sigma_{TOA0\text{-}TOA1}}{\sqrt{2}} = (36.4 \pm 0.8)\text{ps}$$ without gain structure

24 ps with gain layer (but complicated manufacturing
→ mass scale production ???)

Fastpix (CERN) : sub-ns timing with TJ180

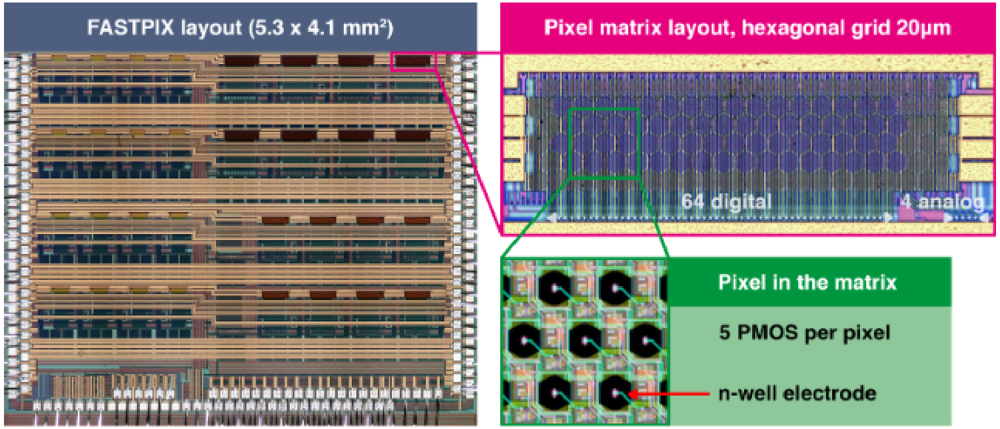


Figure 2. FASTPIX layout (5.3 mm × 4.1 mm) with details of the 20 µm pitch hexagonal grid
zoom on 7 pixels.

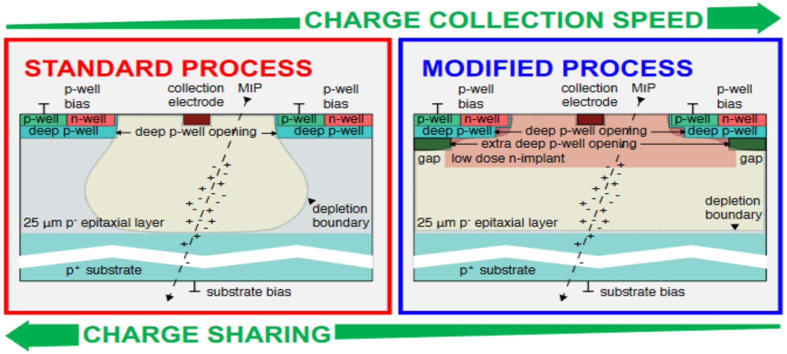


Figure 2. Wafer production process variants for FASTPIX represented by schematic cross-sections of the pixel unit cells, showing a cut perpendicular to the sensor surface. The standard 180 nm CMOS imaging process (left) and the modified process variant (right) with added low-dose n-type implant and optimizations such as a gap in the n-implant, retracted deep p-well and additional extra-deep p-well implant.

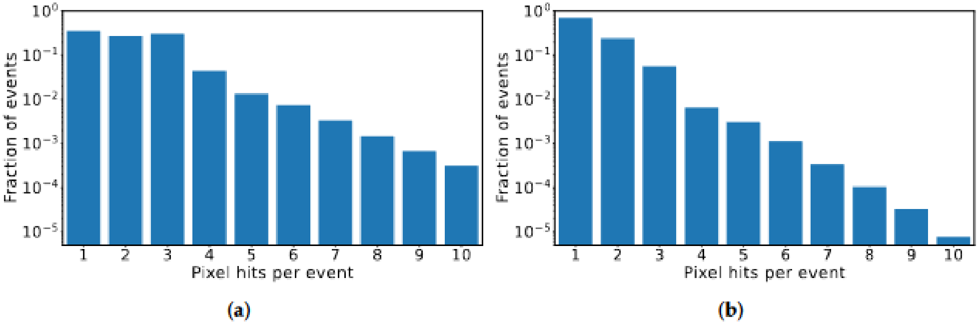


Figure 8. Number of pixel hits per event for the 10 µm (a) and 20 µm (b) pitch matrix.

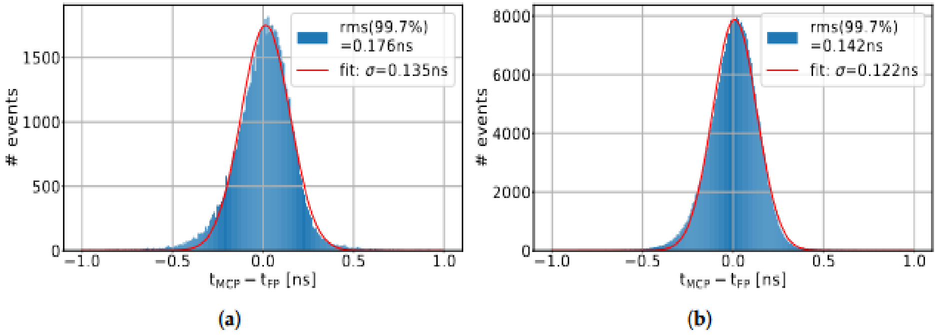
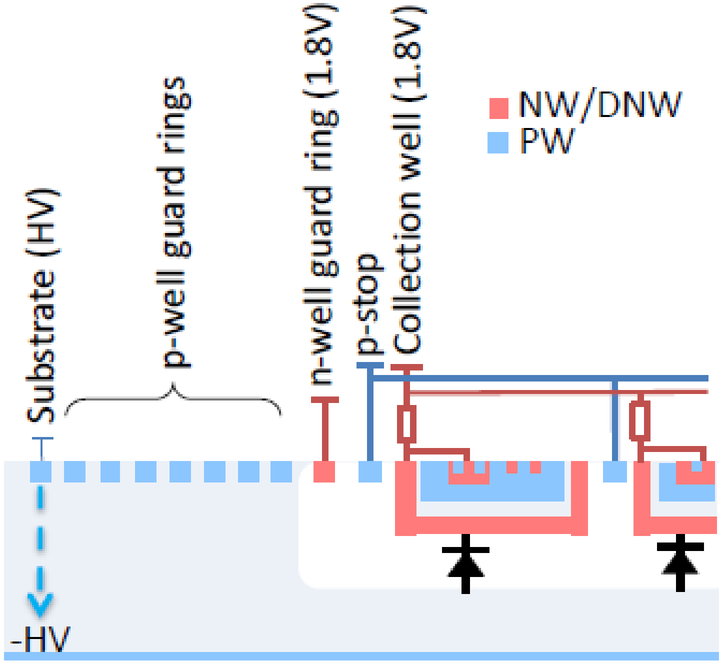


Figure 14. Seed-pixel time residuals after timewalk correction for the inner region of the 10 µm (a) and 20 µm (b) pitch matrix.

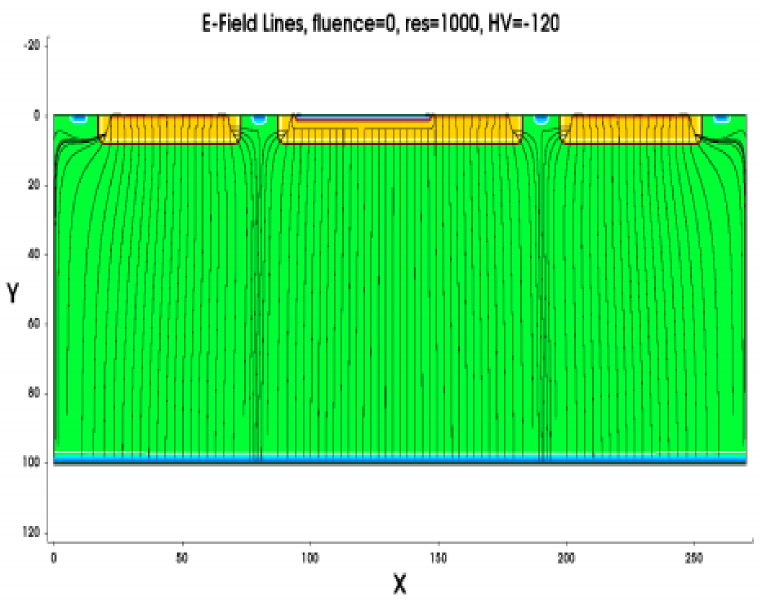
Plan to port and test the concept on TPSCo 65 technology, but small pixels → beware of drift field inhomogeneity !

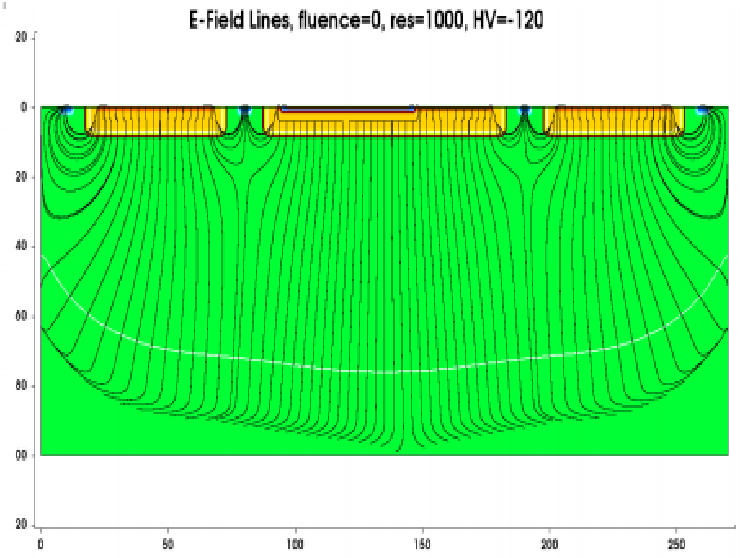
GUARD-RINGS OF LF-MONOPIX1



[M. Barbero et al. JINST 15, 2020]

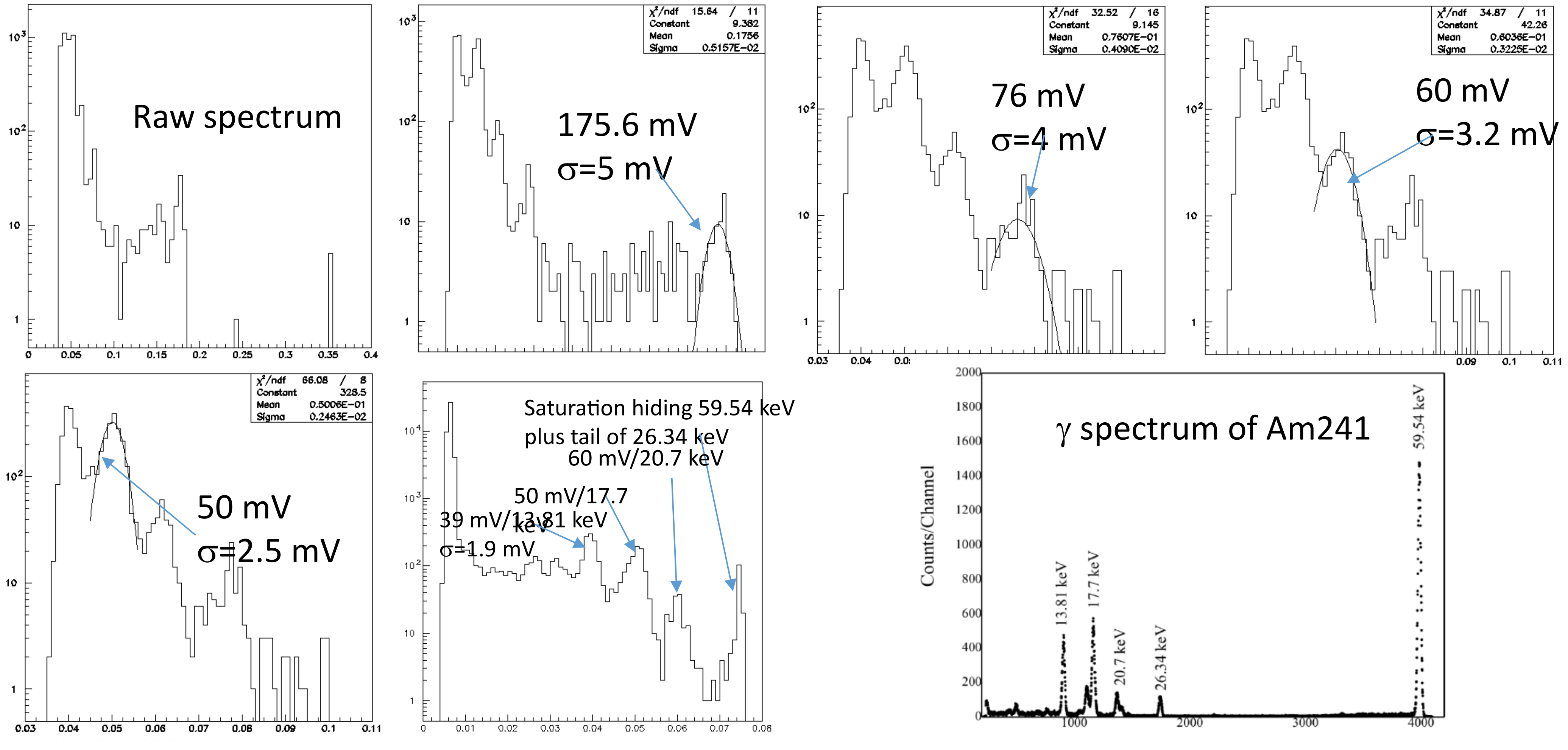
ELECTRIC FIELDS





Backside versus top biasing → Need backside polarization to ensure best charge collection and signal shape uniformity!

241Am Amplitude Spectrum (pixel 5, 50 µm x 150 µm)


Raw spectrum

175.6 mV
σ=5 mV

76 mV
σ=4 mV

60 mV
σ=3.2 mV

50 mV
σ=2.5 mV

Saturation hiding 59.54 keV plus tail of 26.34 keV

60 mV/20.7 keV

50 mV/17.7 keV

39 mV/13.81 keV
σ=1.9 mV

γ spectrum of Am241

Test-beam at Synchrotron Soleil
June 2022

SOLEIL
SYNCHROTRON

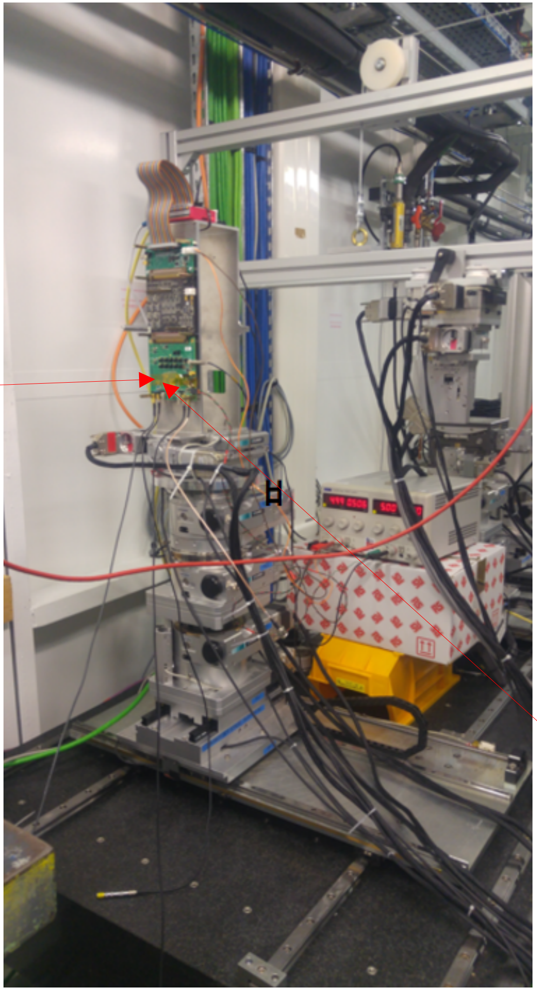
Many thanks to Fabienne Orsini and Arkadiusz Dawiec
(Synchrotron Soleil)
for the beam time and the technical support !

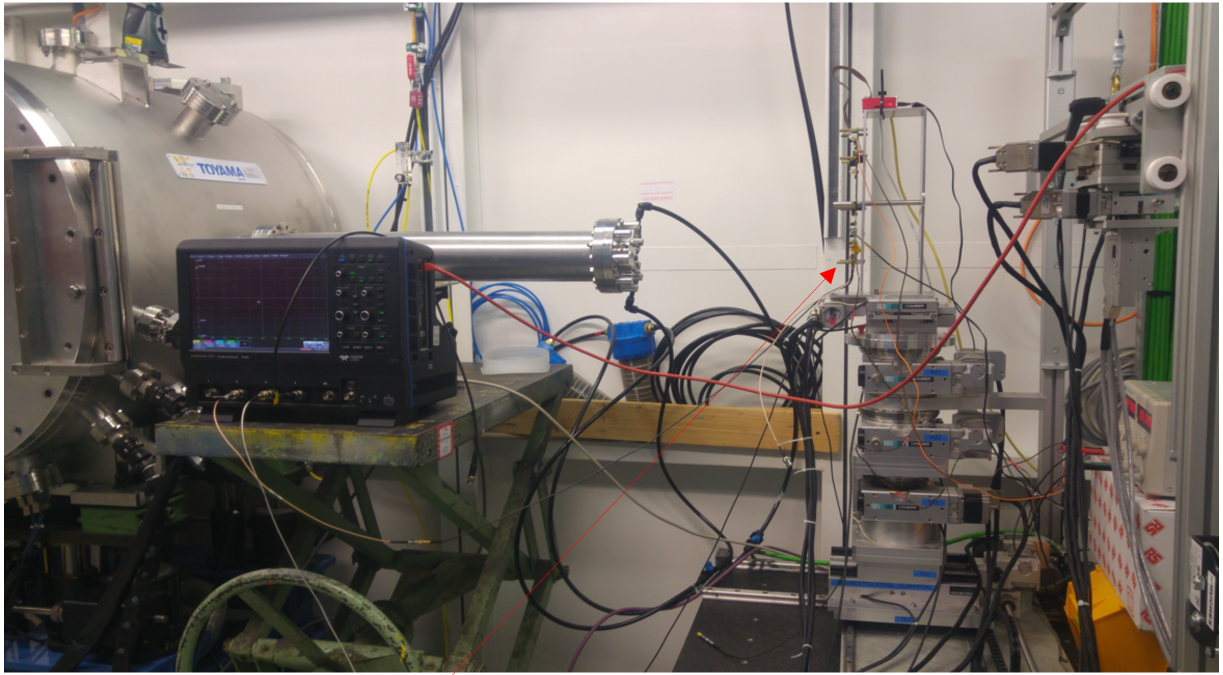
Photon beam is bunched : 90 ps pulse length
Every 2.6 ns

Allows to study energy and time response
Beams of 10 keV, 20 keV, 30 keV, 40 keV
Available, attenuated to have ≈ 1 photon/bunch

With X/γradioactive sources, only energy response can be studied

Setup pictures



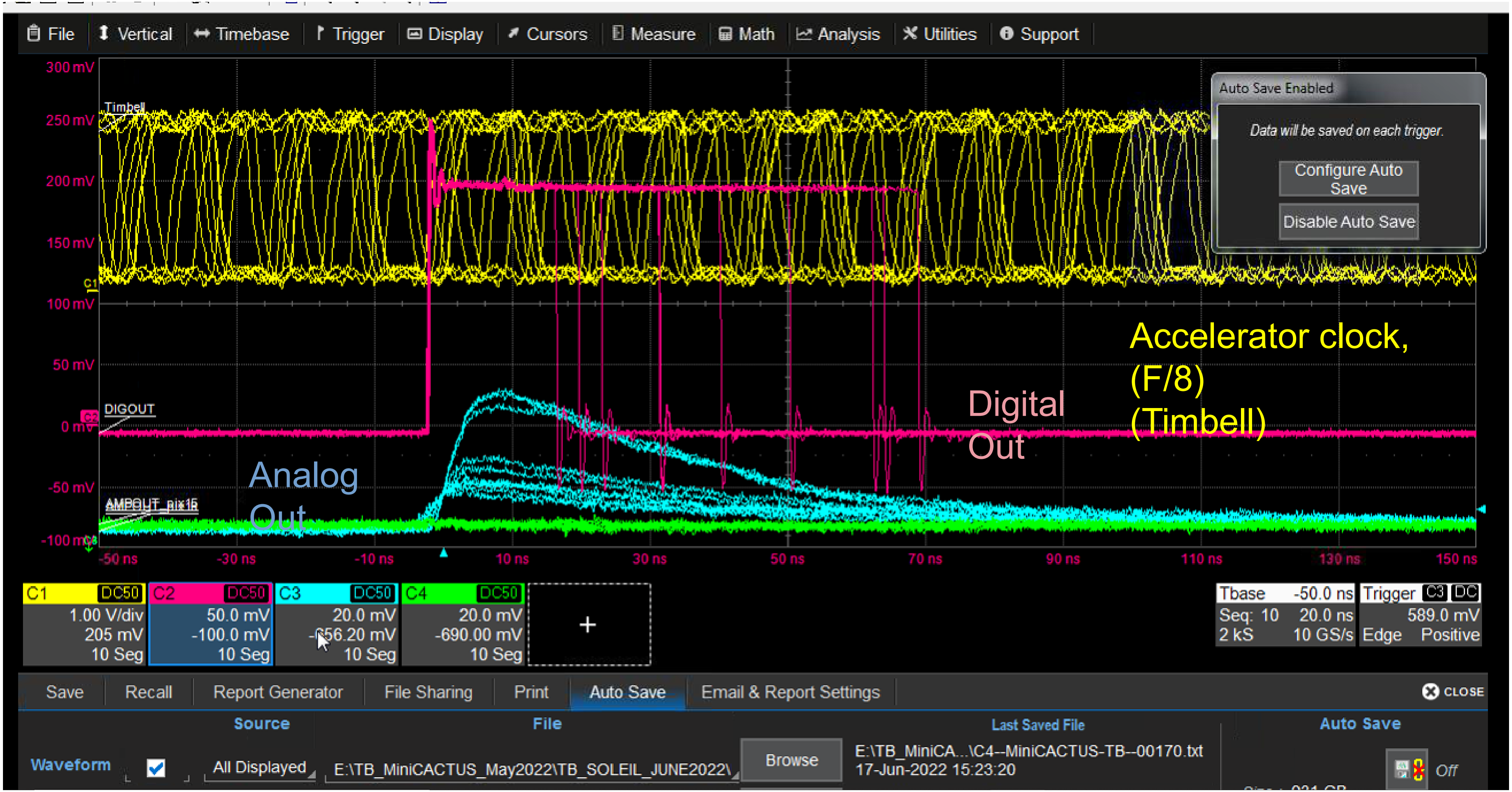


Beam direction

MiniCactus chip

Data acquired with LeCroy oscilloscope,
at 10 GSPS, 8 bits

Typical waveforms



Data will be saved on each trigger.

C1 DC50
1.00 V/div
205 mV
10 Seg

C2 DC50
50.0 mV
-100.0 mV
10 Seg

C3 DC50
20.0 mV
-[illegible]56.20 mV
10 Seg

C4 DC50
20.0 mV
-690.00 mV
10 Seg

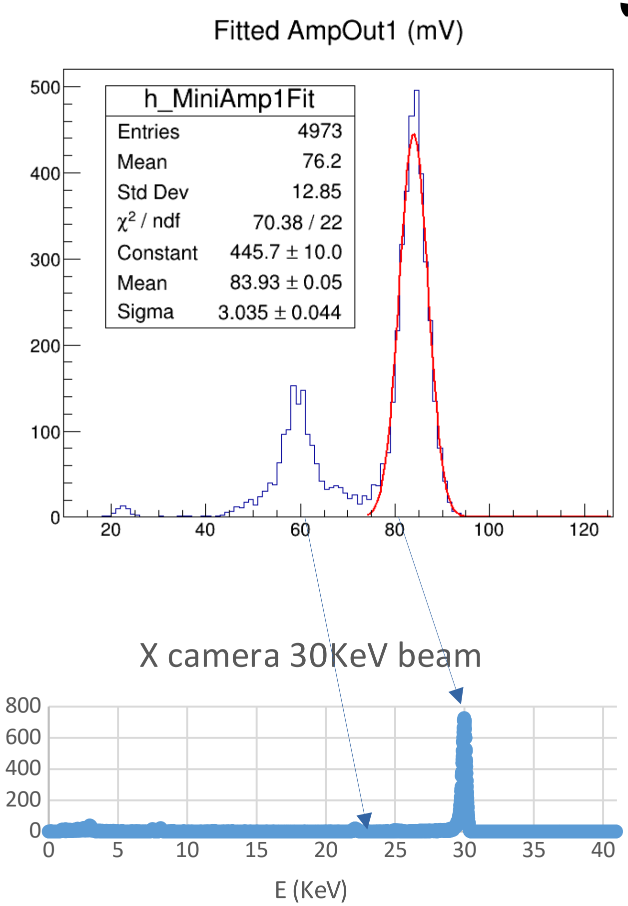
Tbase -50.0 ns
Seq: 10 20.0 ns
2 kS 10 GS/s

Trigger C3 DC
589.0 mV
Edge Positive

Waveform ☑ All Displayed
E:\TB_MiniCACTUS_May2022\TB_SOLEIL_JUNE2022\

E:\TB_MiniCA...\C4--MiniCACTUS-TB--00170.txt
17-Jun-2022 15:23:20

Energy spectra at Soleil

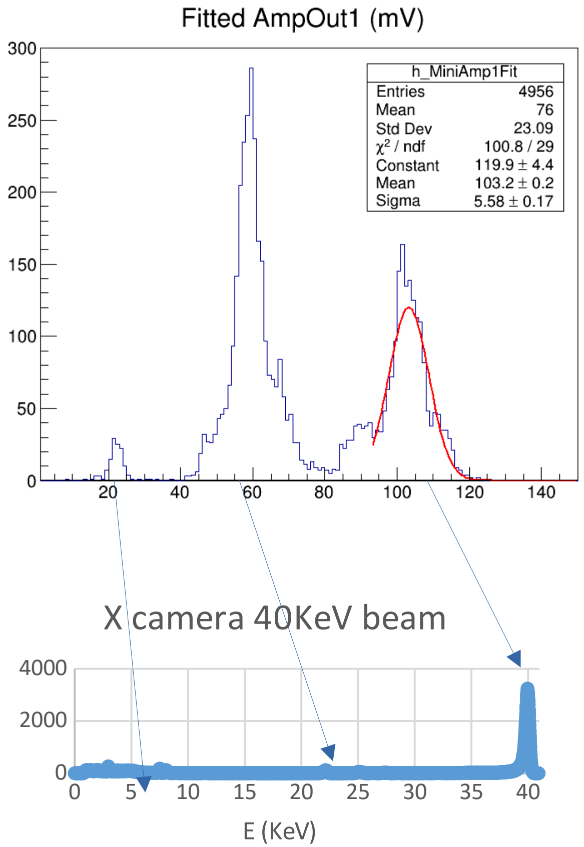


Parasitic energy peaks observed in MiniCactus

Their existence is confirmed by a dedicated camera installed
on the beam line

Most probably due to fluorescence
of PCB material (close to MiniCactus)

Camera sees different amplitude due
to solid angle effect

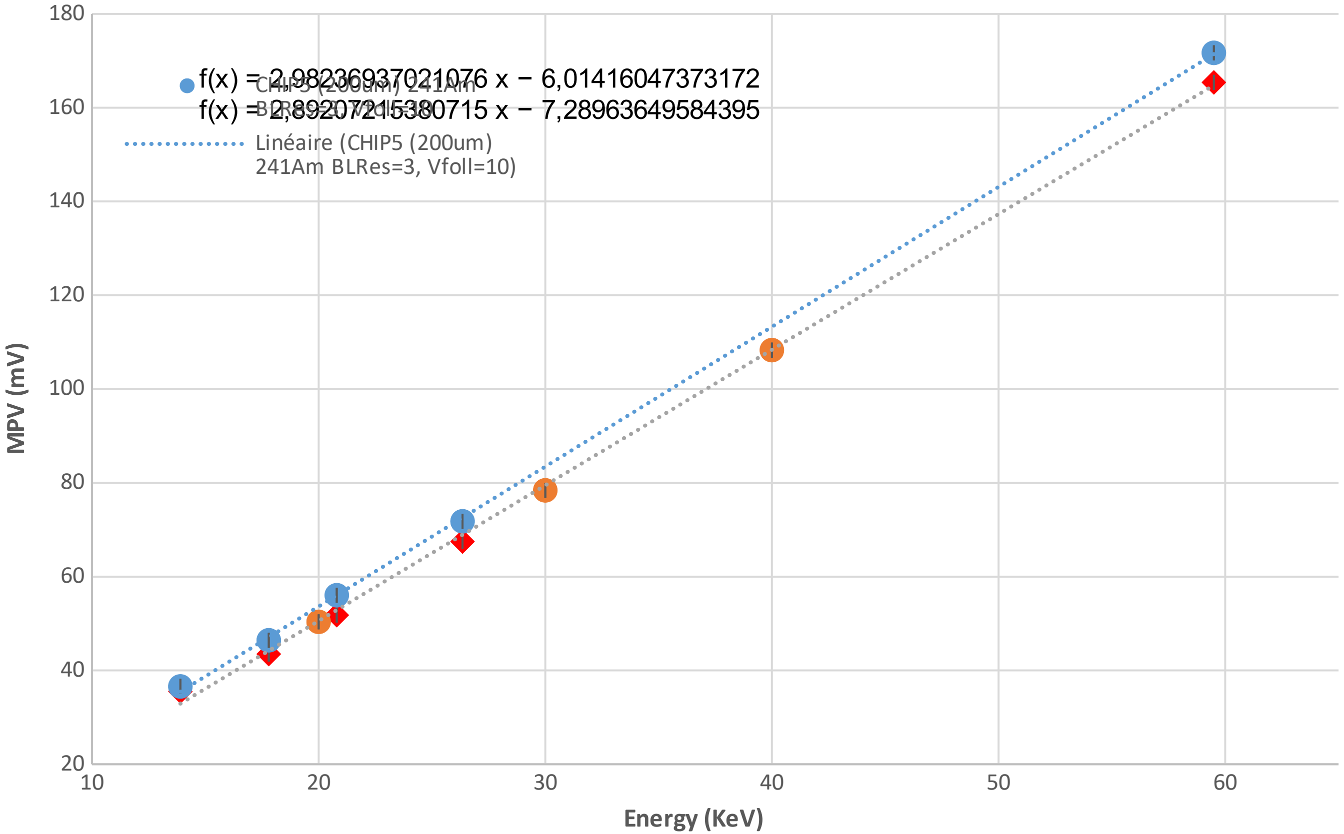


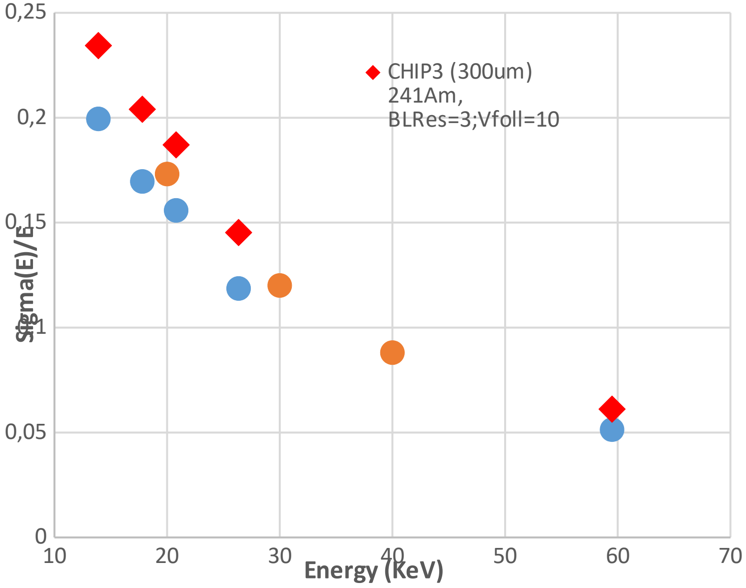
Calibration comparison between Soleil data and 241Am X-ray lines

200 µ chip, 241Am data (200 V), px 8

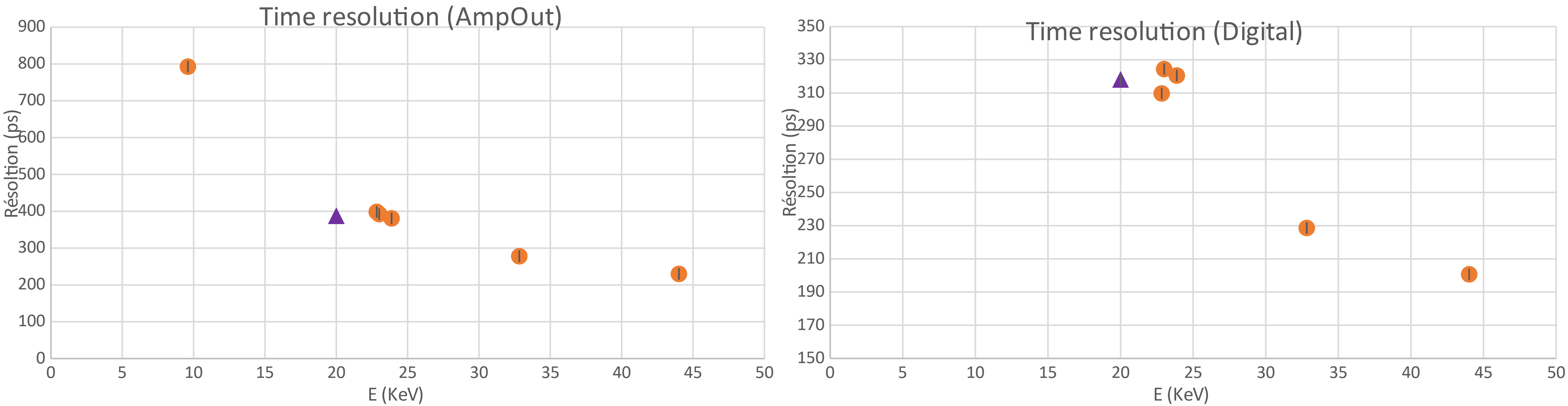
300 µ chip, Soleil data (400 V), px 8

300 µ chip, 241Am (300 V)





Time resolution with photons



Time resolution worse for photons than for MIPs, at similar S/N

40 keV photon (≈200 ps) releases similar charge as a MIP (≈65 ps)

Interpreted as due to the different structure of energy deposits :

Pointlike for photons, along a line for MIPs