环形正负电子对撞机
Circular Electron Positron Collider

Preliminary consideration of the Elec-TDAQ framework for the CEPC Det. Ref-TDR

Wei Wei

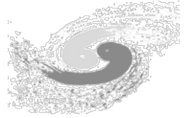
On behalf of the Elec-TDAQ system of the CEPC Ref-TDR

IHEP, CAS

2024-04-09

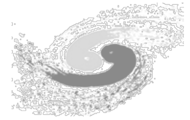
CEPC Workshop EU 2024

Outline

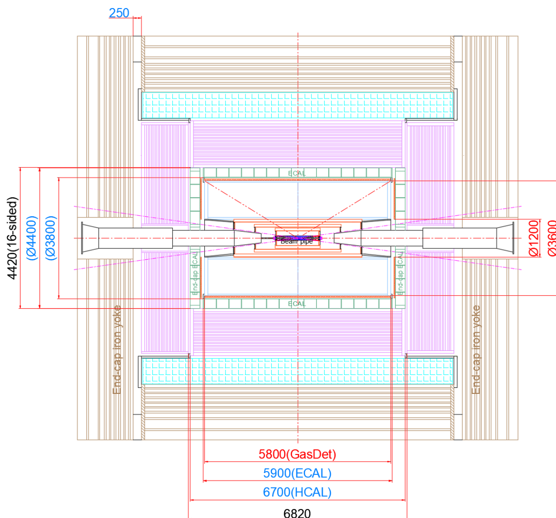


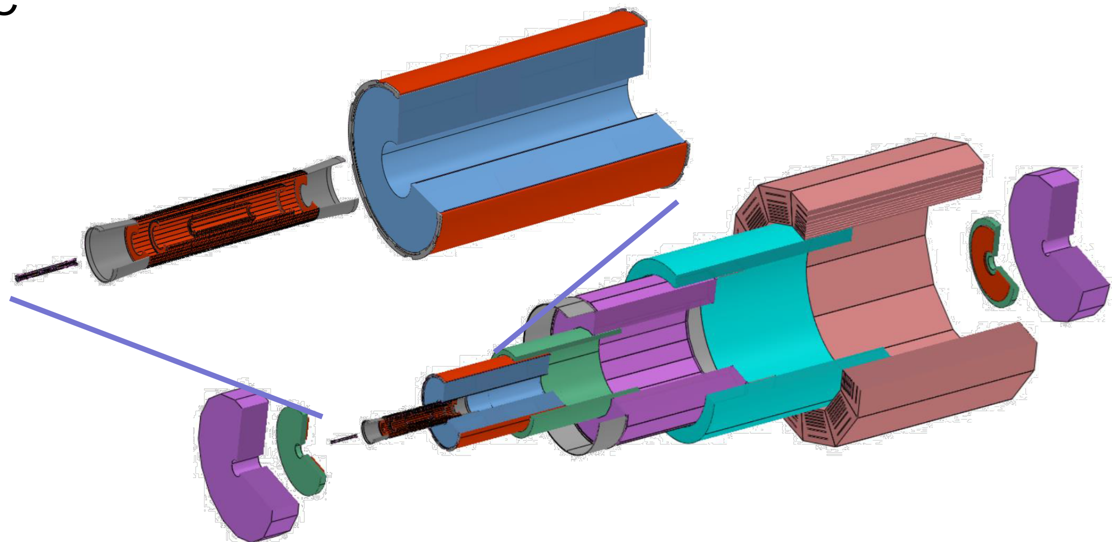
- **Motivation & detector background**
- **Requirements from the CEPC detectors**
- **Considerations for the CEPC electronics design**
  - ➢ The Frontend Electronics (FEE)
  - ➢ The Backend Electronics (BEE)
  - ➢ Common interface to other systems

Motivation & Detector Background



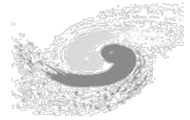
- **Vertex (CMOS Sensor)**
- **Tracker**
  - ➢ Inner Tracker (ITk): Si Pixel Tracker (HVCMOS)
  - ➢ Middle Tracker (MTk) : TPC / Drift Chamber
  - ➢ Outer Tracker(Otk): Si Strip / LGAD-TOF / Pixel (HVCMOS)
- **ECAL & HCAL**
  - ➢ Crystal bar / Stereo crystal / Plastic scintillator / SiW / Glass / RPC …
- **Muon**
  - ➢ Plastic scintillator / RPC





By Ji Q.

Elec-TDAQ overall framework



Trigger System

Electronics System

Clock Synchronization & distribution

Vertex | MAPS
Tracker | HVCMOS
TPC | ASIC
DC | ASIC
CAL | ASIC
TOF | ASIC
LumiCal | ASIC

Data Link & interface

Data Aggregation

Data buffering

FPGA Algorithm (Compression, Patterning, Machine Learning,…)

Command & Slow Control

Data Packaging & Transmission

DAQ system

FEE

Interface

Backend Electronics

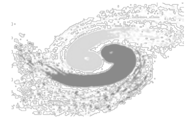
Power Management

Mechanics & Cooling

- **Two main recent targets:**

1. **To collect the detailed requirements from all sub-dets**
2. **To define the preliminary readout frame & strategy of Elec-TDAQ**

Renew of the detector key requirements

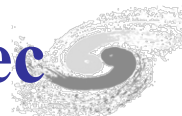


	Vertex	Pix Tracker	TOF	Si Strip	TPC	DC	CAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT
Channels per chip	500k Pixelized	50k Pixelized	128	128	128	-	16
Ref. Signal processing	XY addr + BX ID	XY addr + timing	ADC + TDC / TOT+TOA	Discri.	ADC + BX ID	Ultra fast PA + ADC	TOT + TOA/ ADC + TDC
Main challenge for FEE	• Small pixel size • Fast readout • Low power	• Large area • Cost effective • Low power	• ~50ps timing		• Low power • High density integration	• Ultra fast PA • Ultra fast ADC	• ~10^5 dynamic range • ~400ps timing • Huge channel Low power
Data rate for FEE	160Mbps/chip @Trigger Innermost	~30Mbps/chip Innermost	<kHz/chip	<kHz/chip	~70Mbps/module Innermost	~500Mbps/module /a sector	<100MHz/module

- **Data rate already in conjunction with the preliminary FEE module consideration**
- **Background still under fine calculation, only a rough level of data rate can be given**
- **Muon FEE proposed to be compatible by using the ECAL FEE ASIC**
- **LumiCal proposed to reuse the design from SiPM readout and CMOS pixel detector**

Thanks for the discussion of Liang ZJ, Li YM, Qi HR, Dong MY, Shi X, Liu Y, Zhang L., Wang XL., et al.

Proposal of general readout strategy of CEPC Elec



FEE(Customize)
Rad-hard

FEE-ASIC
FEE-ASIC
FEE-ASIC
FEE-ASIC

Data aggregation (ASIC)

Data interface (GBTx-like)

Optical Module

DC-DC - LV 1.2/2.5V

DC-DC - MV 12/48 V

FEE-0

Fiber (Only)

Power Cable

Fast Trg for VTX(?)

Trigger Comm-Brd

Most Trg

BEE Comm-Brd

DAQ

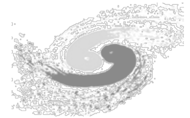
Slow Ctrl

Non Rad-hard

Common platform

- **(Ideally) 1 Power Cable + 1 Fiber for all sub-det FEE module**
- **Almost backend trigger, all frontend raw data can be send-out (frontend triggerless, except VTX)**

Elec scheme - Vertex



Very Long

Taichu | Taichu | Taichu | Flex | LDO | socket

socket | FPGA

Taichu Vertex Prototype @MOST2

Vertex Bracket

Not rad-hard

Vertex Bracket

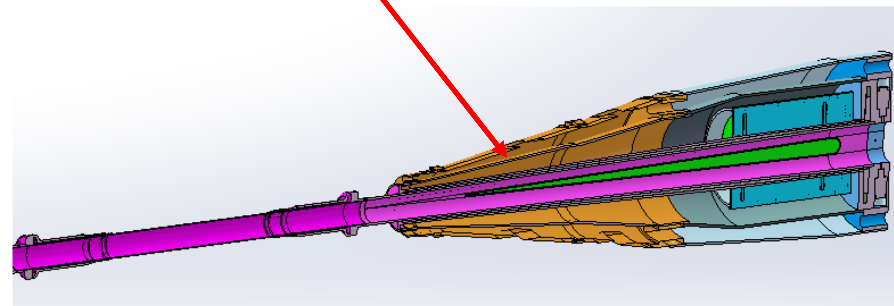
new-Px | new-Px | Flex | DC-DC | Data Aggr. | Data Link

Pwr Cable

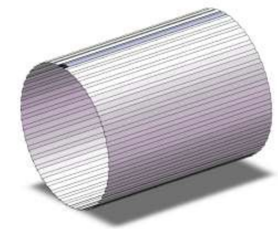
Fiber to BEE

CEPC Vertex Electronics on Ref-TDR

- **Q: height & area & power limit for power & optical module**
- **Q: (probably the only sub-det) need fast trigger to save power & data rate**
- **Q: proposed to design two sized chips for optimized layout of Inner / Med+Outer layer**



Elec scheme – Silicon Tracker



Ladder
L=5.8m
R=1.8m

Stave
Flex < 1m

Power
Fiber
DC-DC
Aggr.
Optical

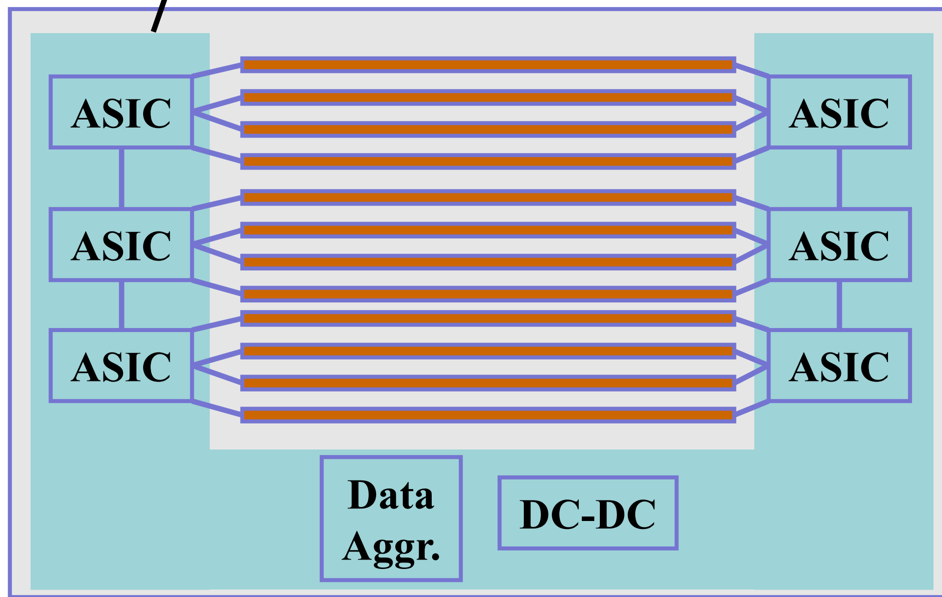
Flex

Module ~10cm

Aggregation Brd @ Stave

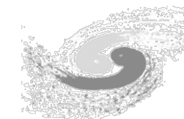
- Data Aggregation → Optical
- Lvl 2 DC-DC & power fanout
- Clocking fanout for TOF

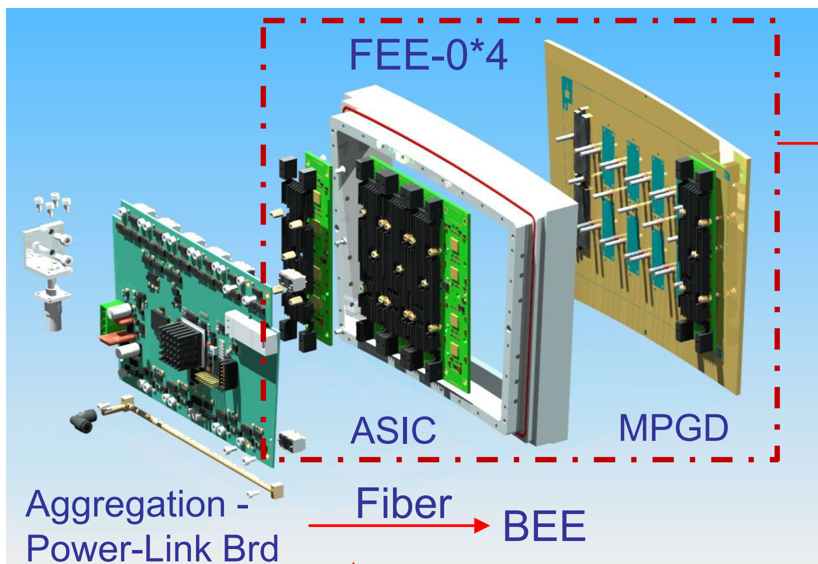
FEE
PCB
@
Module

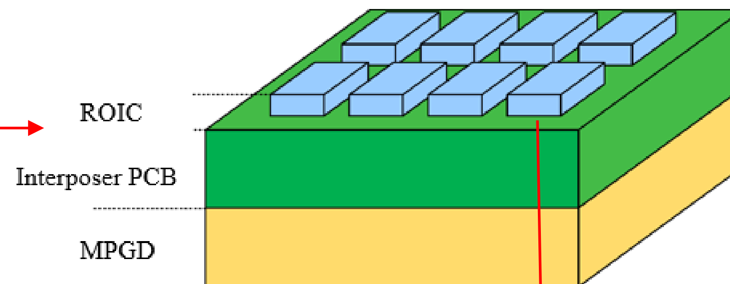


- **Si Pixel Tracker, TOF, Si Strip, can all be compatible with the readout framework**
- **1 Pwr + 1 Fiber for each stave**
  - **Data rate: Mostly < 1Mbps/stave**
  - **~ 30Mbps for SIT Innermost**
- **For high precision timing, clocking fanout needs careful thinking**

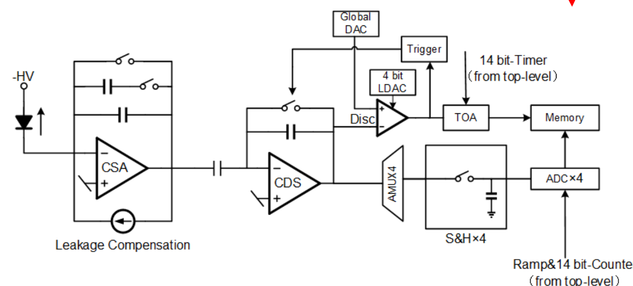
Preliminary readout scheme of Pixel TPC

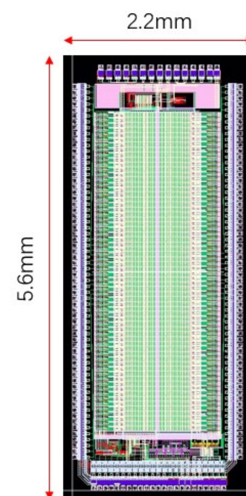




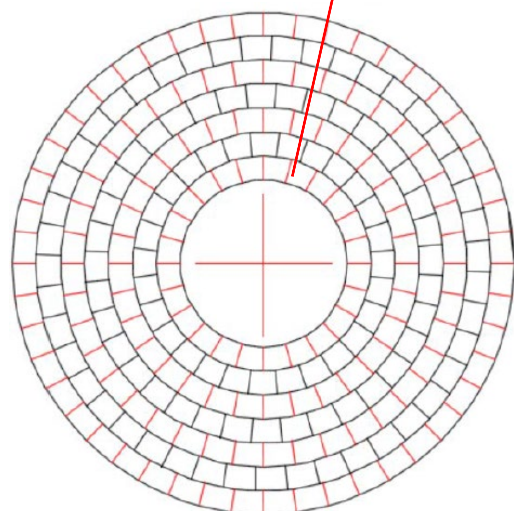


An integrated board with ASIC & MPGD, N(now 4) for a module
0.5mm*0.5mm / pixel





128 chn ASIC, Q+T measurement
142.8k pixel/module → 1115 chip/module→ 279 chip/FEE-0

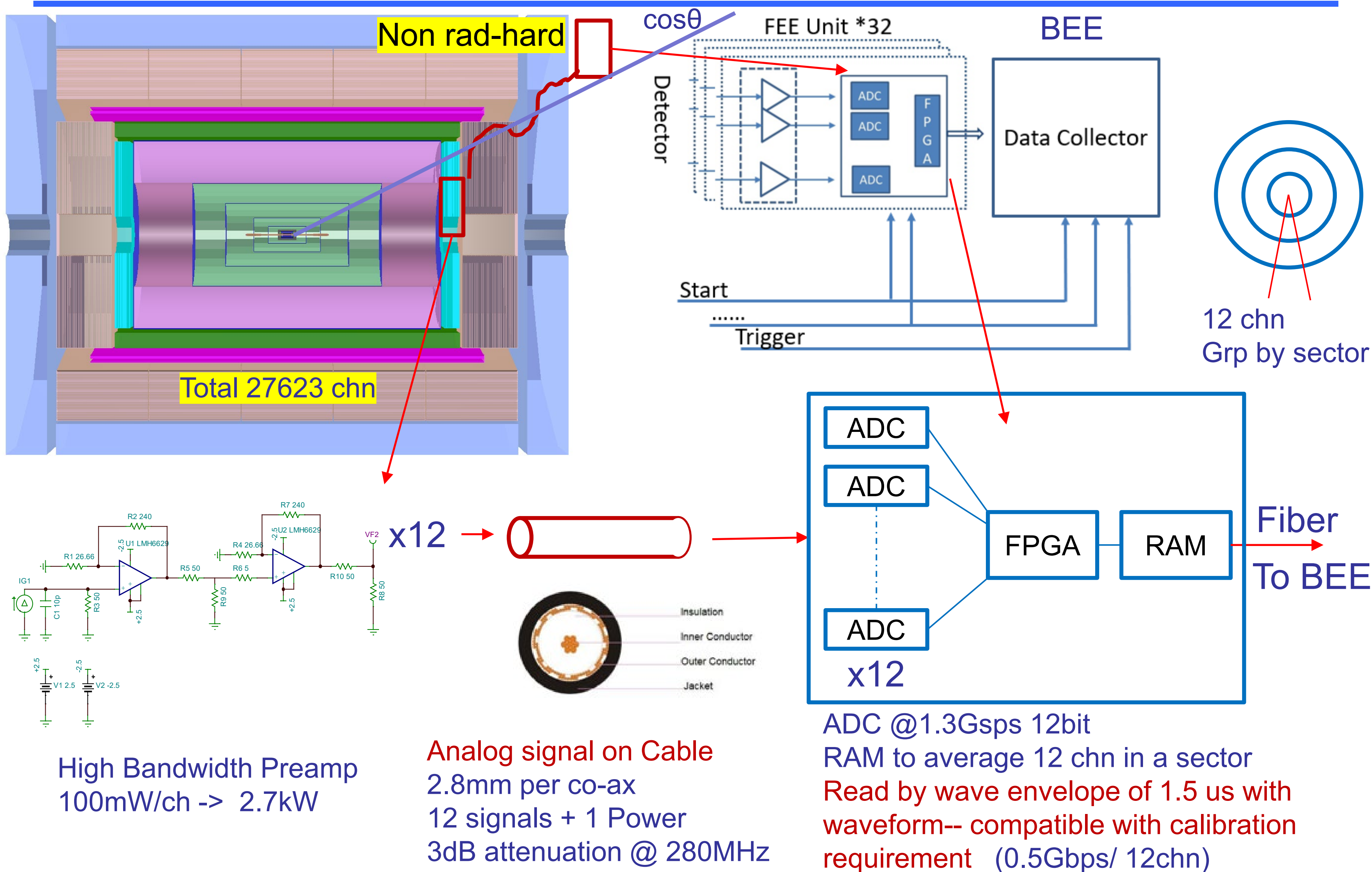


~258 Module/Endplate

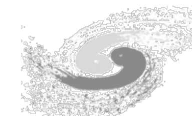
Power:
Limit: <10 kW/endplate ~ 39.7 W/module ~10 W/FEE-0
35mW/ASIC ~ 280μW/chn

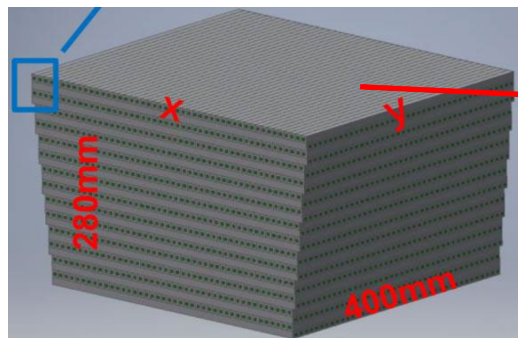
Data rate:
80 particles/BX, 12,000 hit/particle, 32(48)b/hit, @ 40M BX Z pole
1 Module: ~100 Mbps(@ innermost)

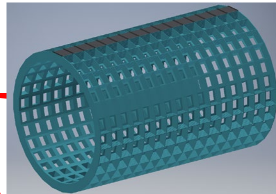
Preliminary readout scheme of Drift Chamber

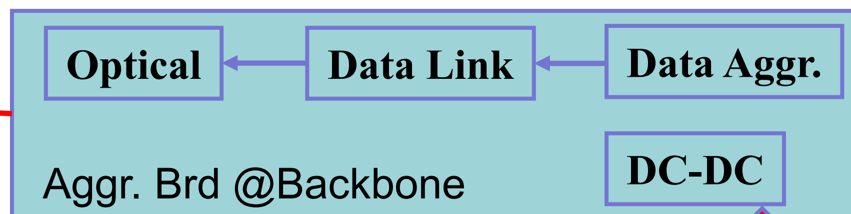


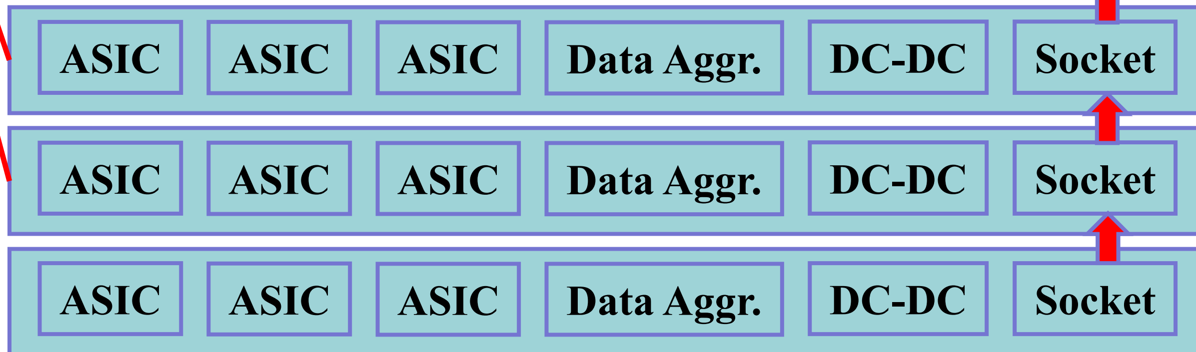
Elec scheme – ECAL



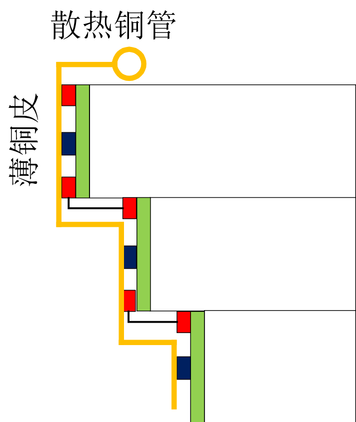




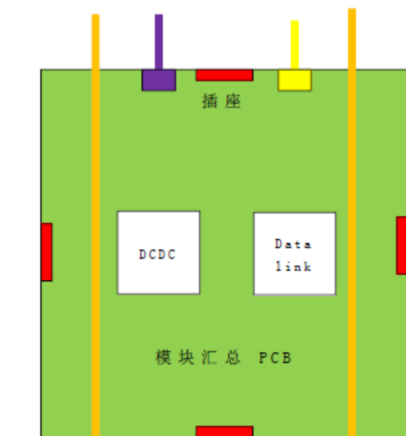




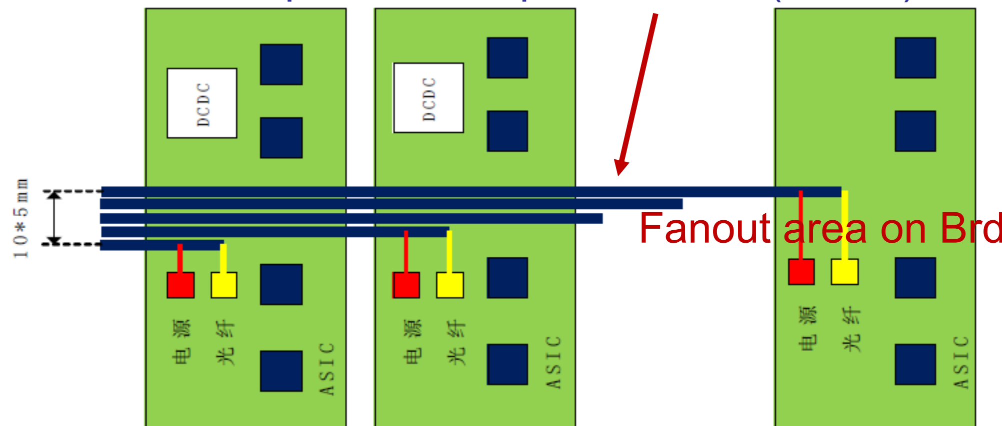
- Q: limited room for fanout & DC-DC module
  - ~ 5mm height
- Q: limited heat dissipation capacity
  - Proposed by Cu tube & sheet ?



FEE Brd @Side

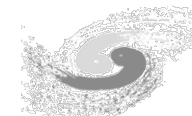


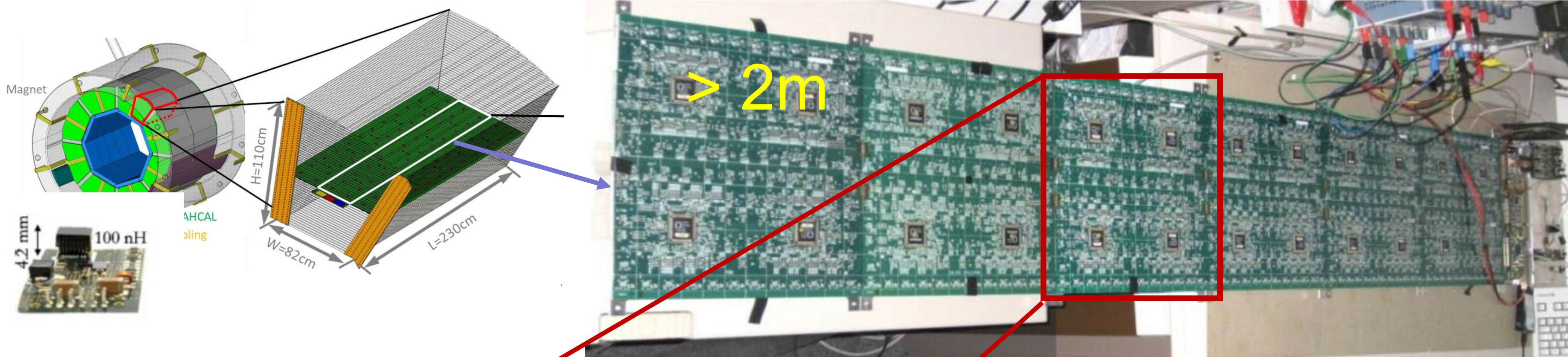
Aggr. Brd @backbone



Barrel fanout @half barrel

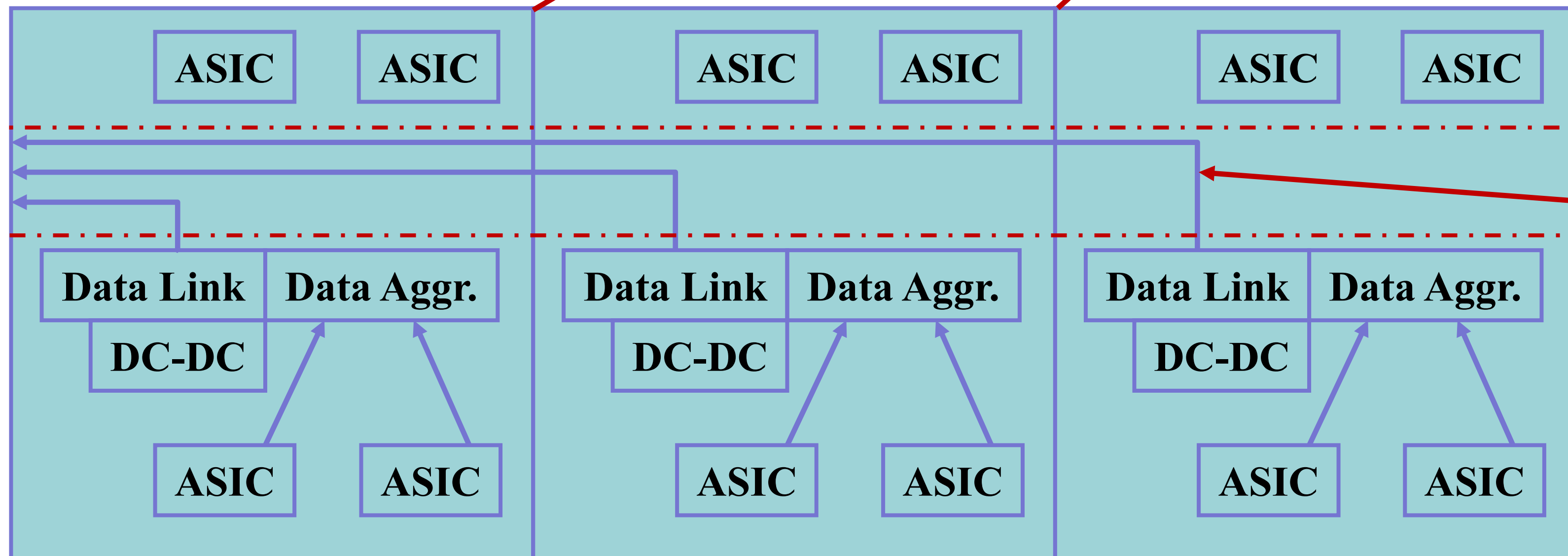
Elec scheme – HCAL





Glass+SiPM evenly distr. on the top side

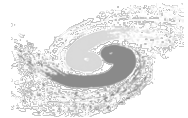
Indep. Brd w/o inter-conn.



Fanout area by opt-elec composite cable

- **Q: high challenge on limited height: 6.7mm including PCB (height of power (ind) & optical & cable)**
- **Q: heat dissip. proposed to rely on the absorber (issue: the Elec is fully at backside)**

Elec scheme – Muon



闪烁体探测器

Muon探测器前端定制电子学

接口

调理放大（CSA）

ADC_ch0

接口

调理放大（CSA）

ADC_ch1

温度补偿

Channel：2

Channel：3

Channel：63

Power

Power

电源模块

时钟，触发模块

FPGA

能量测量

数据组包

能量信息

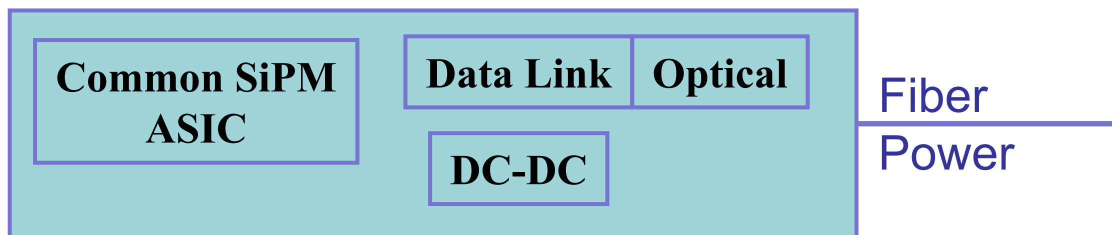
时间信息

脉冲相位处理模块

相位拟合算法模块

时差提取模块

Muon Elec R&D

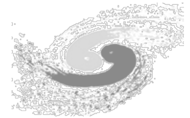


Fiber

Power

CEPC Muon FEE

Common framework on Data Link



Down Link
TX
TX
TX
Decode
Deserializer
CDR
Timing & Trigger
DAQ
Slow Ctrl
Up Link
RX
RX
RX
Phase Aligner
Encode
Serializer
Configuration
PLL
Bi-Direction Data Interface

TIA
PD
Laser Driver
LD
Optical Module

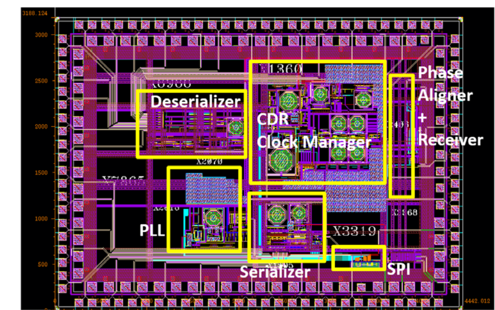
Fiber

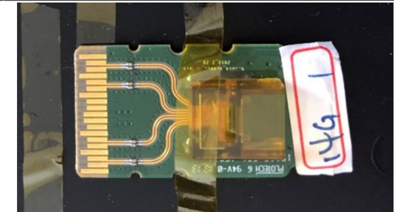
FPGA
Timing & Trigger
DAQ
Slow Ctrl
Backend Electronics

On-Detector
Rad-hard Electronics

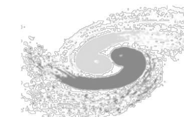
Off-Detector
Commercial Off-The-Shelf

- **Propose to develop a GBTx-like platform as the common communication interface for all the sub-det.**
- **Module height & size are constrained from some key detectors (Vertex & CAL)**
- **Radiation tolerance comes from the innermost Vertex to be O(Mrad/y)**
- **R&D showed preliminary feasibilities for the key blocks, detailed protocol to be defined**





Common framework on Power



Detector Hall | Elec room

CUST PoI module + CUST Power Ctrller ← 48V/12V DC, 20m ← CUST DC-DC Power Crate ← 280V DC, 100m ← Commercial Power Supply ← 480V AC

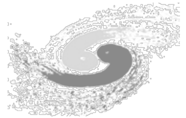
1M rad | 10~100k rad | 0 rad

1.2V/1.8V DC ↓

FEE Powering (TBD） → Serial Powering / LDO…?

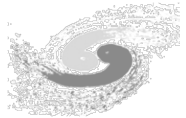
- Propose to develop a rad-hard power module series as the common platform for all sub-det
- Module height & size are constrained from some key detectors (Vertex & CAL)

Summary on current framework



- **Detectors can almost still keep with "triggerless" feature**
  - All FEE raw data go to BEE losslessly
    - ➢ Except for the (innermost) Vertex
  - Trigger will almost communicate only with BEE
    - ➢ "Backend trigger" based
    - ➢ Both hardware / software trigger still possible
    - ➢ Still needs special consideration on Vertex (how to generate Fast Trg)
- **All FEE module based on a similar framework:**
  - ASIC – Aggr. – Data Link – Fiber + DC-DC – Pwr Cable
  - Minimized the module interconnection design, maximize the common platform design for BEE + Trigger
    - ➢ A highly compact & scalable system
  - Based on a successful design of GBTx-like chip & rad-hard DC-DC module
    - ➢ Size & height of the optical & DC-DC modules still with high challenges
    - ➢ Backup plan if failed: back to the cable based architecture

Future Plan towards the Ref-TDR

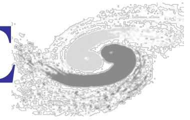


- To conclude and converge into a preliminary scheme for the Ref-TDR
  - Review the detector inputs on data rate
    - ➢ Conclude with limited data rate nodes for the Data Link
  - Review the power and voltage requirements
    - ➢ Conclude with limited number of DC-DC design
  - To define the Elec-Trigger framework
  - To refine the FEE-ASIC design for each sub-det
- Some key R&Ds are urged to initiate
  - Rad-hard powering & link
  - Key ASICs which are currently absent (SiPM FEE, Strip LGAD)
- Prepare for additional backup and innovative schemes
  - To evaluate the possibility by using wireless communication
    - ➢ See Jun Hu's talk

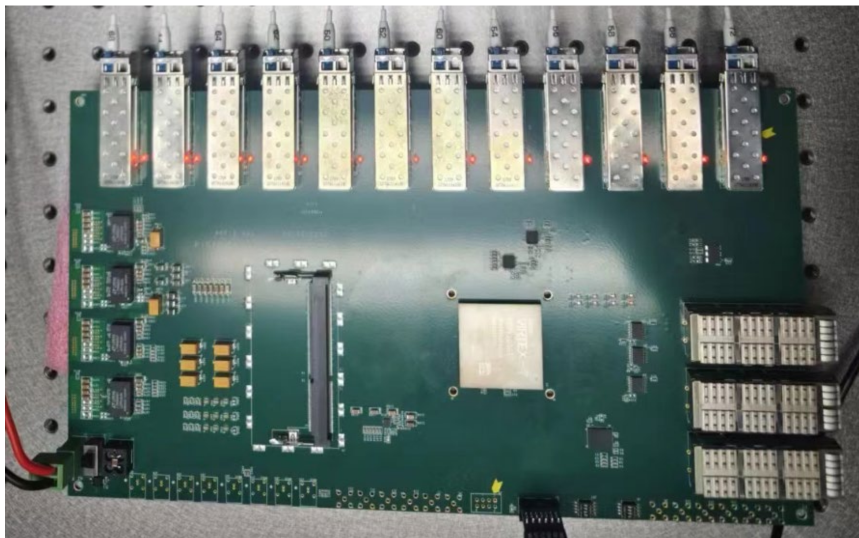
Thank you!

Backup

Preliminary consideration on common BEE

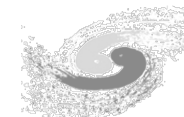


	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory(Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	



- **A common station for fibers from FEE**
- **Providing data buffers till trigger comes**
- **Possible calculation resource needed for trigger algorithm**
- **Number of IOs, port rate & the cost are the major concerns**

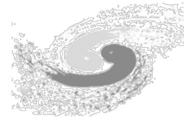
Specification calculation- from hit density



		Hit density (Hits/cm^2/BX)	Bunch spacing (ns)	Hit rate (M Hits/cm^2)	Hit Pix rate (M Px/cm^2)	Hit rate/chip (MHz)	Data rate@triggerless (Gbps)	Pixel/bunch	FIFO Depth @3us rg latency	Data rate@trigger (Mbps)
CDR	Higgs	2.4	680	3.53	10.59	34.62	1.1	23.5	103.9	105.28
	W	2.3	210	10.95	32.86	107.44	3.4	22.6	322.3	101.248
	Z	0.25	25	10	30	98.1	3.1	2.4	294.3	53.76
TDR	Higgs	0.81	591	1.37	4.11	13.44	0.43	7.96	40.4	0.017
	W	0.81	257	3.16	9.45	30.90	0.98	7.96	92.8	3.6
	Z	0.45	23	19.6	58.7	191.9	5.9	4.4	575	118

- **TDR raw hit density: Higgs 0.54， Z 0.3; Safety factor: TDR 1.5, CDR 10;**
- **Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)**
- **Area: 1.28cm*2.56cm=3.27cm^2 (@pixel size 25um*25um)**
- **Word length: 32bit/event (@Taichu's scale, 512*1024 array)**
- **Trigger rate： 20kHz@CDR， 120kHz@Z, 10Hz@Higgs, 2kHz@W TDR**
  - **Trigger latency: 3us(very likely not enough), Error window: 7 bins**
  - **FIFO depth: @3us * hit rate/chip**
  - **Data rate=pixel/bunch*trigger rate*32bit*error window**

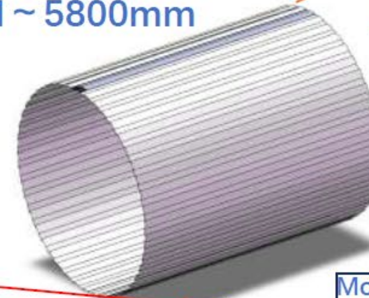
LGAD as a TOF @ Outer Tracker

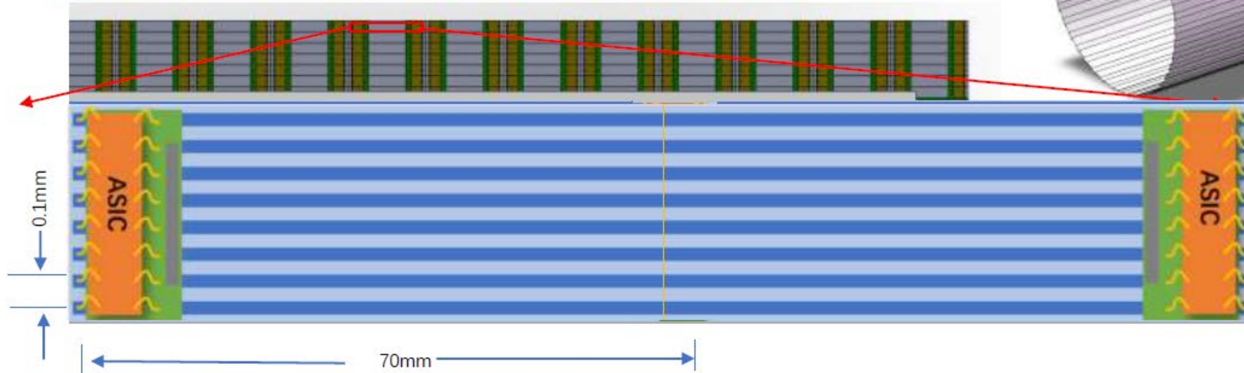


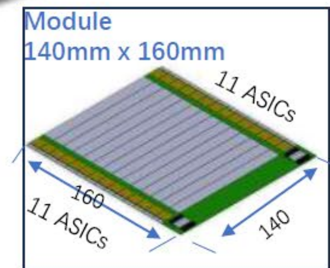
- One layer:
  - 90 ladders, 45 ladders each side,
    - 42 modules/ladder
      - 22 ASIC/module
        - 128 channels/ASIC
- Total modules needed:

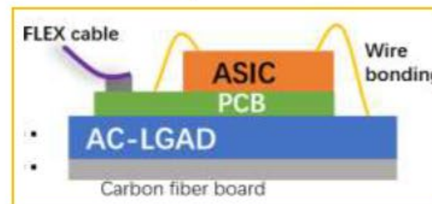
  45 *2*42 = 3780 modules

One layer ToF
R= 1800 mm
H ~ 5800mm

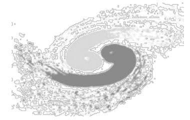




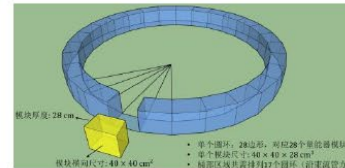




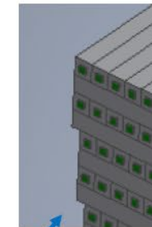
ECAL



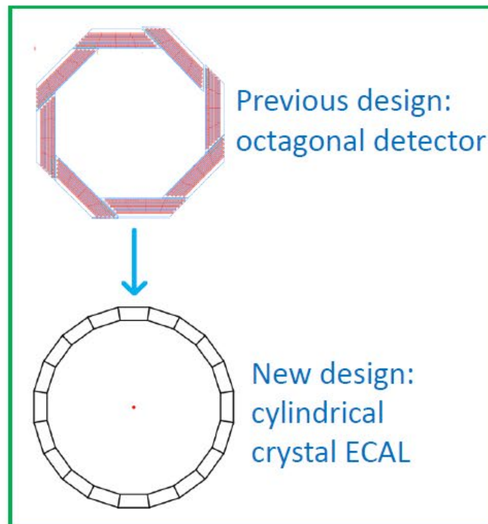
- CEPC crystal ECAL barrel geometry design
  - Finer segmentation of towers for better homogeneity
  - Decrease outer radius for lower cost of the outer detectors
  - 28 towers per ring, 17 rings along beam direction
  - ~25 radiation length: 28 layers

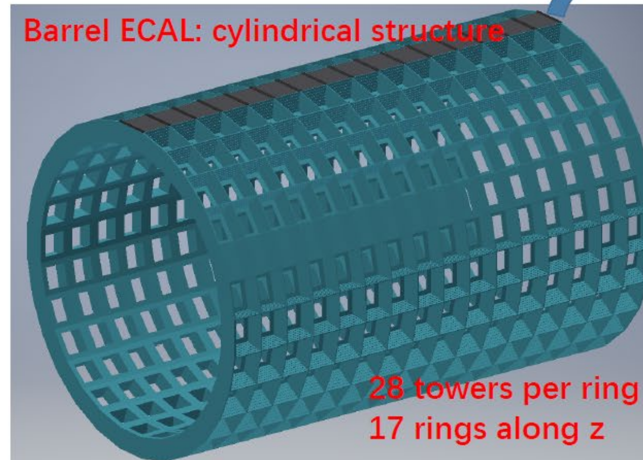


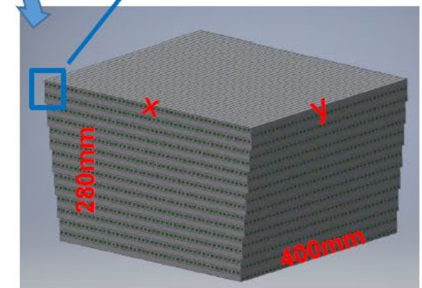
Quan Ji, Chang Shu (IHEP)



4 layers per "step" with the same transverse size







Key questions
- Space for electronics and cooling
- Assembly