SiW-ECAL overview

Entretien Annuel Projet CALICE/ILD

21/10/2019

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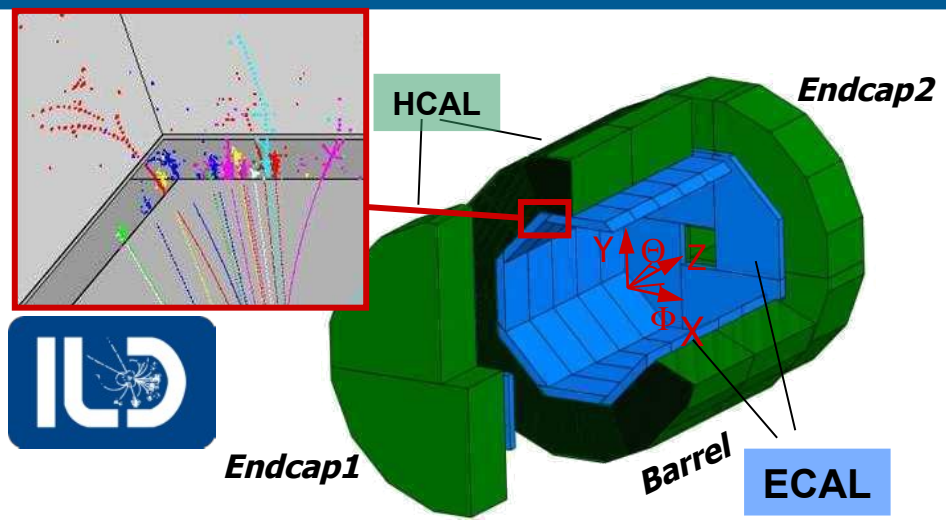
TNA support + WP14

An Ultra-Granular SiW-ECAL for experiments



Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (*E, (θ,φ), t*)
- PFlow requirements:
  - Extremely high granularity
  - Compacity (density)

SiW+CFRC baseline choice for future Lepton Colliders:

- Tungsten as absorber material
  - X_0 = 3.5 mm, R_M = 9 mm, λ_I = 96 mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - **Support compact design: Sensor+RO≤2-3mm**
  - Allows for ~any pixelisation
  - Robust technology
  - **Excellent signal/noise ratio: ≥10**
  - **Intrinsic stability (vs environment, aging)**
  - **Albeit expensive…**
- Tungsten–Carbon alveolar structure
  - **Minimal structural dead-spaces**
  - Cooling, Power Distrib, DAQ
- **Scalability**

To be assessed by prototypes

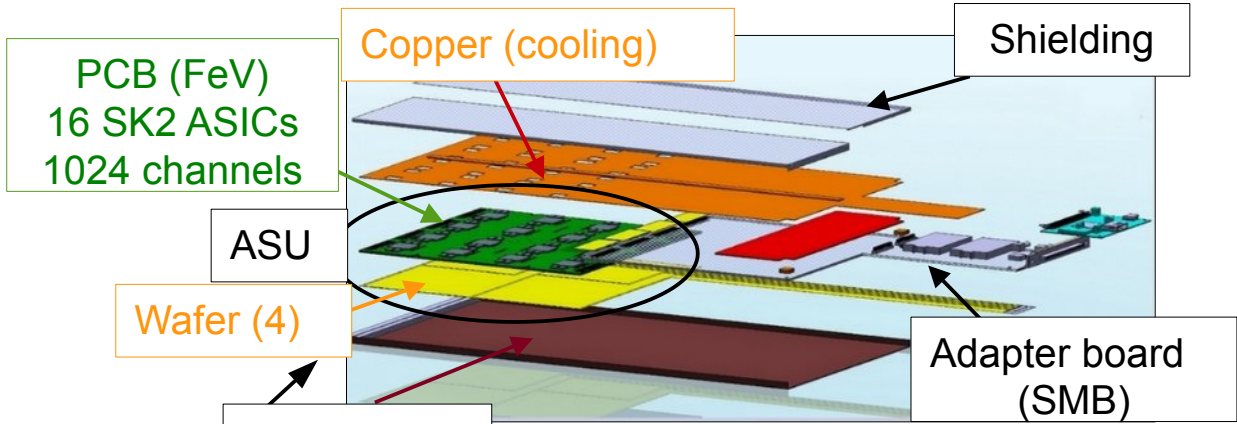
SiW-ECAL Building blocks: SLAB's & ASU's

R&D for "mass production" and QA

- Quality tests & preparation of large production
- Modularity → ASU & SLABs
- Choice of square wafers
  - (≠ from hex: SiD, CMS HGCAL)

Numbers (R_{ECAL} = 1,8 m, $|Z_{Endcaps}|$=2,35m)
(likely to be reduced by 30–40%)

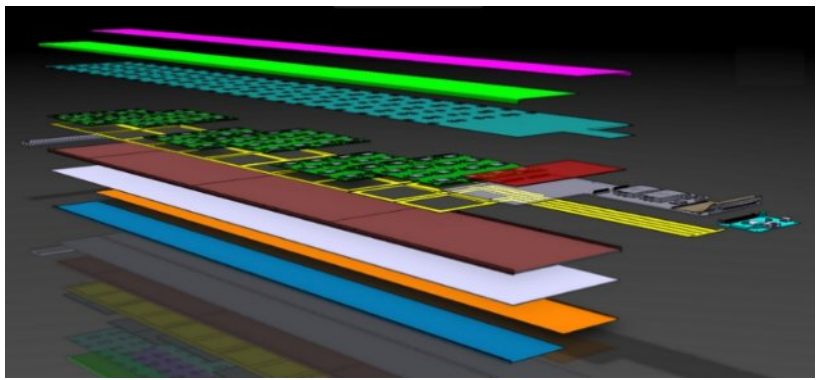
- Barrel modules: 40 (as of today all identical)
- Endcap Modules: 24 (3 types)
- ASUs = ~75,000
  - Wafers ~ 300,000 (2500 m²)
  - VFE chips ~ 1,200,000
  - Channels: 77Mch
- Slabs = 6000 (B) + 3600 (EC) = 9600
  - ≠ lengths and endings



U layout of a **short slab**

Tests of producibility (15)

Tests of feasability (1/4)

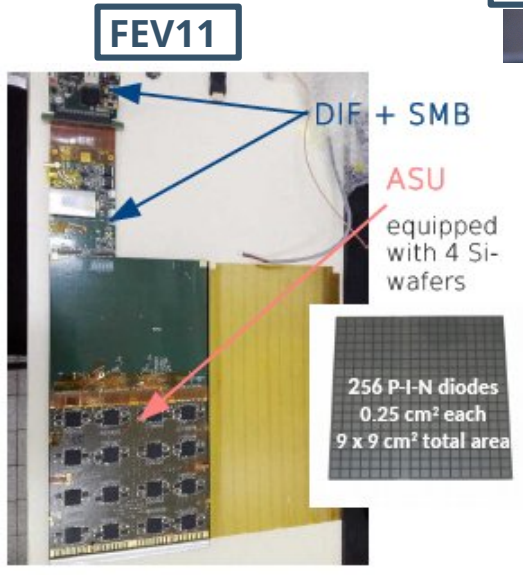


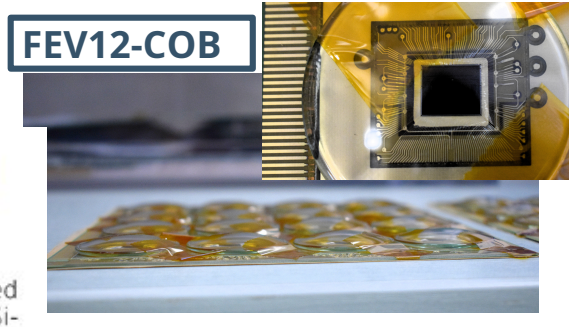
U layout of a **long slab**

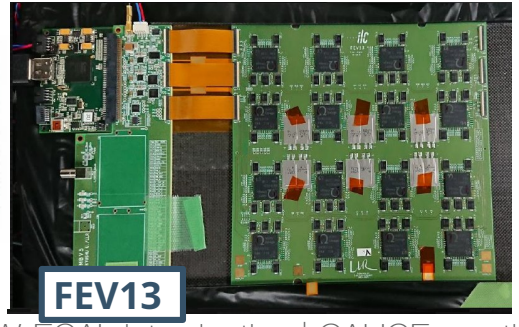
ASU: 12⁺ years of R&D

Most complex element: electro-mechanical integration

- Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints





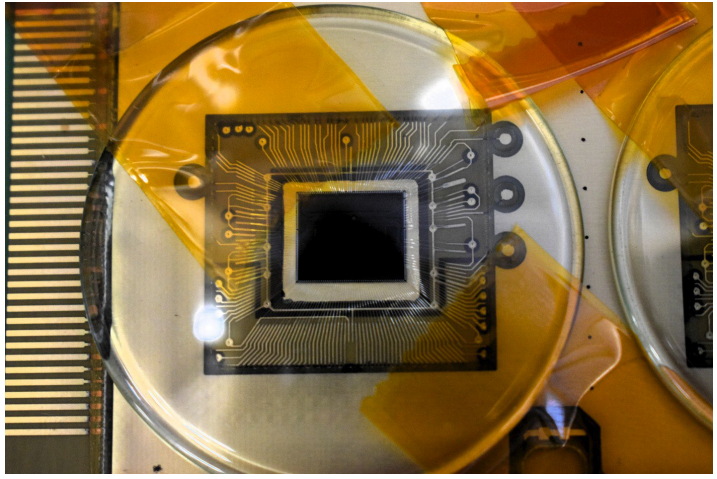


Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	Slab:FEV11	10 units, 320µm	
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 $(12)_{Trig,}$ 6–8 % masked
1st technological ECAL	2018	10 SLAB: 5 FEV11 320µm 5 FEV13 650*µm Compact stack	SK2 & SK2a (⊃timing)	Improved S/N (1/64 masked ch.) Timing...
1st COB	2019	FEV12-COB	1 wafer, 500µm	S/N ~ 22

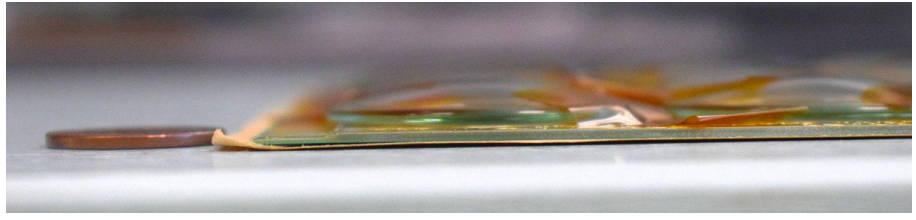
Highlight from 2019 (1)

FEV-COB

- 2 FEV12-COB, SK2a with one 6'' wafer × 500µm
  - long standing work from **LAL+Omega** + SUNG KYUN KWAN UNIVERSITY(SKKU) EOS CORPORATION
  - 1.2mm, 9 layer PCB
  - Good planarity (metrology made in LAL)
  - No extra components on board
  - 4 boards wirebonded at CERN



- 2 FEV12-BGA, SK2a with one 6'' wafer × 500µm

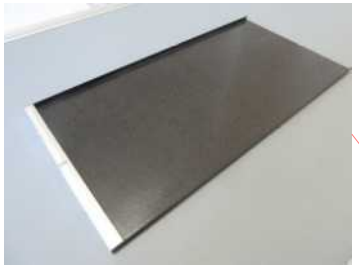


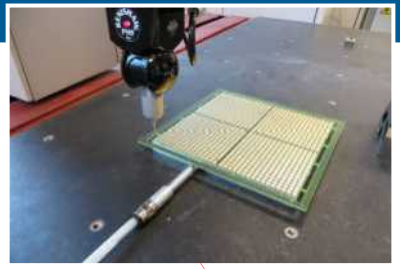
- Gluing @ LPNHE with 100% controlled Wafers pro & post-gluing

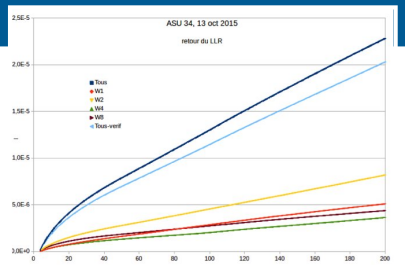
Connections to SL-Board made by GradConn connectors

Assembly chain Paris

To be improved and extended







‘Simplified view’

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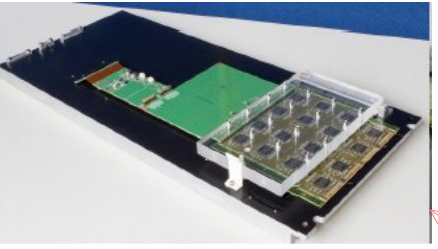
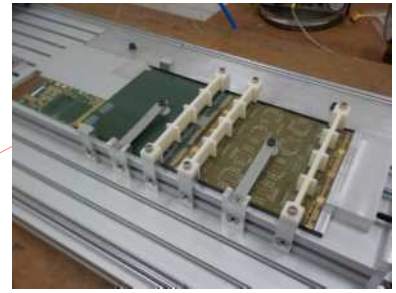
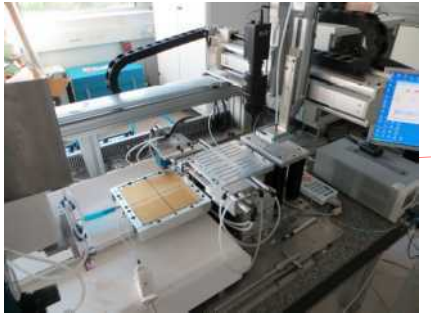
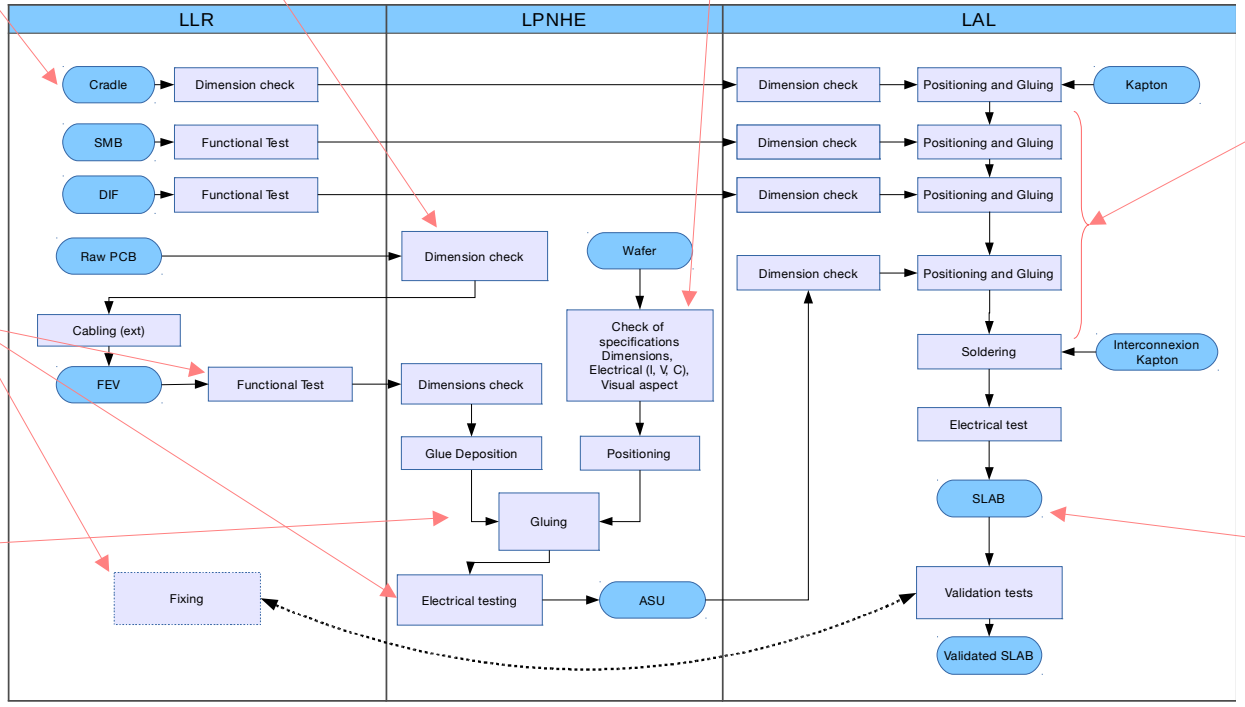
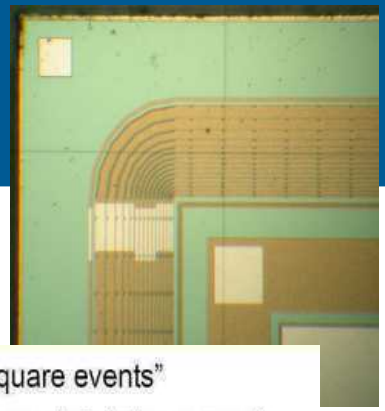


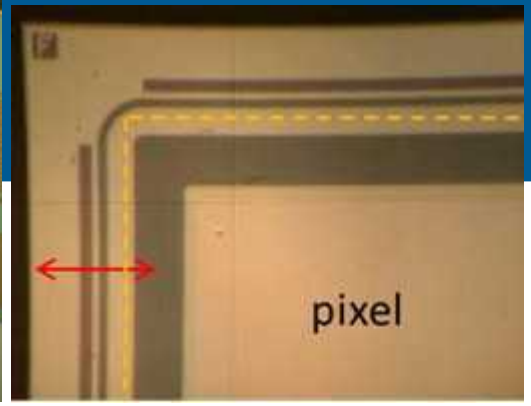






Silicon Sensors

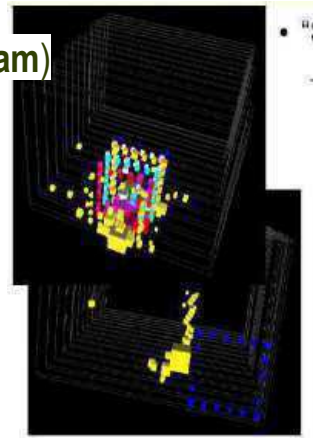




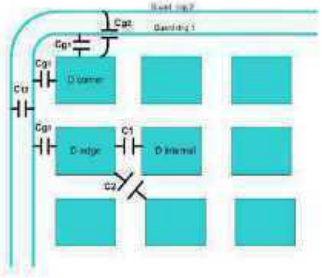
Cost driver

- ~30% of the total cost of the SiW-ECAL
  - ⇒ Units Cost reduction(**CALIIMAX ANR program**)
- Decoupling of Guard Ring (Square Events).
- new design of ILD detector

Wafers glued onto PCB's

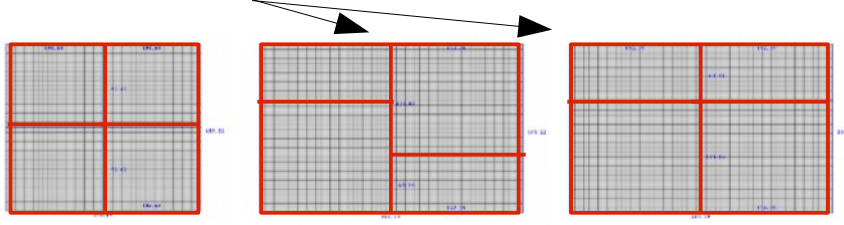


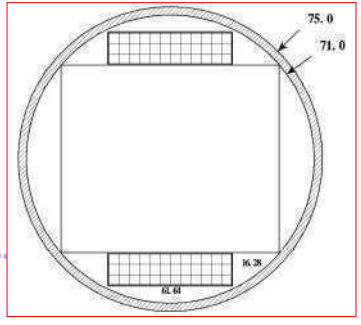
- "Square events"
  - cross talk between guard rings and pixels



Command Sensors (@ Hamamatsu)

- ⚠ Minimal cost of Command ≥ 20k€
- direct contact with HPK engineers
- Possibility of design for 8" in 186mm alveoli **320, 500, 650** → 725 µm ?





'quantum unit' of ILD dimensions (here 6" wafer)

ASU's: brief overview

ASU's

- FEV11, 7 boards (+1 ?), 320 µm, SK2
  - DESY-2017, CERN -2018,
    - $S/N_{ADC} \sim 20^{+}$; $S/N_{Trig} \sim 12^{-}$
- FEV13, 5 boards, 4×650µm + 1×320µm, SK2a
  - DESY-2018, (CERN-2018), DESY-2019:
    - Prelim: $S/N_{ADC} \sim 50$ for 650µm, small Δ Fr vs Jp PCBs
    - Prelim: $S/N_{ADC} \sim 21$ for 320µm
    - Prelim: But time dependance on ped stability ?
- FEV12 & FEV12-COB: (2+2 boards) × 1/4th equipped, SK2a, 500µm
  - DESY-2019 ⇒ COB: promising results
    - Prelim: $S/N_{ADC} \sim 24^{+}$
    - no ch37 pbm
    - no PP

e–Long Slab

- FEV11, 1/64th equipped
  - Required HV decoupling ⇒ Noise prop between ASICs through wafer / HV ?
  - Dependancy on positioning and ASIC seen (TBC) ⇒ opt. power scheme ?

Wafers:

- Sq events 1/10 of physics prototype (DESY-2015)
- Huge gain in signal with 650µm wafers. Effective depletion thickness ?
- 8'', 750µm wafers: when ?

Significant progress but … room for improvement

Are we up-to ILD requirements ?

- Noisy ch37 ? Not seen in COB… ⟶ new packaging ?
- Retriggering by ChipSat ⟶ better decoupling ?
  - only a pbm if noisy channels… but…
- Powering: stability (FEV13 ?), min. ON period, …
- ONLY Low-E performances ⇒ **DAQ, PFA**

Highlight (2): A new DAQ for ILD (and CALICE ?)

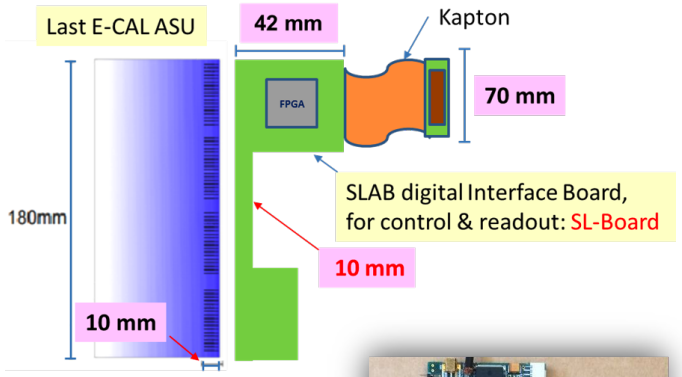
D. Breton, J. Jeglot, J. Maalmi, P. Rusquart, A. Saussac (SERDI ,LAL)

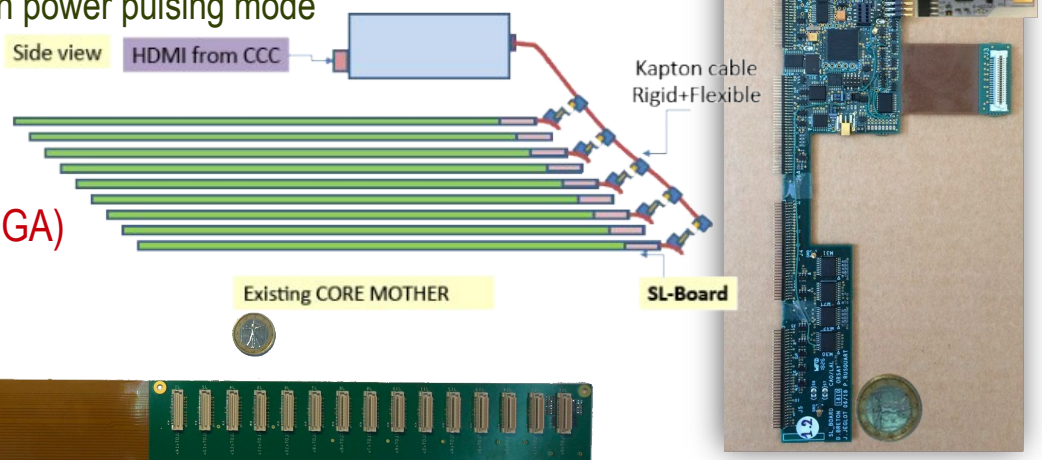
ILD spacing constraints:

- between ECAL and HCAL: 67 mm
  Height ≤ 6 to 12 mm depending on the location
- L-shape because of the cooling system
- Control & Readout electronics at the extremity of the Slab
- Signal Integrity over a Slab: up to 8–12 interconnected ASUs (200 ASICs, ~10,000 ch)
- Very low Power consumption(~ 150 mA/ Slab) : needs to run in power pulsing mode

New HW: **SL-Board**

- Regulated PS: HV and LV + monitoring (ADC)
- Controls ASICs & perform RO: ALTERA MAX10 (CPLD+FPGA)
- Connection to CoreModule by single Kapton 40-pin cable
- Low power (<1W)



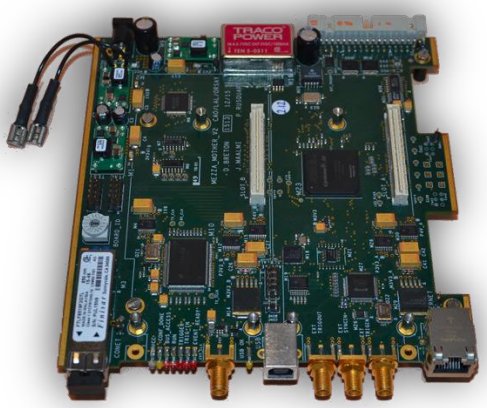


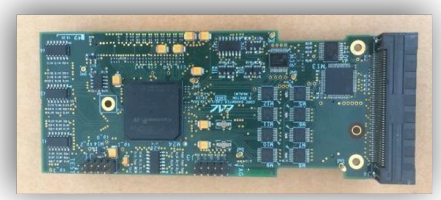
A new DAQ for ILD (and CALICE ?)

D. Breton, J. Jeglot, J. Maalmi, P. Rusquart, A. Saussac (SERDI ,LAL)

Core Mother:

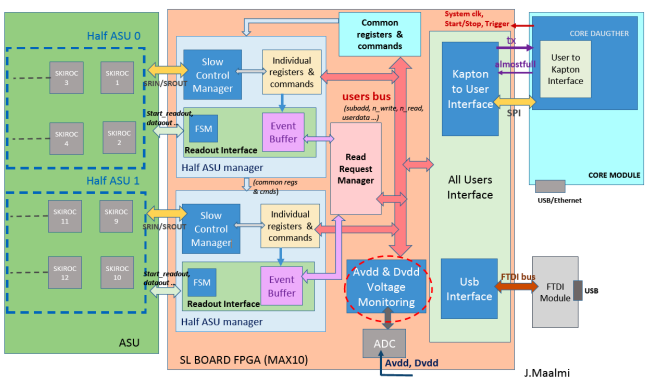
- "generic" Control & Readout MotherBoard ⇒ DAQ + Clock
  - External input * Outputs for sync.
  - 5W consumption
- + (≤2) Specific Mezzanines ⇒ FE part
- USB, UDP or Opt. links (Eth).

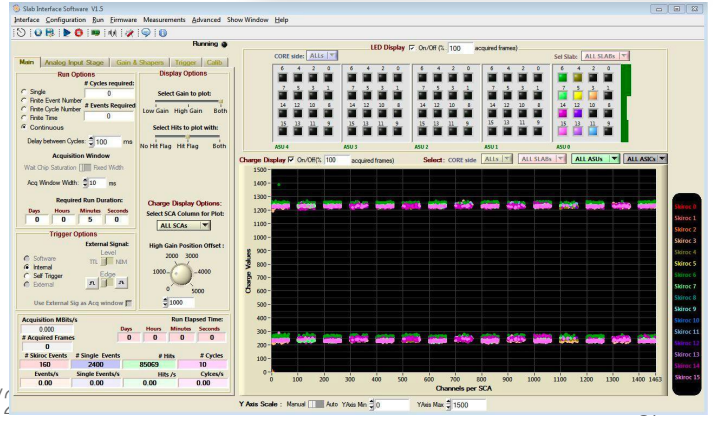




Core Daughter:

- FPGA interface + electric buffers to 15 SLABs
- Data buffers
- 125MBy/s (UDP) – 60 MBy/s (USB)





FirmWares

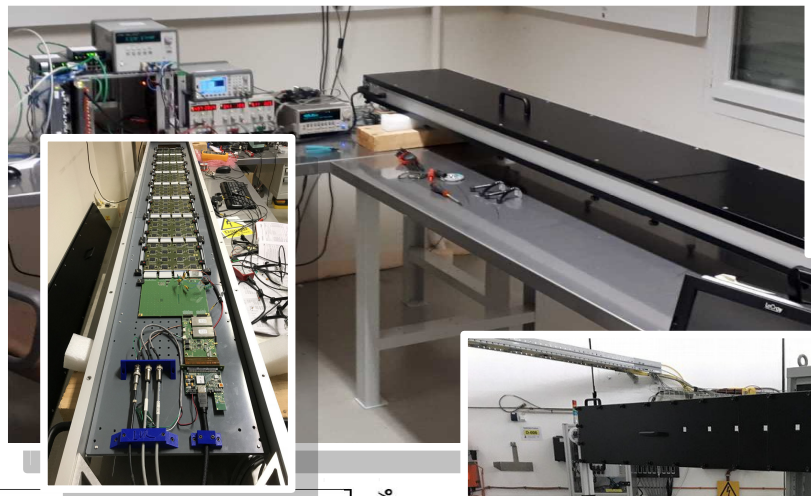
LabWindows Acquisition SW ⇐ interface to higher level: EUDAQ / Pyrame / ...

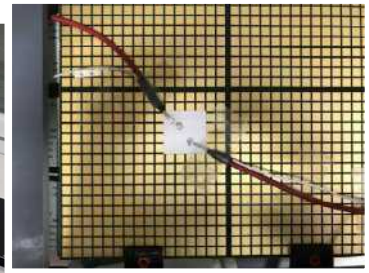
1st 'electric long slab' (2018)

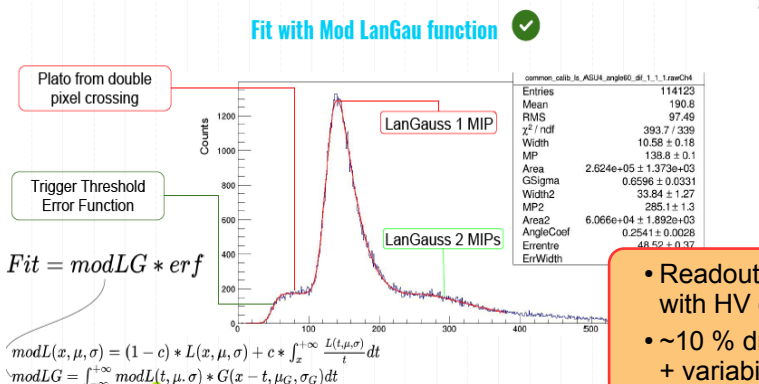
Support of interface boards + 12 ASUs (DBD)

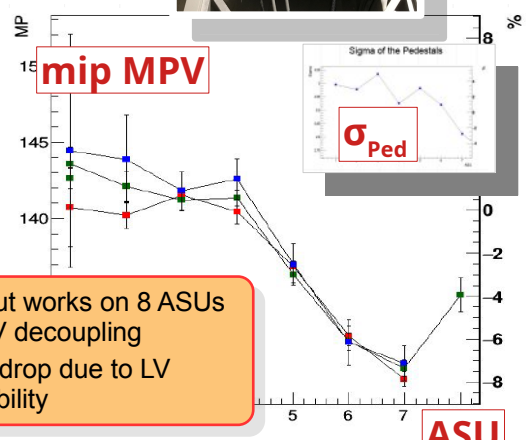
- 2+6+4 ASUs = ~3.2 m
- Rotatably along long axis (for beam test)

  Rigidity : ≤ ~1 mm per ASU
- Total access to upper and lower parts
  - 320µm Baby wafers (4×4 pixels) on the bottom







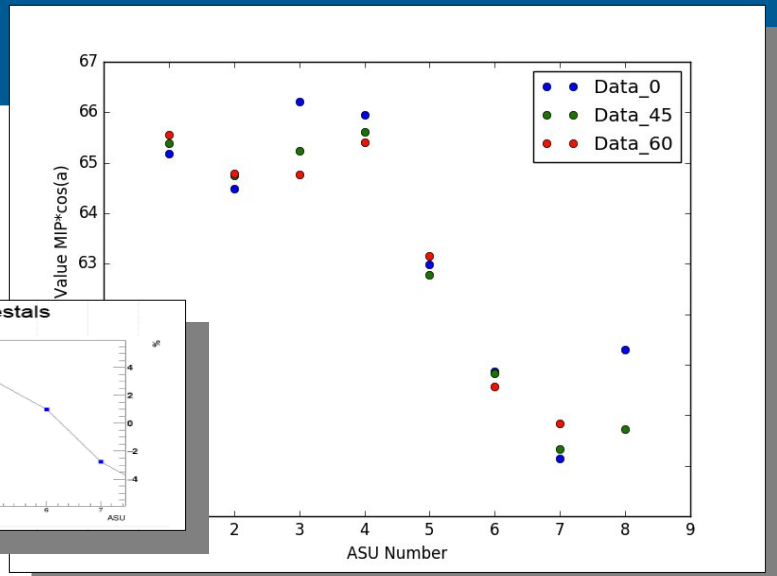


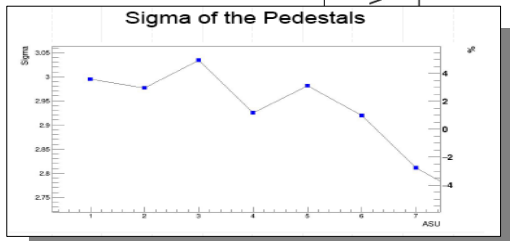
- Readout works on 8 ASUs with HV decoupling
- ~10 % drop due to LV + variability

MIP response vs position

mip MPV *cos(θ) vs ASU#

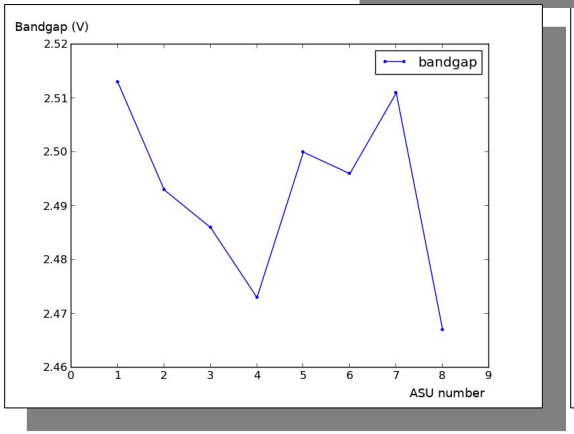
- OK for 4 1st ASU's + Small drop ~of signal ~2%/ASU for ≥ ASU#5
- Also hints similar drop on σ_{ped}



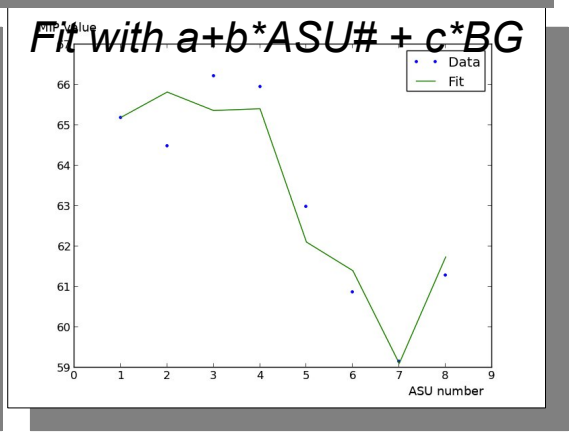


⇒ Voltage or Gain drop ?
Power pulsed mode with ballast et end of slab
or just random build-up effect from chip variability ?

- Answer: Voltage↘ + Band-gap variability
  Data fitted with
  - linear voltage drop (vs distance)
  - BG variability



*Fit with a+b*ASU# + c*BG*

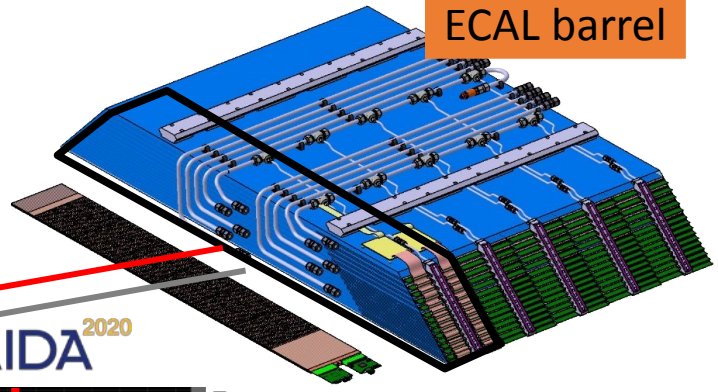


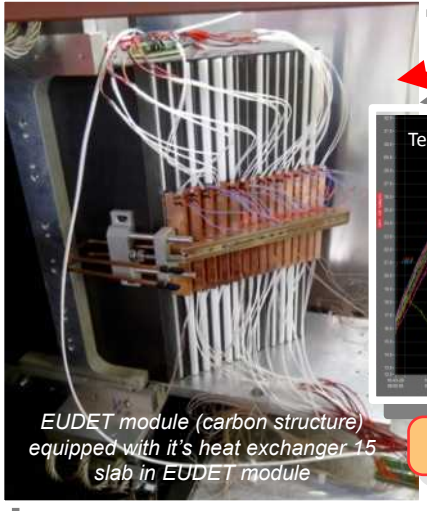
Presented @ VCI'2019; paper submitted march 2019

⊃ ack't of support from AIDA-2020 and P2IO

Rails, Cables & Pipes (Services)

ECAL barrel





EUDET module (carbon structure) equipped with it's heat exchanger 15 slab in EUDET module

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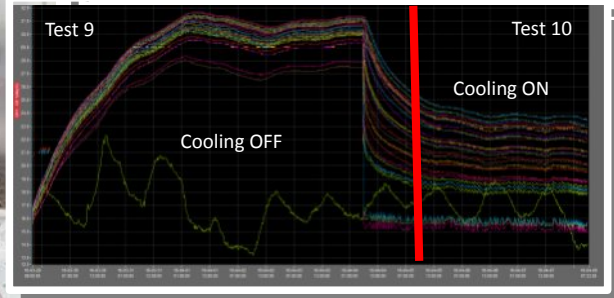
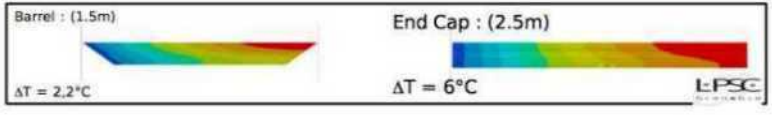
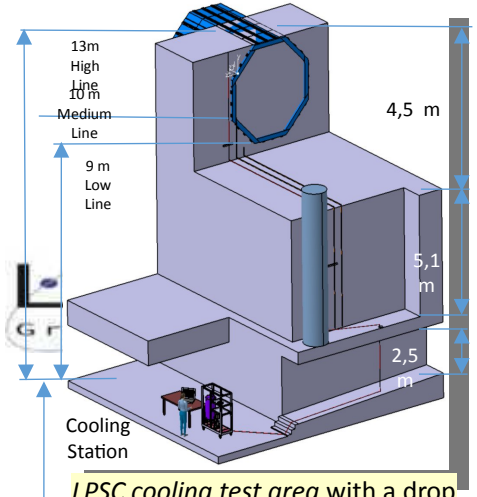


First tests results in line with simulations

ECAL end cap





LPSC cooling test area with a drop of 13 m

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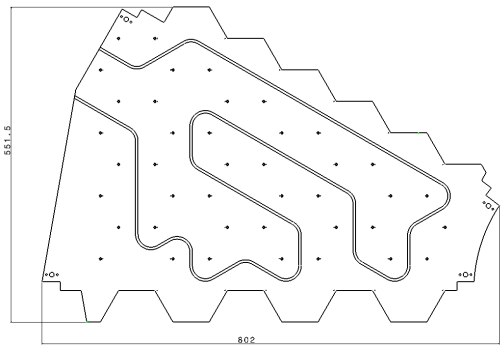
AIDA report 08/18

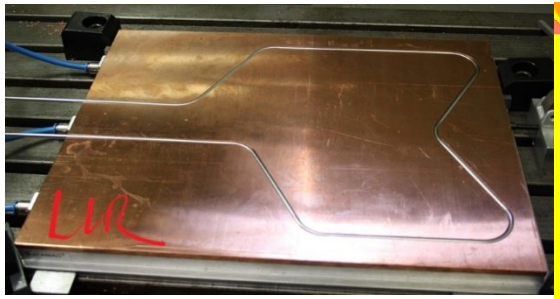
http://cds.cern.ch/record/2624680

Active cooling → 'Continuous colliders'

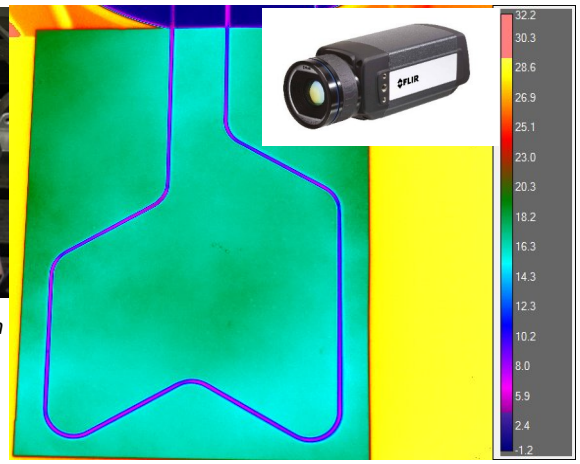
R&D using CMS studies (Thanks to Th. Pierre-Emile from CMS-LLR group)

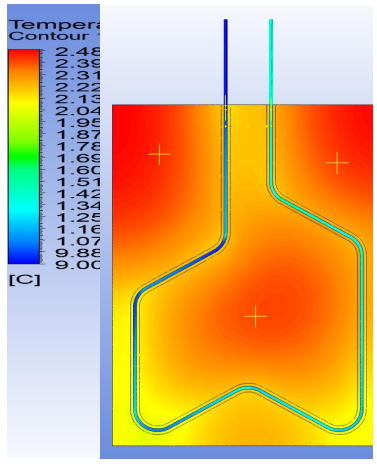


Copper plate prototype dimensions information



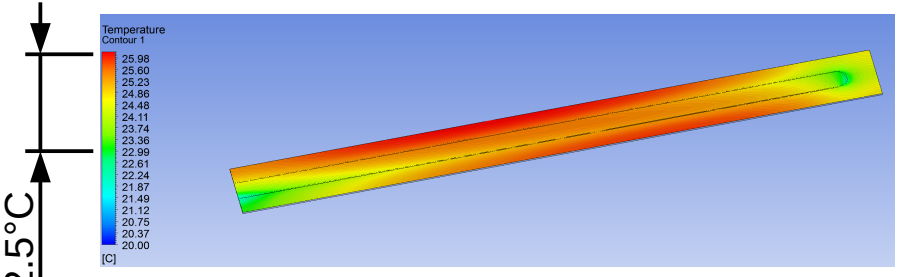
Pipe insertion on a cooling prototype for FEA correlation



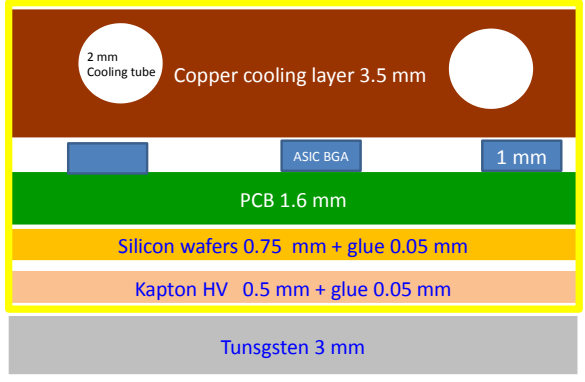


Pipe insertion on a cooling prototype

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling

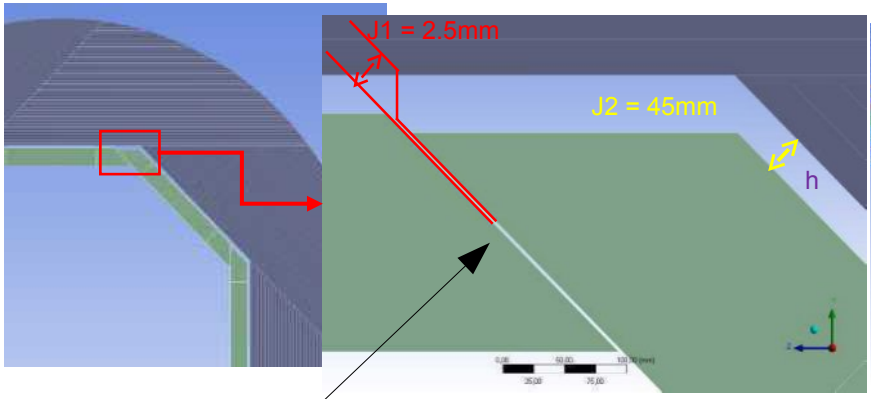


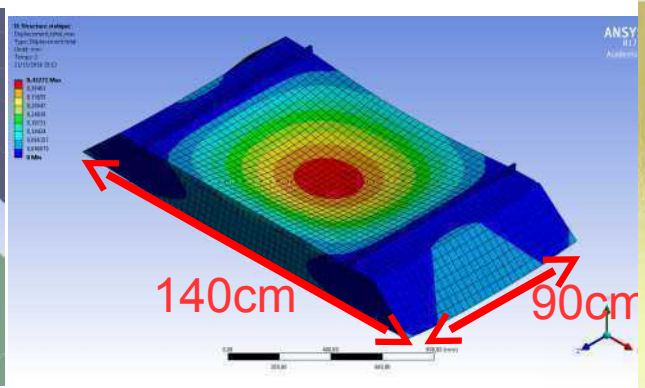
Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe

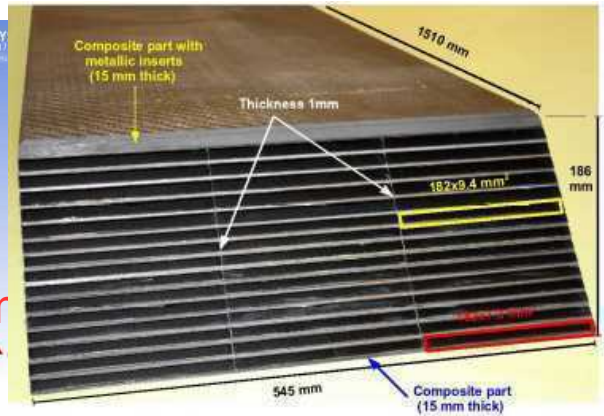


⇒ 9 mm / layer

CFRP+W Structures "standby"



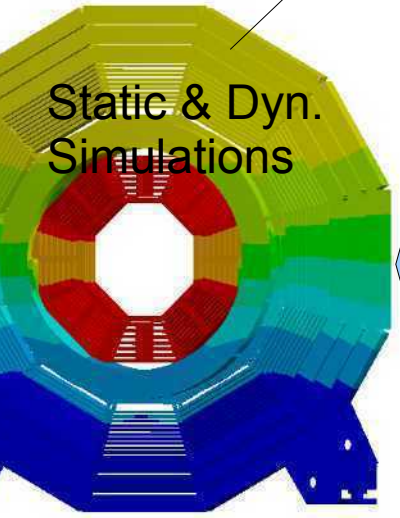


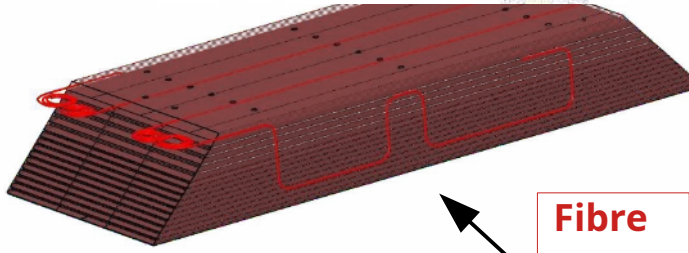


J1 = clearance between modules for the ECAL

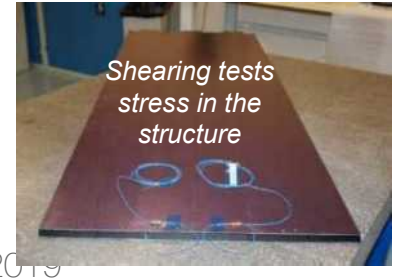
J2 = Clearance at ECAL edges between ECAL and HCAL

h = height of the rails 30mm





Fibre Bragg-Grated



measurements still to be done...

“No show” or anyways

Completion of tech prototypes

- → 20 layers
  - 16 boards avail:
    - 7(+1) FEV11 + 5 FEV13 + 2 FEV12 + 2 FEV12-COB

      Completion to full layers (gluing, ...)
    - + 4 FEV13 ? : 4 PCB avail.
  - Dev’t & Adaptation to New DAQ (when possible)
    - SL-Board v2
  - Upgrade of assembly & test chain (↔ AIDA++ ?)
    - General interest
- Request for BT @ DESY 2×1 wk.
  - CERN || FNAL || SLAC in 2021

Analyses

- Response at high E.
  - Resolution
  - Linearity
  - Uniformity in 1 || 2 stack ?
  - Shower shapes
  - Angular resolution
  - Timing

  → Auto-gain (+TDC), ?? µs + 2 ms trains, X-talks corrections (HGCAL)

PFA & Particle ID

- $e^{\pm}$ vs γ
- ch/γ separation
- Timing

Response of hadrons

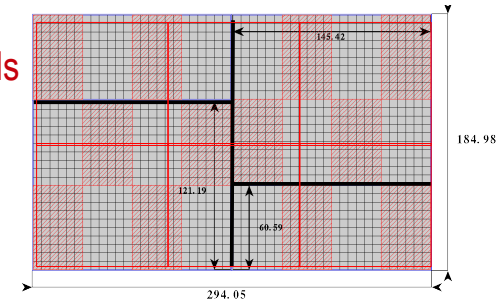
- 1/3 interacting
  - ~10% of ⟨E⟩ in ECAL × 10% of h^0 in jets
- “Academic” but critical for ML ?

Détecteurs FCC-ee/CLIC (aka continuous readout) ?

if there is an ILC…

FEV14 (or new)

- Alignment with lastest ILD models
  - 8" wafers, 750µm ≥ june 2020 ?
  - Larger boards: 32×48 cells
    - (2 + 2×1/2) 8"-wafers
    - (2×3) × 6"-wafers
      - » ~ compatible (smaller readout pads → wafers margins)



  - 24 ASICs: SK2a
    - packaging of 400 with Aptasic SA (CH) on-going (10+15k€)
      - » 16.6666 Boards of 24 ASICs
- HV → Per board
  - e-LS: HV decoupling of pairs of ASUs (≡ 32 chips)
- Incremental change
  - Connector scheme ?
  - Flat capacitors ? Murata stopped… stocks ?

Design of technological Long Slab

- ≤6 FEV14 in Barrel
  ≤8 FEV14 in Endcaps
- Double sided
- To be done with assembler…
- Capacity to handle high $\mathscr{L}$ scheme?
  - 1 ms × 5 Hz → 2 ms × 10 (15 Hz) ?

Dev't of testing & quality procedure

- Characterisation before mounting
  - Wafers
  - ASICs
  - Capacitors
  - FEV's

- **Automatized meas't**
- **Artificial vision**
- **Logging in single DB**
- **Full & simplified benches**
- **pairing of matching batches**

AIDA++ ?
AIDA-IP, InfraInnov

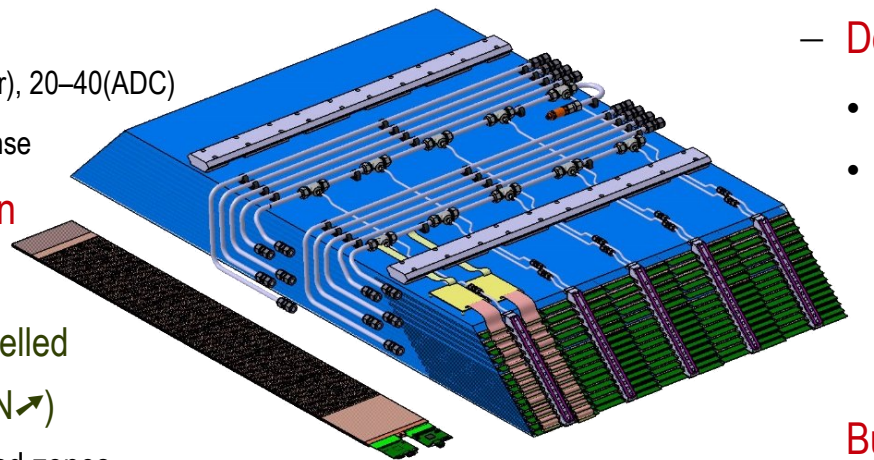
Conclusions & perspectives

Technical Milestones:

At hand on CALICE prototype:

- Workable, scalable design
- Reduced GR event rates
- ASU with 1024 channel
  - » Signal/Noise > 10 (trigger), 20–40(ADC)
  - » to be done: HE e⁻ response

Input for ILD IDR



On-going on ILD-like design

- Connection over 8 ASU's
- Mechanics & Cooling modelled
- Thicker & larger wafer (S/N↗)
  - red. number of layers, dead zones
- Compact DAQ

Next-to-Next steps

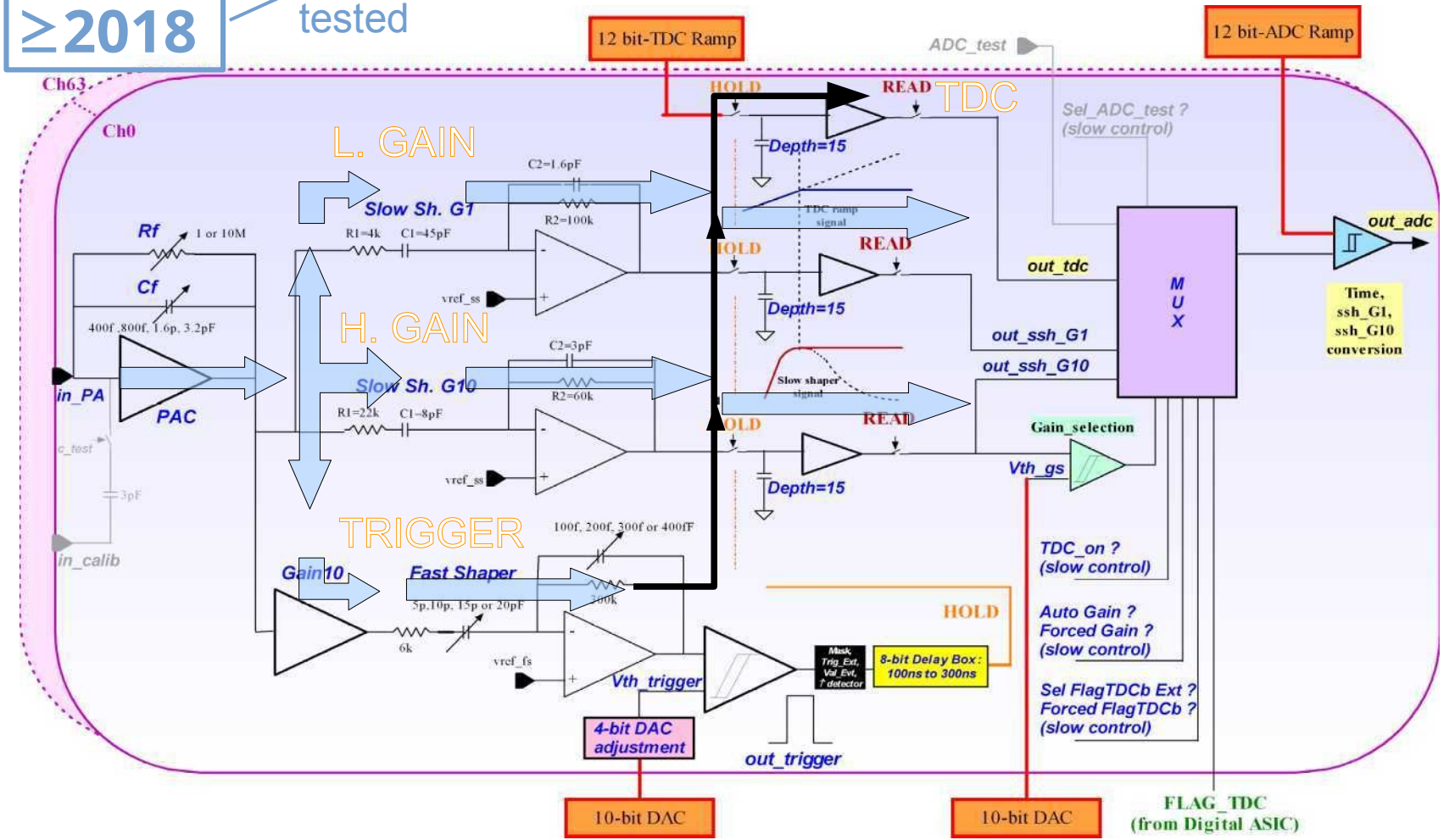
- Final chips (SK3-like): full 0-suppr …
  - machine dependant (duty cycle, timing)
- Industrial aspects (components, aging, …)
- Double Layered Long Slab Prototype
  - Design with larger wafers
  - Demonstrator for industry
    - Estimated cost ~160k€ / piece

Build a module-0.5.1

Extras

SKIROC2 / 2A Analogue core

≥2018 tested



Similar to SiD Kpix

- 64 channels
- Preamp
  + 2 (auto)Gains
  + **TDC** (~1.4ns)
- Auto-triggered
  - **per cell adj.**
- 15 (×2) analogue memories
- Low consumption
  - 25 µW/ch with 0.5% ILC-like duty cycle
- Power-pulsed

Main default: Re-triggering

Not final chip (full 0-suppr.)

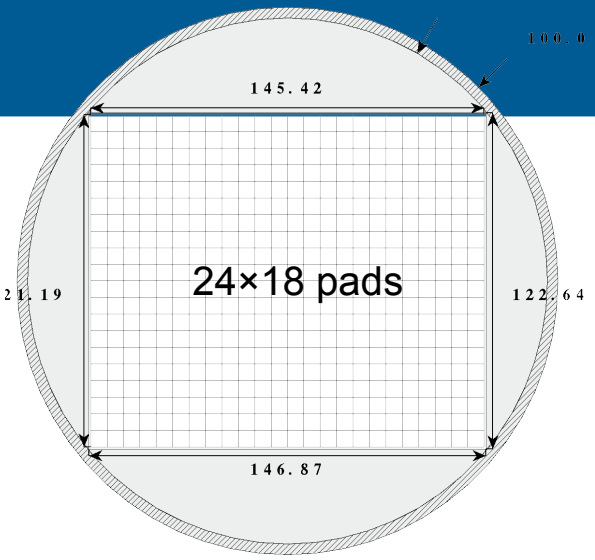
Going to 200mm Wafers…

From CMS HGCAL development & Hamamatsu contacts future is 200mm (8") ingots, 725µm thickness

Mechanical constraints → ~187 mm alveoli, ~12 cm wafer

→ 1.5 Wafers ⊗ cell # mult. of 3 ⊗ cell width ~5 mm ⊗ paving with ~64ch ASICs

→ **30** or 36 cells in width



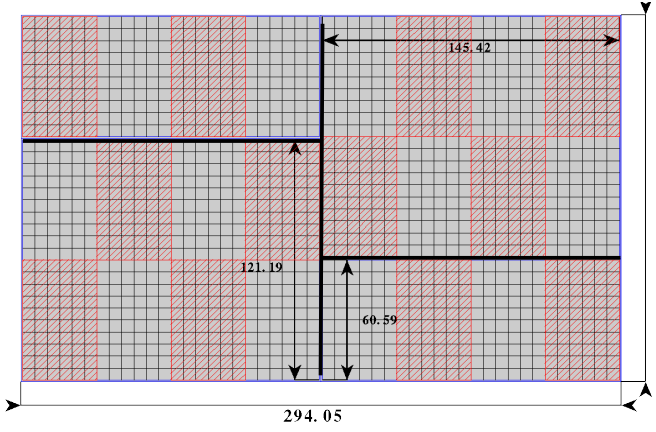
wafers on 200mm ingot ; 63 % use of surface

Optimised ReadOut electronics

- 6×6mm² , ASICs of 60ch.

  wrt 5×5mm² (⚠ ≠5.5² of prototypes)

  30% less electronics consumption cost



- ASU: 1440 pads, 24 ASICs
- Noise ~ C ~ width²/th. ~ cst, Signal ~ th ↗, S/N ~ ×1.5; depl. Voltage ~ th² (×2)

  ⇒ Improved timing perf (esp. for mips)